Structural Test Synchronization Reference Example

Overview

Structural test systems can require a variety of measurement types, including strain, pressure, temperature, and vibration. It is important to have a platform that not only can support the various measurement types, but is also able to start acquisition at the same time to correlate or synchronize all of the data that is acquired.

The PXI platform includes built-in timing and triggering buses to address the need for advanced timing, synchronization, and communication. PXI Express features a 100 MHz differential system clock, differential signaling, and differential star triggers. Using these timing and triggering buses, you can develop structural test systems for applications that require precise synchronization within a single chassis and share these signals across multiple chassis for high-channel-count systems.

Figure 1. High-Channel-Count Structural Test System

National Instruments offers best-in-class synchronization with flexible synchronization options that can meet the most stringent requirements. This paper explains different architectures and provides the reference example code to get you started. Depending on the size and performance requirements for your structural test application, there are different hardware configurations ranging from a single chassis to multiple chassis, with shared or dedicated controllers. This paper assumes that you

understand the basics of synchronizing National Instruments sample clock timed (that is, NI PXIe-63xx, PXIe-430x, and PXIe-435x) and oversample clock timed (that is, NI PXIe-433x and PXIe-449x) DAQ devices. For a review, read Synchronization Explained, an in-depth paper on synchronization techniques.

Reference Example Software

This NI LabVIEW example uses NI-DAQmx and NI-Sync driver software in addition to the Simple Messaging Reference Library (STM). The code supports multiple hardware configurations; therefore, you need the following software to run the example:

- NI LabVIEW 2010 or later
- NI-DAQmx 9.2.3 or later
- NI-Sync 3.2.2 or later
- Simple Messaging Reference Library (STM)

This example is based on an NI-DAQmx example with various case structures to configure the hardware as necessary for the system configurations described below. Figure 2 shows the LabVIEW front panel and user interface for configuration and data viewing.

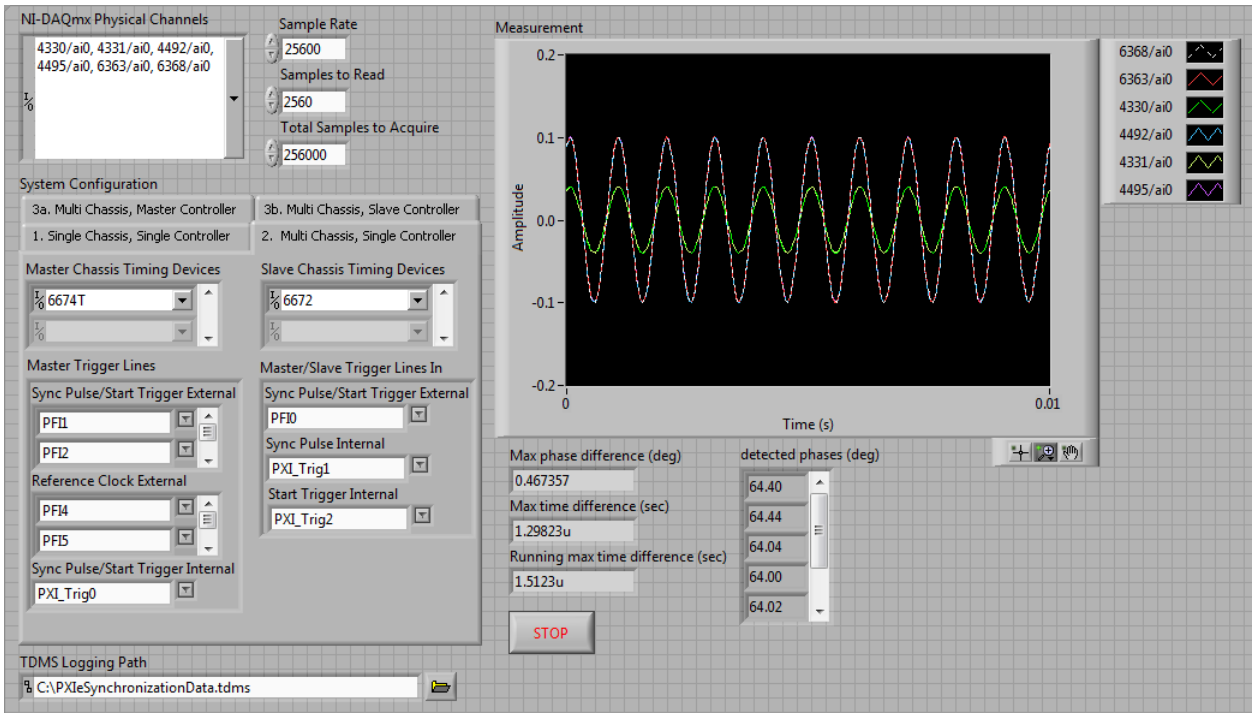

Figure 2. LabVIEW Front Panel for Configuration and Data Viewing

The top level of the example includes NI-DAQmx code, as well as communication and synchronization subVIs (or functions) as shown in Figure 3. The subVIs with the light blue bar on the left include STM functions for communication between controllers. The subVIs with the green bar on the left include NI-Sync functions used for sharing timing signals across chassis.

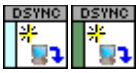

Figure 3. Example SubVIs for Communication and Synchronization

Reference Example Configurations

1. Single Chassis, Single Controller

This configuration is the most basic setup with the most straightforward programming and it can support up to 500 sensor channels, depending on the PXI modules that you select.

Hardware Setup

The configuration requires a single chassis and controller and supports any combination of NI SC Express (NI PXIe-433x), DSA (NI PXIe-449x), and/or X Series (NI PXIe-63xx) modules. This configuration does not require NI PXIe-667x timing modules, because all of the timing signals are passed using built-in timing lines.

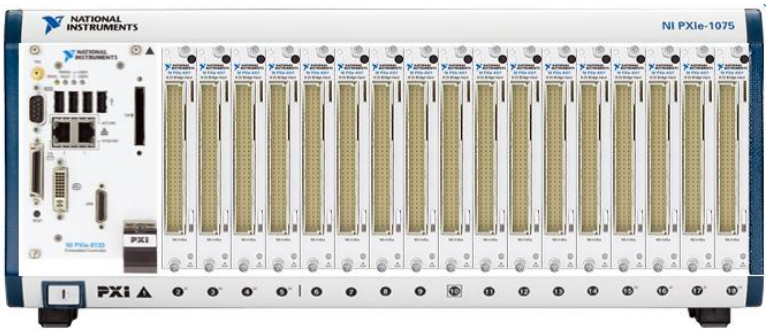

Figure 4. Single Chassis, Single Controller Hardware Configuration

Software Setup

In this case, the oversample clock timed devices are placed in one NI-DAQmx multidevice task and the sample clock timed devices are placed in a separate multidevice task. The two tasks are synchronized by sharing the sample clock from the oversample clock timed device task and using it in the sample clock timed device task. Follow the steps below to run the reference example:

- Select all of the channels to read in the physical channels control
- Select the “1. Single Chassis, Single Controller” tab

2. Multichassis, Single Controller

This configuration allows you to increase channel counts by adding additional chassis in an architecture that only requires a single controller. This option uses MXI Controllers for PXI System Expansion to control the additional chassis.

Hardware Setup

The multichassis, single controller configuration uses one controller and includes MXI Express modules to control additional PXI Express chassis. This requires NI PXIe-667x timing modules, because all of the timing signals are passed between the chassis.

This configuration requires a master chassis with a controller and slave chassis each with a MXI Express module in the controller slot. Each chassis needs an NI PXIe-667x timing module in the timing slot and can include any combination of SC Express (NI PXIe-43xx), DSA (NI PXIe-449x), and/or X Series (NI PXIe-63xx) modules. The master chassis can support multiple NI PXIe-667x timing modules in the chassis to distribute timing signals and is not required to have any data acquisition modules.

The reference clock must be shared from the master chassis through the BNC connector on the back of the PXI Express chassis or through the PFI lines on the front of the NI PXIe-667x timing modules and imported on each slave chassis. The trigger line used to transmit the sync pulse and start trigger must also be shared from the master chassis to the slave chassis through the PFI lines on the front of the NI PXIe-667x timing modules. The trigger lines on the master can be configured so that there is one PFI trigger line for each slave chassis.

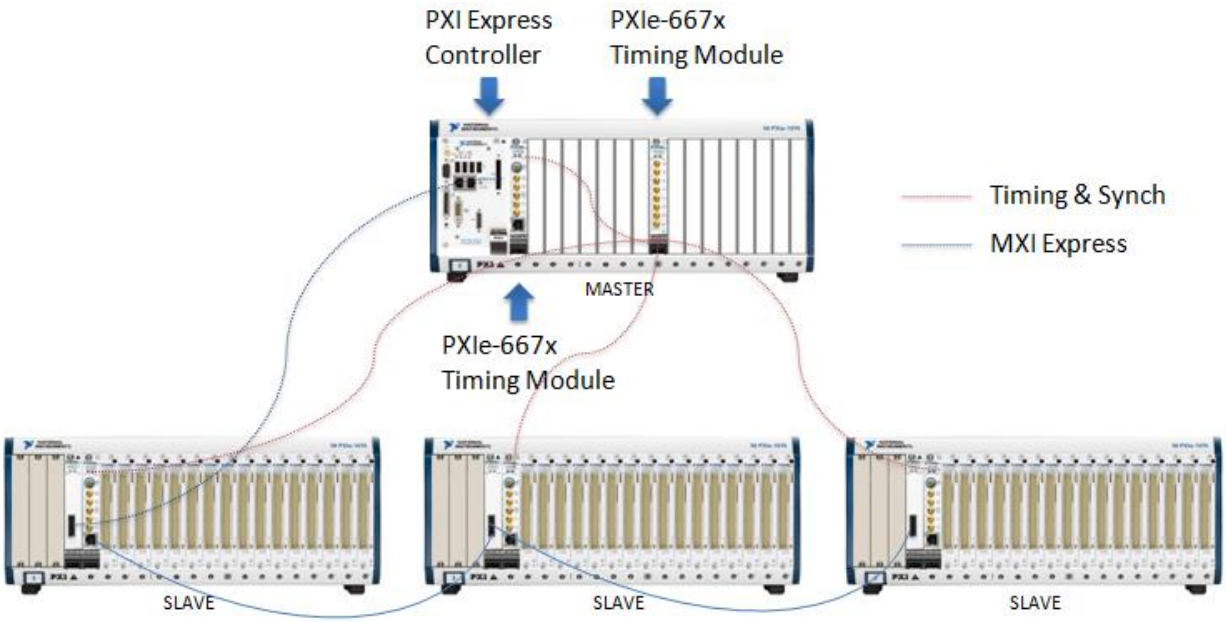

Figure 5. Multichassis, Single Chassis Hardware Configuration

Software Setup

Within each chassis, the oversample clock timed devices are placed in one NI-DAQmx multidevice task and the sample clock timed devices are placed in another multidevice task. The two tasks are synchronized by sharing the sample clock from the oversample clock timed device task and using it in the sample clock timed device task similar to the single chassis case. In addition, the sync pulse and start

trigger are generated and exported from the master chassis and imported in each chassis to be used in the oversample clock timed device task. Follow the steps below to run the reference example:

- Select all of the channels to read in the physical channels control
- Select the "2. Multi Chassis, Single Controller" tab
- Select all of the NI PXIe-667x timing modules in the master chassis as master timing devices (The first module in the list is considered the master).
- Select all of the NI PXIe-667x timing modules in each slave chassis as slave timing devices

3. Multichassis, Multicontroller

This configuration includes dedicated controllers, so there is no limit to the number of devices you can include in your system. Using multiple controllers typically requires additional programming to communicate between controllers, but the reference example code gets you started. This configuration is the most scalable and most reliable. If there is a failure on one system once data has begun to be acquired, the others continue running and acquiring data because they have dedicated controllers.

Hardware Setup

This hardware configuration uses multiple controllers to expand the system to multiple chassis. This requires NI PXIe-667x timing modules because all of the timing signals are passed between the chassis. Because there are multiple controllers in the system, TCP is used for communication between controllers.

This configuration requires multiple chassis with separate controllers and an NI PXIe-667x timing module in each chassis. This setup can include any combination of SC Express (NI PXIe-43xx), DSA (NI PXIe-449x), and/or X Series (NI PXIe-63xx) modules. The chassis designated as the master chassis can support multiple NI PXIe-667x timing modules in the chassis to distribute timing signals and is not required to have any data acquisition modules.

The reference clock must be shared from the master chassis through the BNC connector on the back of the PXI Express chassis or through the PFI lines on the front of the NI PXIe-667x timing modules and imported on each slave chassis. The trigger line must also be shared from the master chassis to the slave chassis through the PFI lines on the front of the NI PXIe-667x timing modules. The trigger lines on the master can be configured so that there is one PFI trigger line for each slave chassis.

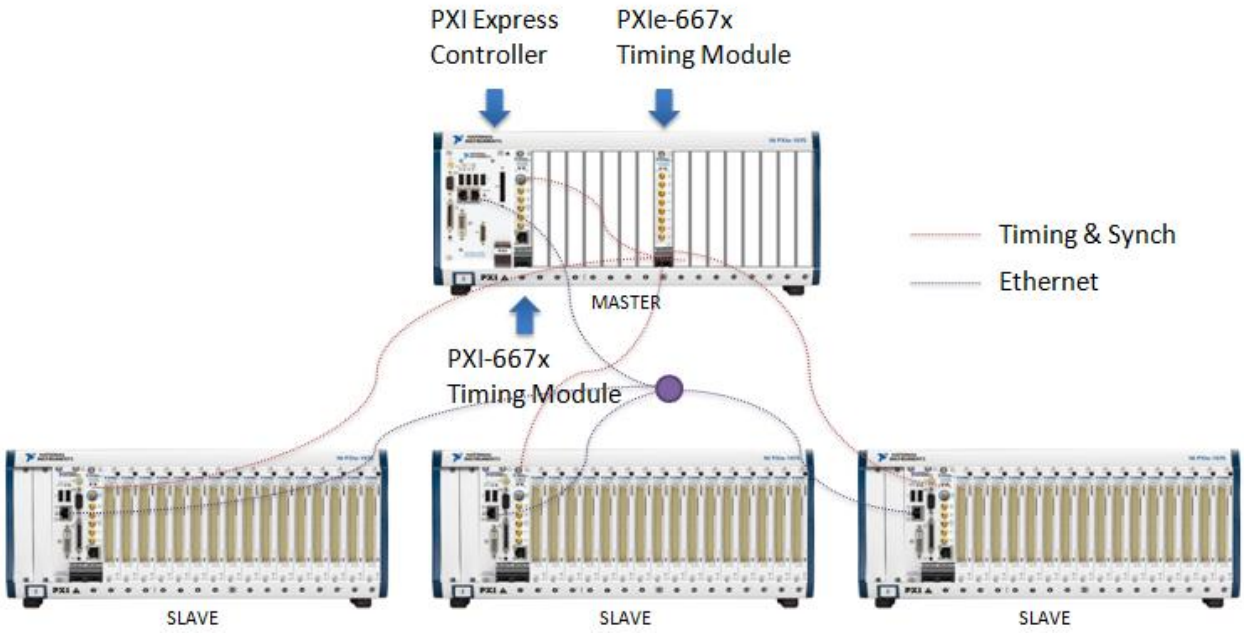

Figure 6. Multichassis, Multicontroller Hardware Configuration

Software Setup

Within each chassis, the oversample clock devices are placed in one NI-DAQmx multidevice task and the sample clock devices are placed in another multidevice task. The two tasks are synchronized by sharing the sample clock from the oversample clock timed device task and using it in the sample clock timed device task similar to the previous cases. In addition, the sync pulse and start trigger will be generated and exported from the master chassis and imported in each chassis to be used in each oversample clock timed device task. Follow the steps below to run the reference example:

- Select all of the channels to read in the physical channels control on each controller
- Select the “3b. Multi Chassis, Slave Controller” tab on all of the slave chassis
- Select all of the NI PXIe-667x timing modules in each slave chassis as slave timing devices
- Run the slave examples to have the IP address displayed on the front panel
- Select the “3a. Multi Chassis, Master Controller” tab on the master chassis
- Select all of the NI PXIe-667x timing modules in the master chassis as master timing devices, the first module in the list is considered the master
- Enter all of the slave IP addresses in the example on the master chassis

Benchmarks

The table below includes synchronization benchmarks for various combinations of modules. The accuracy of synchronization varies from system to system based on factors such as trigger cable length; therefore, the values provided below are typical values from testing. You can synchronize all module

types across chassis with microsecond level skew. Even better synchronization can be achieved among only sample clock timed devices or oversample clock timed devices.

Devices Used	Module-to-Module Skew
Sample clock timed devices: SC Express nonbridge modules (NI PXIe-430x and PXIe-435x) X Series (NI PXIe-63xx)	75 ns
Oversample clock timed devices: SC Express bridge modules (NI PXIe-433x) DSA (NI PXIe-449x)	200 ns
Both sample clock and oversample clock devices	1.5 µs

Figure 7. Synchronization Benchmarks

Conclusion

The PXI platform supports various system architectures for systems from one to thousands of channels. The single chassis approach is the most basic configuration for small to medium channel counts. With the multichassis, multicontroller approach, you have dedicated controllers meaning that your system can scale to an unlimited number of devices and channels. This reference example includes signal-based synchronization, but National Instruments also offers solutions for time-based synchronization with references to GPS, 1588, or IRIG-B. With the flexible and powerful PXI platform, you can easily scale your system to meet your application requirements with best-in-class synchronization.

Resources

Read an in-depth paper on synchronization
View a fully configured PXI system for static and fatigue structural tests
View a fully configured PXI system for dynamic structural tests