# Essential synchronization technologies in PXI

*By Kaustubh Wagle*

*Many test and measurement applications, such as mixed-signal test and channel expansion, demand precise timing and synchronization. In this article, Kaustubh explains why synchronization is essential for improving accuracy and reducing test time. He also provides an overview of the various synchronization schemes available today, including T-Clock (TClk), a new technology that enables picosecond accuracy.*

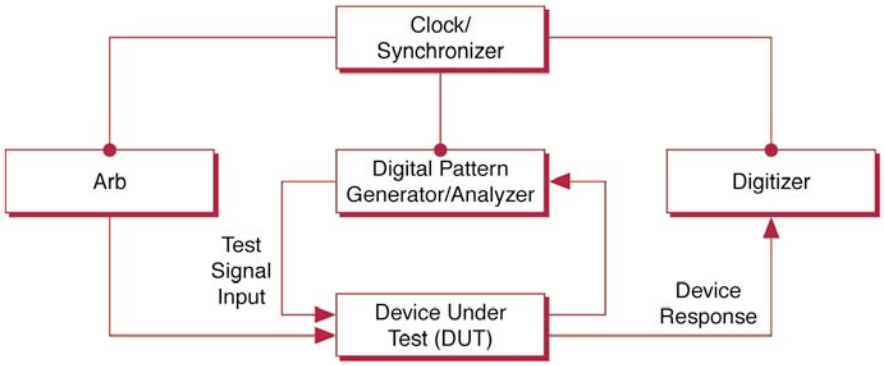



**Figure 1**

## Basics of synchronization

Mixed-signal devices, by definition, comprise both analog and digital signals. The most basic example of a mixed-signal device is an analog-to-digital converter (A/D converter). One of the tests commonly performed on an A/D converter is a stimulus-response test, which involves feeding an analog signal generated with an arbitrary waveform generator (arb) into the A/D converter and acquiring its digital output using a digital waveform analyzer. To most accurately characterize an A/D converter, the analog input and digital output must be phase-correlated to support synchronization of the arb with the digital waveform analyzer.

The diagram in Figure 1 represents a typical setup for mixed-signal test systems, which includes at least two of the following devices: arbitrary waveform generator, digitizer, digital waveform generator, or digital waveform analyzer.

Mixed-signal test applications often test the analog and digital features of the mixed-signal device in parallel to reduce test time. The analog and digital components on the mixed-signal device often operate at different frequencies that are not necessarily multiples of each other. Therefore, the instruments that test these components need to sample at different rates. The challenge here is that the analog and digital data from these instruments must be phase-correlated and, hence, must be synchronized. To overcome these challenges, engineers can employ such technologies as Phase-Locked Loops (PLL) and sophisticated TClk synchronization, as detailed later in this article.

One of the other purposes of synchronization is channel expansion. Common applications needing channel expansion include structural vibration analysis, wind tunnel test, acoustic monitoring, and machine condition monitoring. For example, Lockheed Martin Aeronautics Company uses a wind tunnel test system to test their F-35 Joint Strike Fighter planes. The test system includes multiple synchronized NI PXI-4472 dynamic signal acquisition modules with 128 simultaneously sampled input channels. Figure 2 shows a multichassis synchronization setup for achieving more than 5,000 synchronized channels.

## Synchronization schemes

A variety of bus schemes are available today that can achieve certain levels of synchronization.

## Synchronization with only the start trigger

This is the simplest form of synchronization, involving a single trigger from the master to the slaves. The master is configured to look for and meet a specific external trigger condition. When it meets that condition, it sends a trigger to all of the slave instruments (see Figure 3). The only advantage of this scheme is that it is very simple to implement. One of the disadvantages is that the master instrument starts before the slave instruments. In addition, the master and each

**Figure 2**

of the slave instruments run on different internal clocks, which have inherent jitter. Therefore, the sampling periods on the instruments cannot be correlated.

**Synchronization with the start trigger and sample clock**

In this scheme, the master not only sends a trigger to all of the slave instruments as with the start-trigger-only scheme, but also sends its internal clock to each of the slaves (see Figure 4). The advantage of this scheme is that all of the instruments, master and slaves, run based on the same oscillator. Although clock jitter still exists, it is the same for all the instruments. Hence, the sampling periods can be correlated across the instruments. The trade-off of this scheme is that it forces all instruments to run at the same speed. As mentioned previously, most mixed-signal tests involve instruments that run at variable rates. In this case, one cannot use this synchronization scheme. Another disadvantage is that this scheme limits the speed at which the instruments can run because it is physically extremely difficult to share clocks at high speeds. Furthermore, as in the start-trigger-only scheme, the master instrument starts before the slave instruments.

**Synchronization with start trigger and reference clock using PLL technology**

This synchronization scheme allows the instruments to run at high speeds. It eliminates the obstacle of sending high-speed clocks to slaves. Instead, it involves a reference clock, which is much slower than the individual sample clocks and can easily send signals to the slaves. (See Figure 5 for an illustration of this scheme.) The source of this reference clock can be any one of the following, depending on the desired level of accuracy:

- The 10 MHz backplane clock
- Module capable of overriding the backplane clock
- External user-provided clock using a timing and synchronization module

The slave instruments lock their sample clocks to this reference clock using a built-in PLL circuitry. The top of Figure 6 shows two high-speed clocks with the same frequency, but they are not phase-aligned. This implies that the two instruments will sample at slightly different times. The bottom of the diagram illustrates PLL where each rising edge of the reference clock coincides with the rising edges of the two sample

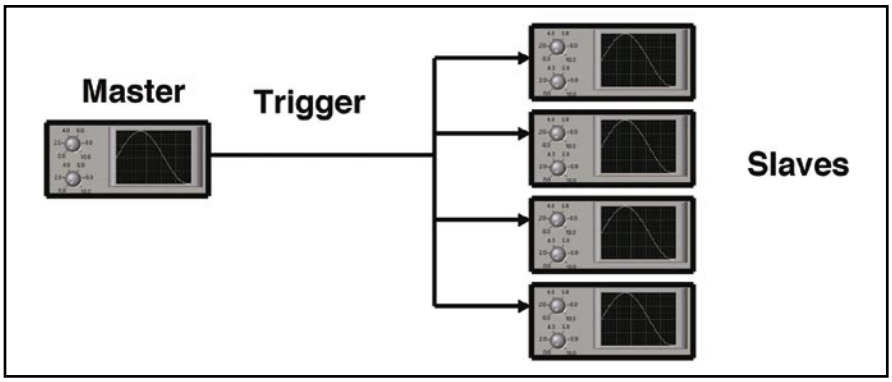



Figure 3

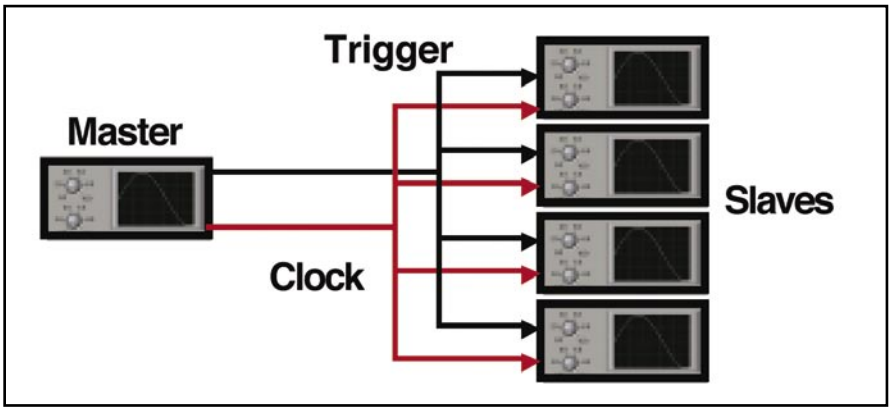



Figure 4

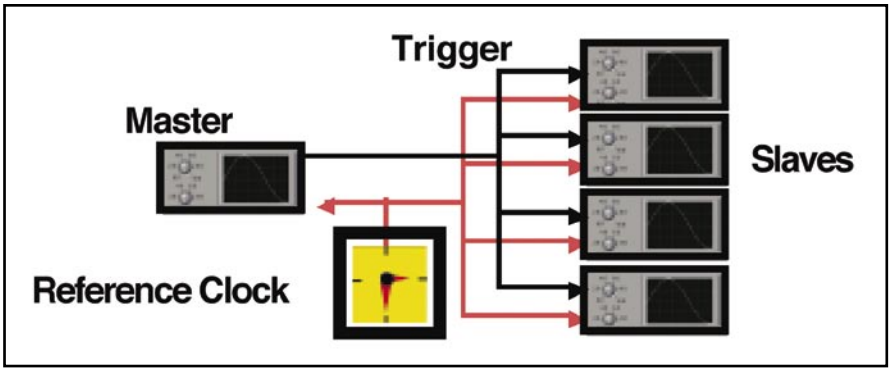



Figure 5

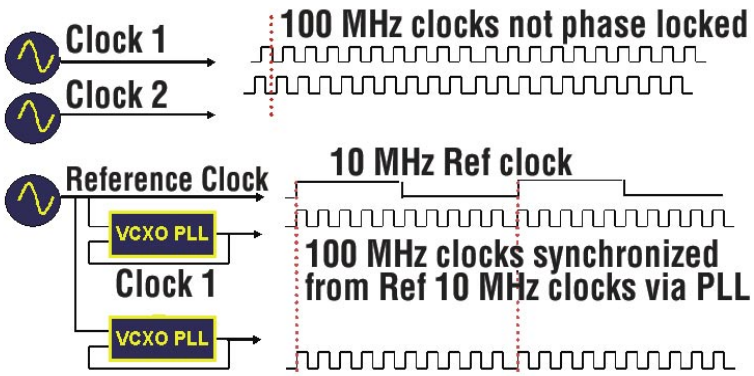



Figure 6

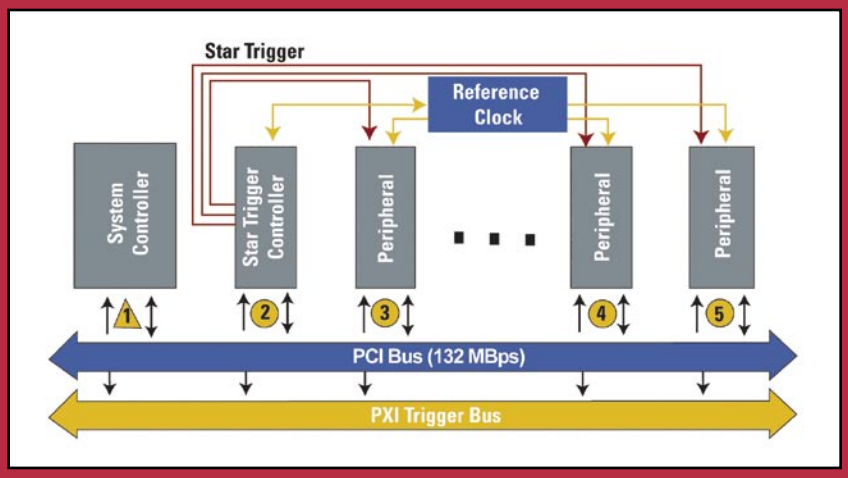
# feature sidebar

## Overview of the PXI backplane

The PXI modular instrumentation platform has an integrated backplane architecture designed to meet engineers' requirements for synchronizing multiple instruments. The backplane has three main features for synchronization – the 10 MHz reference clock, trigger bus, and star trigger.

## 10 MHz reference clock

The PXI backplane provides a built-in common reference clock for synchronizing multiple modules in a measurement or control system. Refer to Sidebar Figure 1 for an illustration of the backplane, which shows how the clock is distributed to each peripheral slot with equal-trace-length lines, yielding less than 1 ns of slot-to-slot skew. The accuracy of the 10 MHz clock is typically ±25 ppm, making it a relatively reliable clock for synchronization applications that rely on PLL methods. If an accurate reference clock is needed, one can insert a PXI timing and synchronization module, such as an NI PXI-665x series module (Sidebar Figure 2 shows the NI PXI-6653) or a ZTec ZT1000PXI module, into Slot 2 of the chassis. The Slot 2 modules feature an oven-controlled crystal oscillator (OCXO) clock source that overrides the backplane clock and can increase the accuracy to ±50 ppb. A common application of the 10 MHz reference clock is the synchronization of measurement devices that operate at sample rates from 1 MHz to several GHz.




**Sidebar Figure 1**

## Trigger bus

The PXI trigger bus provides eight lines for inter-module communication and synchronization. It can pass triggers, clocks, or event signals from one module to any number of modules.

## Star trigger

The star trigger bus provides independent dedicated lines from Slot 2 to each of 13 peripheral slots in a PXI system. The star trigger lines match in propagation delay to within 1 ns, providing precise triggering for high-speed synchronization.

**Sidebar Figure 2**

clocks. Hence, the two sample clocks are phase-aligned. As with the previous two schemes, the master instrument sends a trigger to all of the slave instruments once it meets trigger conditions.

This synchronization scheme represents an enormous improvement over the other two schemes. However, it is not perfect, and has the following drawbacks.

- When all the instruments have sample clocks that are integer multiples of the 10 MHz reference clock, PLL ensures that they are phase-aligned. However, what happens when the sample clocks are not integer multiples of the 10 MHz reference clock, as in the case of most mixed-signal applications? For example, let's say there are two 25 MHz clocks on two instruments requiring synchronization. The problem is that there is no guarantee that the sample clocks will be phase-aligned in spite of being phase-locked to the 10 MHz reference clock, as Figure 7 shows. Resetting all the PLLs at the same time can overcome this drawback.
- Let's say we overcome the problem above. We still face the challenge of starting the instruments on the exact same clock period, due to metastability on the trigger.
- The master instrument starts before the slave instruments, as in all the schemes.

## Achieving picosecond accuracy with T-Clock

The drawbacks from the previously discussed synchronization schemes led to the development of a most compelling synchronization technology – trigger clock – referred to as TClk and pronounced as T-Clock. TClk, a patent-pending technology, is available on devices with National Instruments' Synchronization and Memory Core (SMC) architecture.

SMC is the digital core architecture on National Instruments' 100 MSps and 200 MSps modular instruments and includes the following features shown in Figure 8:

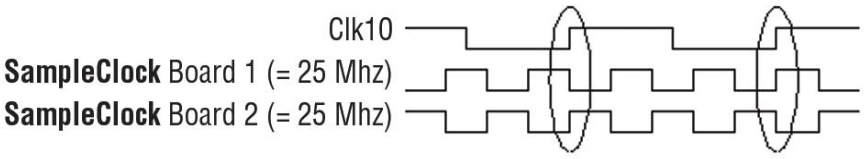
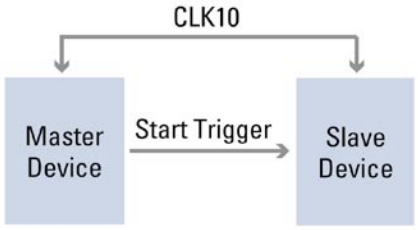



Figure 7



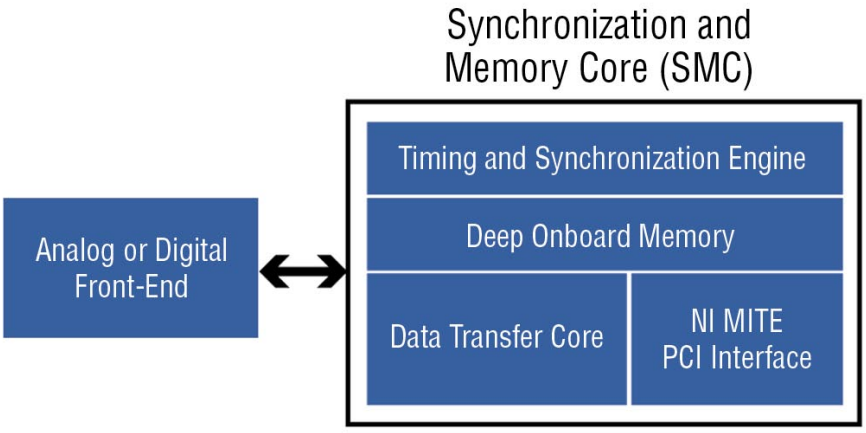




Figure 8

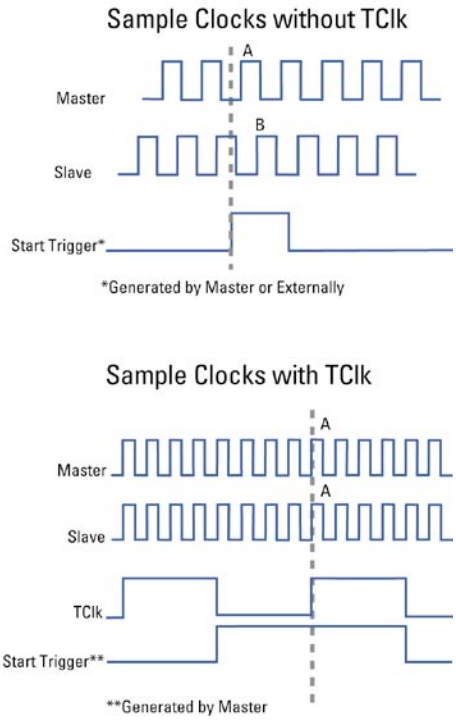



Figure 9

- A precise timing and synchronization engine
- Flexible input and output data transfer cores
- Deep, flexible onboard memory, up to 512 MB per channel

In the TClk scheme, each device generates its own copy of TClk by dividing down its sample clock to a frequency that is low enough for the reliable transmission of triggers over the PXI trigger bus. The TClk period is 200 ns or greater, and therefore enables sufficient time for the trigger pulse to propagate to all the devices before the next rising edge of the TClk. This feature ensures that multiple devices can react to the trigger in the same sample clock period.

TClk fixes the problem of the master starting before the slaves by establishing a predefined protocol, as follows:

- The master will send the start trigger only on the falling edge of its TClk once it meets trigger conditions.
- All the slaves, as well as the master, will start acquisition on the immediate rising edge of each TClk.

Figure 9 illustrates this protocol showing how the master starts at A and the slave starts at B without TClk. With TClk, both the master and the slave start together at A.

## Performance and programming of TClk synchronization

Instruments synchronized using TClk have a channel-to-channel skew in the picoseconds range, with typical skews between 200 and 500 ps. Figure 10 depicts this skew using LabVIEW, illustrating synchronization between multiple arbitrary waveform generators and digitizers. Only three functions/VIs are required to incorporate TClk synchronization for picosecond-level accuracy. Using manual calibration can achieve even less channel-to-channel skew, for example, less than 30 ps between devices.

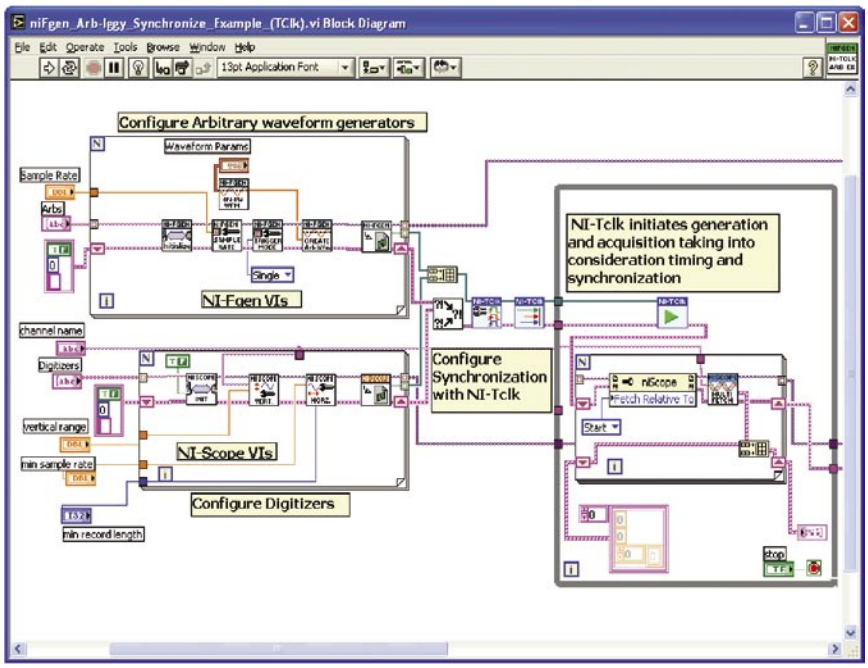



Figure 10

# Synchronizing measurement systems

National Instruments has made it extremely easy for engineers to implement TClk in their applications. Users can now synchronize multiple instruments with accuracy levels that were previously available only in expensive high-end systems.

## References


1. Duraiappah, Lokesh and Chris Bartz, "National Instruments' T-Clock Technology for Timing and Synchronization of Modular Instruments"
2. Lokesh Duraiappah, "National Instruments' Synchronization and Memory Core – A Modern Architecture for Mixed Signal Test" White Paper



***Kaustubh Wagle*** *is a product marketing engineer at National Instruments. Kaustubh joined the company in 2003 as an applications engineer before moving to product marketing in the modular instrumentation group. He holds a B.S. in Computer Sciences and a B.A. in Economics from the University of Texas at Austin.*


For more information, contact National Instruments directly:


**National Instruments**
11500 N. Mopac Expressway
Austin, TX 78759
Tel: 888-280-7645
Fax: 512-683-8411
E-mail: kaustubh.wagle@ni.com
Website: www.ni.com