Register Map and Descriptions

Table 3-1. PCI-6713 Register Map

Register Name	Offset Address Hex	Offset Address Decimal	Type	Size
Misc Register Group				
Serial Command Register	0D	13	Write-only	8-bit
Misc Command Register	0F	15	Write-only	8-bit
Status Register	01	1	Read-only	8-bit
CAL ADC Register Group				
ADC Command Register	W19	W25	Write-only	8-bit
ADC Status Register	W1A	W26	Read-only	8-bit
ADC Conversion Data Register	W1B	W27	Read-only	16-bit
ADC Config Data High Word Register	W1C	W28	Read-and-Write	16-bit
ADC Config Data Low Word Register	W1D	W29	Read-and-Write	16-bit
Analog Output Register Group				
AO Configuration Register	16	22	Write-only	16-bit
DAC FIFO Data Register	14	20	Write-only	32-bit
AO Window addr Register	18	24	Write-Only	16-bit
AO Window Data Register	1E	30	Write-Only	16-bit
DAC<0..7> Direct Data Register	W(0-7)	W(0-7)	Write-only	16-bit
AO Timed Register	W 10	W16	Write-only	16-bit
AO Immediate Register	W 11	W17	Write-only	16-bit
AO FIFO Offset Load Register	W 13	W19	Write-only	32-bit
AO Later Single Point Updates Register	W 14	W20	Write-only	16-bit
AO Waveform Generation Register	W 15	W21	Write-only	16-bit
AO Misc Register	W 16	W22	Write-only	16-bit
AO Cal Chan Sel Register	W17	W23	Write-Only	16-bit
AO Config][Register	W18	W24	Write-Only	16-bit
DAQ-STC Register Group				
Window Address Register	0	0	Write	16-bit
Window Data Register	2	2	Read and Write	16-bit
Window Data Register	2	2	Read-and-write	16-bit
Interrupt A Acknowledge Register	4	4	Write	16-bit
Interrupt B Acknowledge Register	6	6	Write	16-bit
AI Command 2 Register	8	8	Write	16-bit
AO Command 2 Register	A	10	Write	16-bit
G0 Command Register	C	12	Write	16-bit
G1 Command Register	E	16	Write	16-bit
AI Status 1 Register	4	4	Read	16-bit
AO Status 1 Register	6	6	Read	16-bit
G Status Register	8	8	Read	16-bit
AI Status 2 Register	A	10	Read	16-bit
AO Status 2 Register	C	12	Read	16-bit
DIO Parallel Input Register	E	14	Read	16-bit

Serial Command Register

The Serial Command Register controls the PCI-6713 serial EEPROM and DACs. The contents of this register are cleared upon power up and after a reset condition.

Address: Base address + 0D (hex)
Type: Write-only
Word Size: 8-bit
Bit Map:

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	**SerDacLd1**	**SerDacLd0**	**EEPromCS**	**SerData**	**SerClk**

Bit	Name	Description
7–5	Reserved	Reserved—Always write 0 to these bits.
4	SerDacLd1	Serial DAC Load1— This bit is used to load the second set of serial DACs with the serial data previously shifted into the DACs.
3	SerDacLd0	Serial DAC Load0—This bit is used to load the first set of serial DACs with the serial data previously shifted into the DACs.
2	EEPromCS	EEPROM Chip Select—This bit controls the chip select of the onboard EEPROM used to store calibration constants. When EEPromCS is set, the chip select signal to the EEPROM is enabled.
1	SerData	Serial Data—This bit is the data for two onboard serial devices—the calibration EEPROM and the serial DACs. This bit should be set to the desired value prior to the active write to the SerClk bit.
0	SerClk	Serial Clock—This bit is the clock input to the three onboard serial devices (the calibration EEPROM, the serial DACs, and the temperature sensor). In order to write to the EEPROM or the DACs, this bit should be set first to 0 and then to 1. The data in the SerData bit will be written to the devices on the low-to-high transition of the serial clock.

Status Register

The Status Register is used to indicate the status of various PCI-6713 resources.

Address: Base address + 01 (hex)
Type: Read-only
Word Size: 8-bit
Bit Map:

7	6	5	4	3	2	1	0
Reserved	**Temp OUT**	**AO PFF**	**AO OVERRUN**	Reserved	Reserved	Reserved	**PROMOUT**

Bit	Name	Description
6	Temp OUT	Temperature Out - This bit reflects the serial output data from the temperature sensor. The clock input to the temperature sensor is in the Serial Command Register.

5	AO PFF	AO Programmable Full Flag - This bit reflects the status of the AO programmable full flag. If this bit is set, the AO FIFO has (full - AO offset value) points or less stored in it. The AO offset value is specified in the AO FIFO Offset Load Register.
4	AO OVERRUN	AO Overrun - This bit reflects the status of the AO overrun error detection circuitry; if this bit is set an overrun error has been detected. Write the X bit in the AO MISC register to clear this bit.
2–1	Reserved	Reserved
0	PROMOUT	EEPROM Output Data—This bit reflects the serial output data of the serial EEPROM. The clock input to the EEPROM is in the Serial Command Register.

CAL ADC Register Group

ADC Command Register

The ADC Command Register is used to issue commands to the serial CAL ADC.

Address: Window Address + 19 (hex)
Type: Write-only
Word Size: 8-bit
Bit Map:

7	6	5	4	3	2	1	0
CB	SC	CC	R/W	RSB2	RSB1	RSB0	PS/R

Bit	Name	Description
7	CB	Command Bit - when this bit is 1, the command bits in this register are shifted out to the ADC, and the command is executed. This bit is cleared when the command has finished executing.
6	SC	Start Conversion - when CB is 1 and this bit is 1, the ADC begins a single conversion. The conversion is complete when the ADC BUSY bit in the ADC status register is 0.
5	CC	Continuous Conversion mode - when CB is set and this bit is set, the ADC is placed into continuous conversion mode. The ADC is ready to deliver the latest conversion data when the ADC BUSY bit in the ADC status register is 0. Exit continuous conversion mode by issuing a command with CB = 1.
4	R/W	Read/Write bit - Set this bit to 1 when reading from a register on the ADC; set this bit to 0 when writing to a register on the ADC.
3-1	RSB<2..0>	Register Select Bits - These bits are used to select the register on the ADC to read from or write to, according to the following table: 000 - Offset Register 001 - Gain Register 010 - Configuration Register 011 - Not used 100 - Not used 101 - Not used 110 - Not used 111 - Not used
0	PS/R	Power Save Mode / Run Mode - The ADC's power save mode is not used on the PCI-6713; always write a 0 to this bit.

ADC Status Register

The ADC Status Register reflects the current status of the serial ADC.

Address: Window Address + 1A (hex)
Type: Read-only
Word Size: 8-bit
Bit Map:

7	6	5	4	3	2	1	0

D7	D6	D5	D4	D3	OF	OD	ADC BUSY

Bit	Name	Description
2	OF	Overrange Flag- This bit is an error flag returned from the ADC- when this bit is 1, the input to the ADC was out of the ADC's range, and the data returned from the ADC is not valid. This bit is cleared when the ADC completes a conversion without an error.
1	OD	Oscillation Detect- This bit is an error flag returned from the ADC; when this bit is 1, the data returned from the ADC is not valid. This bit is cleared when the ADC completes a conversion without an error.
0	ADC BUSY	When this bit is 1, the ADC is working on its latest task. When this bit is 0, the ADC is ready to receive its next command from the ADC command register.

ADC Conversion Data register

This register holds the 16-bit conversion data returned from the serial ADC.

Address: Window Address + 1B (hex)
Type: Read-only
Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**

7	6	5	4	3	2	1	0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

Bit	Name	Description
15-0	D<15..0>	The 16 bit conversion data returned from the ADC. This register should only be read when the ADC Busy bit in the ADC Status Register is 0.

ADC Config Data High Word Register

This register holds the most significant 8 bits of ADC configuration data. This register and the ADC Config Data Low Word Register combine to make the 24-bit configuration data either read from or written to one of the configuration registers on the ADC (Configuration, Gain, or Offset registers).

Address: Window Address + 1C (hex)
Type: Read-and-Write
Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
D31	***D30***	***D29***	***D28***	***D27***	***D26***	***D25***	***D24***

7	6	5	4	3	2	1	0
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**

Bit	Name	Description

31-24	D<31..24>	Reserved
23-16	D<23..16>	The most significant 8 bits of ADC configuration data. These bits should be read or written only when the ADC Busy bit in the ADC Status register is 0.

ADC Config Data Low Word Register

This register holds the least significant 16 bits of ADC configuration data. This register and the ADC Config Data High Word Register combine to make the 24-bit configuration data either read from or written to one of the configuration registers on the ADC (Configuration, Gain, or Offset registers).

Address: Window Address + 1D (hex)
Type: Read-and-Write
Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**

7	6	5	4	3	2	1	0
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

Bit	**Name**	**Description**
15-0	D<15..0>	The least significant 16 bits of ADC configuration data. These bits should be read or written only when the ADC Busy bit in the ADC Status register is 0.

Analog Output Register Group

DAC FIFO Data Register

The DAC FIFO Data Register is used to load the desired data into the DAC data FIFO.

The empty, half-full, and full flags from the DAC data FIFO are available in a status register in the DAQ-STC. These flags indicate when the FIFO is empty, half-full, or full, respectively. Whenever the FIFO is not full the host is free to write additional data.

Address: Base address + 14 (hex)
Type: Write-only
Word Size: 32-bit
Bit Map:

31	**30**	**29**	**28**	**27**	**26**	**25**	**24**
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**

23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**

15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

Bit	Name	Description
31–0	D<31..0>	Data bits 31 through 0—The 32-bit data to be written to the DAC data FIFO. This data is interpreted in **straight binary** form. On a 6713 the high 16 bits are the first sample and the low 16 bits are a separate sample. On a 6713, each register write adds two samples to the FIFO. In contrast, for a 6711, this register is only 16 bits, and so each register write adds just one sample to the FIFO.

AO Configuration Register

The AO Configuration Register is used to control the configuration of each AO channel.

Address: Base address + 16 (hex)
Type: Write-only
Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
D15	D14	D13	D12	**DACSEL3**	**DACSEL2**	**DACSEL1**	**DACSEL0**

7	6	5	4	3	2	1	0
D7	D6	D5	D4	**DACLINCAL**	**ExtREF**	**ReGlitch**	**BIP/UNI**

Bit	Name	Description
15-12,7-4	D<15:12,7:4>	Data bits 15-12, 7-4 - Reserved. Always write 0 to these bits.
11–8	DACSEL<3:0>	DAC Select bits - These bits are used to choose the destination DAC for the configuration bits. For example, write 0011 to these bits to select DAC3.
3	DacLinCal	DacLincal bit - Writing a 1 to this bit grounds the reference for all DACs.
2	ExtREF	External reference select bit. Use this bit to choose the reference for the selected DAC. When this bit is 0, the board's internal reference is selected. When this bit is 1, the reference on the IO Connector is selected.
1	ReGlitch	ReGlitch enable - Set this bit to enable the reglitching circuit associated with the selected DAC.
0	BIP/UNI	Bipolar/Unipolar select - Write a 1 to this bit to select Bipolar mode, write a 0 to select Unipolar mode.

AO Configuration][Register

The AO Configuration][Register is used to control the configuration for the AO channels.

Address: Window address + 18 (hex)
Type: Write-only
Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
D15	D14	D13	D12	**DACSEL3**	**DACSEL2**	**DACSEL1**	**DACSEL0**

7	6	5	4	3	2	1	0

D7	**Channel EXTREF**	Reserved	**AC/DC**	**DAC EN**	Reserved	Reserved	Reserved

Bit	**Name**	**Description**
15-12,7	D<15:12,7>	Data bits 15-12, 7 - Reserved
11–8	DACSEL<3:0>	DAC Select bits - These bits are used to choose the destination DAC for the configuration bits. For example, write 0011 to these bits to select DAC3.
6	Channel EXTREF	Channel EXTREF Bit - This bit will enable the channel reference on a per DAC basis.
4	AC/DC	AC/DC coupling - Write a 1 to this bit to select AC coupling. Write a 0 to select DC coupling.
3	DAC EN	DAC Enable bit - Write a 1 to this bit to tri-state the output of the selected DAC.

DAC<0:7> Direct Data Registers

The DAC Direct Data Registers load the desired data directly into the corresponding DAC, without using the DAC data FIFO.

Address:

DAC0 Direct Data Register	Window Address + 00 (hex)
DAC1 Direct Data Register	Window Address + 01 (hex)
DAC2 Direct Data Register	Window Address + 02 (hex)
DAC3 Direct Data Register	Window Address + 03 (hex)
DAC4 Direct Data Register	Window Address + 04 (hex)
DAC5 Direct Data Register	Window Address + 05 (hex)
DAC6 Direct Data Register	Window Address + 06 (hex)
DAC7 Direct Data Register	Window Address + 07 (hex)

Type: Write-only
Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
D15	*D14*	*D13*	*D12*	D11	D10	D9	D8

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	**Name**	**Description**
15-12	D<15:12>	Not used on the PCI-6713. Always write zeros to these bits
11–0	D<11:0>	Data bits 11 through 0 — The 12-bit data to be written to the corresponding DAC itself. This data is interpreted in **straight binary** form.

AO FIFO Offset Load Register

The AO FIFO Offset Load Register sets the depth for the Programmable Full Flag. This controls when DMA transfers use burst or wait state protocol. This register must be written after every DAC FIFO clear. The value 0x06 should be written unless a programmable FIFO depth is being used.

Address: Window address + 13 (hex)
Type: Write-only
Word Size: 32-bit
Bit Map:

31	***30***	***29***	***28***	***27***	***26***	***25***	***24***
D31	***D30***	***D29***	***D28***	***D27***	***D26***	***D25***	***D24***
23	***22***	***21***	***20***	***19***	***18***	***17***	***16***
D23	***D22***	***D21***	***D20***	***D19***	***D18***	***D17***	***D16***
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

Bit	**Name**	**Description**
31–0	D<31..0>	Data bits 31 through 0—These bits set the point in the AO FIFO at which the programmable full flag is set.

AO Timed Register

The AO Timed register is used to configure each DAC for timed update. The DACs power on in immediate mode.

Address: Window address + 10 (hex)
Type: Write-only
Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7	6	5	4	3	2	1	0
DAC7 TIMED	**DAC6 TIMED**	**DAC5 TIMED**	**DAC4 TIMED**	**DAC3 TIMED**	**DAC2 TIMED**	**DAC1 TIMED**	**DAC0 TIMED**

Bit	**Name**	**Description**
15–8	D<15:8>	Data bits 15 through 8 - Reserved, write 0 at all times
7–0	DAC<7:0> Timed	DAC<7:0> Timed select - Write a 1 to configure the corresponding DAC for Timed update. Write a 1 to this bit in the AO Immediate register to configure the corresponding DAC for Immediate Update.

AO Immediate Register

The AO Immediate register is used to configure each DAC for immediate update.

Address: Window address + 11 (hex)
Type: Write-only

Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

7	6	5	4	3	2	1	0
DAC7 Immed	**DAC6 Immed**	**DAC5 Immed**	**DAC4 Immed**	**DAC3 Immed**	**DAC2 Immed**	**DAC1 Immed**	**DAC0 Immed**

Bit	**Name**	**Description**
15–8	D<15:8>	Data bits 15 through 8 - Reserved, write 0 at all times
7–0	DAC<7:0> Immed	DAC<7:0> Immediate select - Write a 1 to configure the corresponding DAC for Immediate update. Write a 1 to this bit in the AO Timed register to configure the corresponding DAC for Timed Update.

Later Single Point Updates

The Later Single Point Updates register is used to configure a DAC so it will receive the timed update pulses at all times if the corresponding bit in the AO Timed Register is also set. Later Mode is normally used when a single point generation is desired on several channels at the same time. The single point on each channel is "saved till later" when the update pulse can synchronize the DACs in later mode. DACs in Later Mode remain in Later Mode after a waveform generation is cleared using the AO Misc Register.

Address: Window address + 14 (hex)
Type: Write-only
Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

7	6	5	4	3	2	1	0
DAC7 Later Enable	**DAC6 Later Enable**	**DAC5 Later Enable**	**DAC4 Later Enable**	**DAC3 Later Enable**	**DAC2 Later Enable**	**DAC1 Later Enable**	**DAC0 Later enable**

Bit	**Name**	**Description**
15–8	D<15:8>	Data bits 15 through 8 - Reserved, write 0 at all times
7–0	DAC<7:0> Later	DAC<7:0> Later select - Write a 1 to place the corresponding DAC into Later Single Point Mode. Write a 0 to remove the corresponding DAC from Later Mode.

AO Waveform Generation Register

The AO Waveform Generation Register is used to place the DAC into Waveform Generation (WG) Mode. This register is used to determine which DACs participate in the WG operation and the order in which they are updated. Successive writes to this register are required to create a multiple-DAC update sequence; the first DAC written to this register will be the first DAC updated during WG.

Address: Window address + 15 (hex)
Type: Write-only
Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	**Dacnum2**	**Dacnum1**	**Dacnum0**

Bit	**Name**	**Description**
15–3	D<15:3>	Data bits 15 through 3 - Reserved, write 0 at all times
2-0	Dacnum<2:0>	DAC0 WG select - These bits controls which DACs participate in WG

Dacnum2	Dacnum1	Dacnum0	DAC Participating
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

AO Misc Register

The AO Misc Register is used for a variety of AO operations. The WG Clr Strobe bit should be written at the end of a WG operation.

Address: Window address + 16 (hex)
Type: Write-only
Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	**AOPFF INTEN**	**WG CLR STRB**

Bit	**Name**	**Description**
15–2	D<15:0>	Data bits 15 through 2 - Reserved, write 0 at all times
1	AOPFF INTEN	AOPFF Interrupt Enable - If this bit is set an interrupt is generated if the AOPFF bit in the Status Register is set. Service this interrupt by writing data to the AO FIFO.

0	WG CLR STRB	Waveform Generation Clear Strobe - Write a 1 to this bit to mask (disable) the update pulse to all DACs that where enabled through the AO Waveform Generation Register. This bit should always be written at the conclusion of a WG operation. DACs in Later Mode will remain in Later Mode (see Later Single Point Updates Register).

AO Cal Chan Sel Register

The AO Cal Channel Select Register is used to select the AO channel for calibration.

Address: Window address + 17 (hex)
Type: Write-only
Word Size: 16-bit
Bit Map:

15	14	13	12	11	10	9	8
Reserved	Reserved	Reserved	Reserved	**REFSEL3**	**REFSEL2**	**REFSEL1**	**REFSEL0**

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	**DACSEL2**	**DACSEL1**	**DACSEL0**

Bit	**Name**	**Description**
15–12	D<15:12>	Data bits 15 through 12 - Reserved, write 0 at all times
11-8	REFSEL<3:0>	Reference Select - These bits select the reference to be used for calibration.

Selection	REFSEL3	REFSEL2	REFSEL1	REFSEL0
Internal Ref	0	0	0	0
Ground	0	0	0	1
Ch0 REF	0	0	1	0
CH1 REF	0	0	1	1
CH2 REF	0	1	0	0
CH3 REF	0	1	0	1
CH4 REF	0	1	1	0
CH5 REF	0	1	1	1
CH6 REF	1	0	0	0
CH7 REF	1	0	0	1

7–3	D<7:3>	Data bits 7 through 3 - Reserved, write 0 at all times
2-0	DACSEL<2:0>	DAC Select bits - These bits are used to select the DAC for calibration. For example, writing 011 to these bits will select DAC3.

DMA Control Register Group

AI AO Select Register

The AI AO Select Register selects the DMA channel used for Analog Output. The contents of this register are cleared upon power up and after a reset condition.

Address: Base address + 09 (hex)
Type: Write-only
Word Size: 8-bit

Bit Map:

7	6	5	4	3	2	1	0
AO CHD	**AO CHC**	**AO CHB**	**AO CHA**	Reserved	Reserved	Reserved	Reserved

Bit	**Name**	**Description**
7–4	AO CH<D..A>	Analog Output DMA Channel D through A—These bits select the DMA channels to be used by analog output. These bits must be set prior to enabling the channel.

Calibration EEPROM Information

This board uses MB88341 CALDACs. Refer to the E-Series RLPM for information on how to address the registers on this type of CALDAC.

8804 CALDACs accept serial data in the same format as 88341 CALDACs, except the order of the address bits is reversed A3,A2,A1,A0 instead of A0,A1,A2,A3.

EEPROM Map for the 6713.

LOC	**DESCRIPTION**
467	Factory CALDAC 9 value - Ch 0 gain
466	Factory CALDAC 5 value - Ch 0 linearity
465	Factory CALDAC 8 value - Ch 0 offset
464	Factory CALDAC 3 value - Ch 1 gain
463	Factory CALDAC 11 value - Ch 1 linearity
462	Factory CALDAC 7 value - Ch 1 offset
461	Factory CALDAC 12 value - Ch 2 gain
460	Factory CALDAC 2 value - Ch 2 linearity
459	Factory CALDAC 10 value - Ch 2 offset
458	Factory CALDAC 6 value - Ch 3 gain
457	Factory CALDAC 1 value - Ch 3 linearity
456	Factory CALDAC 4 value - Ch 3 offset
455	Factory CALDAC 21 value - Ch 4 gain
454	Factory CALDAC 17 value - Ch 4 linearity
453	Factory CALDAC 20 value - Ch 4 offset
452	Factory CALDAC 15 value - Ch 5 gain
451	Factory CALDAC 23 value - Ch 5 linearity
450	Factory CALDAC 19 value - Ch 5 offset
449	Factory CALDAC 24 value - Ch 6 gain
448	Factory CALDAC 14 value - Ch 6 linearity
447	Factory CALDAC 22 value - Ch 6 offset
446	Factory CALDAC 18 value - Ch 7 gain
445	Factory CALDAC 13 value - Ch 7 linearity

444	Factory CALDAC 16 value - Ch 7 offset
443	Factory Calibration Temperature
442	
…	
369	User 1 CALDAC 9 value - Ch 0 gain
368	User 1 CALDAC 5 value - Ch 0 linearity
367	User 1 CALDAC 8 value - Ch 0 offset
366	User 1 CALDAC 3 value - Ch 1 gain
365	User 1 CALDAC 11 value - Ch 1 linearity
364	User 1 CALDAC 7 value - Ch 1 offset
363	User 1 CALDAC 12 value - Ch 2 gain
362	User 1 CALDAC 2 value - Ch 2 linearity
361	User 1 CALDAC 10 value - Ch 2 offset
360	User 1 CALDAC 6 value - Ch 3 gain
359	User 1 CALDAC 1 value - Ch 3 linearity
358	User 1 CALDAC 4 value - Ch 3 offset
357	User 1 CALDAC 21 value - Ch 4 gain
356	User 1 CALDAC 17 value - Ch 4 linearity
355	User 1 CALDAC 20 value - Ch 4 offset
354	User 1 CALDAC 15 value - Ch 5 gain
353	User 1 CALDAC 23 value - Ch 5 linearity
352	User 1 CALDAC 19 value - Ch 5 offset
351	User 1 CALDAC 24 value - Ch 6 gain
350	User 1 CALDAC 14 value - Ch 6 linearity
349	User 1 CALDAC 22 value - Ch 6 offset
348	User 1 CALDAC 18 value - Ch 7 gain
347	User 1 CALDAC 13 value - Ch 7 linearity
346	User 1 CALDAC 16 value - Ch 7 offset
345	User 1 Calibration Temperature
344	User 2 CALDAC 9 value - Ch 0 gain
343	User 2 CALDAC 5 value - Ch 0 linearity
342	User 2 CALDAC 8 value - Ch 0 offset
341	User 2 CALDAC 3 value - Ch 1 gain
340	User 2 CALDAC 11 value - Ch 1 linearity
339	User 2 CALDAC 7 value - Ch 1 offset
338	User 2 CALDAC 12 value - Ch 2 gain
337	User 2 CALDAC 2 value - Ch 2 linearity
336	User 2 CALDAC 10 value - Ch 2 offset
335	User 2 CALDAC 6 value - Ch 3 gain
334	User 2 CALDAC 1 value - Ch 3 linearity
333	User 2 CALDAC 4 value - Ch 3 offset
332	User 2 CALDAC 21 value - Ch 4 gain
331	User 2 CALDAC 17 value - Ch 4 linearity
330	User 2 CALDAC 20 value - Ch 4 offset
329	User 2 CALDAC 15 value - Ch 5 gain
328	User 2 CALDAC 23 value - Ch 5 linearity
327	User 2 CALDAC 19 value - Ch 5 offset

326	User 2 CALDAC 24 value - Ch 6 gain
325	User 2 CALDAC 14 value - Ch 6 linearity
324	User 2 CALDAC 22 value - Ch 6 offset
323	User 2 CALDAC 18 value - Ch 7 gain
322	User 2 CALDAC 13 value - Ch 7 linearity
321	User 2 CALDAC 16 value - Ch 7 offset
320	User 2 Calibration Temperature

Below is the EEPROM Map for the 6711.

LOC	**DESCRIPTION**
467	Factory CALDAC 9 value - Ch 0 gain
466	Factory CALDAC 5 value - Ch 0 linearity
465	Factory CALDAC 8 value - Ch 0 offset
464	Factory CALDAC 3 value - Ch 1 gain
463	Factory CALDAC 11 value - Ch 1 linearity
462	Factory CALDAC 7 value - Ch 1 offset
461	Factory CALDAC 12 value - Ch 2 gain
460	Factory CALDAC 2 value - Ch 2 linearity
459	Factory CALDAC 10 value - Ch 2 offset
458	Factory CALDAC 6 value - Ch 3 gain
457	Factory CALDAC 1 value - Ch 3 linearity
456	Factory CALDAC 4 value - Ch 3 offset
369	User 1 CALDAC 9 value - Ch 0 gain
368	User 1 CALDAC 5 value - Ch 0 linearity
367	User 1 CALDAC 8 value - Ch 0 offset
366	User 1 CALDAC 3 value - Ch 1 gain
365	User 1 CALDAC 11 value - Ch 1 linearity
364	User 1 CALDAC 7 value - Ch 1 offset
363	User 1 CALDAC 12 value - Ch 2 gain
362	User 1 CALDAC 2 value - Ch 2 linearity
361	User 1 CALDAC 10 value - Ch 2 offset
360	User 1 CALDAC 6 value - Ch 3 gain
359	User 1 CALDAC 1 value - Ch 3 linearity
358	User 1 CALDAC 4 value - Ch 3 offset
357	
345	User 1 Calibration Temperature
344	User 2 Reference MSB
343	User 2 Reference LSB
342	User 2 CALDAC 9 value - Ch 0 gain
341	User 2 CALDAC 5 value - Ch 0 linearity
340	User 2 CALDAC 8 value - Ch 0 offset
339	User 2 CALDAC 3 value - Ch 1 gain
338	User 2 CALDAC 11 value - Ch 1 linearity
337	User 2 CALDAC 7 value - Ch 1 offset

336	User 2 CALDAC 12 value - Ch 2 gain
335	User 2 CALDAC 2 value - Ch 2 linearity
334	User 2 CALDAC 10 value - Ch 2 offset
333	User 2 CALDAC 6 value - Ch 3 gain
332	User 2 CALDAC 1 value - Ch 3 linearity
331	User 2 CALDAC 4 value - Ch 3 offset

CalDAC addresses
AD8804 / AO Gain
Load 0,CALDAC 8 (channel 0)
AD8804 / AO Linearity
Load 0,CALDAC 4 , (channel 0)
AD8804 / AO Offset
Load 0,CALDAC 7 , (channel 0)
AD8804 / AO Gain
Load 0,CALDAC 2 , (channel 1)
AD8804 / AO Linearity
Load 0,CALDAC 10 , (channel 1)
AD8804 / AO Offset
Load 0,CALDAC 6 , (channel 1)
AD8804 / AO Gain
Load 0,CALDAC 11 , (channel 2)
AD8804 / AO Linearity
Load 0,CALDAC 1 , (channel 2)
AD8804 / AO Offset
Load 0,CALDAC 9 , (channel 2)
AD8804 / AO Gain
Load 0,CALDAC 5 , (channel 3)
AD8804 / AO Linearity
Load 0,CALDAC 0 , (channel 3)
AD8804 / AO Offset
Load 0,CALDAC 3 , (channel 3)