

NI Single-Board RIO General Purpose Inverter Control (GPIC)



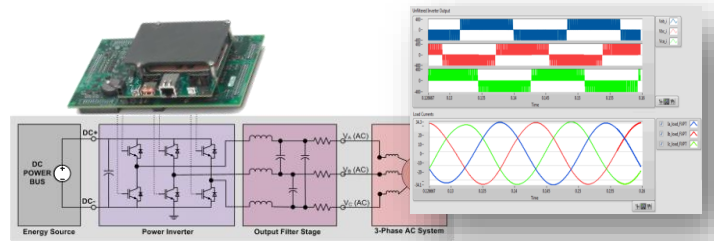
- Industry-proven power electronics control and I/O system with complete development toolchain for industrial power conversion
- Carefully designed to meet both technical and price requirements of high-volume OEM equipment design teams
- Compatible with industry standard SEMIKRON intelligent power modules (SKiiP3, SKiiP4, SEMIKUBE SL, ...)
- Reconfigurable System-On-a-Chip (RSOC) technology with 220 DSP cores: 69x higher performance per dollar than traditional DSPs
- Outperform your competition with the same control and I/O budget
- NI embedded technology quadruples the productivity of embedded design teams: 114-person-month average reduction in development cost
- Get your power conversion equipment to market on time with limited resources
- Integrated power electronics co-simulation, mini-scale control development, analysis/validation and real-time HIL simulation tools
- Complete toolchain for professional OEM equipment design teams
- Hundreds of open source power electronics control IP cores and application examples (AFE with 1547, buck-boost, IBDC, VFD, ...)
- Suitable for any converter topology (bi-directional AFE, DC/AC, AC/DC, DC/DC, buck-boost IBDC, back-to-back AC/DC/AC, modular multi-level)
- Reliable performance in high EMC, rugged, wide temperature industrial equipment deployments
- Long-term assurance against obsolescence with NI 15 year hardware life cycle
- Automatic fault logging and remote system management tools

Development Toolchain (follow links to order)

- [NI sbRIO-9607 Zynq-7020 General Purpose Inverter Controller Industry Development Kit \(academic kit\)](#)
- [NI LabVIEW HIL and Real-Time Test Suite](#) (LabVIEW Pro, RT, FPGA, CD&Sim, Veristand)
- [NI Developer Suite Multisim Circuit Design Option](#) (Multisim/Ultiboard with Co-Simulation)
- [Open Source Linux RT Eclipse C/C++ Toolchain for ARM with LabVIEW FPGA Interface API](#)
- [OpalRT Electrical High Speed Power Electronics Real-Time HIL Simulator](#)

Open Source IP, Designs and Examples (ni.com/powerdev)

- [LabVIEW FPGA open source power electronics IP core and examples library](#)
- [NI GPIC Reference Design Code and Online Training Course](#)
- [LabVIEW FPGA Floating Point Control Engineering Toolkit](#)
- [GPIC Interface Board for Dual SEMIKRON SKiiP3 Power Modules](#)
- [Dual SKiiP3 Replica Mini-Scale Control Development System](#)



Specifications

Xilinx Reconfigurable System-On-a-Chip (RSOC)

- Zynq 7020 RSOC
- 220 DSP cores
- LabVIEW FPGA
- 14,500 MMACS DSP performance
- 85,000 logic cells
- Optional VHDL/Verilog integration

Dual-core 667 MHz ARM Cortex-A9 Processors

- Linux Real-Time Operating System (open source)
- 512 MB DDR3 RAM
- Eclipse C/C++ IDE/BSP or LabVIEW Real-Time IDE/BSP (fully integrated)
- 512 MB Nonvolatile Flash Storage, Reliance file system

Communication Ports

- Gigabit Ethernet
- CANbus
- RS-232 Serial
- USB 2.0, Hi-Speed (additional storage)

Physical Characteristics

- 11.9x17.9x4.4 cm
- -40 to 85 °C local ambient op. temp.

Half-Bridge Digital Output (to IPM or Gate Driver)

- 14 channels source/sink (push-pull)
- 5-30 V, external power
- Up to 500 kHz switching freq. ($C_{LOAD} = 0.47$ nF)
- Up to 5 ns PWM resolution
- 100 Ω output impedance
- 10 ns no load rise/fall time
- 10 mA/ch continuous
- ≤ 100 ns propagation delay ($V_{ext} = 15$ V, $C_{LOAD} = 50$ pF)
- Non-isolated, no overcurrent or short-circuit protection
- Glitch-free power up state: OFF

Sourcing Digital Input

- 28 channels, sourcing digital input
- 3-6 V or 10-24 V range
- 4 μ s max update time
- Non-isolated, ± 30 V protection
- 4.32 k Ω pull-up resistors

LVTTTL Digital Input/Output

- 32 channels, FPGA IOBs
- 3.3 V DIO, non-buffered
- Unprotected, 800 MHz max
- Non-isolated FPGA IOBs

Sinking and Relay Control Digital Output

- 28 channels total
- Sinking driver, 0-30 V
- 50 μ s max update time
- 20 mA/ch continuous
- Power up state: Open
- Relay Control DO:
 - 4 of the 28 channels, isolated
 - 8 A/ch inrush, 300 ms max, 60 s interval
 - 500 mA continuous

Simultaneous Analog Input

- 16 simultaneous channels, pseudo differential, 12-bit
- 115 kS/s per ch, single rate
- ± 4.95 V or ± 9.9 V range
- ± 30 V protection, 1.5 mV_{RMS} noise
- 0.39% (38.5 mV) typ. accuracy for ± 5 V range, 2.44 mV resolution
- 0.32% (65.5 mV) typ. accuracy for ± 10 V range, 4.88 mV resolution
- 210 kHz -3 dB bandwidth, 60 VDC CAT I bank isolation

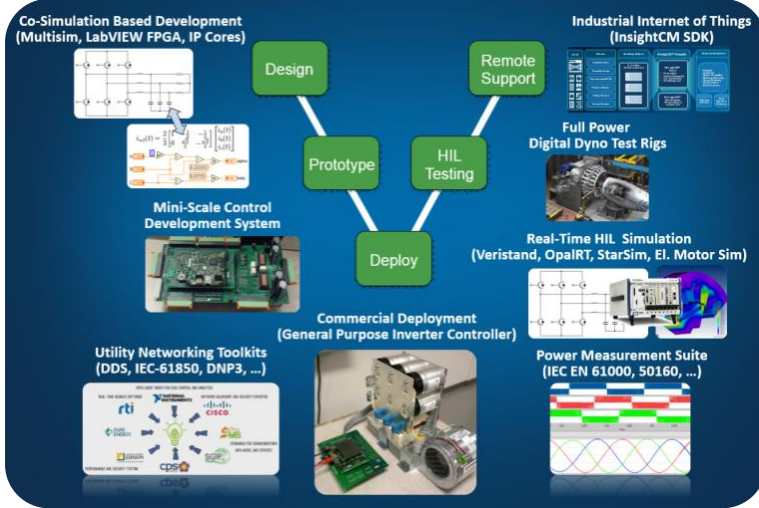
Scanned Analog Input

- 8 single-ended channels
- 12-bit, 0-4.97 V range
- Multiplexed sampling
- 1 kS/s scan rate, all chan.
- 0.06% typical accuracy
- 10 k Ω input impedance, < 2 k Ω source impedance recommended
- Non-isolated, ± 30 V protection

Analog Output

- 8 single-ended channels
- 12-bit, 0-4.97 V range
- Simultaneous update
- 1 kS/s update rate
- 0.12% typical accuracy
- 4 mA/ch output current
- Power on state: 0 V
- Non-isolated, $\pm 15/-5$ V protection

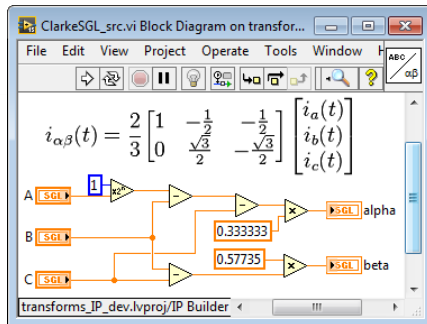
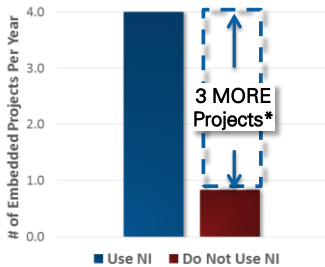
Complete Toolchain for OEM Design Teams



FPGA IP and Examples Libraries (download)

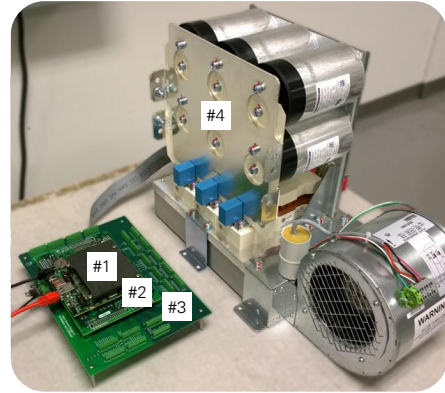
- Dozens of open source example apps. Examples: 3-phase bidirectional active front end (AFE), induction motor VFD (V/Hz, FOC), buck-boost energy storage converter, isolated bidirectional DC (IBDC), ...
- Hundreds of open source IP cores. Examples: Field oriented control transforms (i.e. ABC to DQ), sine-triangle PWM, space-vector PWM, PID control, 1547 anti-islanding, FRF control stability analyzer, ...
- [StarSim Control IP Library and Power System Simulator](#)

What More Could You do with 3 Additional Embedded Projects/Year with the Same Development Budget?

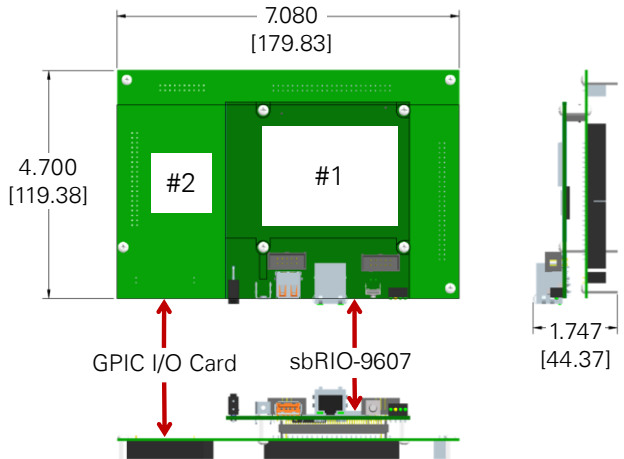


Typical Configuration (user manual links)

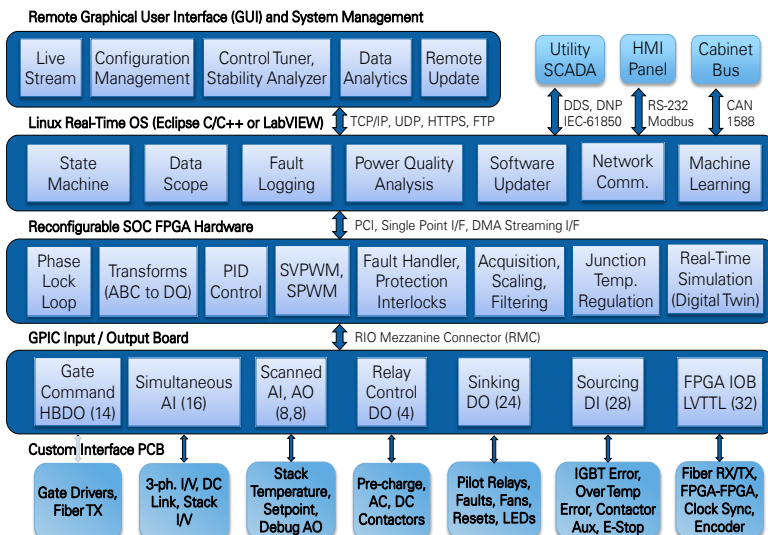
1. [NI sbRIO-9607 Zyng-7020 Reconfigurable System-On-a-Chip \(RSOC\) Control System](#) (with heat spreader thermal kit)
2. [NI GPIC 9683 Input/Output Board](#) (download CAD files)
3. [GPIC Interface PCB for Dual SEMIKRON SKiiP3 Power Modules](#) (open source interface PCB template)
4. [SEMIKRON Intelligent Power Module Stack](#)



- sbRIO-9607 thermal kit heat spreader (#1) mounts to cabinet panel
- GPIC I/O Board (#2) IDC headers mates to custom interface PCB (#3)



Typical Hardware/Software Architecture



Mini-Scale Control Development System (info)

- Full scale power converter control code is rapidly developed and tested using the mini-scale system
- Open source design with back-to-back 3-phase inverter IPMs, full bridge rectifiers, pre-charge contactors, DC link capacitors, built-in voltage/current/temp sensors, jumper support for external sensors

