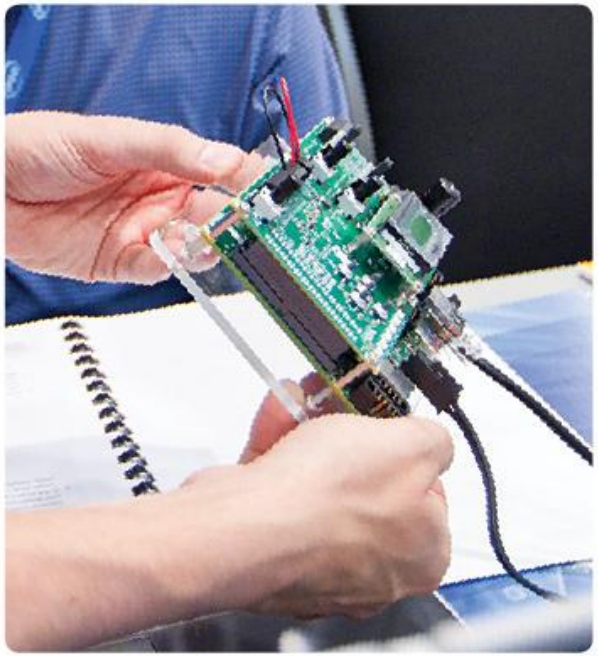

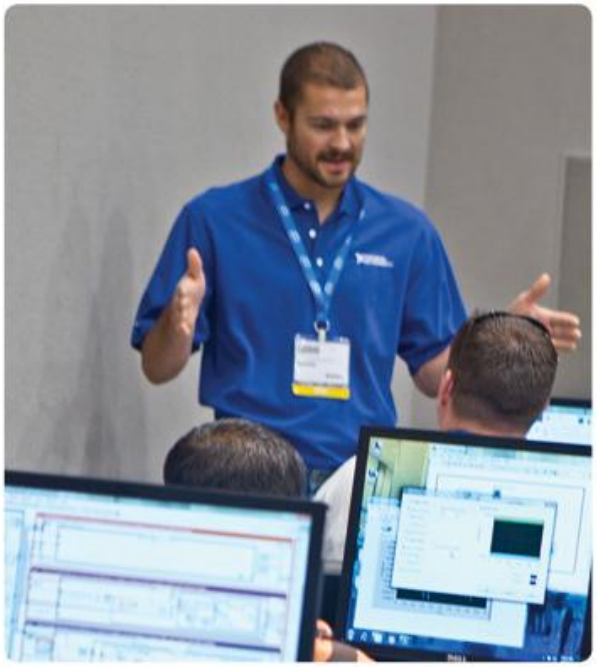

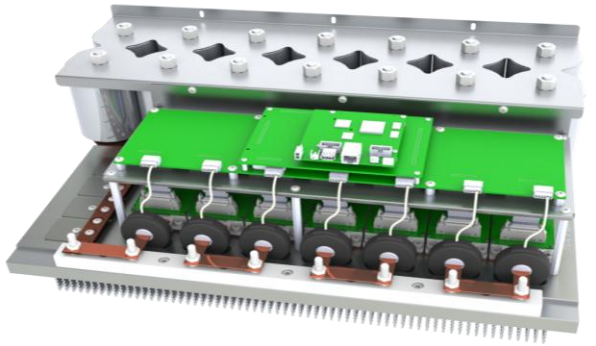

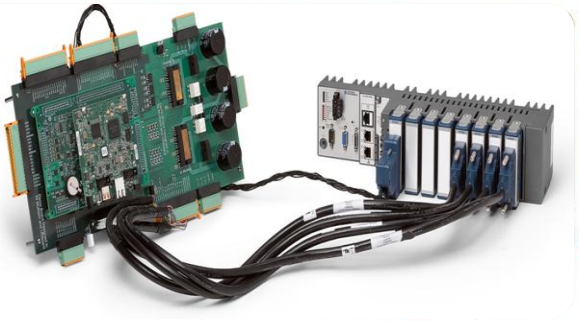

NI Power Electronics Control Design V Training Workshop

ni.com/powerdev

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NI Power Electronics Control Design V Training Workshop

Pre- Requisites

If you hit a snag or have questions, make a note of it and move on to the next exercise. Email your notes to the instructor when finished.

1. Install the development tools on your computer. Follow the instructions in the PDF document below. Install in evaluation mode.

Download and install the NI development tools and NI CompactRIO Driver Software

2. Review the introduction to LabVIEW tutorials:

Introduction to NI LabVIEW

3. Complete the introduction to Multisim exercise:

Introduction to Multisim: Learn to Capture and Simulate in Less Than 30 Minutes

4. Complete the introduction to FPGA co-simulation exercise, beginning with part 3.

Introduction to Digital and Analog Co-simulation Between NI LabVIEW and NI Multisim

5. Download and unzip the power electronics hands on training software and instruction manual.

Download and unzip the training software (NI GPIC Reference Design Project)

(You must unzip to a short directory path such as C:\PowerDev.)

Download the instruction manual

[Discussion]
Open questions from pre-requisite work?

NI Power Electronics Control Design V Training Workshop

Workshop Agenda

1. Power Electronics
2. NI Design V Toolchain
3. Training Kits & Reference Design
4. The NI LabVIEW RIO Approach
5. Hands On Modules 1-3
6. Case Studies & Latest Releases

Hands-On Exercises

Module 1: Single Phase Power Conversion

1. Configuring your NI RIO Embedded System
2. Understand the GPIC Reference Design App.
3. Half-Bridge DC-to-AC Inverter Control
4. Pulse Width Modulation Logic
5. Sine-Triangle Pulse Width Modulation
6. Comparing Simulated vs. Experimental Results

Module 2: Three Phase Grid Synchronized Inverter Control

1. Understanding 3-Phase Power and the PLL
2. 3-Phase DC-to-AC Inverter Control
3. Comparing Simulated vs. Experimental Results
4. Grid Synchronized Inverter Control

Module 3: AC Induction Motor Control

1. Understanding the 3-Phase AC Induction Motor
2. Sine-Triangle AC Induction Motor Control
3. Comparing Simulated vs. Experimental Results
4. Voltage-over-Frequency Control
5. PID Control Tutorial

Module 4: Power Electronics Real-Time HIL Simulation

1. LabVIEW FPGA Floating Point Math Palette
2. Transfer Function and State-Space Modeling
3. Single-Phase Inverter HIL (Transfer Function)
4. Three-Phase Inverter HIL (State-Space)
5. AC Induction Motor HIL (Custom)
6. Automatic Multisim-to-FPGA Conversion HIL

Power Electronics

The Digital Energy Revolution

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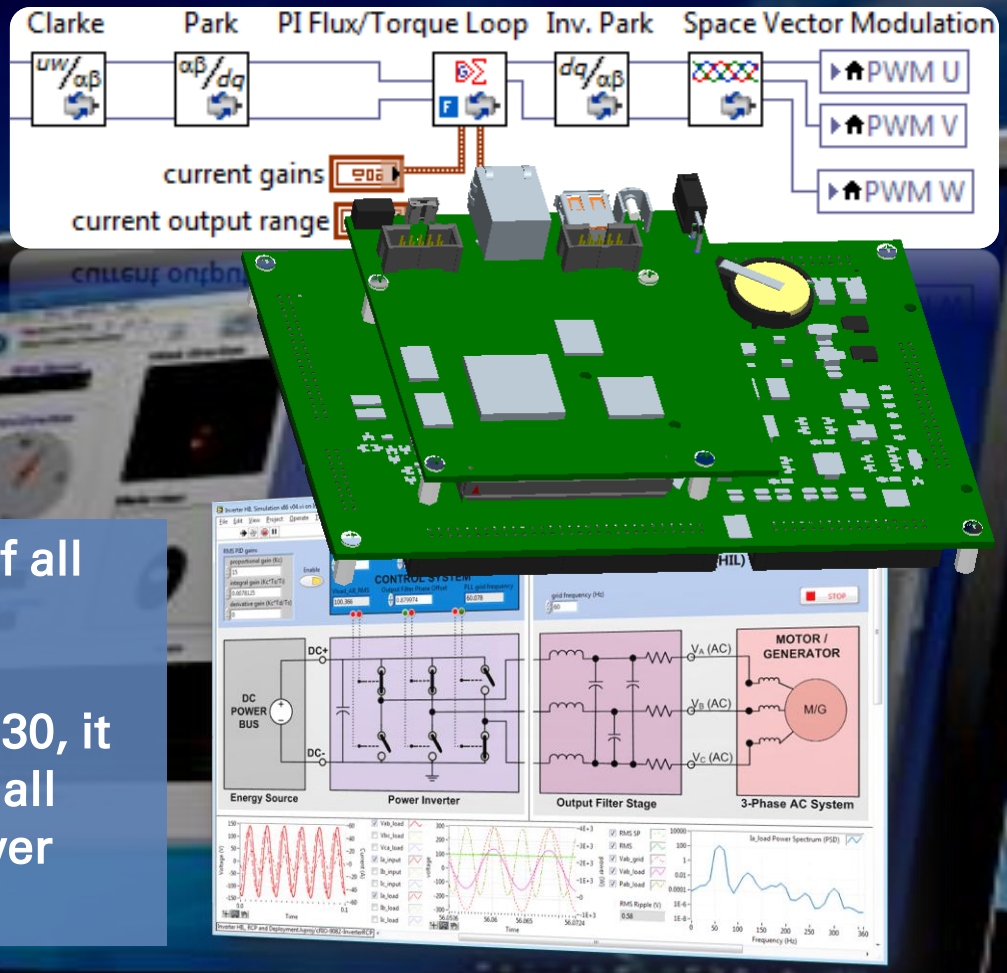
The Digital Energy Revolution

- Digitized and digitally controlled
- Networked
- Field reconfigurable
- Modeled and simulated
- Improving at exponential rates



"Today, approximately 30 percent of all power generation utilizes power electronics between the point of generation and consumption. By 2030, it is expected that up to 80 percent of all generated electricity will utilize power electronics." –US Dept. of Energy

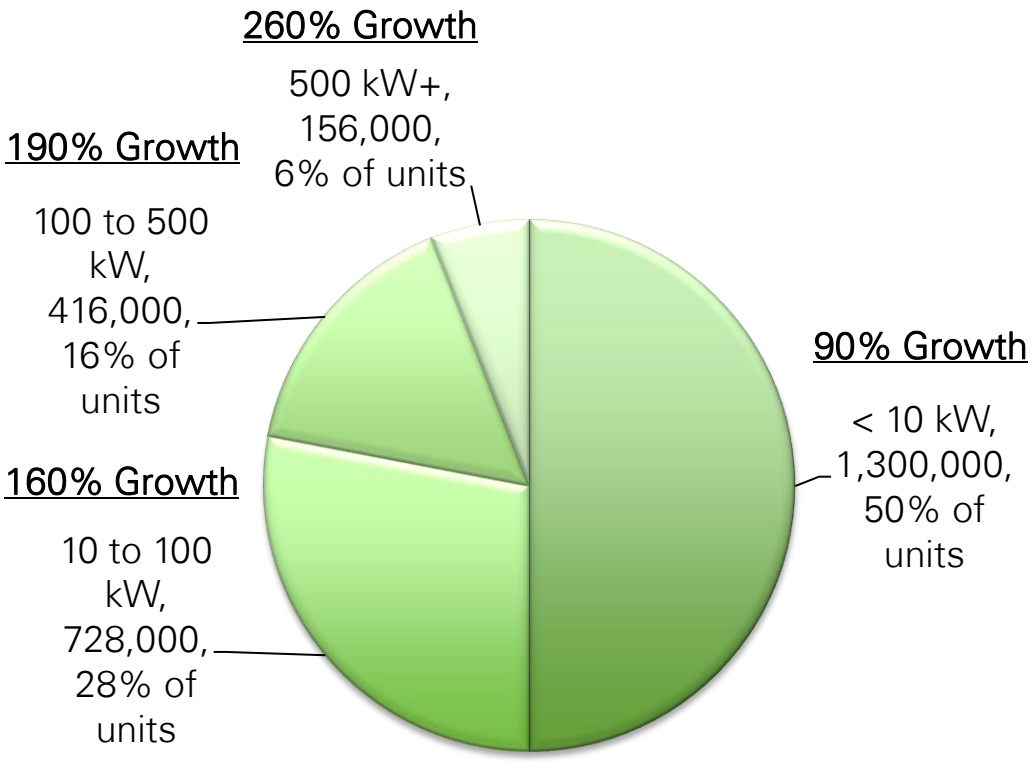
Join the developer community at ni.com/powerdev

2020 compared to 2000…

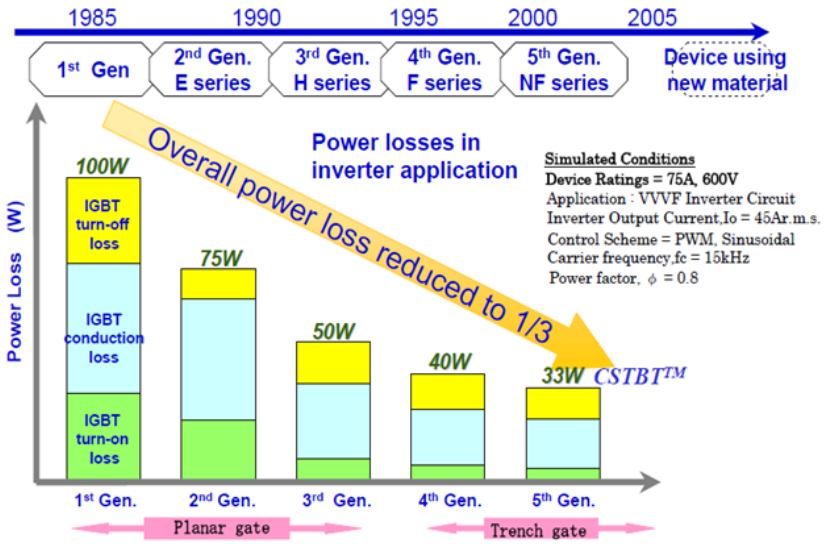
- Processing performance is 113 thousand times cheaper per dollar
- A power converter controls 27 times more power for its size
- Lithion-Ion batteries deliver 29 times more energy storage (kWh) per dollar
- Typical inverters are 99.5% efficient (3.4 times less waste heat)
- Solar module cost is 110 times cheaper per watt, solar installed cost is 24 times cheaper per watt
- Overall inverter market is expected to be ~$75B in 2020 (currently ~$44B)

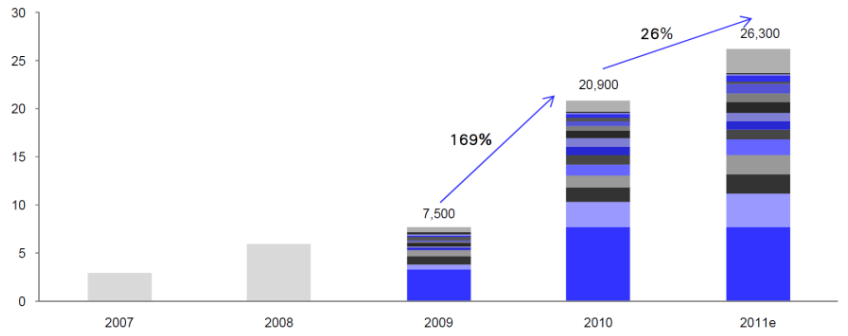
The Power Electronics Renaissance

"Since the industrial revolution I do not know of a single financial push towards a solitary focus as large as renewable energy outside of war."- Glenn A. Knierim, Ph.D., founder of Infinity Physics



2010 INVERTER UNITS AND GROWTH RATE BY INVERTER SIZE (kW)

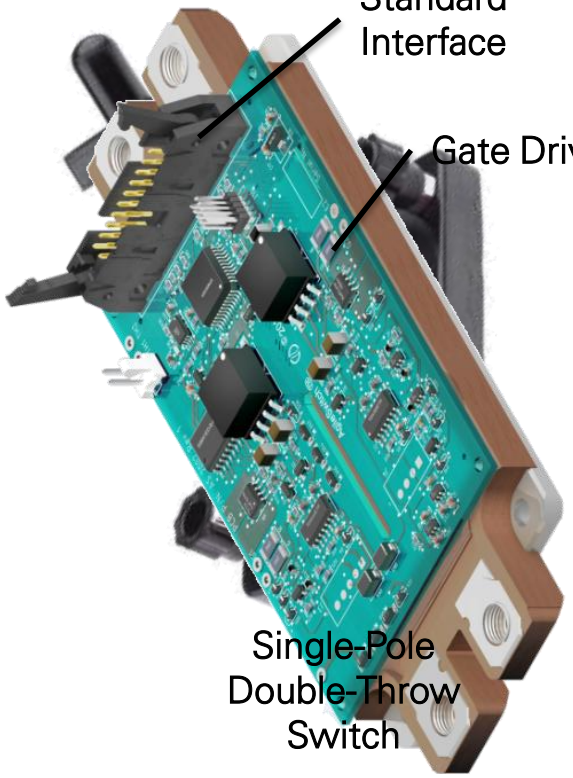




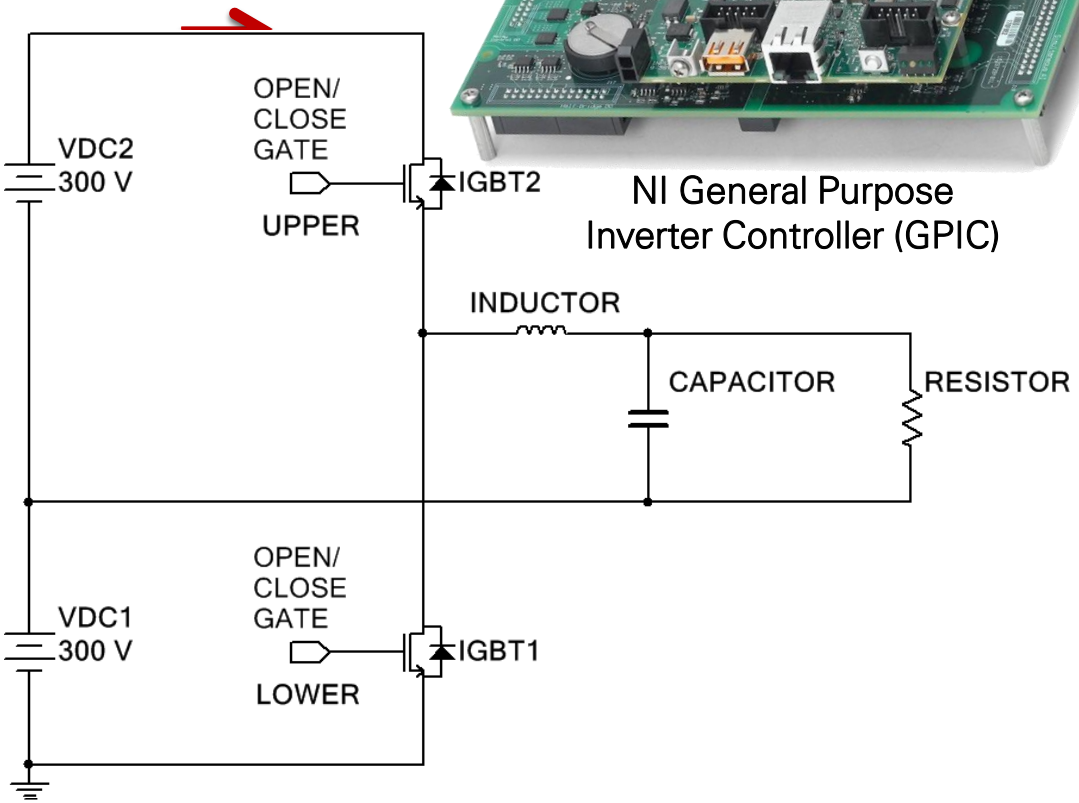
INVERTER SHIPMENTS (MWp)

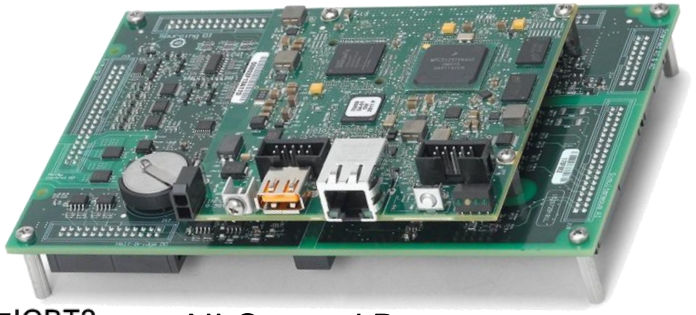
Inverter Control Crash Course

Understand Power Electronics in 5 Minutes



Half-Bridge IGBT Module (Econodual)

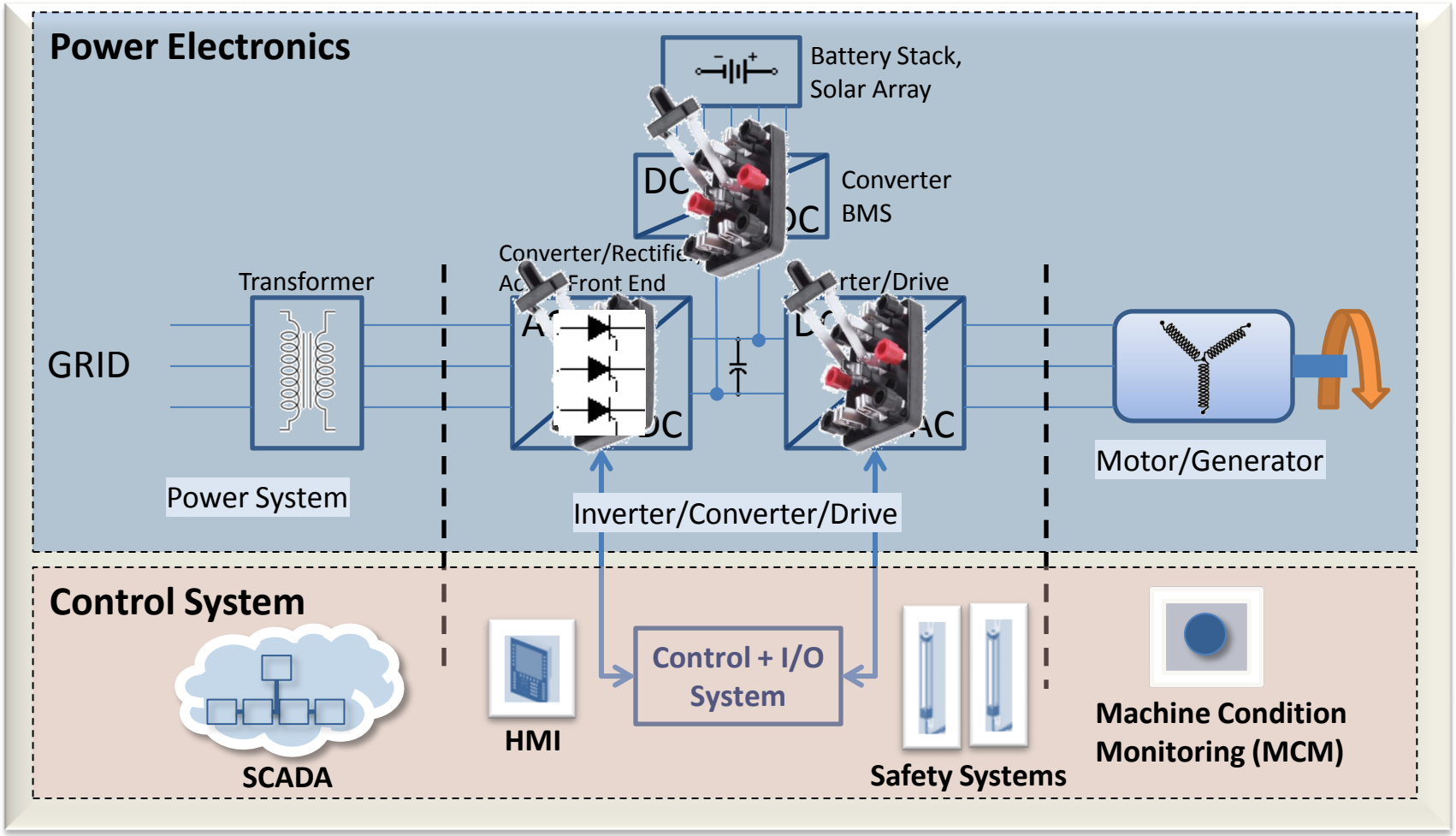




NI General Purpose Inverter Controller (GPIC)

Putting It All Together

Complete Inverter Control System



NI Power Electronics Design V Toolchain

A Formal Approach to Embedded Systems Design

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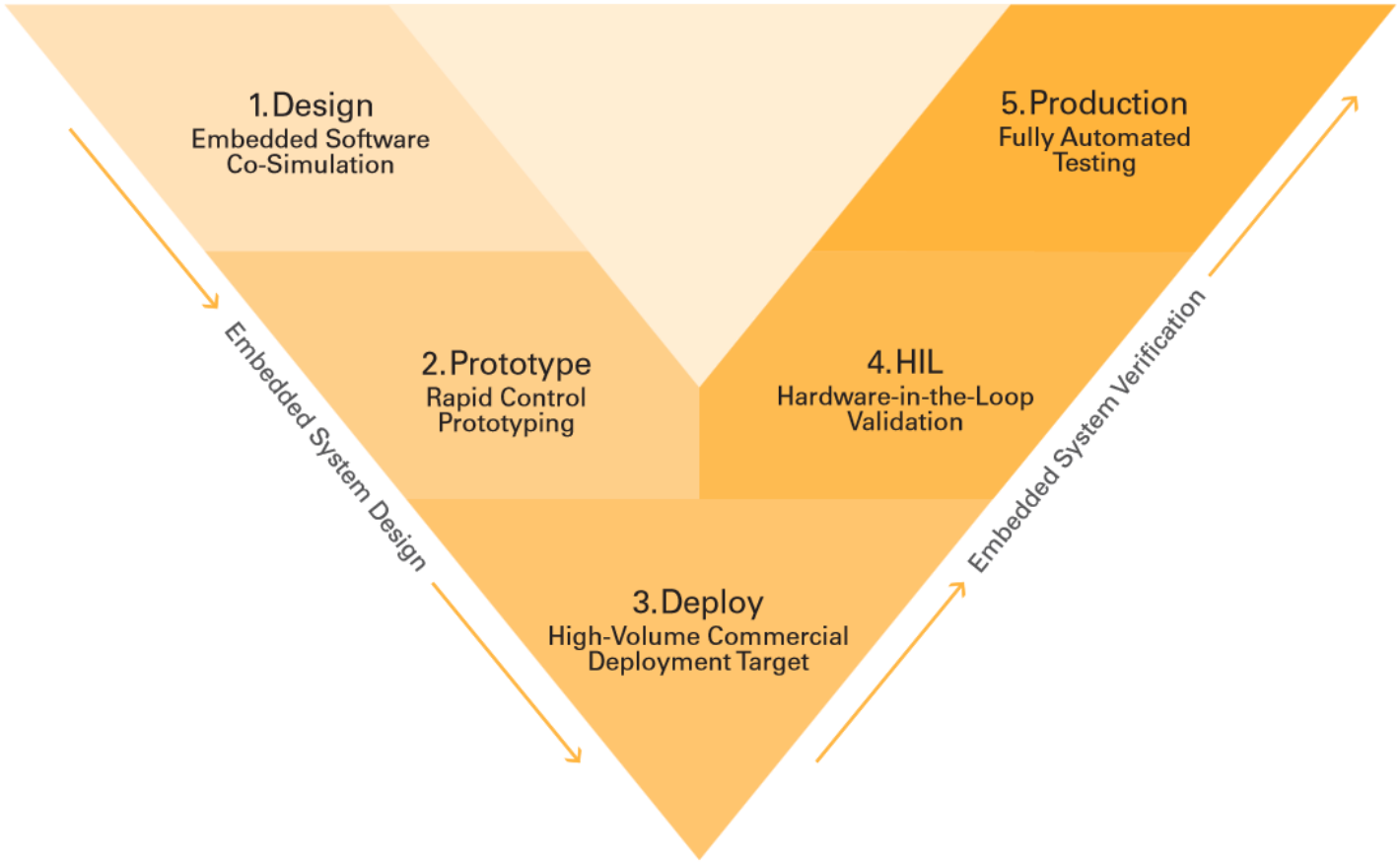
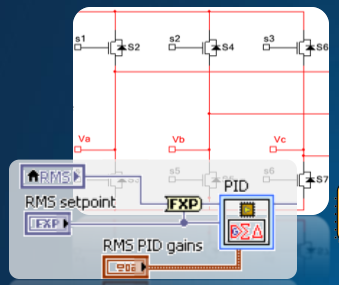
Design V Approach to Embedded System Design



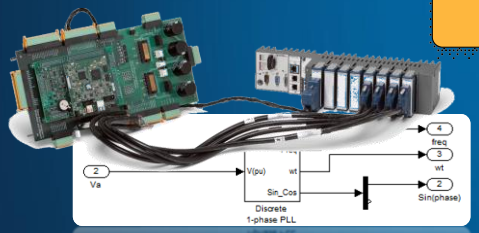
- The Design V Process represents the standard for repeatable methodology within embedded system design. Its use of system-level design, verification tools, and reconfigurable COTS embedded systems not only enables cost and risk reduction, it also helps teams focus on new features and innovations by exponentially increasing performance per dollar.

NI Power Electronics Control Design V Toolchain

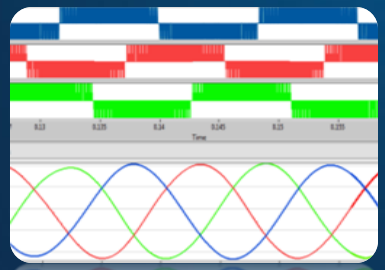
Graphical Co-Simulation (Multisim, LabVIEW FPGA)



Rapid Control Prototyping (CompactRIO, Veristand)



Power Measurement Suite (IEC EN 61000, 50160, …)



Design

Prototype

Deploy

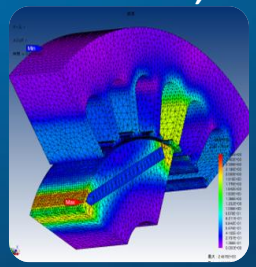
Test Cells

HIL Testing

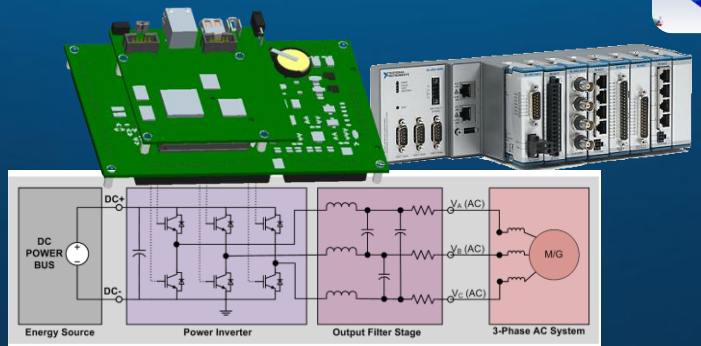
Deployed System Management & Remote Monitoring

Full Power HIL Simulation

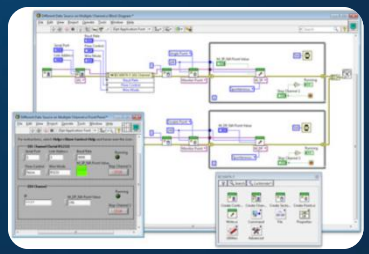
Real-Time HIL Simulation (StarSim, FPGA Motor Sim, FPGA TF/SS Solvers)



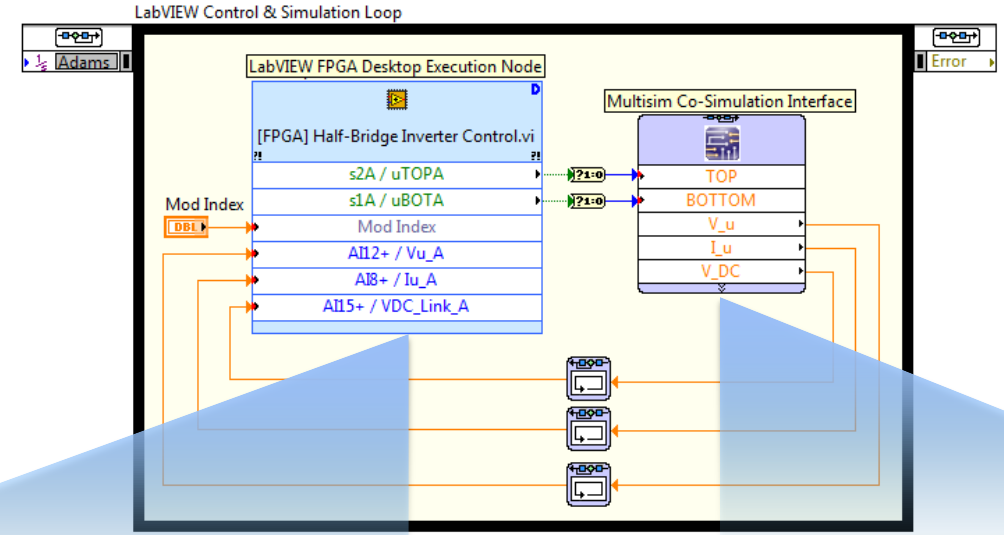
Commercial Deployment (General Purpose Inverter Controller)

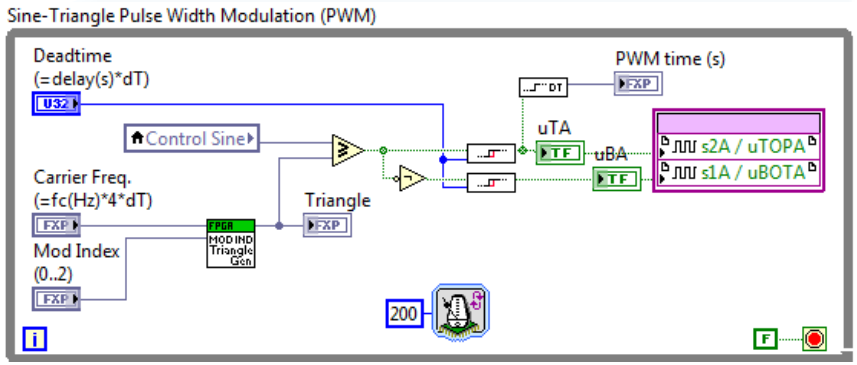


Utility Networking (IEC-61850, DNP3, …)

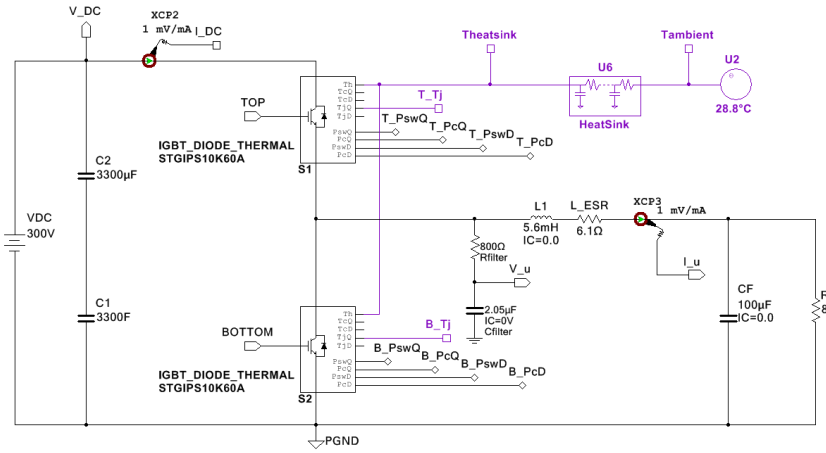


Cyber-Physical System Co-Simulation





Time Adaptive Synchronized Co-Simulation (TASCS)



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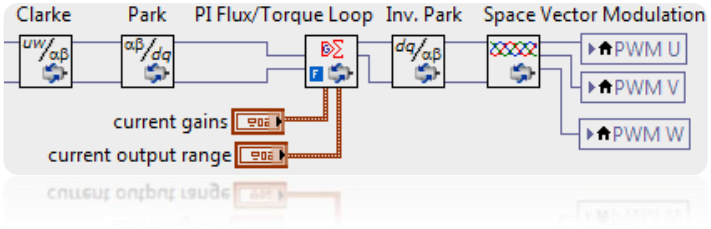
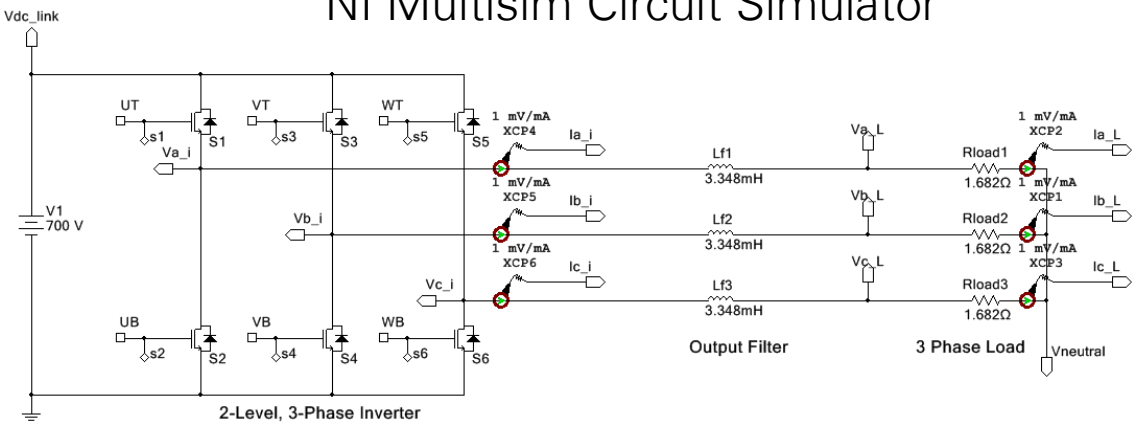
PATENTED TIME-ADAPTIVE SYNCHRONIZED CO-SIMULATION (TASCS)

ACCURATE SIMULATION OF CYBER-PHYSICAL SYSTEM DYNAMICS

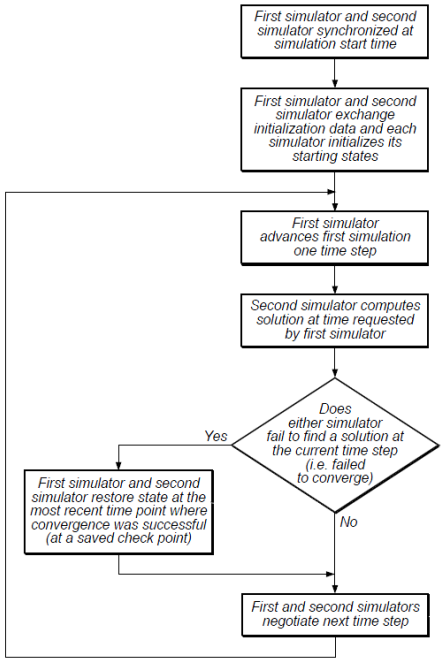
NI LabVIEW FPGA Simulator

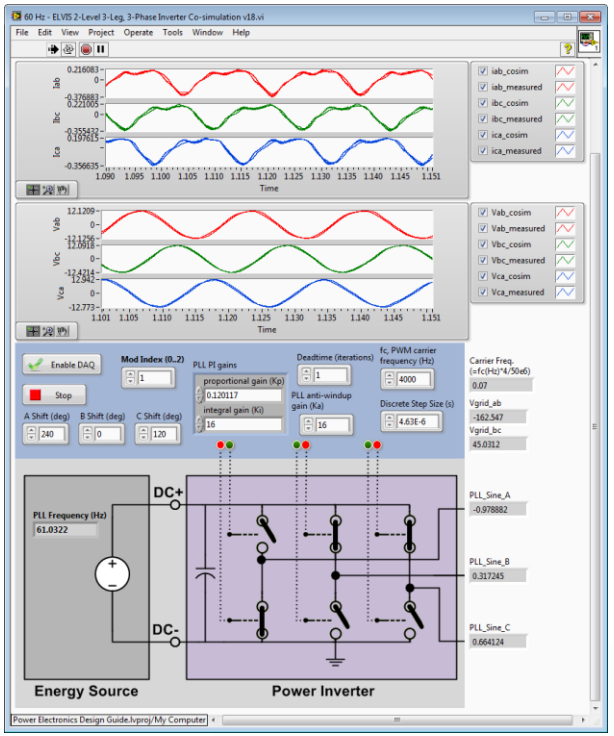


NI Multisim Circuit Simulator

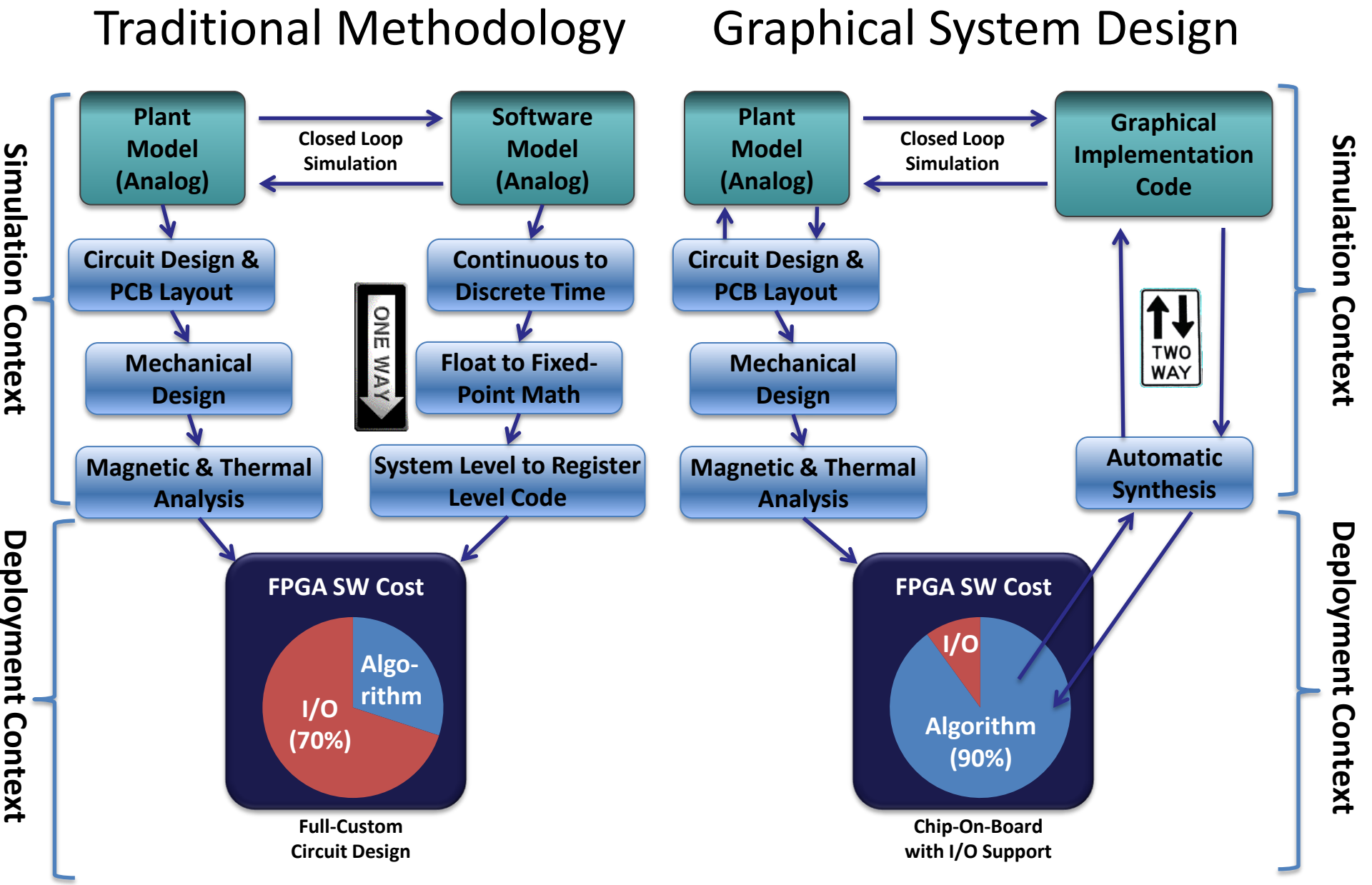


- TASCS enables accurate, time synchronized co-simulation of the FPGA and switched-mode power electronics, automatically adapting for fast transient events such as faults and short-circuits.





The Evolution of System Level Design



Accelerating Cyber-Physical Systems Design

E POWER SWISS

ONE YEAR FROM CO-SIMULATION TO HIGH VOLUME PRODUCTION

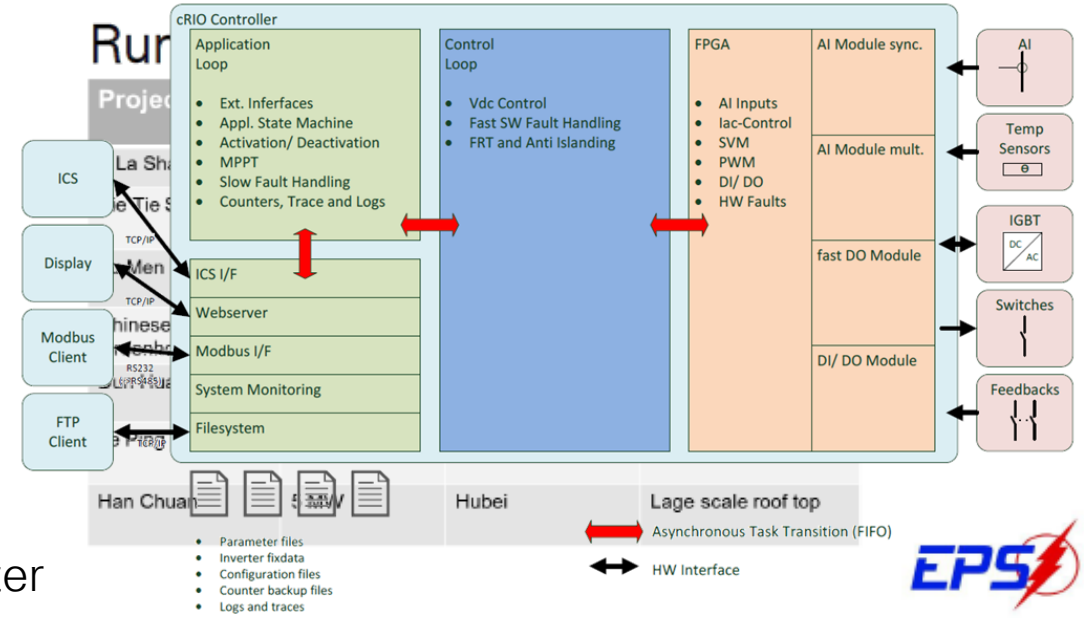
We will tell you the story about

- ➥ Developing a 500kW PV-inverter
- ➥ Setting-up a factory in China
- ➥ Make the prototypes
- ➥ Passing the certifications
- ➥ Commissioning the zero series

- Accurate cyber-physical co-simulation accelerated project
- Remote access to inverters deployed in China
- Over 120 megawatts deployed in first two years

…all within 1 year

EPS 500 kVA Solar Inverter



EPS

helbling

NI LabVIEW RIO Approach vs. Conventional Full Custom Embedded Design

- **Wilson Research Study**

	NI Embedded Customers (2012)[1]	EETimes Overall Embedded Market (2012)[2]	Ratio
Average Development Team Size (HW, SW, Firmware Engineers)	4.8	11.5	2.4
Average Months to Complete Project	6.2	12.5	2.0
Average Person-Months to Complete Project	30	144	4.8 (average of 114 person-month savings per design)
Average Development Cost (assuming $100k/person/year with overhead)	$248,000	$1,198,000	4.8 (average $950,000 cost savings per design)
Percent of Projects Completed On or Ahead of Schedule	58% of NI customers	42% of embedded market	0.7
Percent of Projects Completed Behind Schedule/Late	38% of NI customers	55% of embedded market	1.4

NOTE1: The overall embedded market study was a global Email/web study including over 1,700 responses from embedded engineers from Americas, Europe and Asia
NOTE2: The study of NI embedded customers was a global Email/web study including over 1,100 responses NI embedded customers from Americas, Europe and Asia

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NI Power Electronics Control Design V Training Workshop

Workshop Agenda

1. Power Electronics
2. NI Design V Toolchain
3. Training Kits & Reference Design
4. The NI LabVIEW RIO Approach
5. Hands On Modules 1-3
6. Case Studies & Latest Releases

Hands-On Exercises

Module 1: Single Phase Power Conversion

1. Configuring your NI RIO Embedded System
2. Understand the GPIC Reference Design App.
3. Half-Bridge DC-to-AC Inverter Control
4. Pulse Width Modulation Logic
5. Sine-Triangle Pulse Width Modulation
6. Comparing Simulated vs. Experimental Results

Module 2: Three Phase Grid Synchronized Inverter Control

1. Understanding 3-Phase Power and the PLL
2. 3-Phase DC-to-AC Inverter Control
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4. Grid Synchronized Inverter Control

Module 3: AC Induction Motor Control

1. Understanding the 3-Phase AC Induction Motor
2. Sine-Triangle AC Induction Motor Control
3. Comparing Simulated vs. Experimental Results
4. Voltage-over-Frequency Control
5. PID Control Tutorial

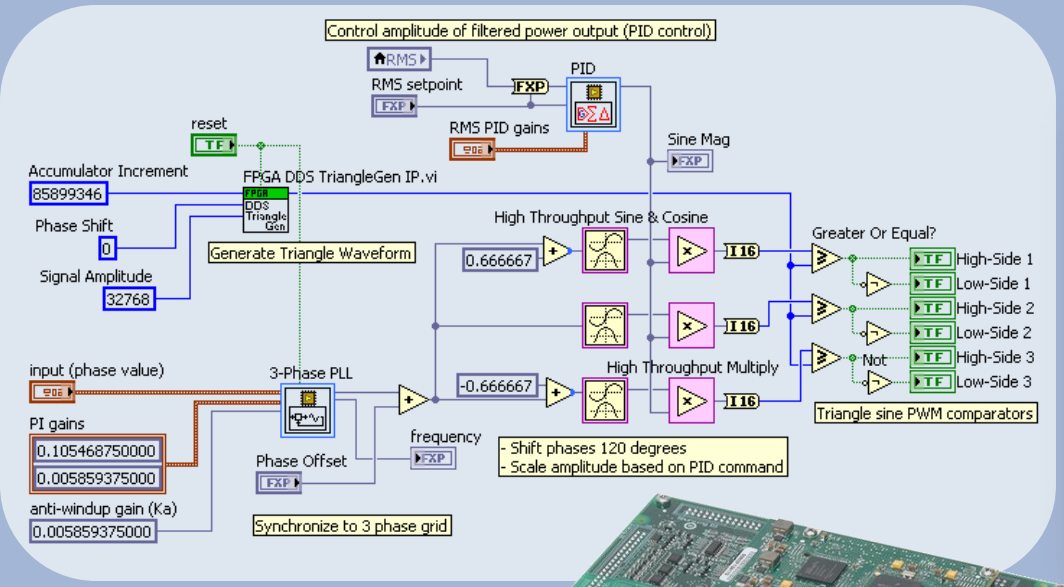
Module 4: Power Electronics Real-Time HIL Simulation

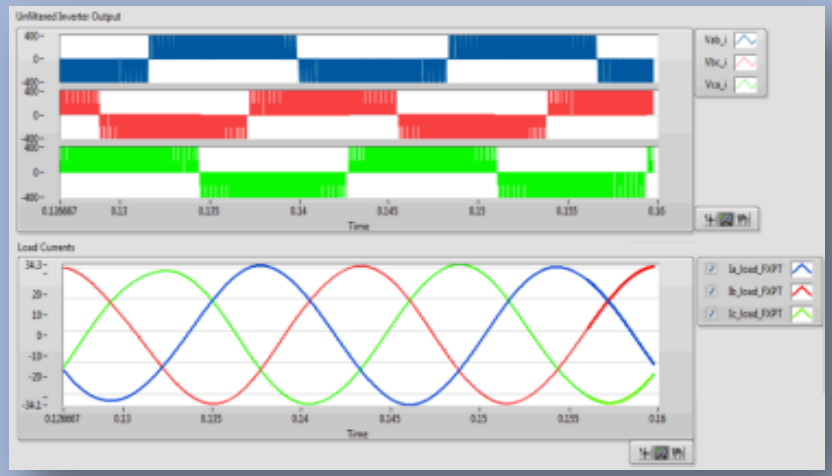
1. LabVIEW FPGA Floating Point Math Palette
2. Transfer Function and State-Space Modeling
3. Single-Phase Inverter HIL (Transfer Function)
4. Three-Phase Inverter HIL (State-Space)
5. AC Induction Motor HIL (Custom)
6. Automatic Multisim-to-FPGA Conversion HIL

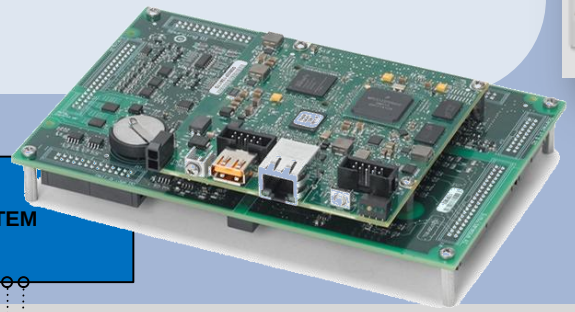
Power Electronics Training Kits

NI sbRIO General Purpose Inverter Controller (GPIC)

NI Single-Board RIO General Purpose Inverter Controller (GPIC)



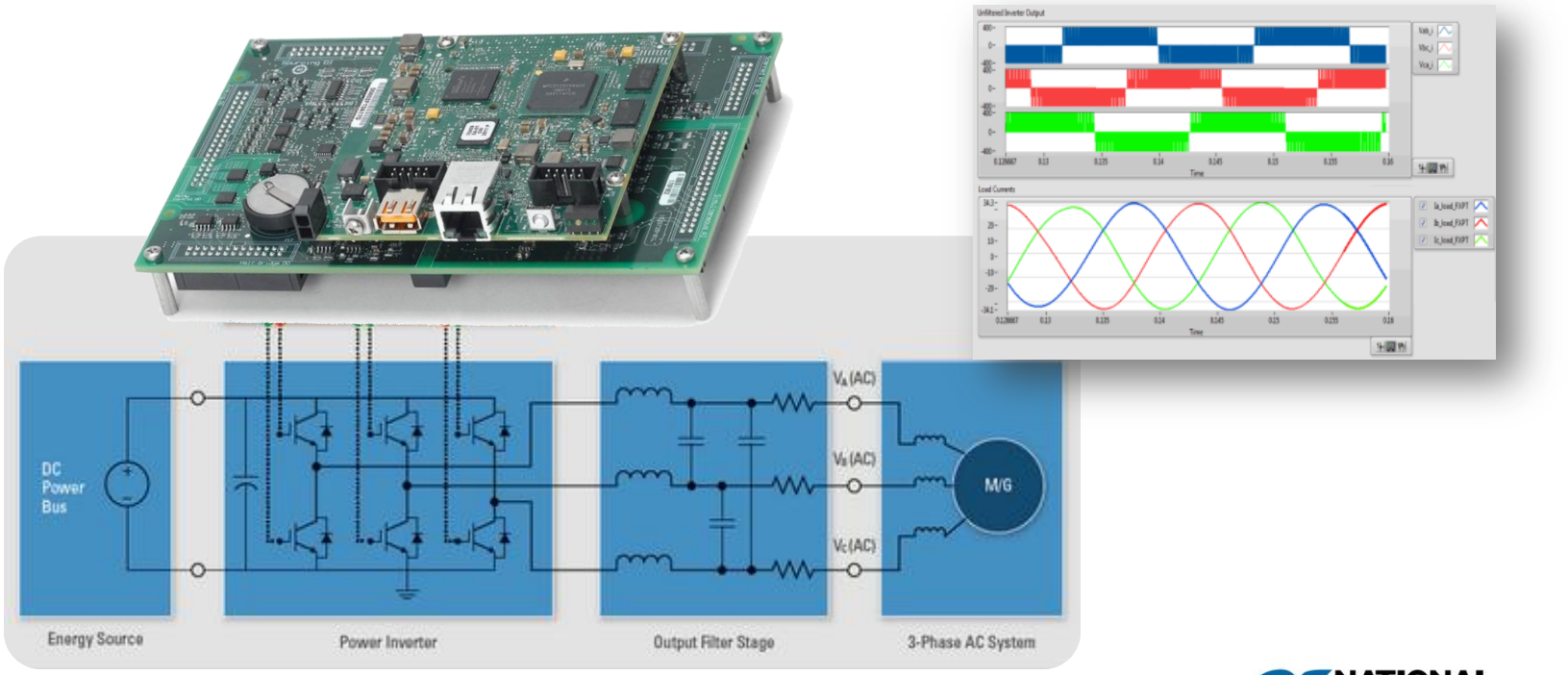




NREL
NATIONAL RENEWABLE ENERGY LABORATORY

NI Single-Board RIO General Purpose Inverter Controller (NI GPIC)

- Industry-proven NI LabVIEW RIO architecture and cutting-edge co-simulation tools
- Deployment-ready for high volume commercial applications
- Heterogeneous FPGA with 58 DSP cores delivers 40x higher performance per dollar than traditional DSPs



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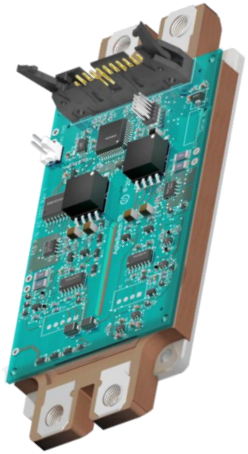
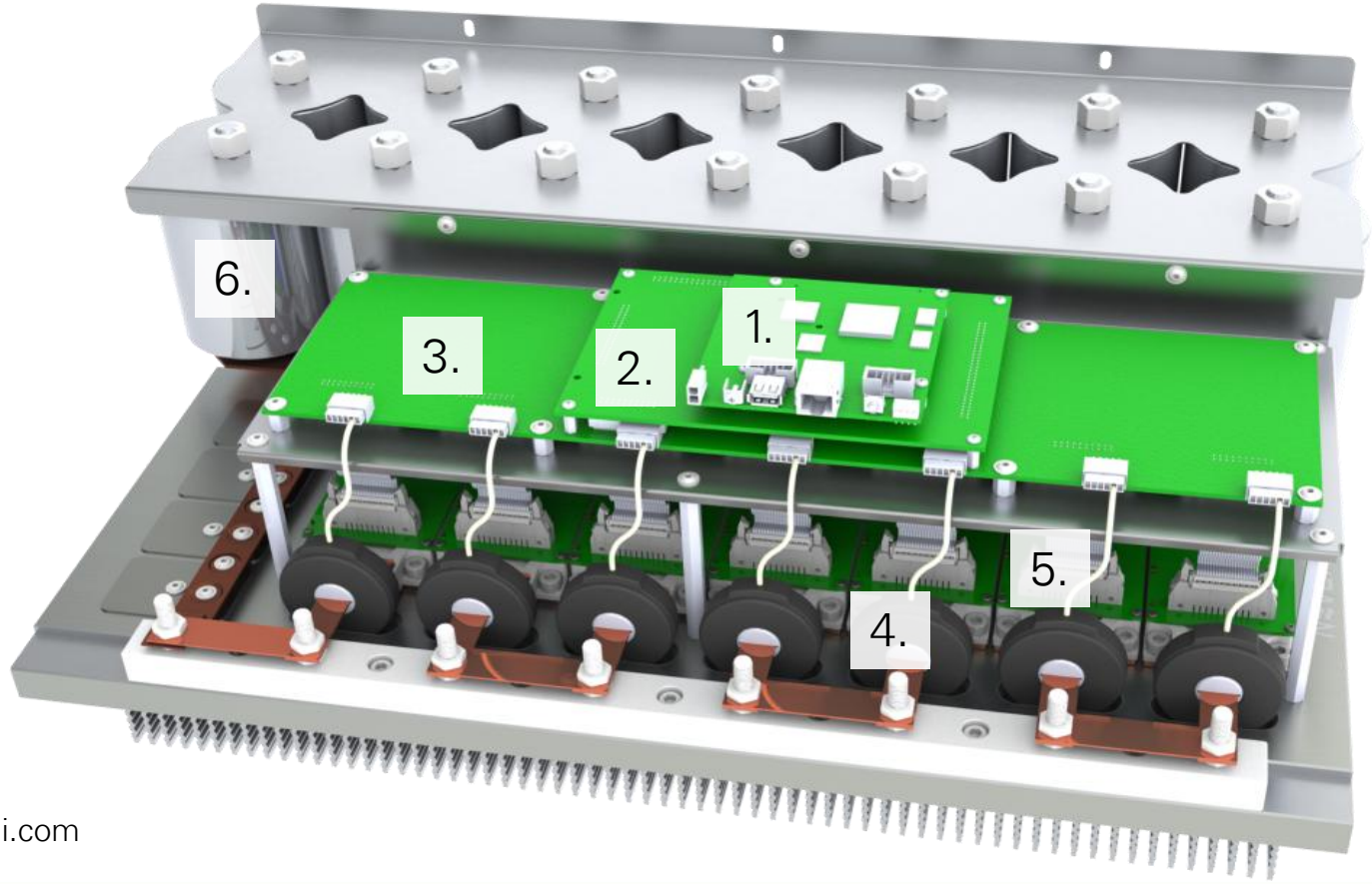
Typical Application

1. NI Single-Board RIO sbRIO-9606 (FPGA, PowerPC, Network)
2. NI GPIC 9683 RIO Mezzanine Card (bottom orientation connectors)
3. Custom interface or gate drive PCB (template available)
4. Isolating sensors
5. IGBT modules or Power Stack
6. DC link capacitors





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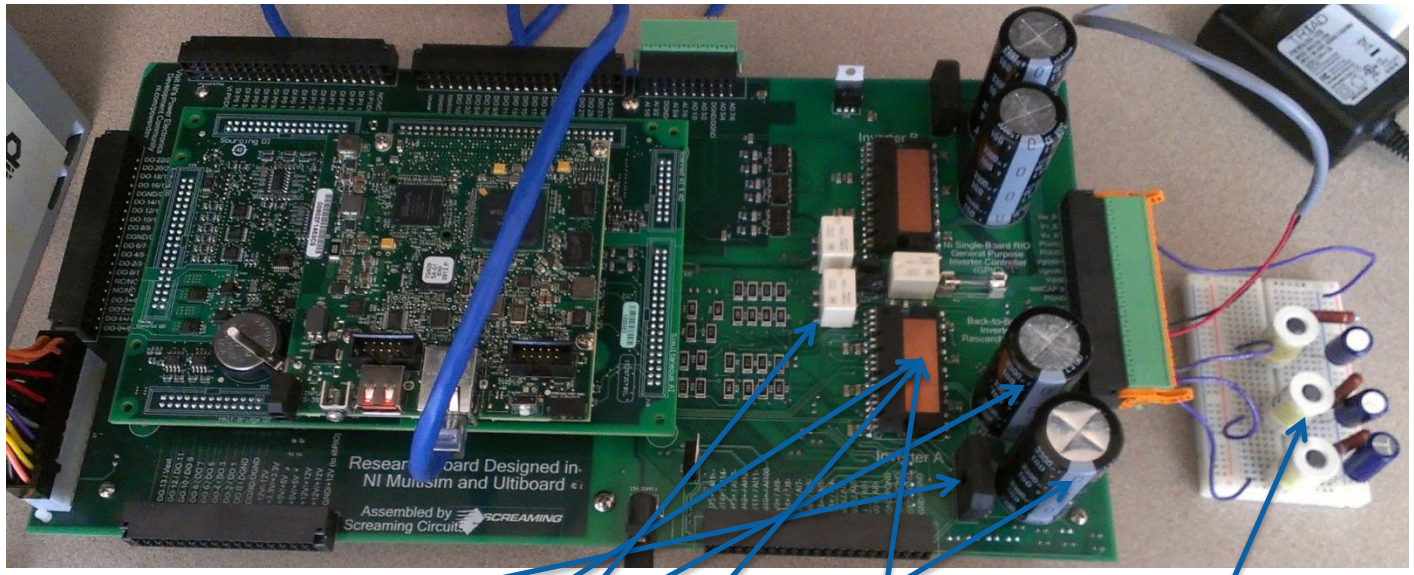
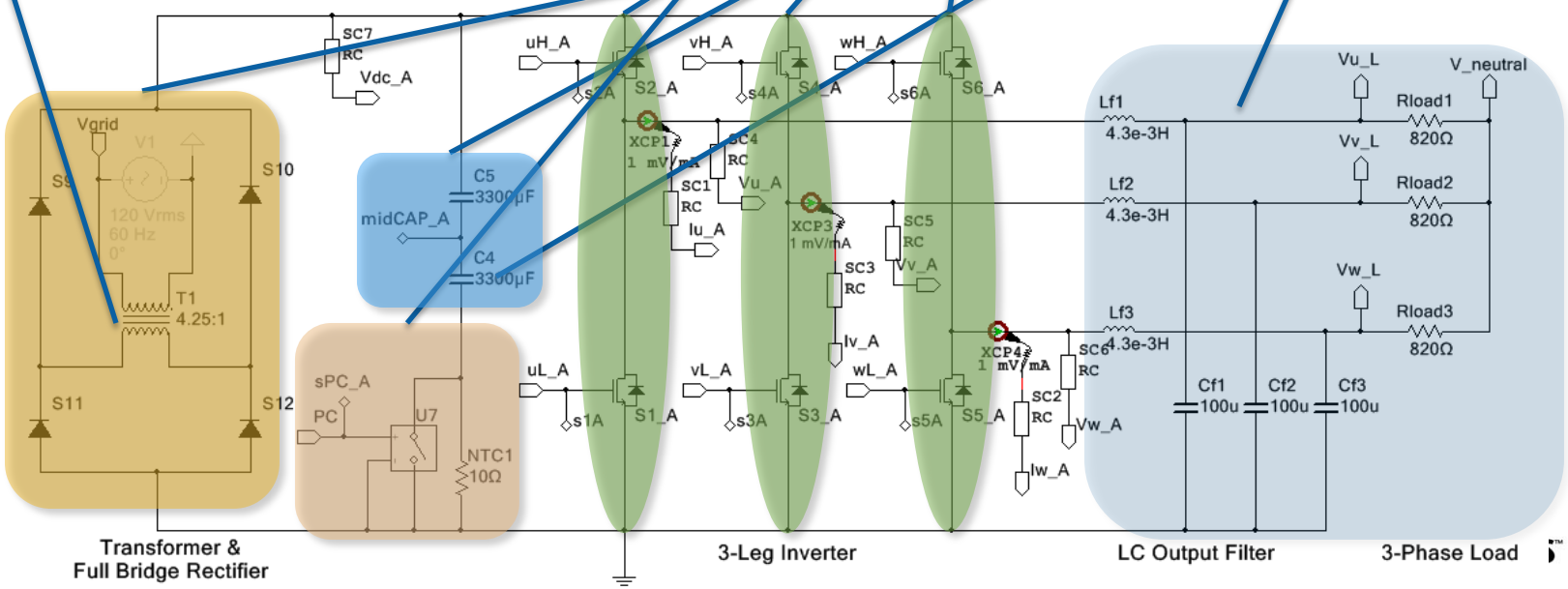
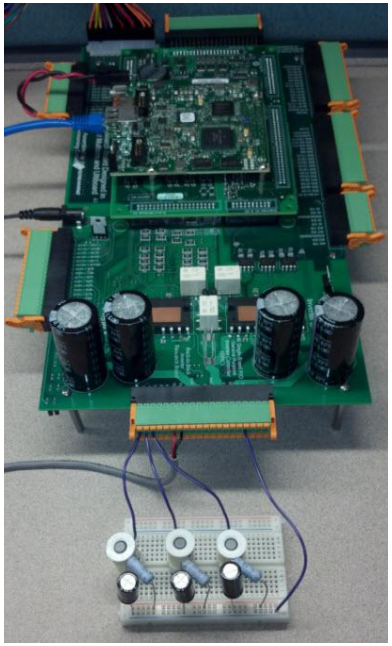
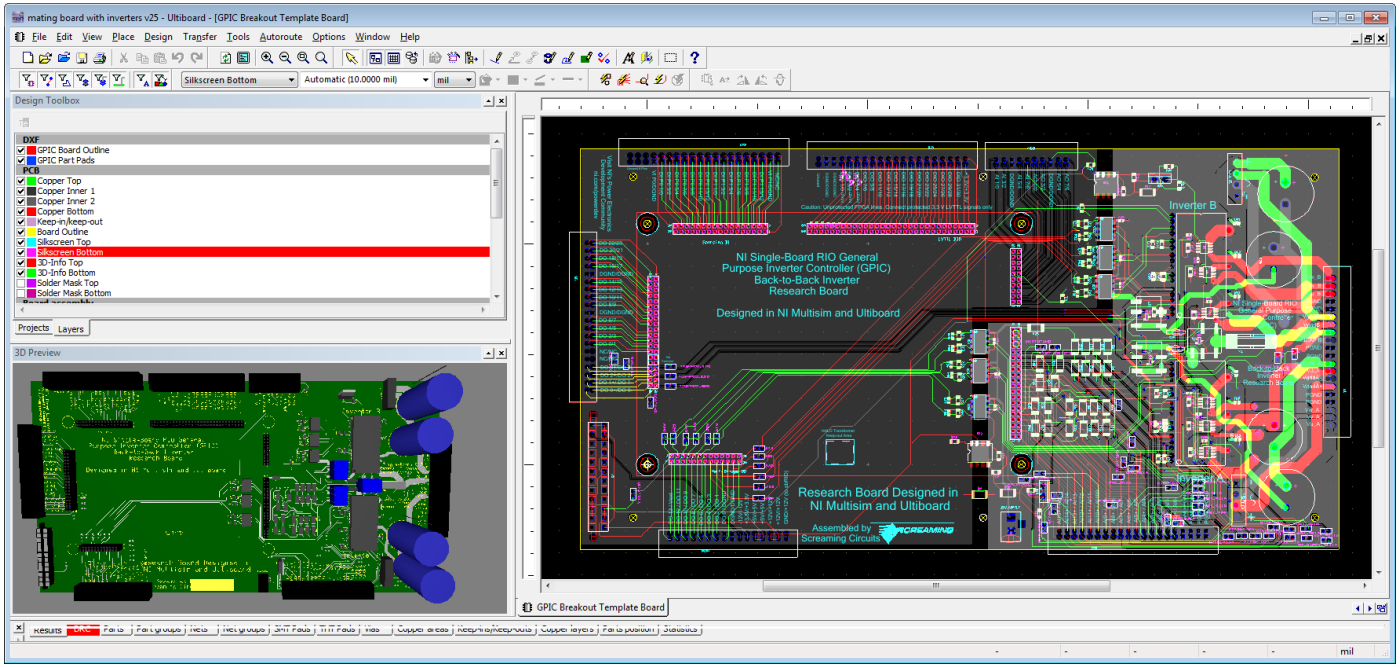
Open Source Back-to-Back Inverter Research Board



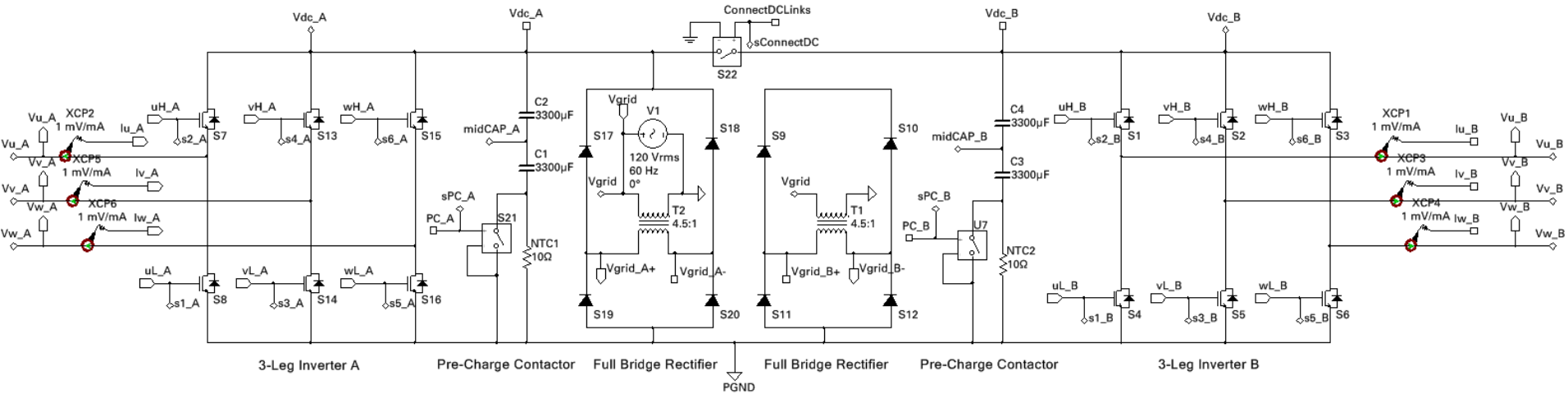


Open Source Back-to-Back Inverter Research Board

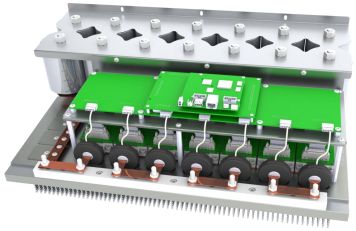




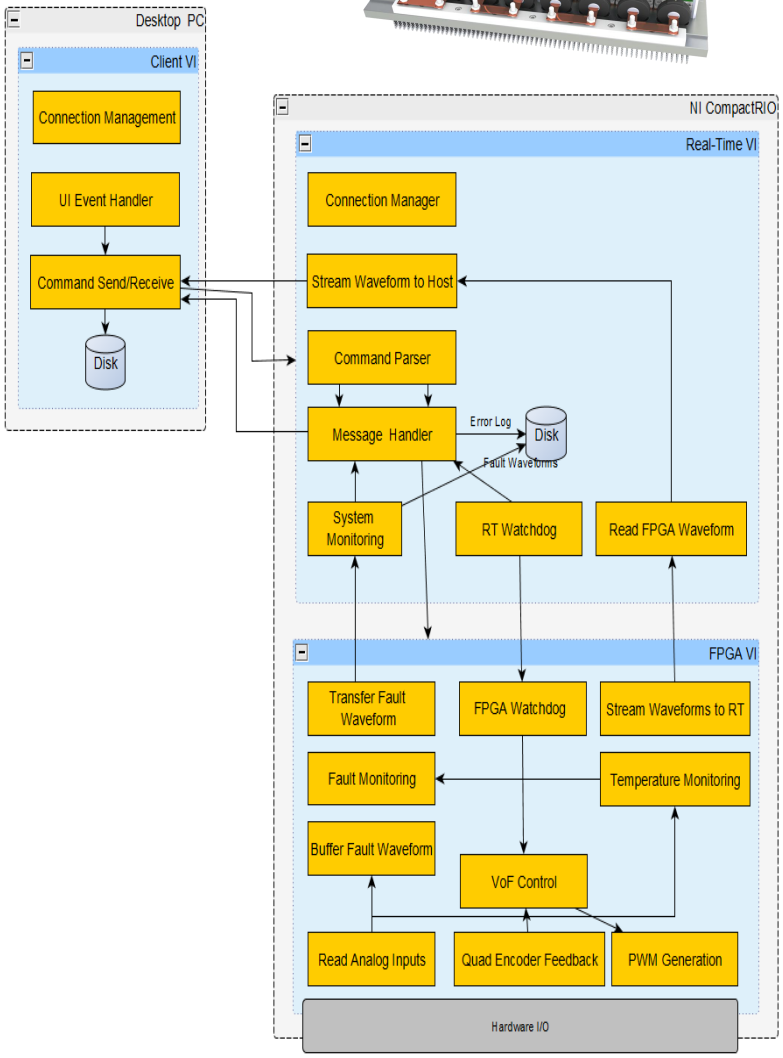
NI Single-Board RIO General Purpose Inverter Controller 3-Phase Back-to-Back Inverter Research Board



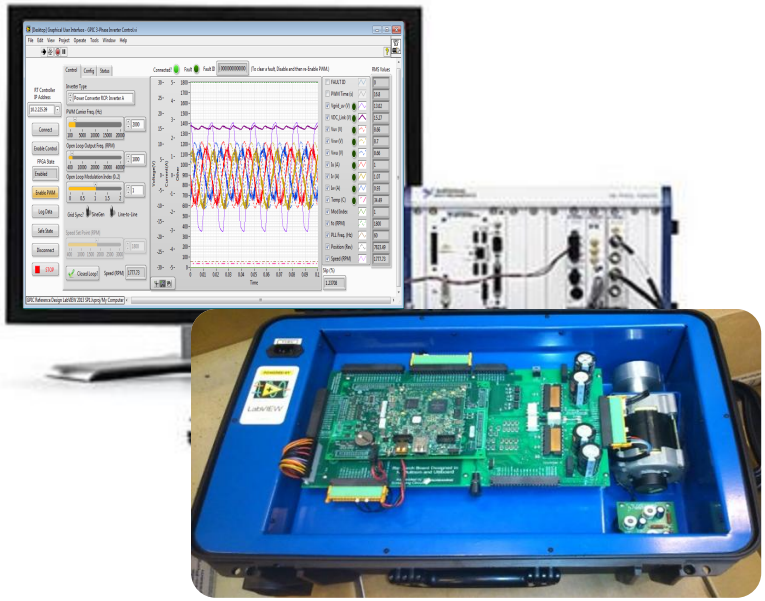
NI GPIC Reference Design Software



- Fully instrumented turnkey control demonstration software with network user interface, live scope display, and configurable control settings
- 10 kHz waveform graphing and data logging with live status display and automatic fault capture (up to 116 kS/s)
- Support for external isolated voltage and current sensors with configurable gain, offsets and filtering
- Datalog and fault log viewing and analysis with Microsoft Excel, The MathWorks, Inc. MATLAB®, NI DIAdem, and NI LabVIEW (including 3-phase power quality analysis)
- Open source reference design code
- Download: ftp://ftp.ni.com/evaluation/powerdev/training/GPICReferenceDesign.zip



NATIONAL INSTRUMENTS



Desktop PC

Client VI

Connection Management

UI Event Handler

Command Send/Receive

Disk

NI CompactRIO

Real-Time VI

Connection Manager

Stream Waveform to Host

Command Parser

Message Handler

Error Log

Disk

Fault Waveforms

System Monitoring

RT Watchdog

Read FPGA Waveform

FPGA VI

Transfer Fault Waveform

FPGA Watchdog

Stream Waveforms to RT

Fault Monitoring

Temperature Monitoring

Buffer Fault Waveform

VoF Control

Read Analog Inputs

Quad Encoder Feedback

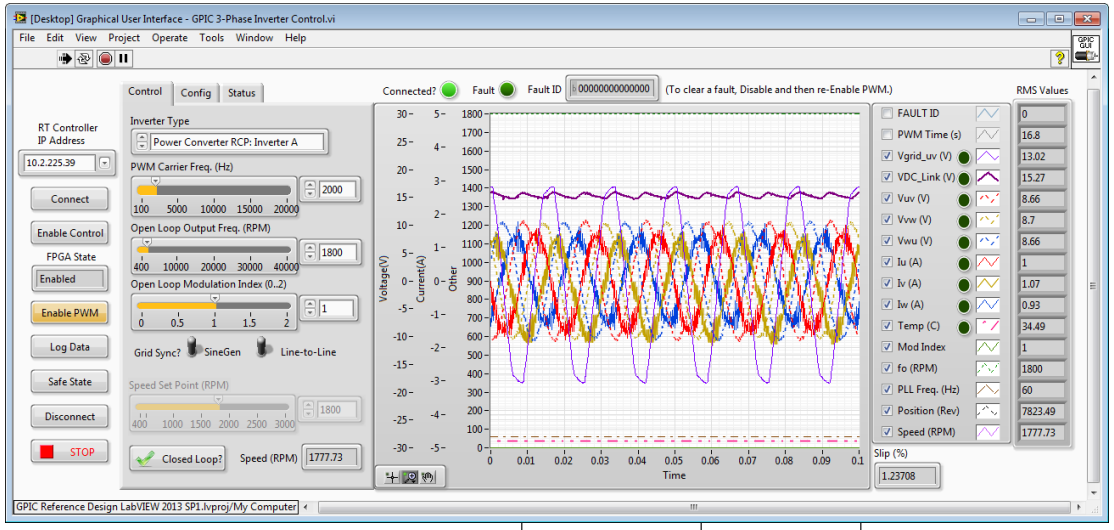
PWM Generation

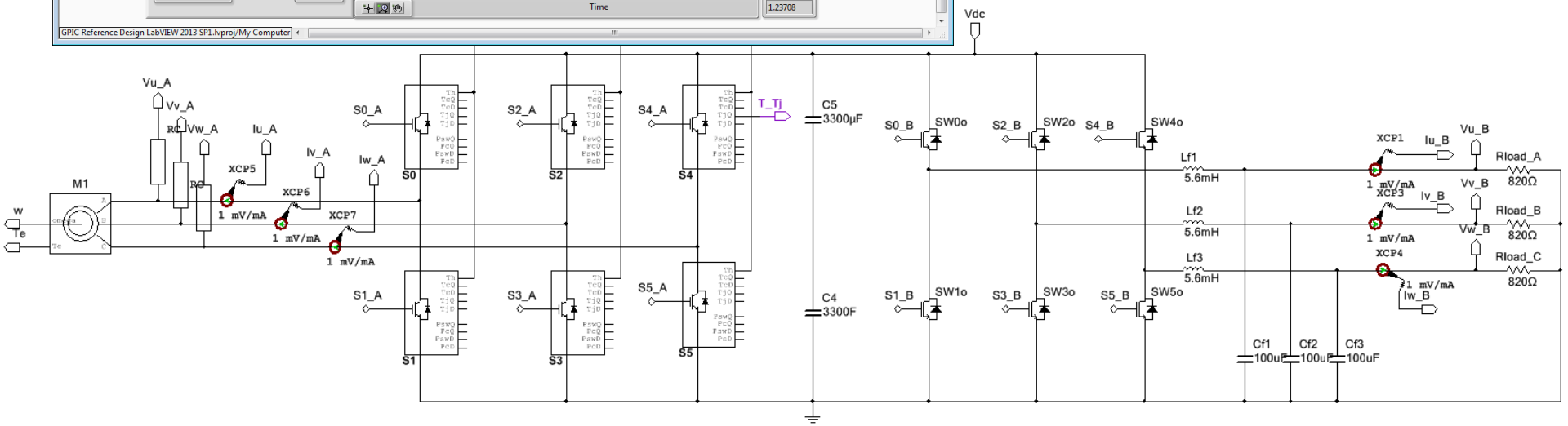
Hardware I/O

[Module 1, Exercise 2]

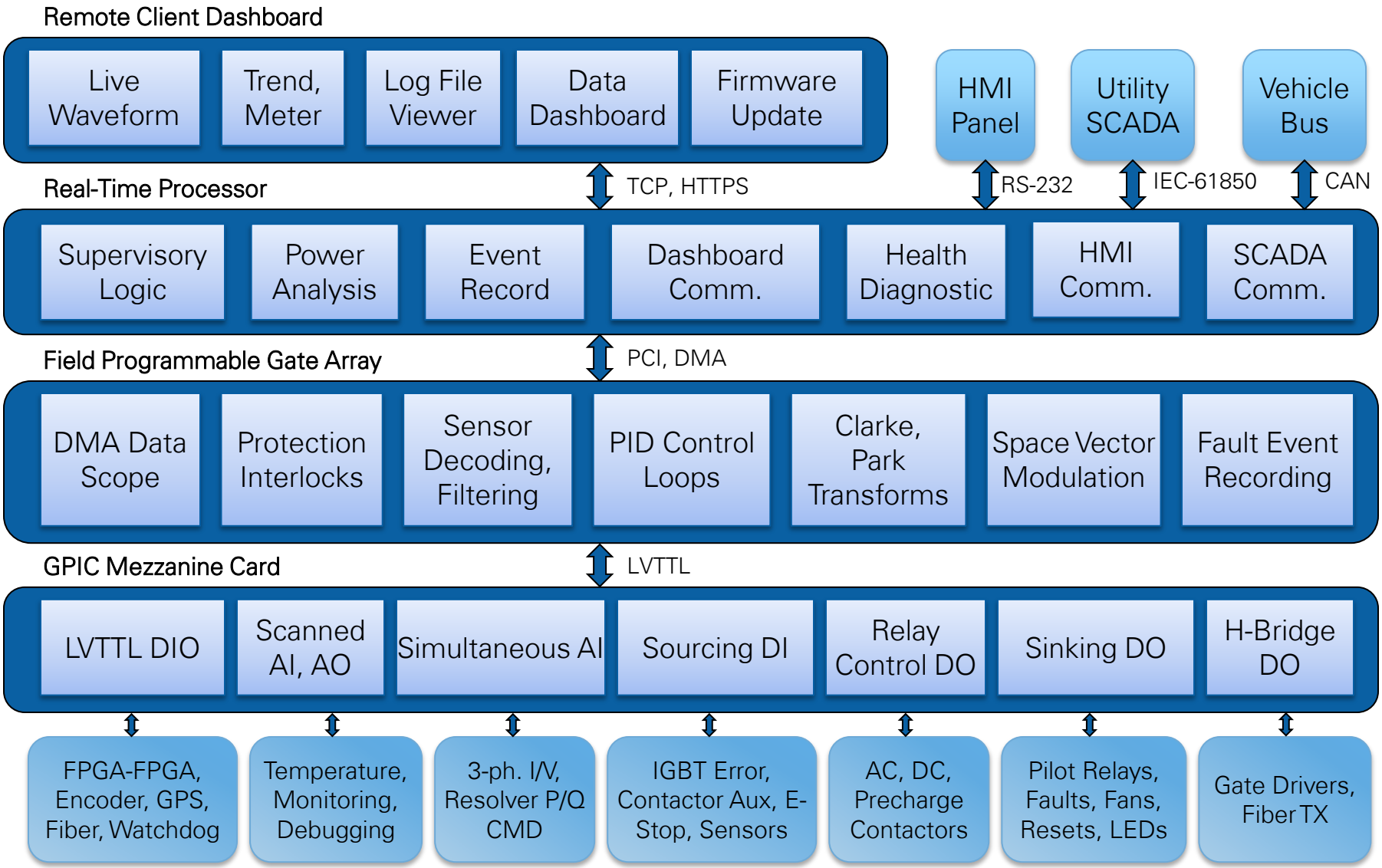
Understanding the GPIC Reference Design Application

Induction Motor Drive (Inverter A) and Grid Synchronized Inverter (Inverter B)





Typical sbRIO GPIC Control System Architecture

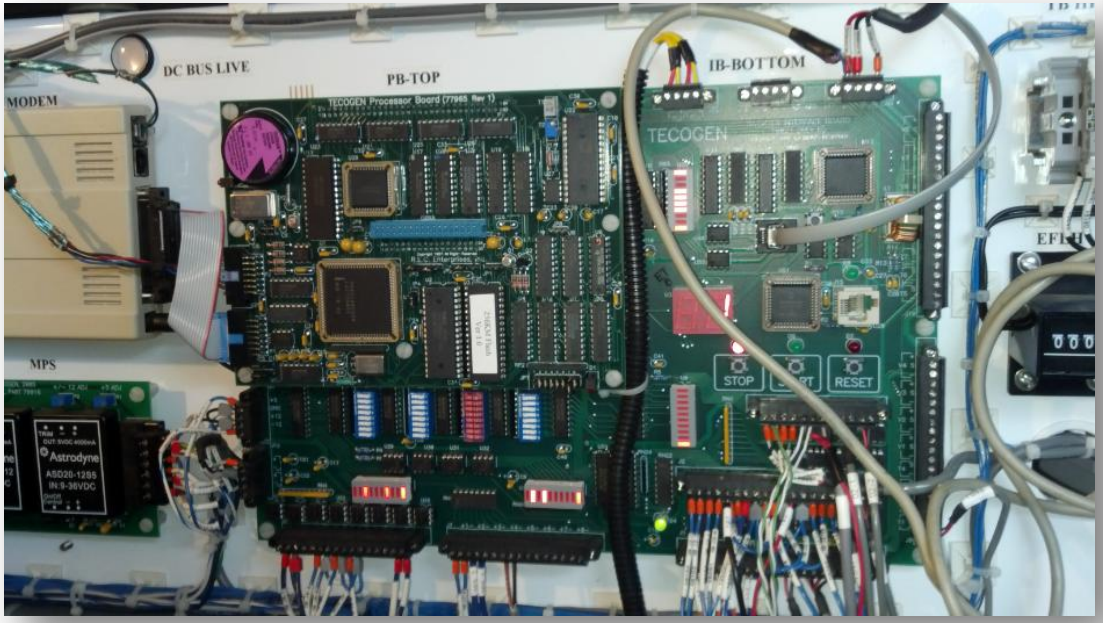


The Alternative

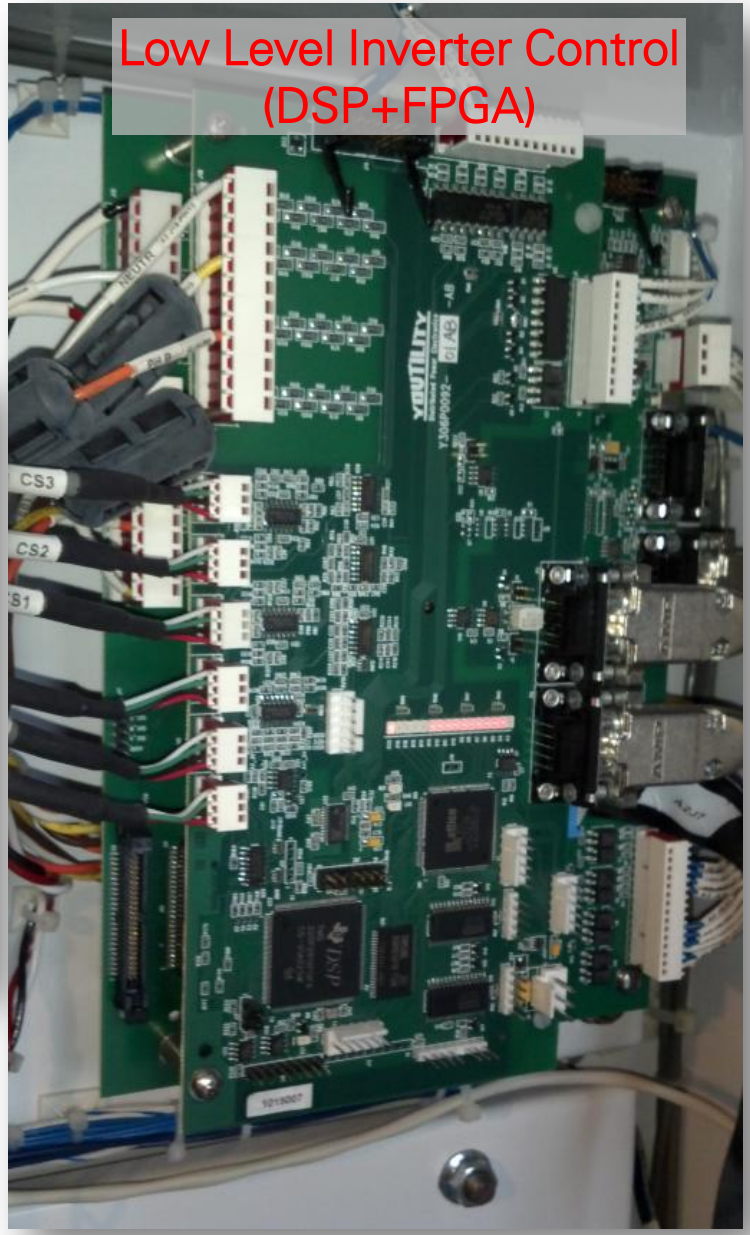
(Traditional full custom design)

Typical Full Custom Design – Natural Gas Turbine Inverter (100 kW)

Supervisory Control & Networking (Processor)



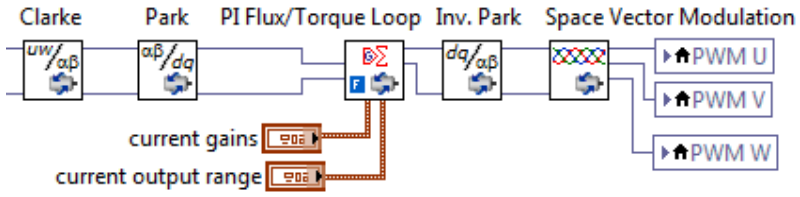
Low Level Inverter Control (DSP+FPGA)



DSP Programming– Text vs. Graphical

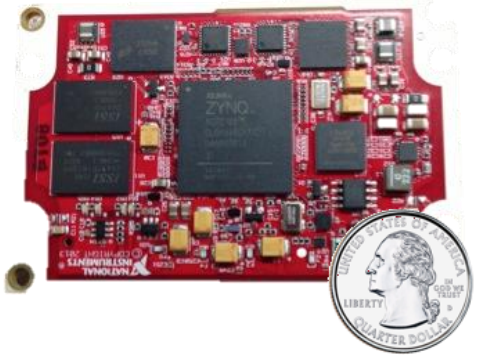
```
// ResonantConv_CNF(int16 n, int16 period, int16 deadband)
//
// Function arguments defined as:
//-------------------------------
// n =      Target ePWM module, 1,2,...16.  e.g. if n=2, then target is ePWM2
// period = PWM period in Sysclks
// deadband = PWM deadband
//-----------------------------------------------------------------------------
void ResonantConv_CNF(int16 n, int16 period, int16 deadband)
{

    (*ePWM[n]).TBCTL.bit.PRDLD = TB_IMMEDIATE;  // Set immediate load
    (*ePWM[n]).TBPRD = period;                  // PWM frequency = 1 / period
    (*ePWM[n]).CMPA.half.CMPA = period/2;       // Set duty as initial period (Lower Left)
    (*ePWM[n]).CMPB = period/4;                    // Set duty as initial period/2 (Upper Left)
    (*ePWM[n]).TBPHS.half.TBPHS = 0;            // Set as master, phase =0
    (*ePWM[n]).TBCTR = 0;                       // Time base counter =0

    (*ePWM[n]).TBCTL.bit.CTRMODE = TB_COUNT_UP; // Count-up mode: used for asymmetric PWM
    (*ePWM[n]).TBCTL.bit.PHSEN = TB_DISABLE;    // Disable phase loading
    (*ePWM[n]).TBCTL.bit.SYNCOSEL = TB_CTR_ZERO;// Used to sync EPWM(n+1) "down-stream"
    (*ePWM[n]).TBCTL.bit.HSPCLKDIV = TB_DIV1;   // Set the clock rate
    (*ePWM[n]).TBCTL.bit.CLKDIV = TB_DIV1;      // Set the clock rate

    (*ePWM[n]).CMPCTL.bit.LOADAMODE = CC_CTR_PRD; // Load on CTR=PRD
    (*ePWM[n]).CMPCTL.bit.LOADBMODE = CC_CTR_PRD; // Load on CTR=PRD
    (*ePWM[n]).CMPCTL.bit.SHDWAMODE = CC_SHADOW;  // Shadow mode. Operates as a double buffer.
    (*ePWM[n]).CMPCTL.bit.SHDWBMODE = CC_SHADOW;  // Shadow mode. Operates as a double buffer.

    (*ePWM[n]).AQCTLA.bit.ZRO = AQ_SET;           // Set PWM1A on Zero
    (*ePWM[n]).AQCTLA.bit.CAU = AQ_CLEAR;         // Clear PWM1A on event A, up count
    (*ePWM[n]).AQCTLB.bit.CAU = AQ_SET;           // Set PWM1B on event B, up count
    (*ePWM[n]).AQCTLB.bit.PRD = AQ_CLEAR;         // Clear PWM1B on PRD
```

vs.



The Problem with Embedded Design

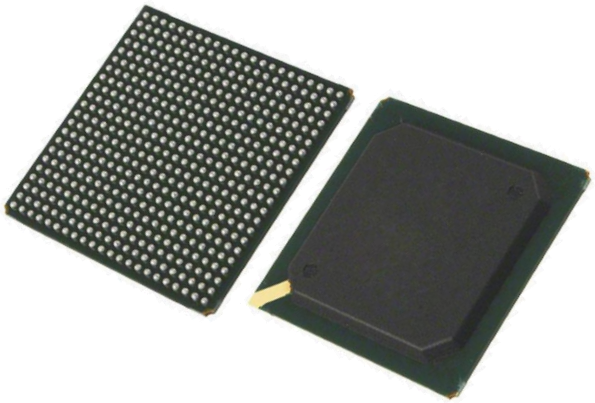
- Transistor count doubles every 18 months
- Performance per dollar doubles every 14 months
- Full custom embedded design takes 12-13 months
- Logic voltage levels dropping closer and closer to noise floor
- PCB design/layout increasingly complex, risky, costly



Solution: Pre-Validated Heterogeneous SOC with Complete Platform-based Design Toolchain

DIP Package

Low Profile Quad Flat Package



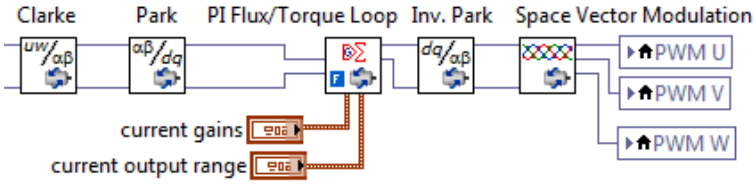
Ball Grid Array (BGA) Package

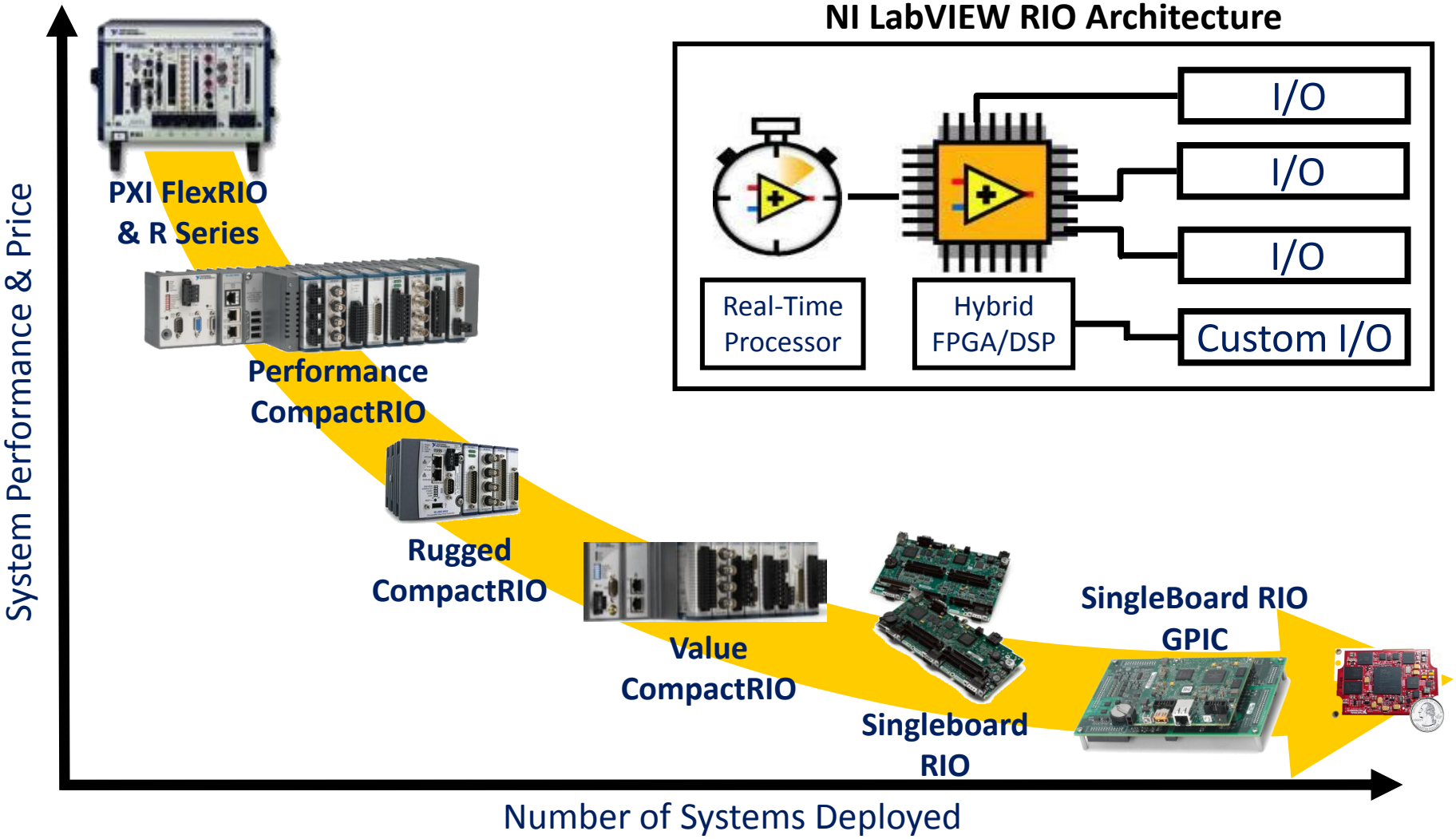
The NI LabVIEW RIO Approach

An Improved Methodology for Embedded Systems Design

NATIONAL INSTRUMENTS

NI RIO Deployment Curve





Key Enablers

1. The availability of heterogeneous field programmable gate array (FPGA) hardware containing an array of integrated digital signal processor (DSP) cores capable of efficiently executing floating point math operations. These modern FPGAs are actually hybrid devices containing hard-core DSP processing elements, integrated within the reconfigurable computing fabric, and capable of achieving MHz speeds for simulation and control.

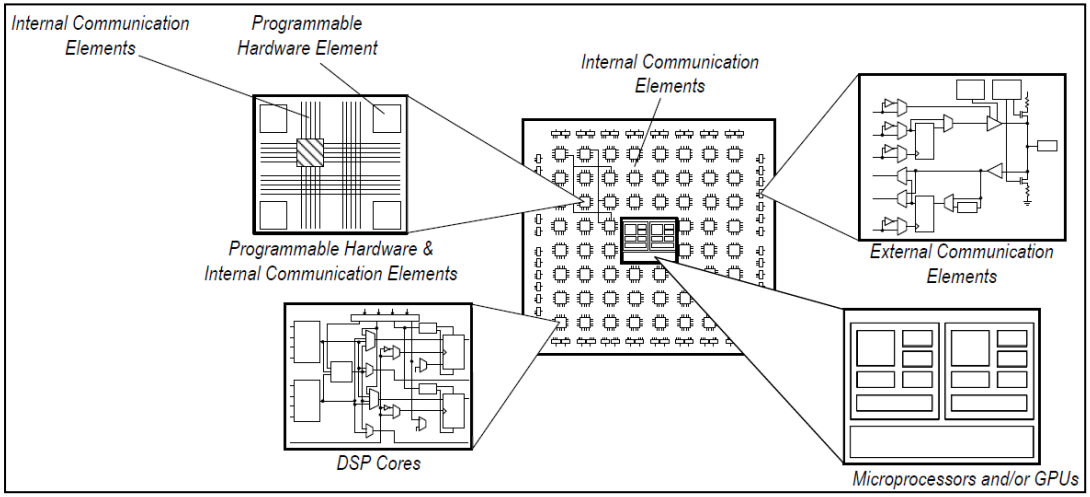
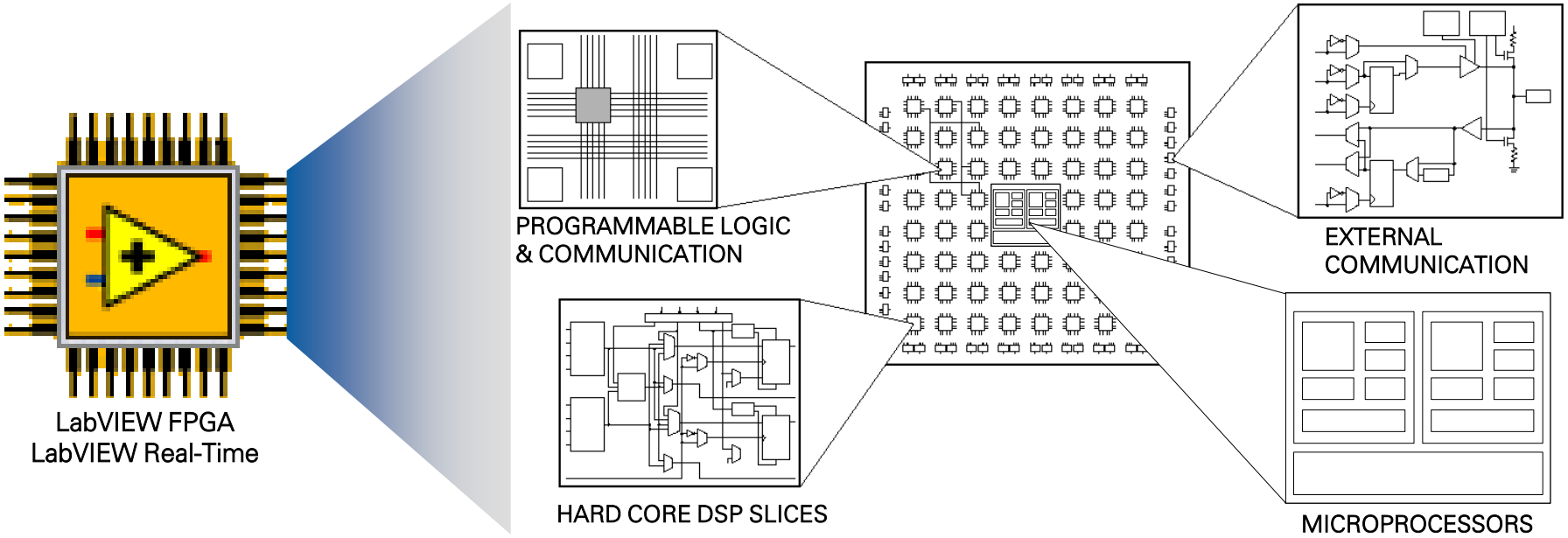


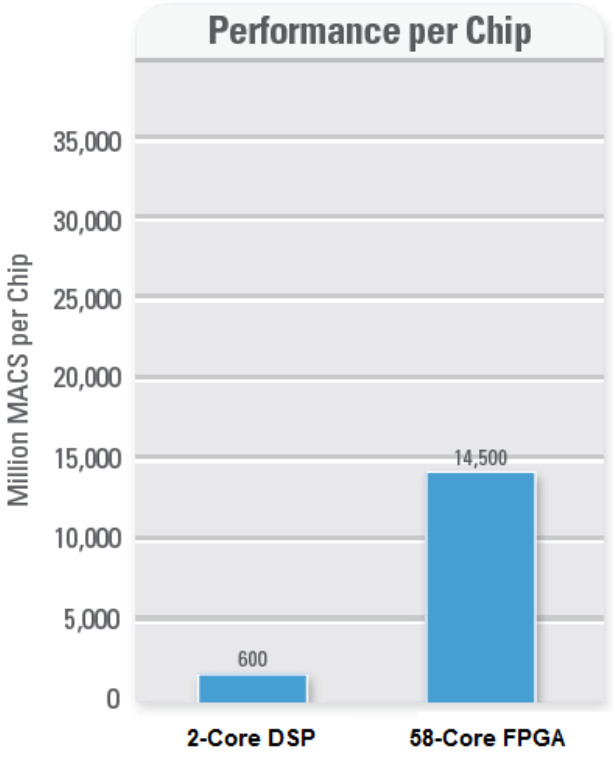
Figure 1. Heterogeneous FPGA system-on-a-chip (SOC) devices contain an array of programmable hardware logic, DSP cores, and communication elements that can now be programmed using graphical floating point math.

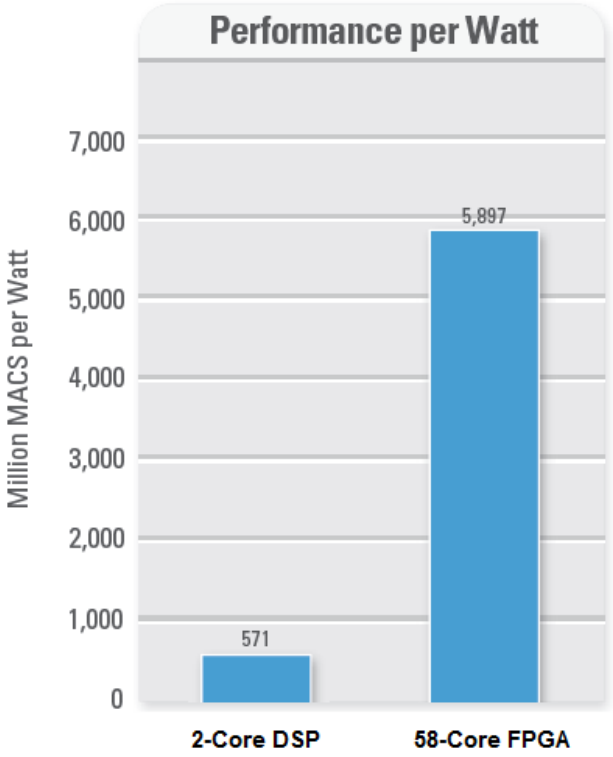
The future of Moore's Law is heterogeneous, massively parallel SOCs

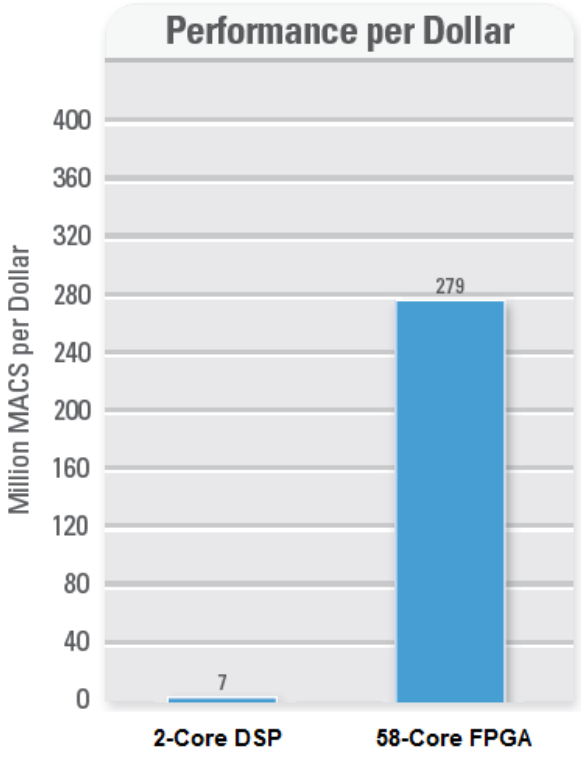


Modern Hybrid DSP/FPGA/ARM System-on-Chip

Modern hybrid FPGAs offer higher performance than traditional DSPs







	Dual-Core DSP	Spartan-6 LX45 HFPGA	Zynq 7020 SFPGA	Performance Ratio (FPGA/DSP)	Performance Ratio (Zynq-7020/DSP)
Million MACS per Chip	600	14,500	92,000	24	153
Million MACS per Watt	571	5,897	23,000	10	40
Million MACS per Dollar	7	279	515	40	74

MACS = Multiply-accumulate operations per second
(measure of DSP performance)

Computing Price-Performance: 1910-2020

2013: Xilinx Zynq-7020x220 (FPGA+ARM x2+multicore DSP x220), CPS/$=369,478,000

2012: Xilinx Spartan-6 LX45x58 (FPGA+multicore DSP x58), CPS/$=183,544,000

2012: Raspberry Pi (ARM x1), CPS/$=58,824,000

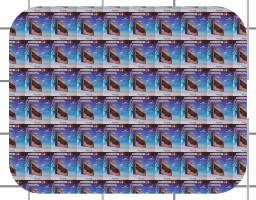
Analog OpAmp, CPS/$=~22,000,000

2008: Mac_Pro/2.8GHz (multicore processor x8), CPS/$=18,286,000

2001: Dell WorkStation 340 (Pentium 4, 2.53 GHz x1), CPS/$=1,107,000

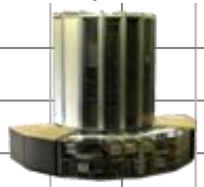
1995: PowerMac 8500/120 (RISC processor), CPS/$=45,000

R^2: 0.884



1982: Commodore 64 (microprocessor), CPS/$=400

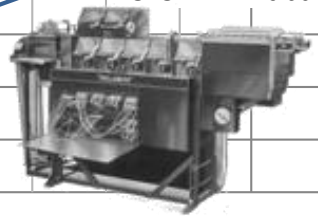
1976: Cray 1 (integrated circuit), CPS/$=15



1960: DEC PDP-1 (discrete transistors), CPS/$=0.83

1953: IBM 650 (vacuum tube), CPS/$=0.00483

1919: IBM Tabulator (mechanical gear calculator), CPS/$=0.0000021



Calculations per Second per Dollar (log scale)

1.00E+11
1.00E+10
1.00E+09
1.00E+08
1.00E+07
1.00E+06
1.00E+05
1.00E+04
1.00E+03
1.00E+02
1.00E+01
1.00E+00
1.00E-01
1.00E-02
1.00E-03
1.00E-04
1.00E-05
1.00E-06
1.00E-07
1.00E-08
1.00E-09
1.00E-10

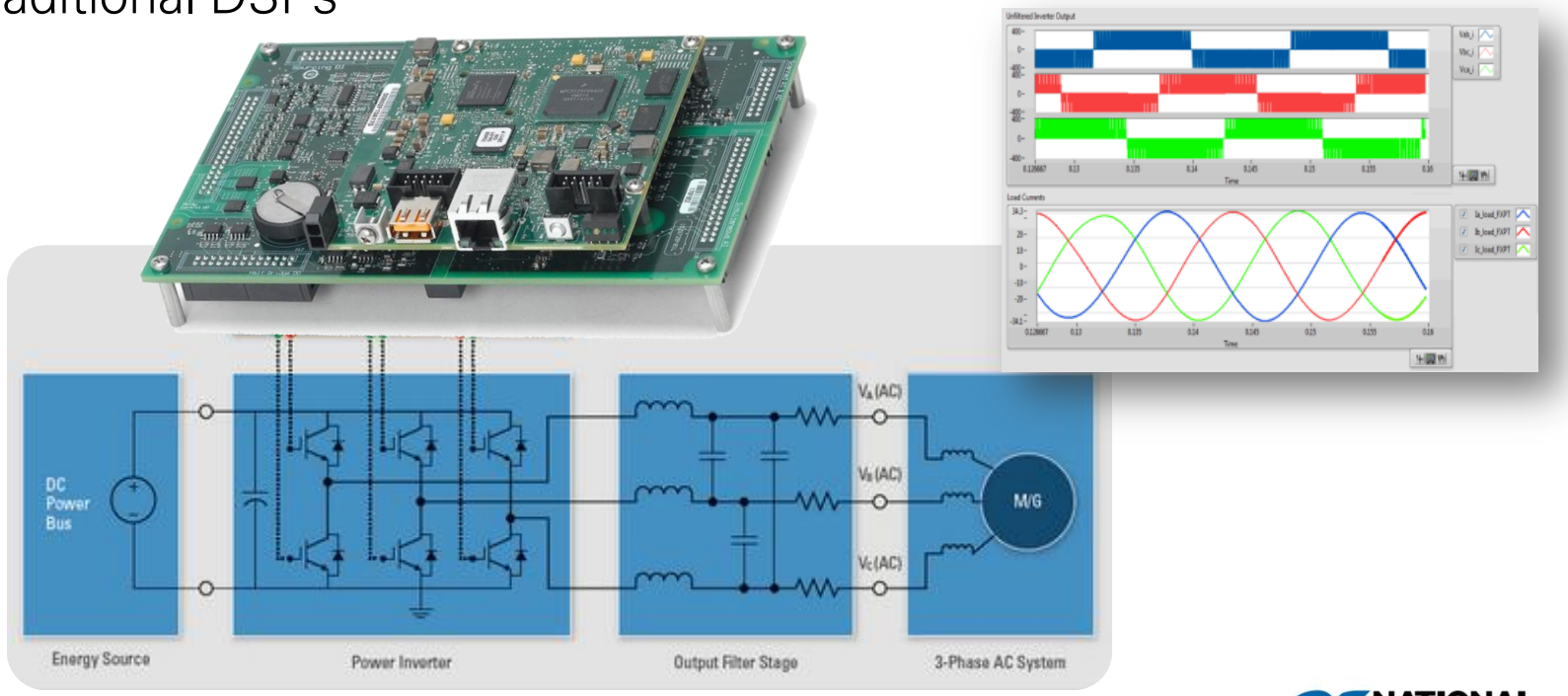
1910 1930 1950 1970 1990 2010

CPS/$ Data Used for Fit (1946-2009) Fit CPS/$

Data Source: http://www.frc.ri.cmu.edu/~hpm/book97/ch3/processor.list

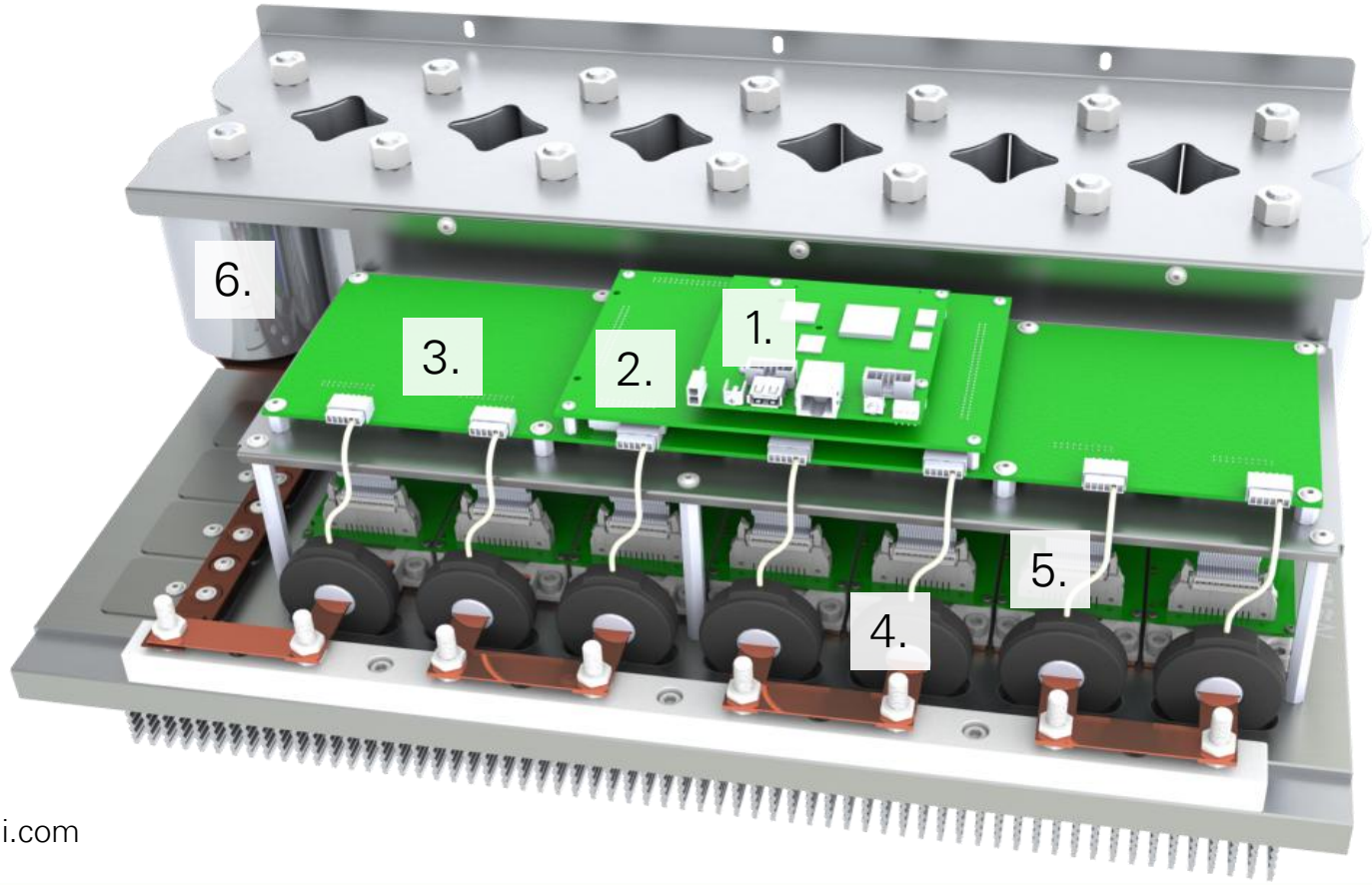
NI Single-Board RIO General Purpose Inverter Controller (NI GPIC)

- Industry-proven NI LabVIEW RIO architecture and cutting-edge co-simulation tools
- Deployment-ready for high volume commercial applications
- Multicore FPGA delivers 40x higher performance per dollar than traditional DSPs



Typical Application

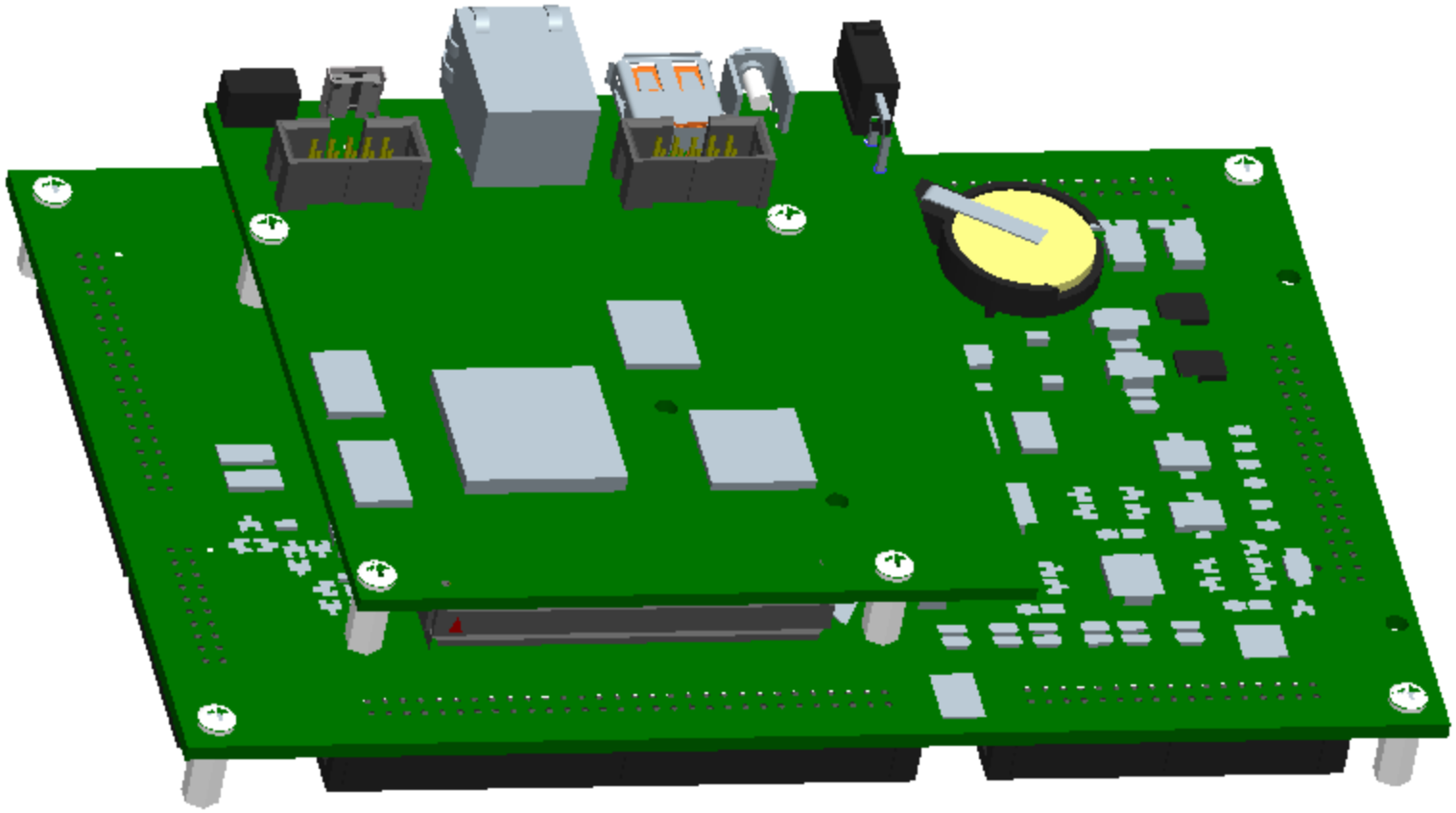
1. NI Single-Board RIO sbRIO-9606 (FPGA, PowerPC, Network)
2. NI GPIC 9683 RIO Mezzanine Card (bottom orientation connectors)
3. Custom interface or gate drive PCB (template available)
4. Isolating sensors
5. IGBT modules or Power Stack
6. DC capacitors



NATIONAL INSTRUMENTS

Typical GPIC Stack

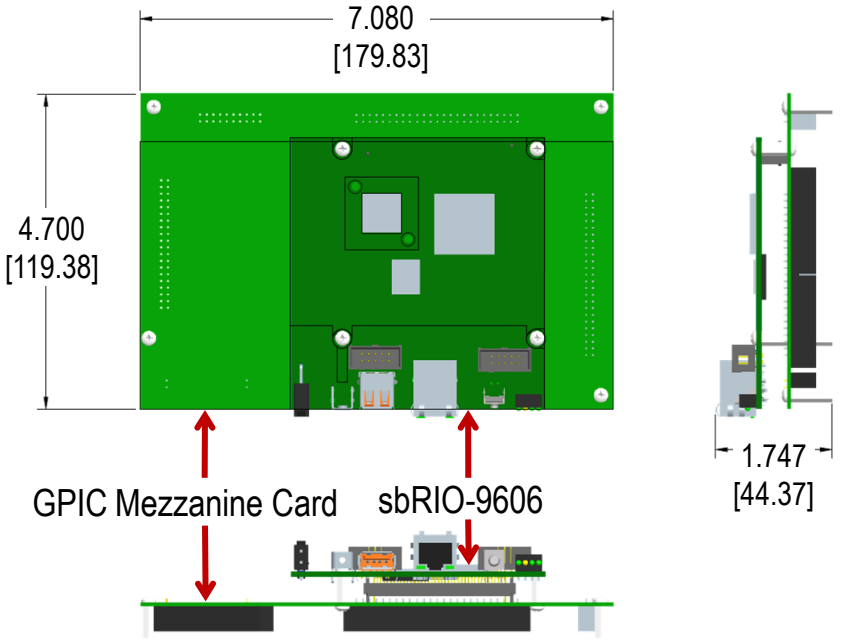
1. NI Single-Board RIO sbRIO-9606
2. NI GPIC 9683 RIO Mezzanine Card (bottom orientation connectors)

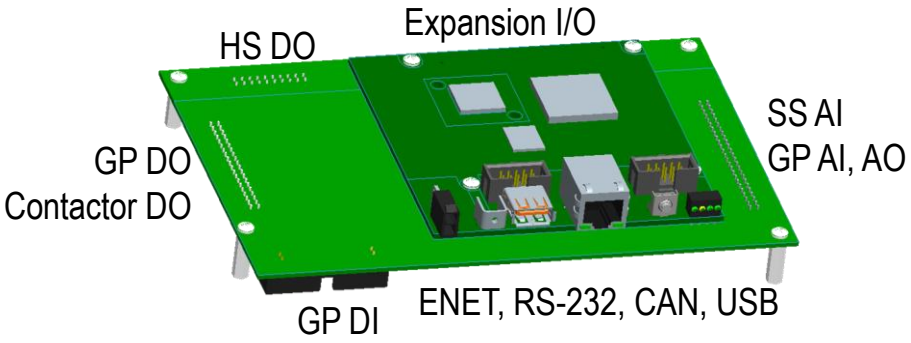


NI GPIC

High Speed Digital Output (Gate Drive) *(20-pin 100 mil header)*	• 12-ch HS DO (18-pins, 6 GND) • 1 V_{PWR_IN} (1-pin) • 1-pin reserved
General Purpose and Contactor Digital Output *(40-pin 100 mil header)*	• 24-ch GP DO (28-pins, 4 GND) • 4-ch Contactor DO (8-pins, 4 GND) • 4-pins reserved
FPGA and Processor Expansion I/O *(50-pin 100 mil header)*	• 16-ch +3.3 V FPGA IO (24-pins, 8 GND) • +3.3 V $FPGA_{PWR\_IN}$ (1-pin) • +5 V SYS_{PWR_OUT} (1-pin) • 24-pins reserved
General Purpose Digital Input *(26-pin 100 mil header)*	• 24-ch GP DI (26-pins, 2 V_{PWR_IN})
High Speed Simultaneous AI, General Purpose Scanned AI , General Purpose AO *(60-pin 100 mil header)*	• 16-ch Differential SS AI (32 pins) • 8-ch Scanned GP AI (9-pins,1 COM) • 8-ch GP AO (9-pins, 1 COM) • 10-pins reserved

Bottom Mount Connectors

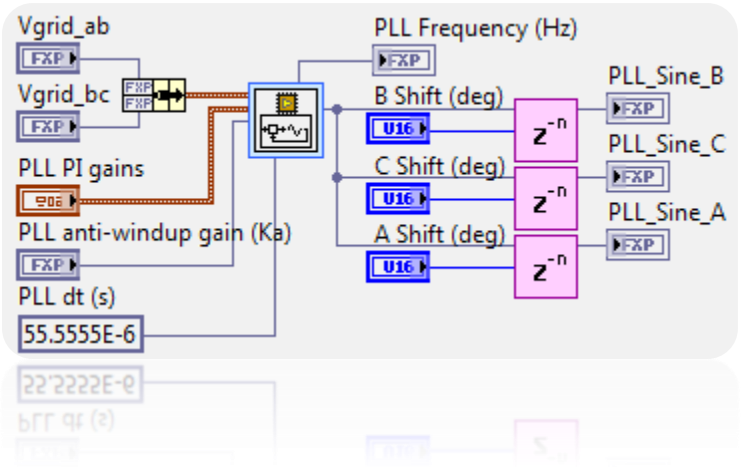


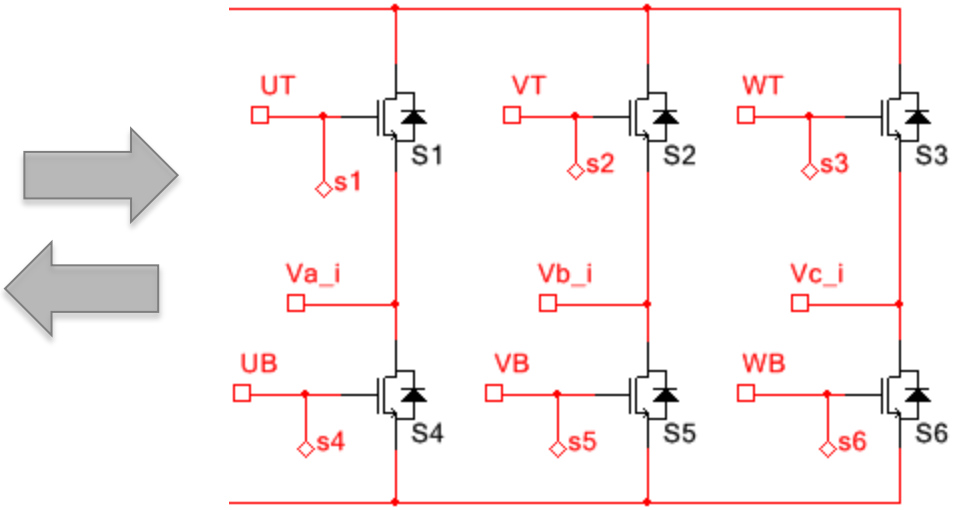


Design Flow with the NI GPIC

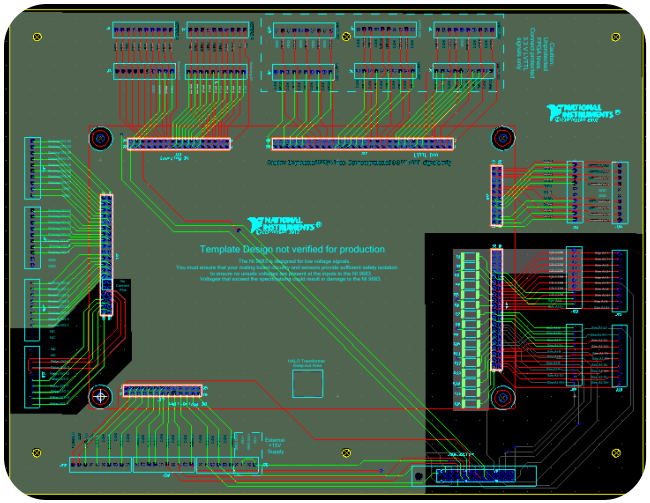
1. Co-Simulation, 2. Interface Board Design, 3. Commercial Deployment

1.

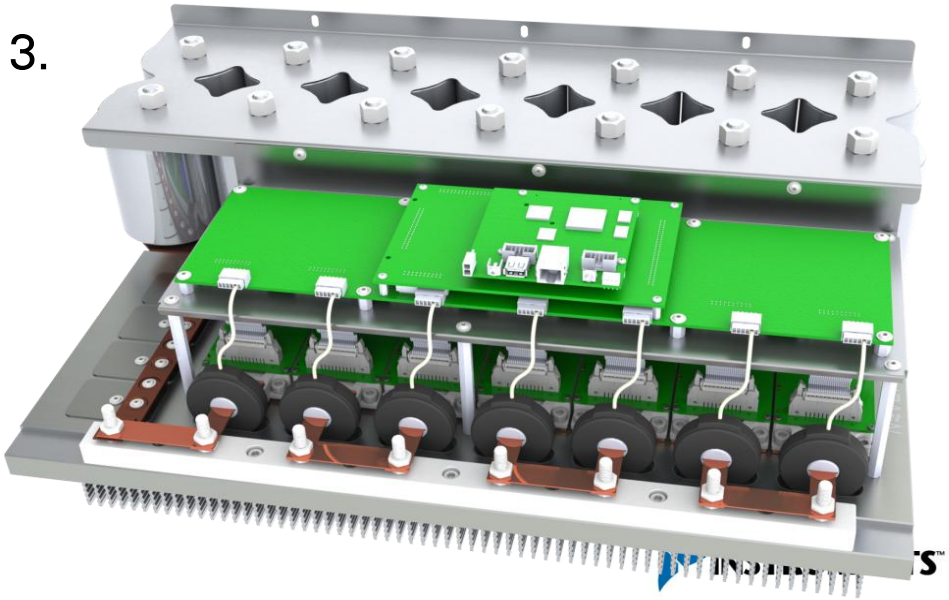




2.

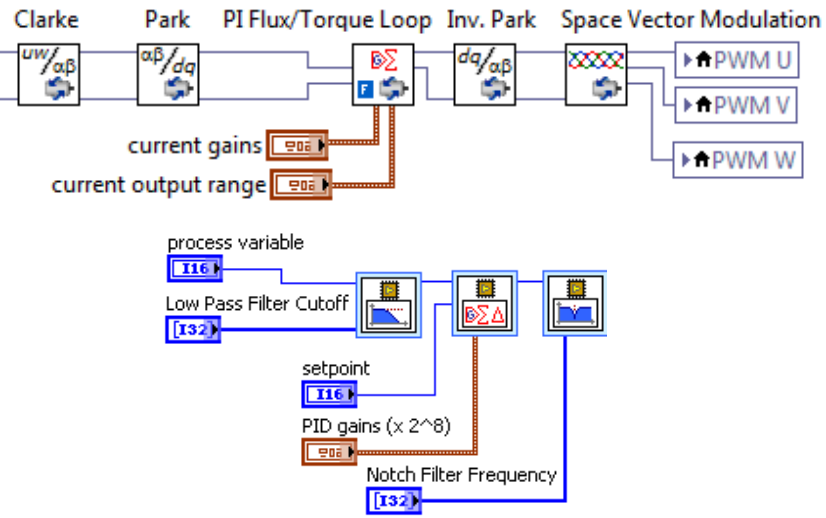


3.

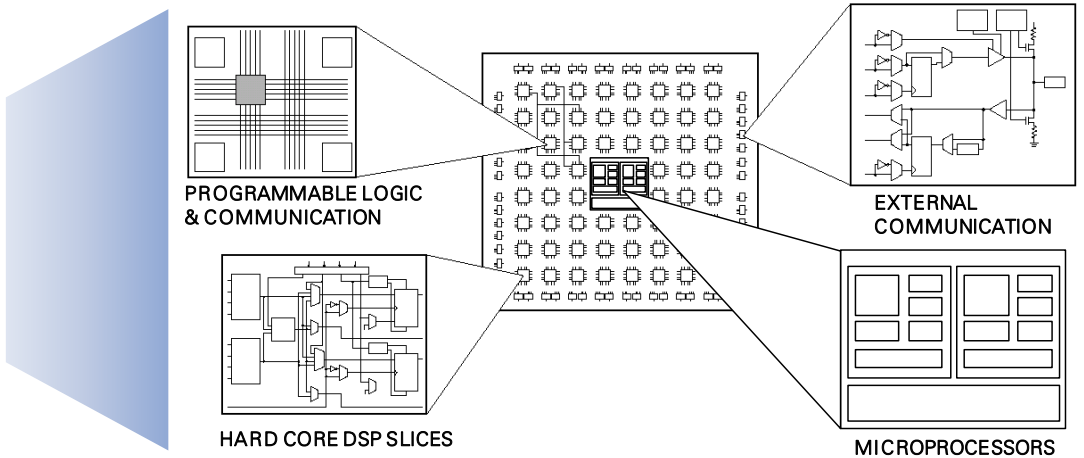


Graphical System Design

Graphical Programming → Desktop Co-Simulation → Auto Compilation → Auto Synthesis → Auto Place & Route → Deployment



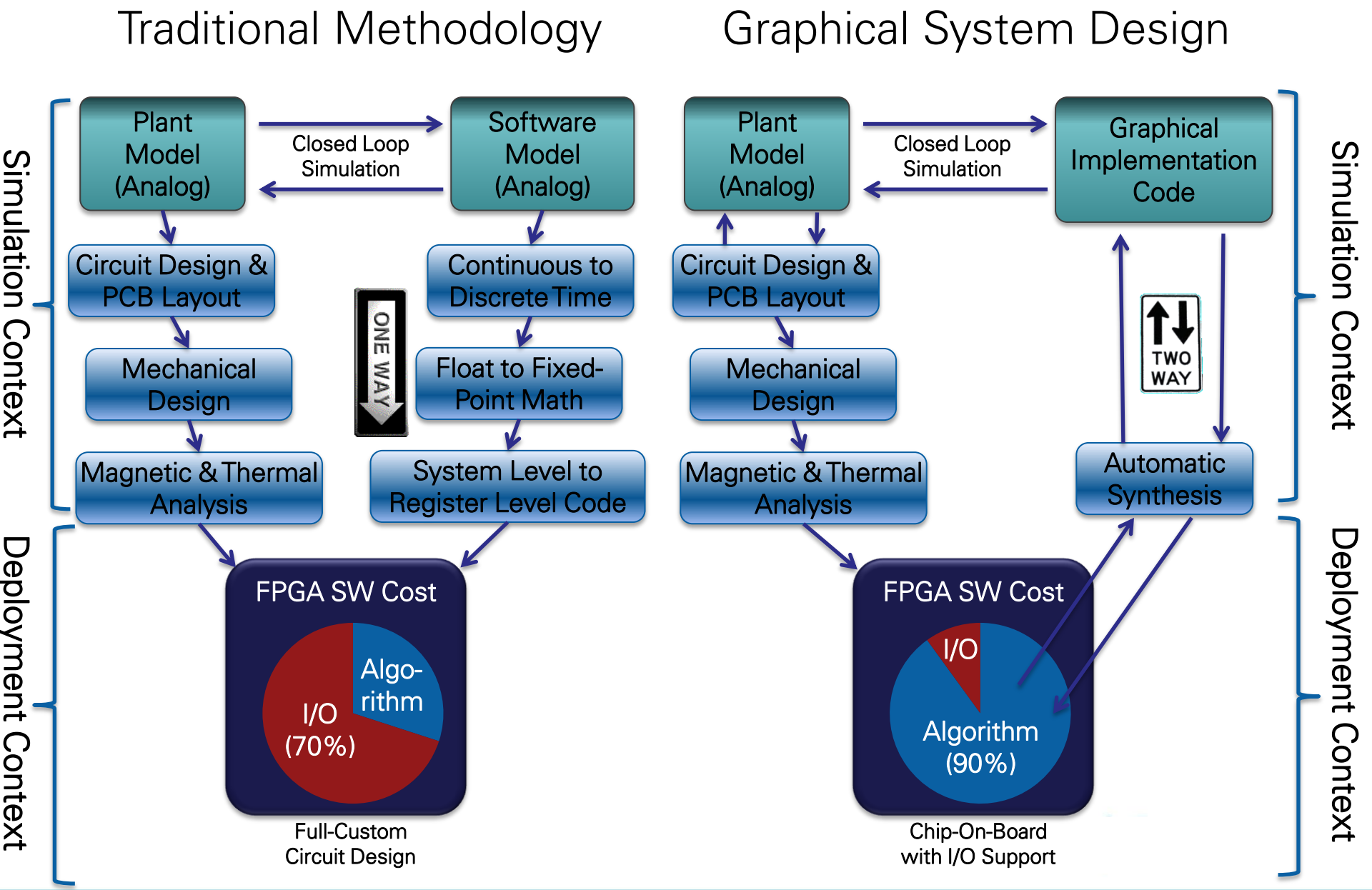
LabVIEW FPGA



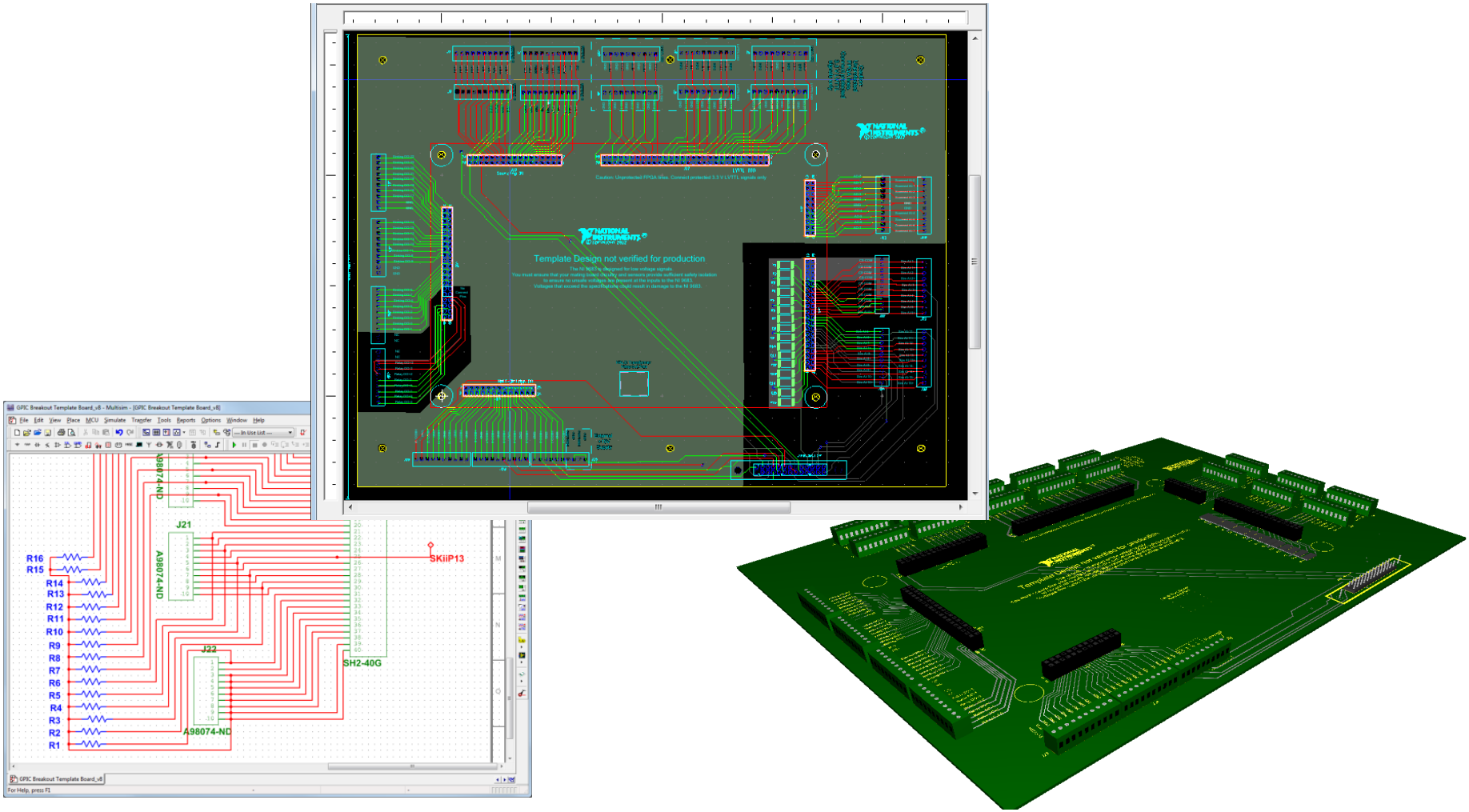
Hybrid DSP-uP-FPGA

NATIONAL INSTRUMENTS

The Evolution of Model Based Design



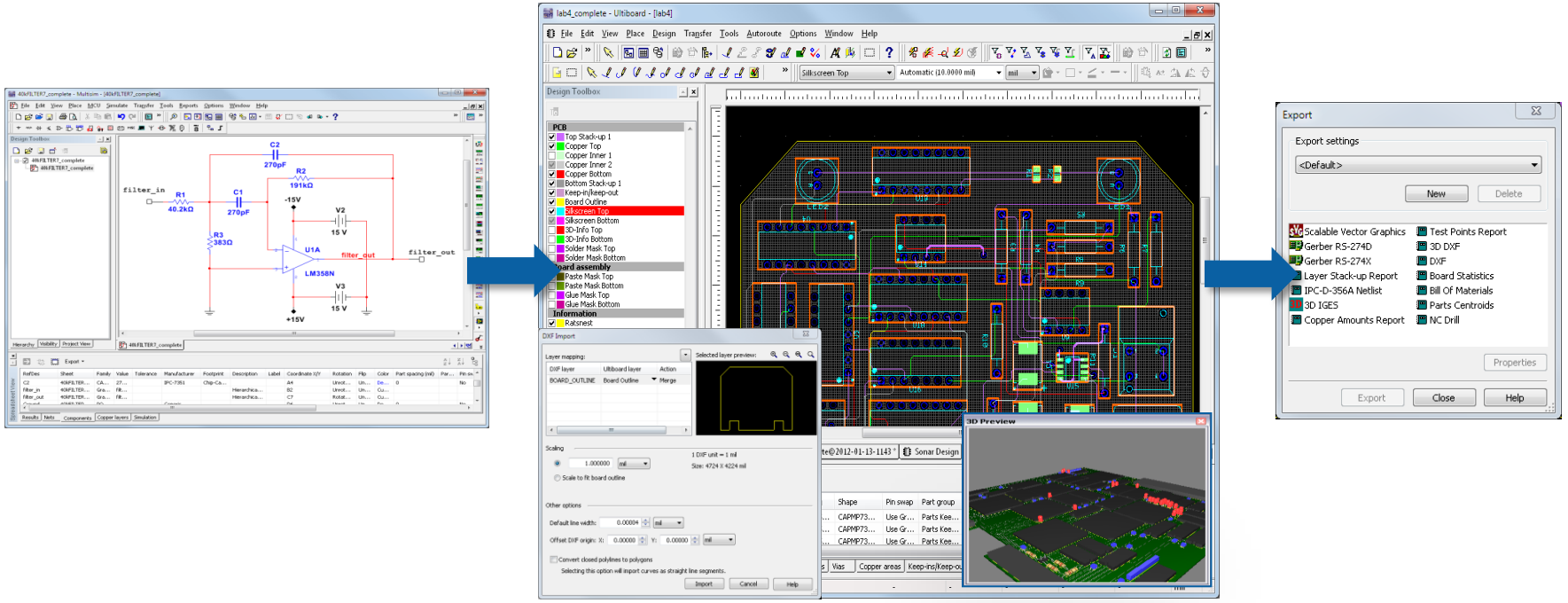
GPIC Interface PCB Template



NATIONAL INSTRUMENTS

PCB Design with NI Ultiboard

- Improved productivity with rapid prototyping tools
  - Integrated and synchronized schematic capture and layout environments
  - Place land patterns and routes with manual and automated tools
  - Import and export of standard file formats for accurate fabrication



NATIONAL INSTRUMENTS

NI Power Electronics Control Design V Training Workshop

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1. Power Electronics
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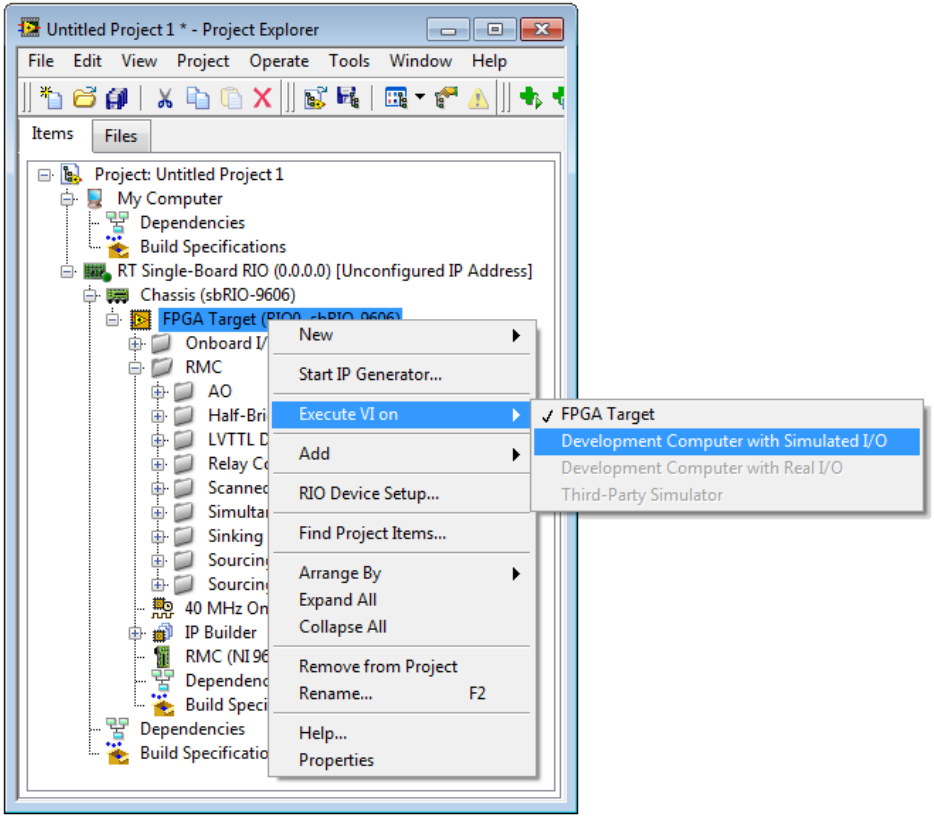
[Demo]
Create a New LabVIEW Project and Add RT, FPGA Targets

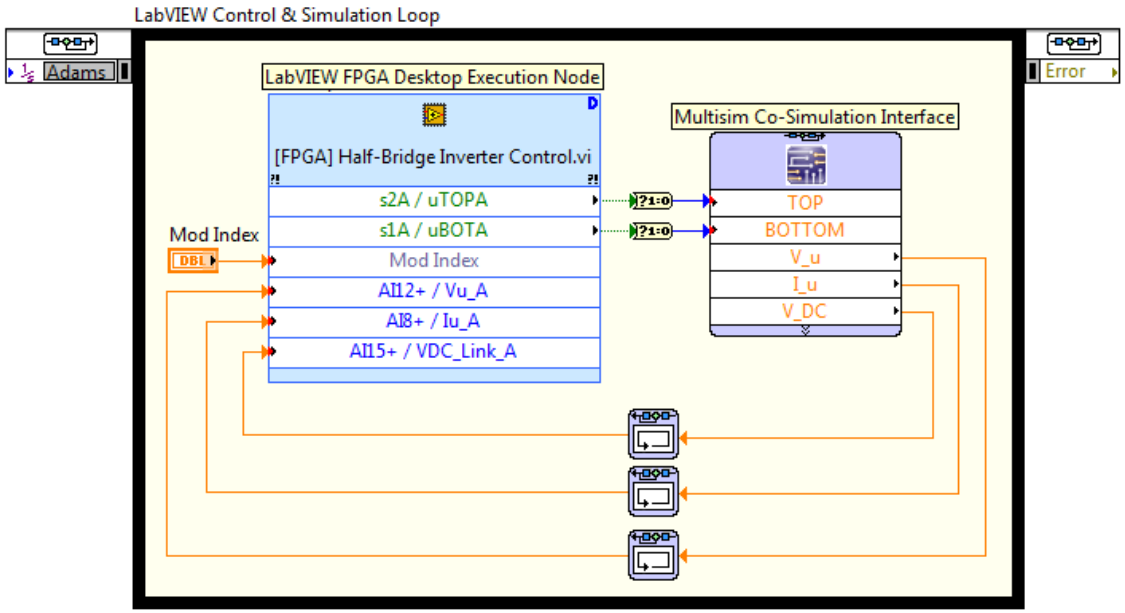
Understand Execution Contexts and FPGA Simulation Mode

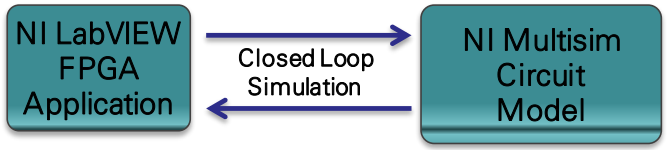


NATIONAL INSTRUMENTS

[Module 1, Exercise 1] Half-Bridge DC-to-AC Inverter Control

FPGA – Multisim Co-Simulation for Manual IGBT Control

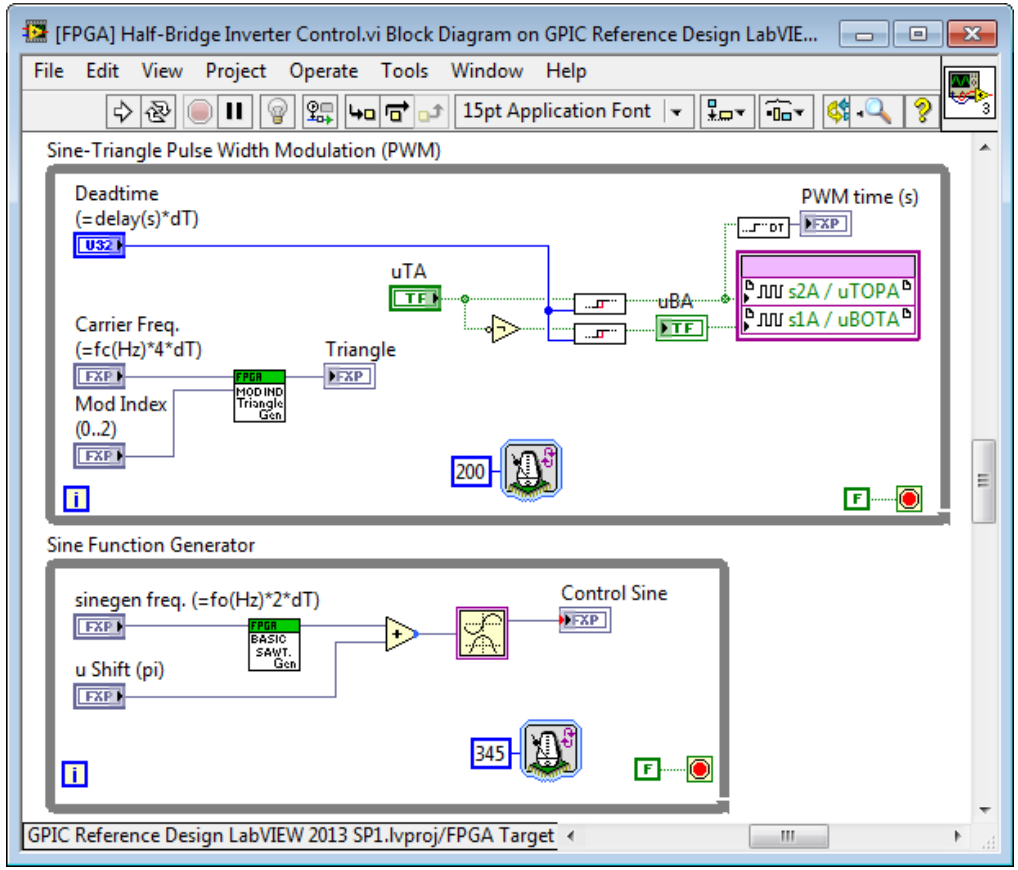




NATIONAL INSTRUMENTS

[Module 1, Exercise 2]
Pulse Width Modulation

Complementary switching logic with deadtime



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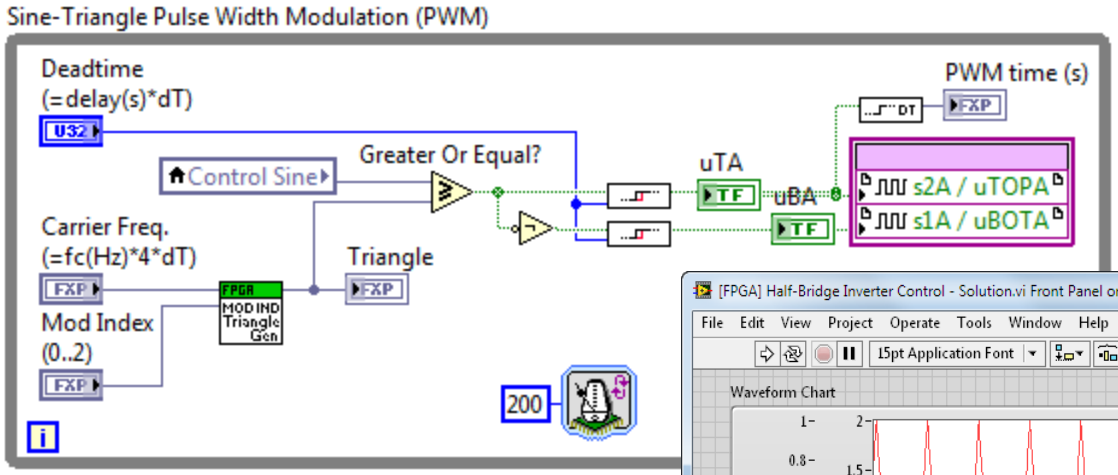
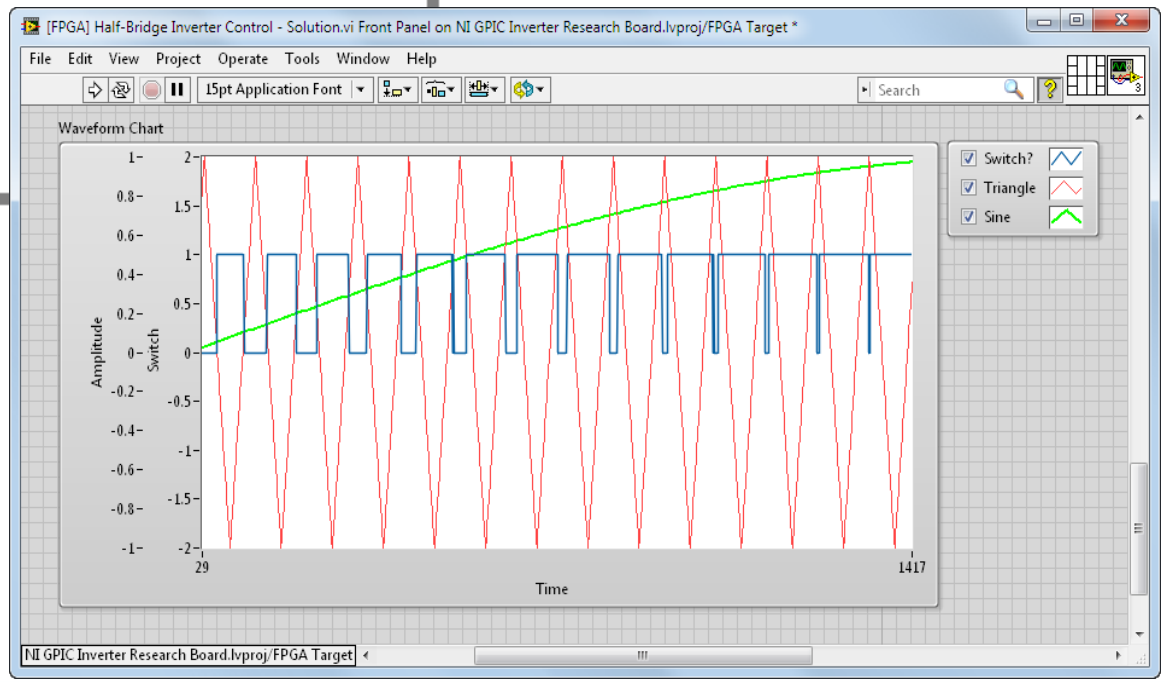
[Module 1, Exercise 3]

Sine-Triangle Pulse Width Modulation

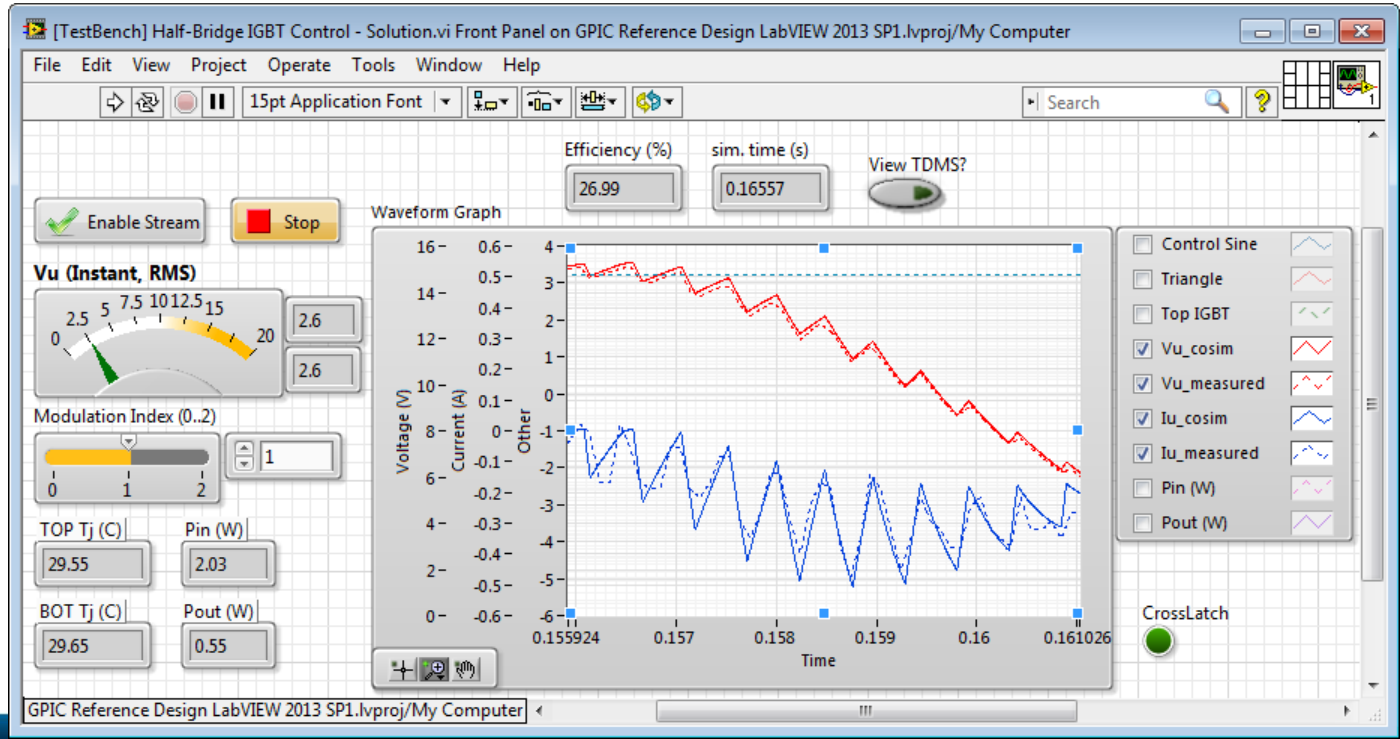
Reproduce a control sine wave using PWM





[Module 1, Exercise 4] Comparing Simulated vs. Experimental Results

Download and run control application and retrieve waveforms



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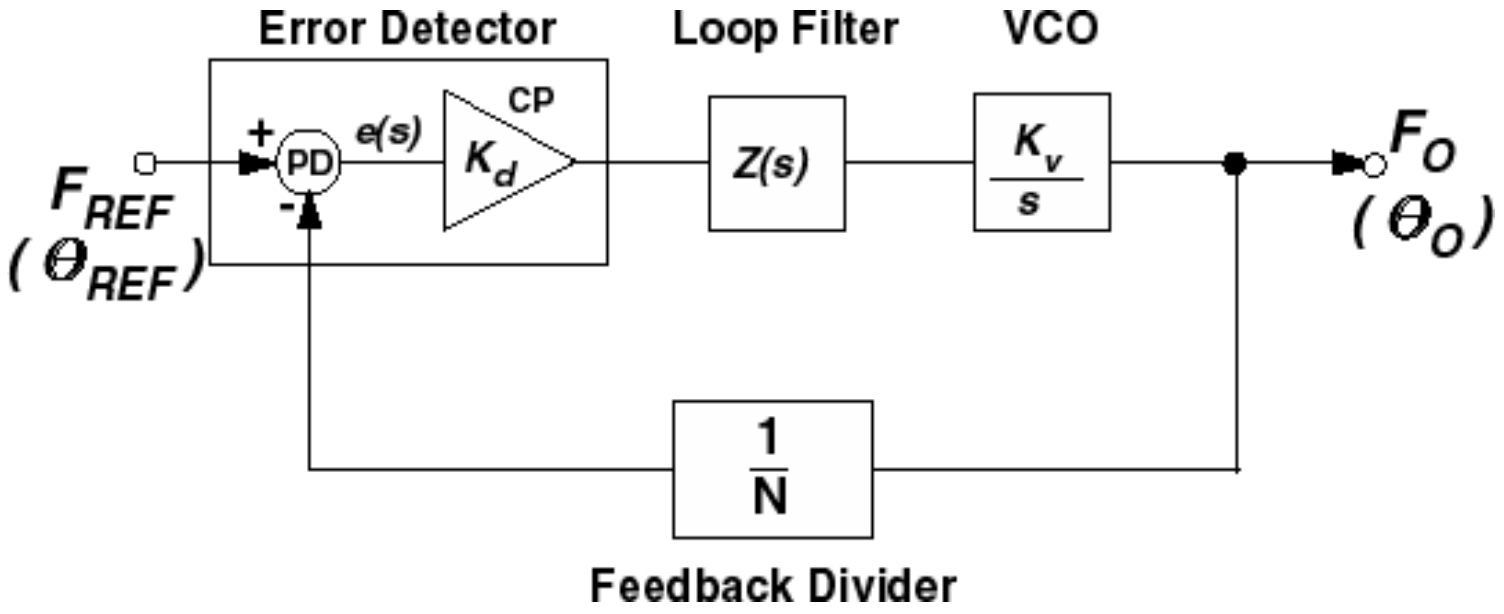
NATIONAL INSTRUMENTS

[Module 2, Exercise 1] Understanding the Phase-Lock Loop (PLL)

Experiment with the PLL using co-simulation



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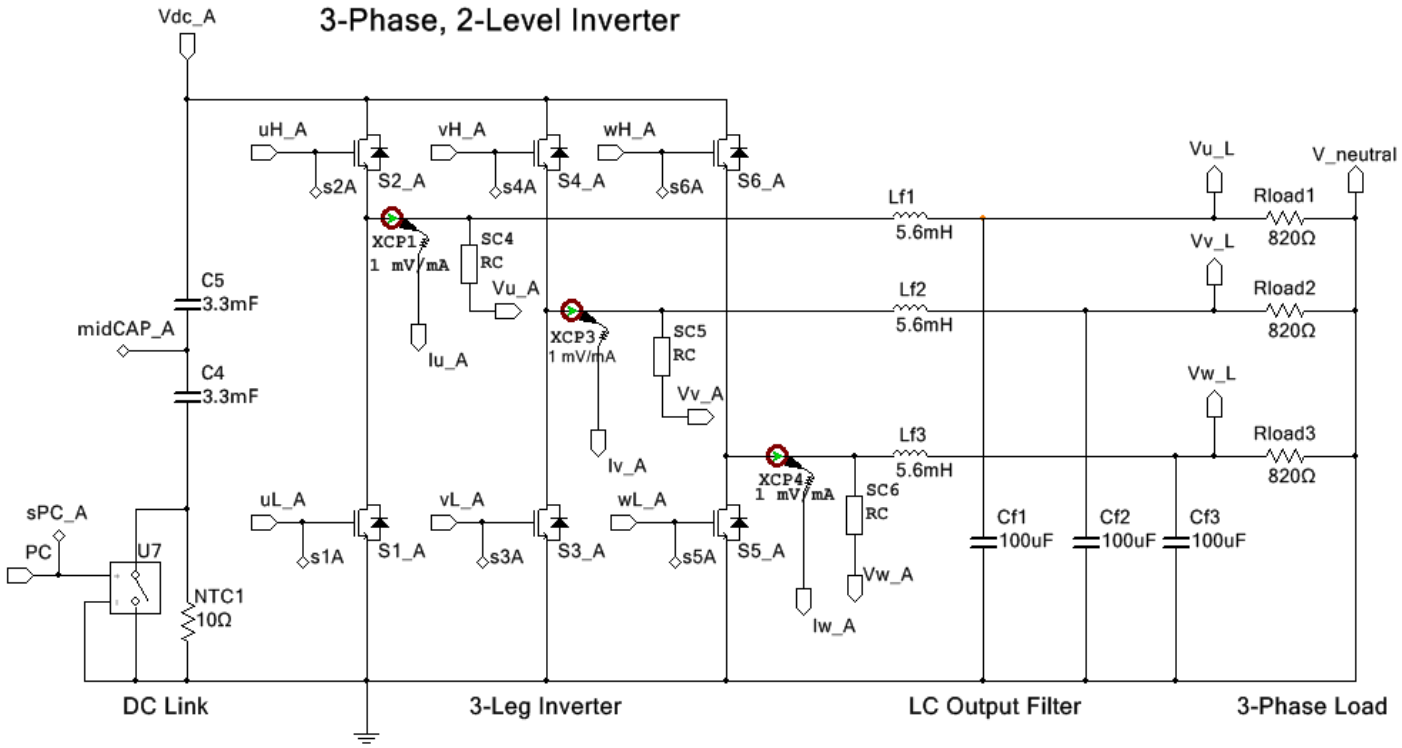
[Module 1, Exercise 2]
3-Phase Inverter Control and Experimental Comparison

Understand the 3-phase inverter circuit and grid synchronized control



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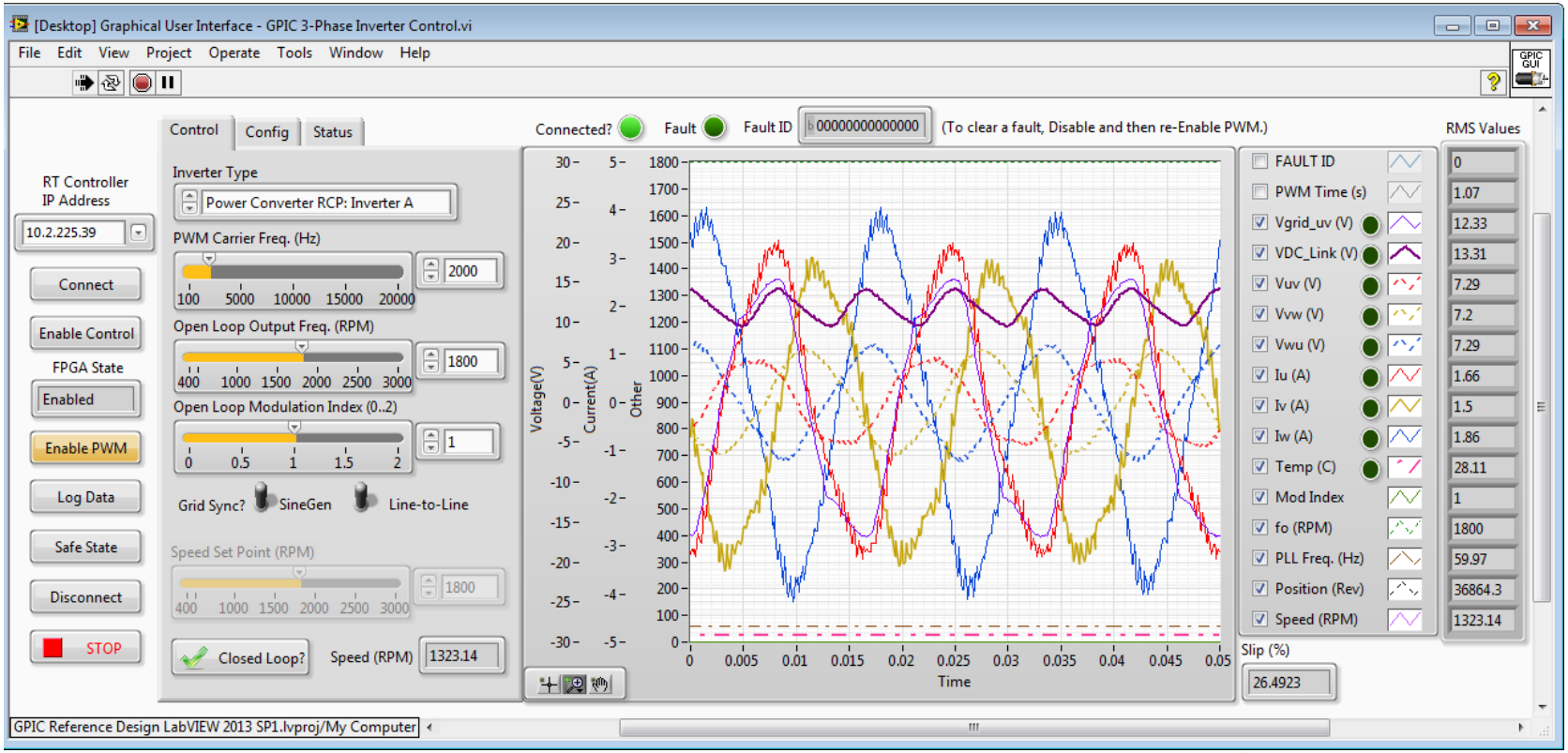
[Module 3, Exercise 1] Understanding the 3-Phase AC Induction Motor

Review motor equations and theory of operation

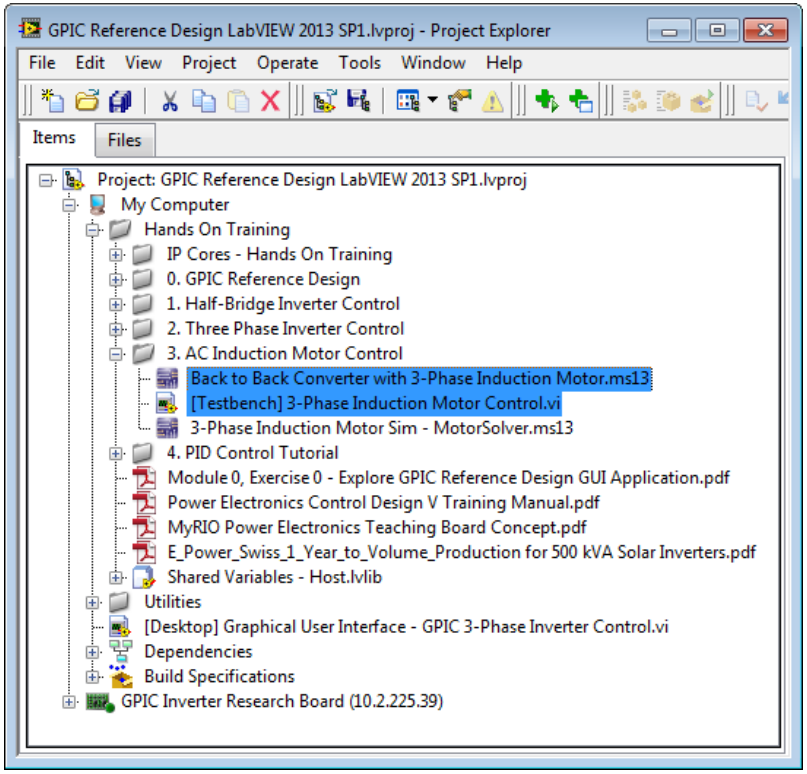
[Module 3, Exercise 2]
Sine-Triangle AC Induction Motor Control

Open loop 3-phase motor operation



[Module 3, Exercise 3] Comparing Simulated vs. Measured Results

Open loop 3-phase motor operation



Note:

- Simulated and Measured current and voltage waveforms are not expected to match, since the initial angle of the physical motor is random.

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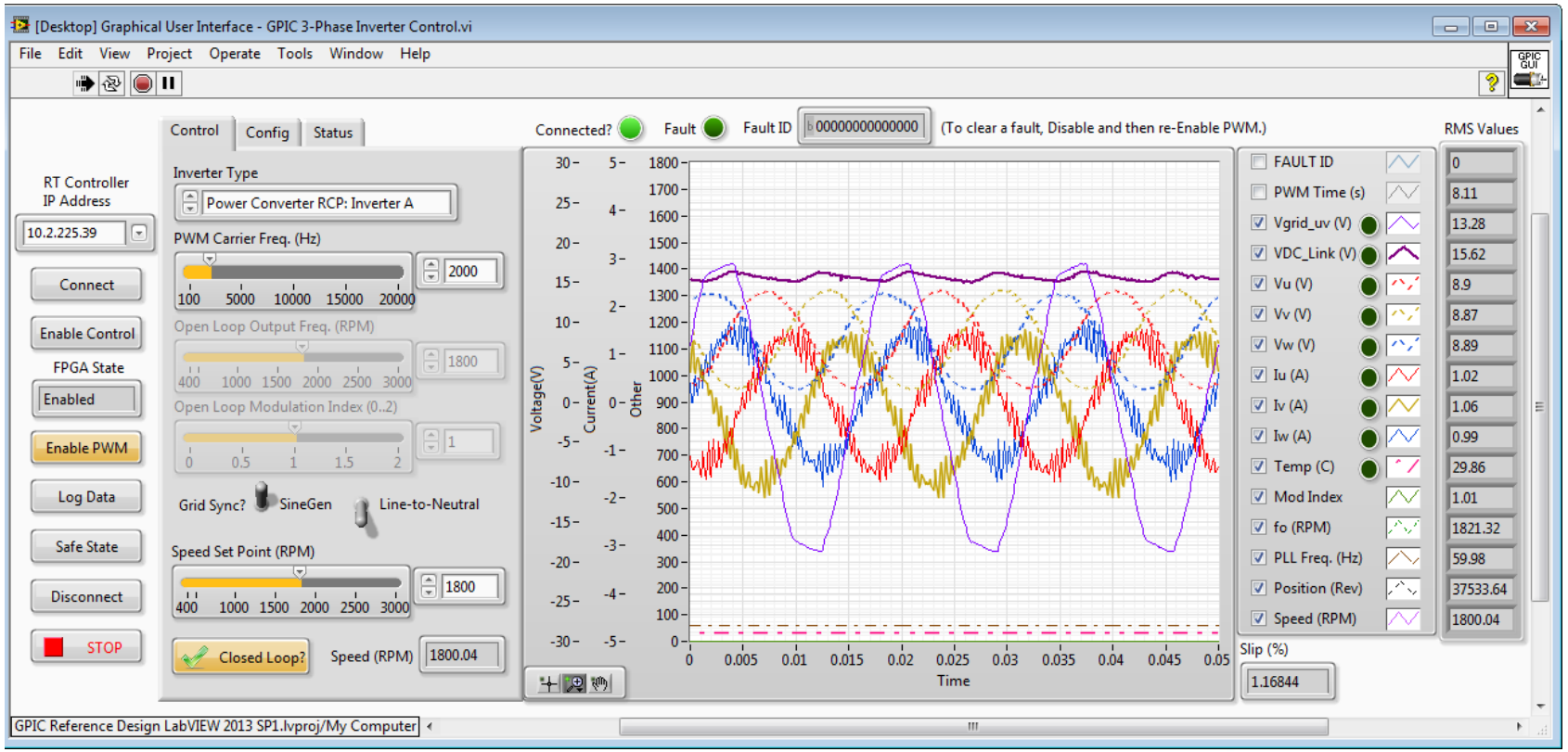
[Module 3, Exercise 4]
AC Induction Motor Voltage-over-Frequency Control

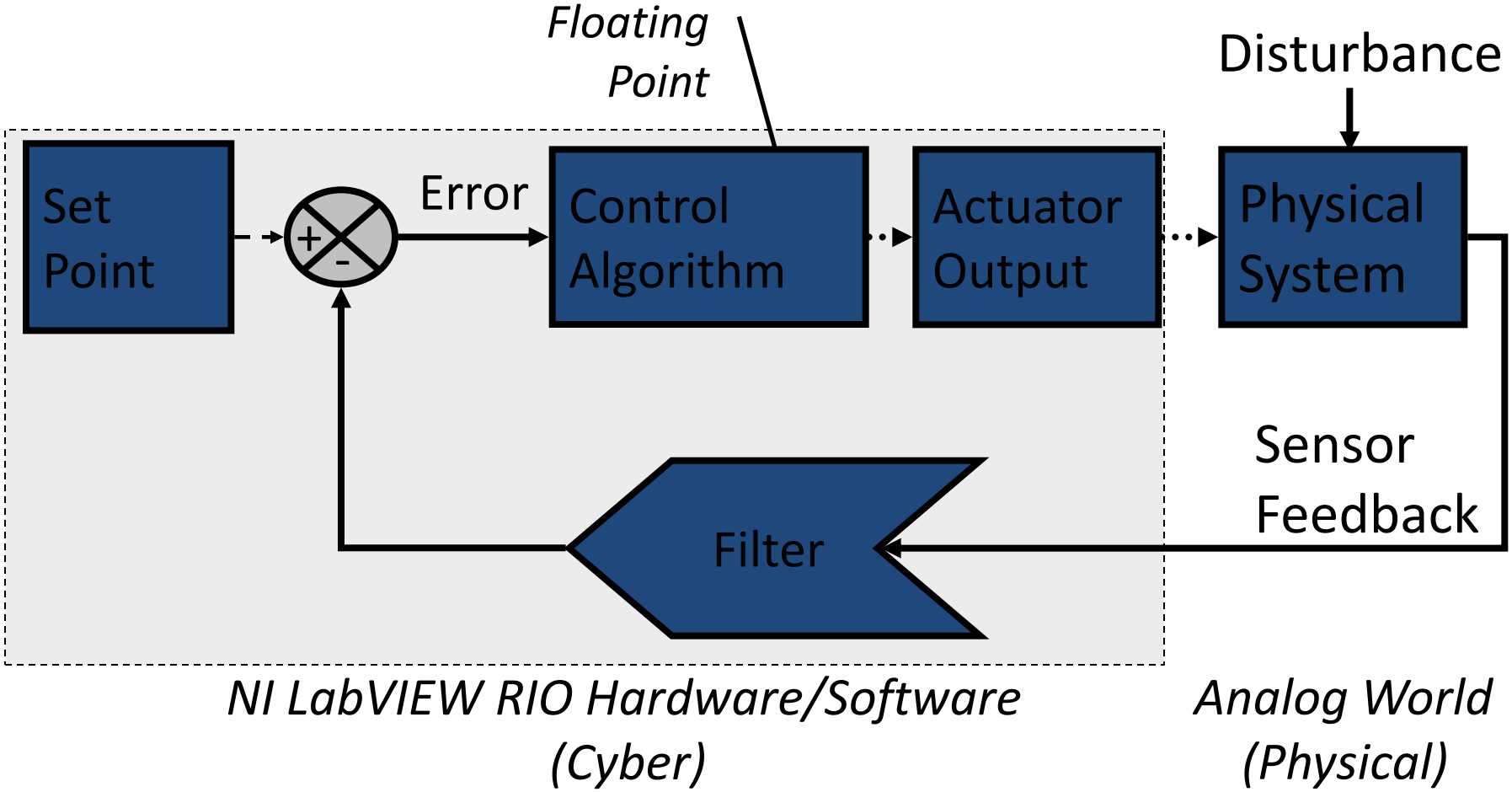
Closed loop 3-phase motor operation



PID Control Tutorial

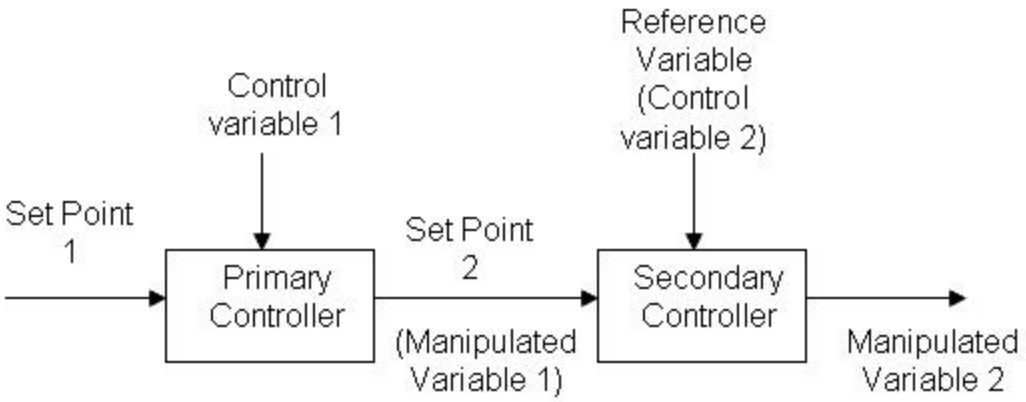
Understanding cascaded PID control, time constants, and frequency response

Cyber Physical System (CPS)



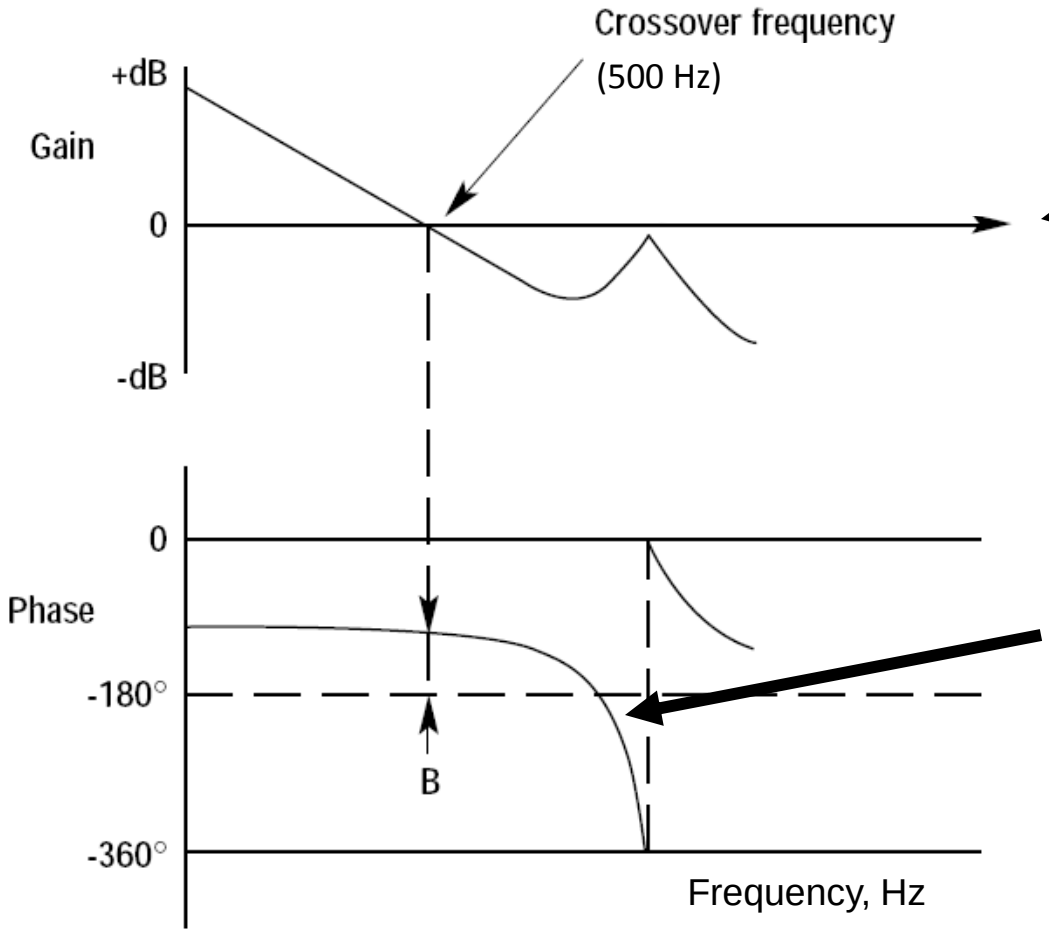
Cascaded Control Loops

- The inner most loop typically executes the fastest
- The Output of the outer controller is the setpoint to the inner controller



Frequency Response

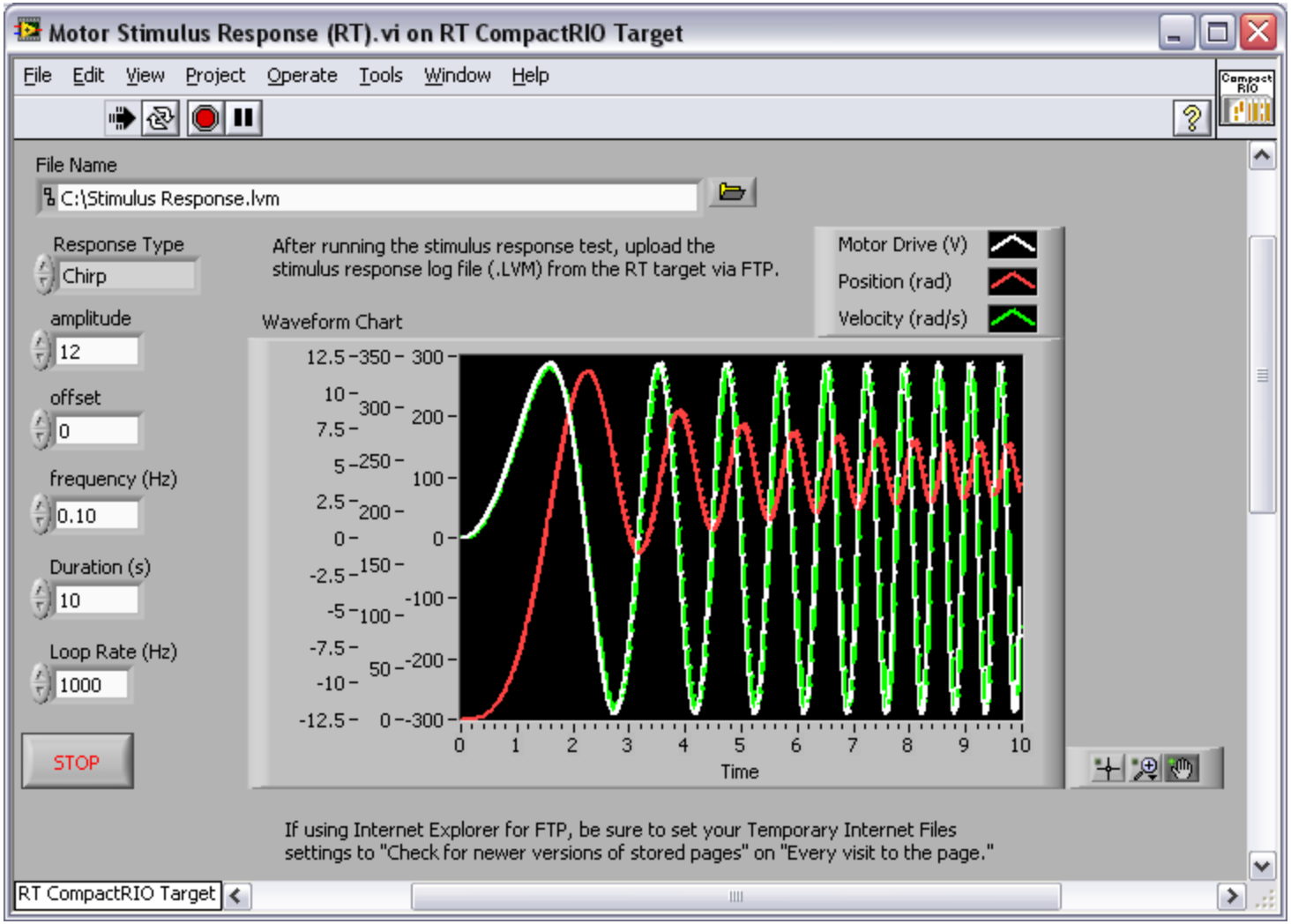
- The gain and phase response of a system is frequency dependent



0 dB represents a gain of 1:
The amplitude of response equals the amplitude of the stimulus
(a.k.a. unity-gain frequency, phase margin frequency)

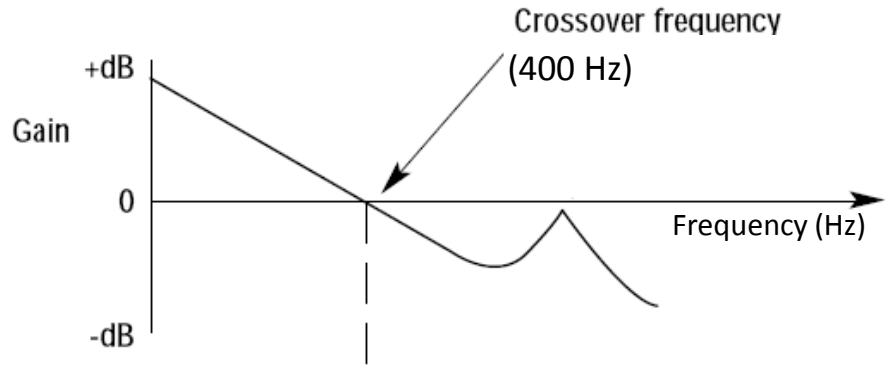
Phase < -180º indicates positive feedback
Gain must be < 1 for stability in this region
(Gain margin is measured at the -180º crossing frequency)

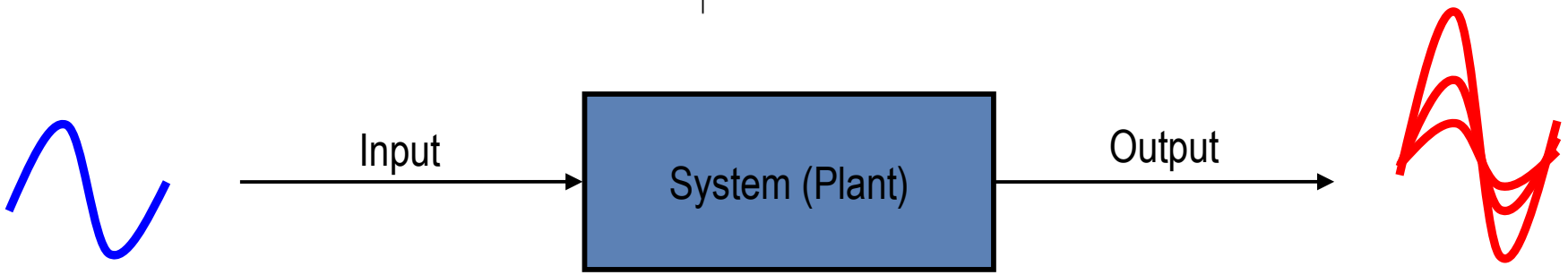
Frequency Dependence of Amplitude and Phase



Frequency Response

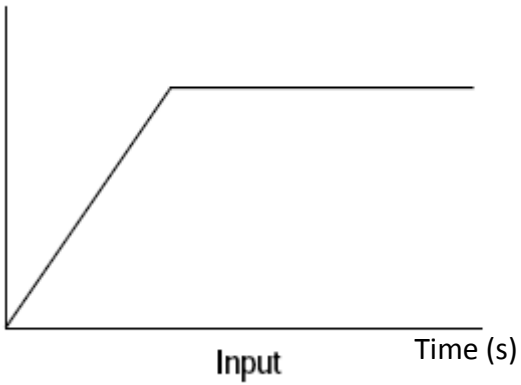
- Gain Crossover Frequency
  - The frequency at which the amplitude response of the system has a gain of 1 (0 dB)

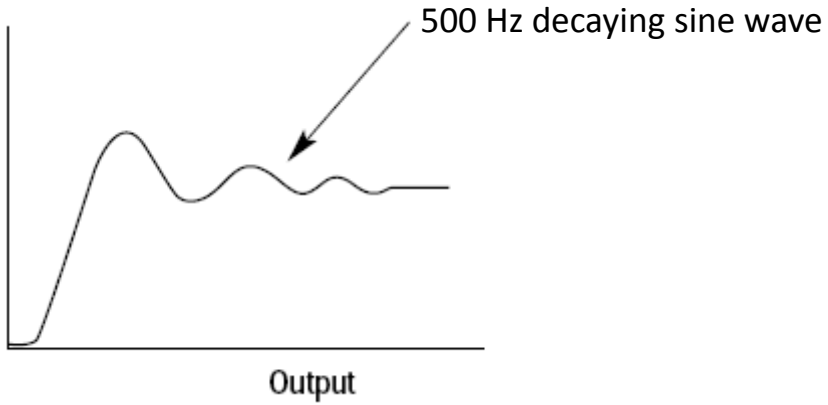


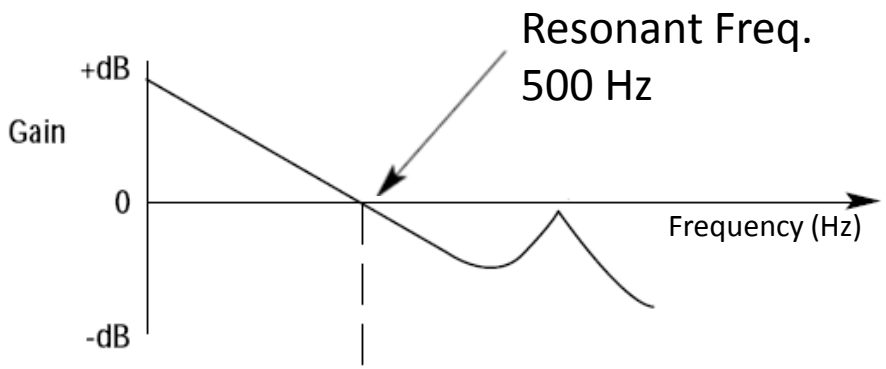


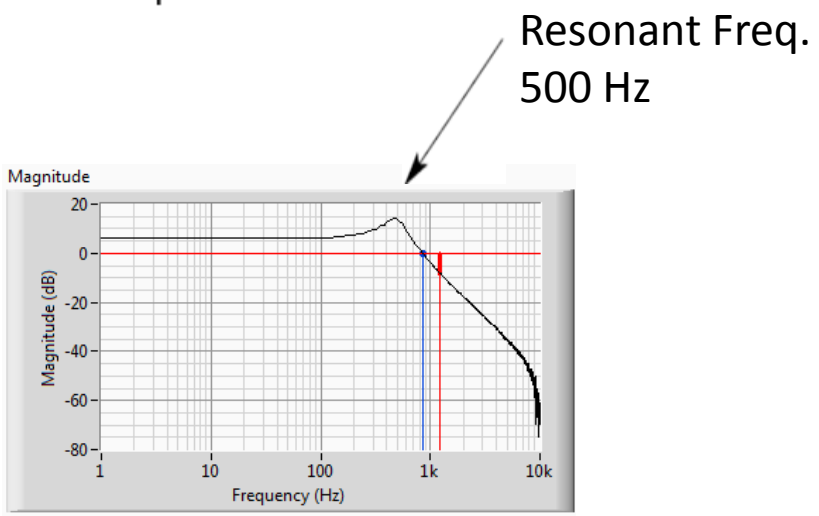
Resonant Frequency

- Resonant ringing occurs at natural frequency or unity gain frequency



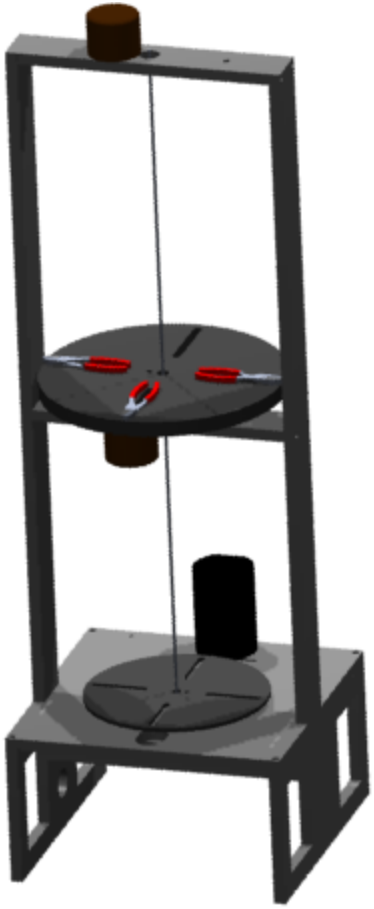


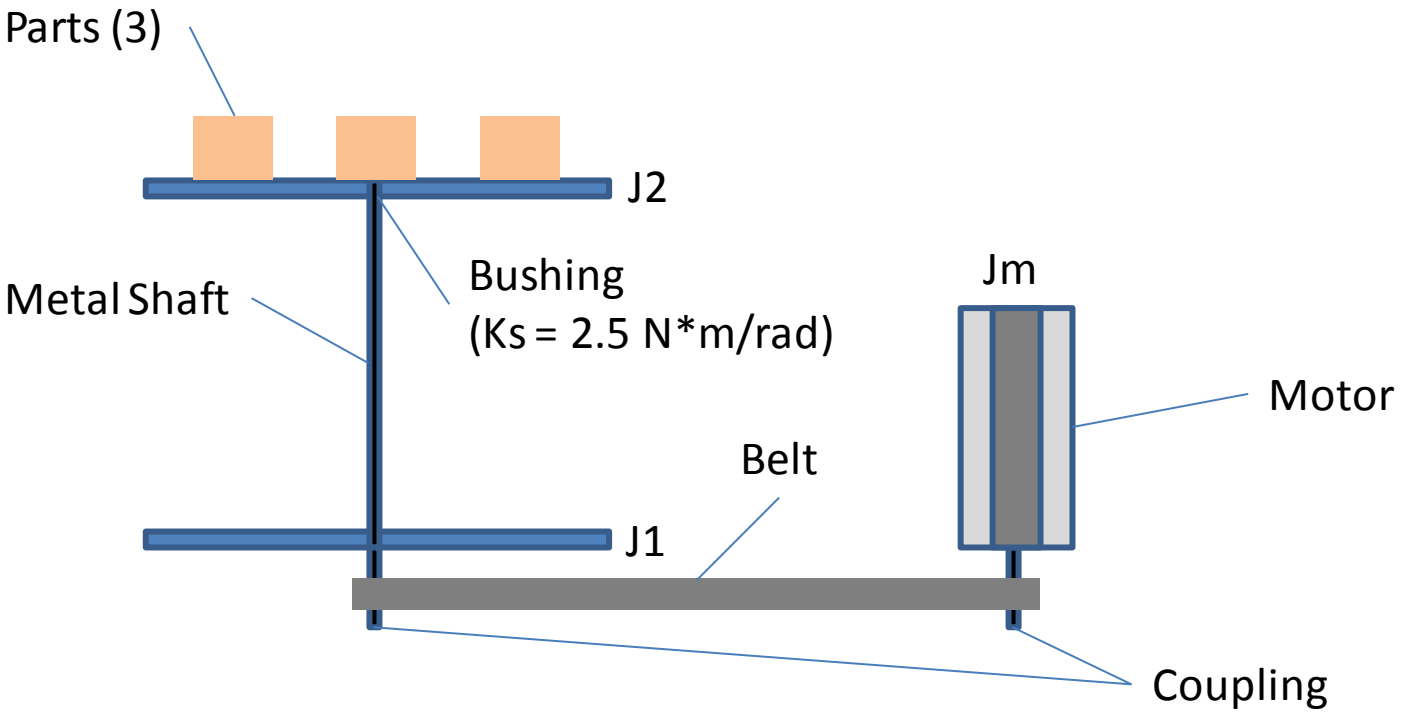




Second Order Systems (Mass-Spring-Damper)

(Systems That Are Not Perfectly Stiff)

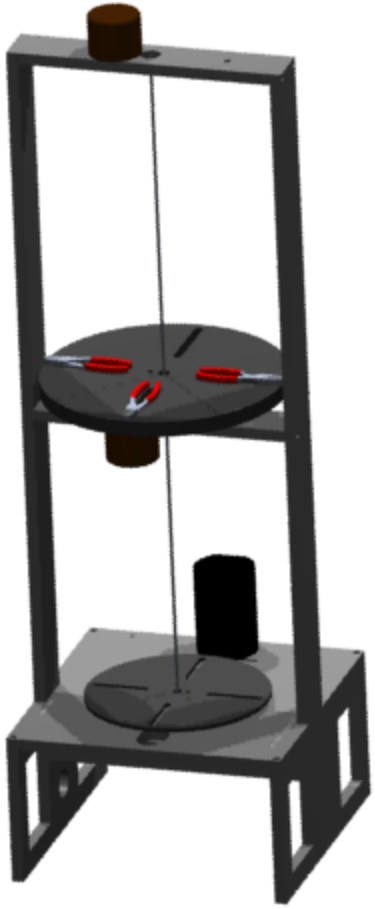




Metal Shaft with Torsional Compliance

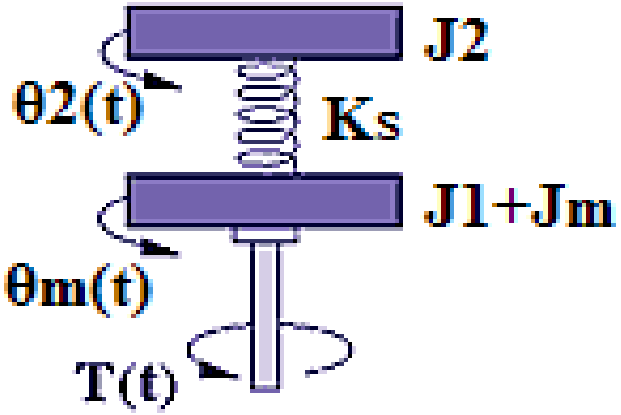
Second Order Systems (Mass-Spring-Damper)

(Systems That Are Not Perfectly Stiff)



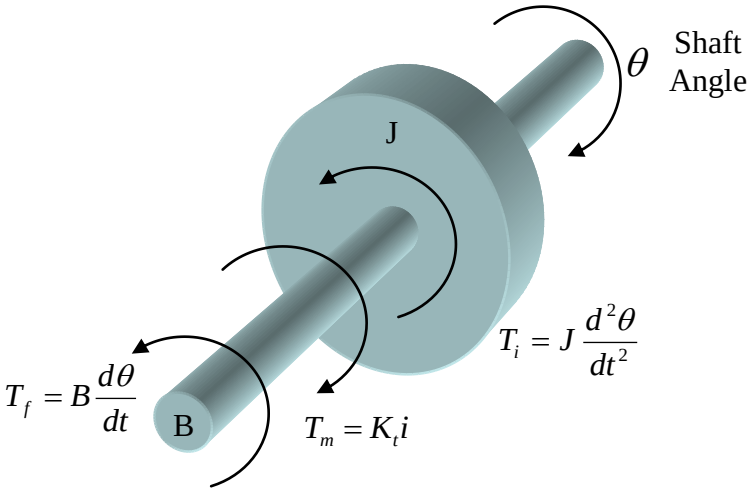
$$\ddot{\theta}_2(t) = -\frac{K_s}{J_2}[\theta_2(t) - \theta_m(t)]$$

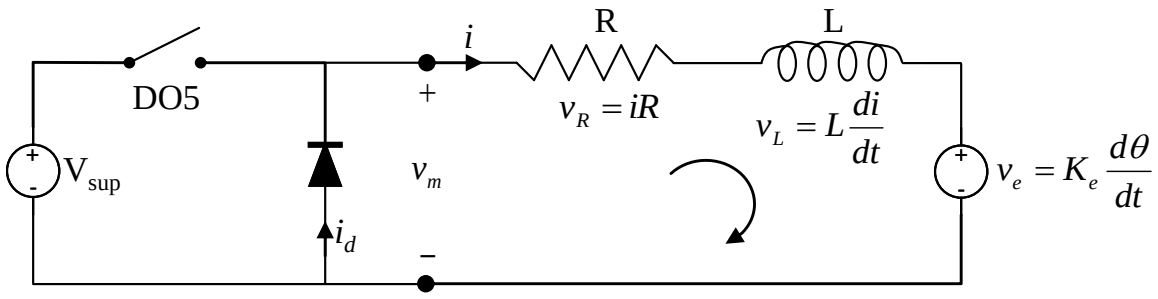
$$\ddot{\theta}_m(t) = \frac{K_t}{J_m + J_1} i - \frac{K_s}{J_m + J_1}[\theta_m(t) - \theta_2(t)] - \frac{B_m}{J_m + J_1}\dot{\theta}_m(t)$$



Mechanical Model

Brushed DC Motor Model
(Mechanical and Electrical)





Sum of Forces = 0

$$0 = K_t i - J\frac{d^2\theta}{dt^2} - B\frac{d\theta}{dt}$$

Kirchoff's Voltage Law

$$v_m = Ri + L\frac{di}{dt} + K_e\frac{d\theta}{dt}$$

Rearrange to put highest order derivative terms on the left side of equation:

$$\frac{d^2\theta}{dt^2} = \frac{K_t}{J}i - \frac{B}{J}\frac{d\theta}{dt}$$

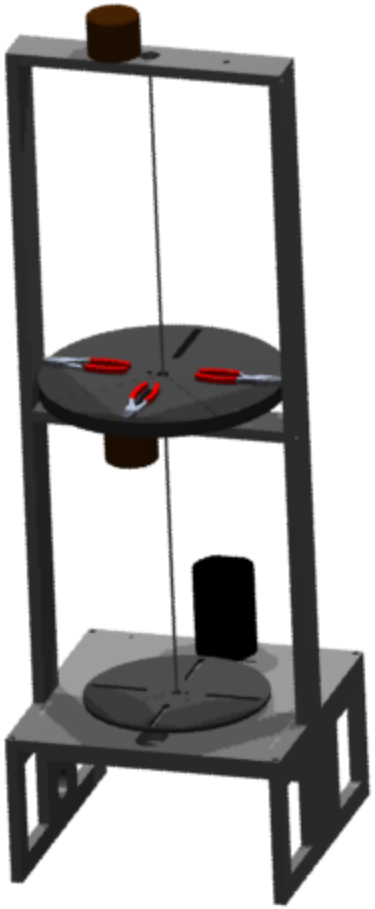
$$\frac{di}{dt} = -\frac{R}{L}i - \frac{K_e}{L}\frac{d\theta}{dt} + \frac{v_m}{L}$$

Mechanical Model

Electrical Model

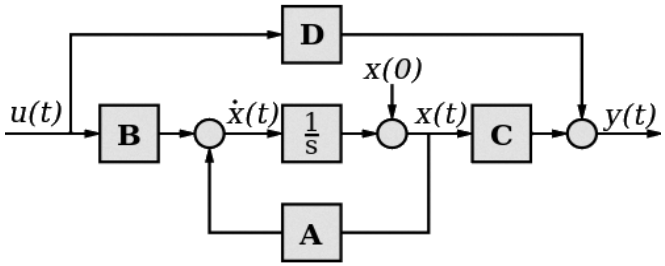
State-Space Model

(Multiple-Inputs, Multiple-Outputs)



$$\dot{x}(t) = A(t)x(t) + B(t)u(t)$$

$$y(t) = C(t)x(t) + D(t)u(t)$$



$$\begin{matrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{matrix} = \begin{matrix} \theta_2 \\ \dot{\theta}_2 \\ \theta_m \\ \dot{\theta}_m \end{matrix} \qquad \begin{matrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \\ \dot{x}_4 \end{matrix} = \begin{matrix} x_2 \\ \ddot{\theta}_2 \\ x_4 \\ \ddot{\theta}_m \end{matrix} = \begin{matrix} \dot{\theta}_2 \\ \ddot{\theta}_2 \\ \dot{\theta}_m \\ \ddot{\theta}_m \end{matrix} \qquad \begin{matrix} u_1 \\ u_2 \\ u_3 \\ u_4 \end{matrix} = \begin{matrix} i \\ 0 \\ 0 \\ 0 \end{matrix} \qquad \begin{matrix} y_1 \\ y_2 \\ y_3 \\ y_4 \end{matrix} = \begin{matrix} \theta_2 \\ \dot{\theta}_2 \\ \theta_m \\ \dot{\theta}_m \end{matrix}$$

$$\begin{matrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \\ \dot{x}_4 \end{matrix} = \begin{matrix} \dot{\theta}_2 \\ \ddot{\theta}_2 \\ \dot{\theta}_m \\ \ddot{\theta}_m \end{matrix} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ \frac{-K_s}{J_2} & 0 & \frac{K_s}{J_2} & 0 \\ 0 & 0 & 0 & 1 \\ \frac{K_s}{J_m + J_1} & 0 & \frac{-K_s}{J_m + J_1} & \frac{-B_m}{J_m + J_1} \end{bmatrix} \begin{bmatrix} \theta_2 \\ \dot{\theta}_2 \\ \theta_m \\ \dot{\theta}_m \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \frac{K_t}{J_m + J_1} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

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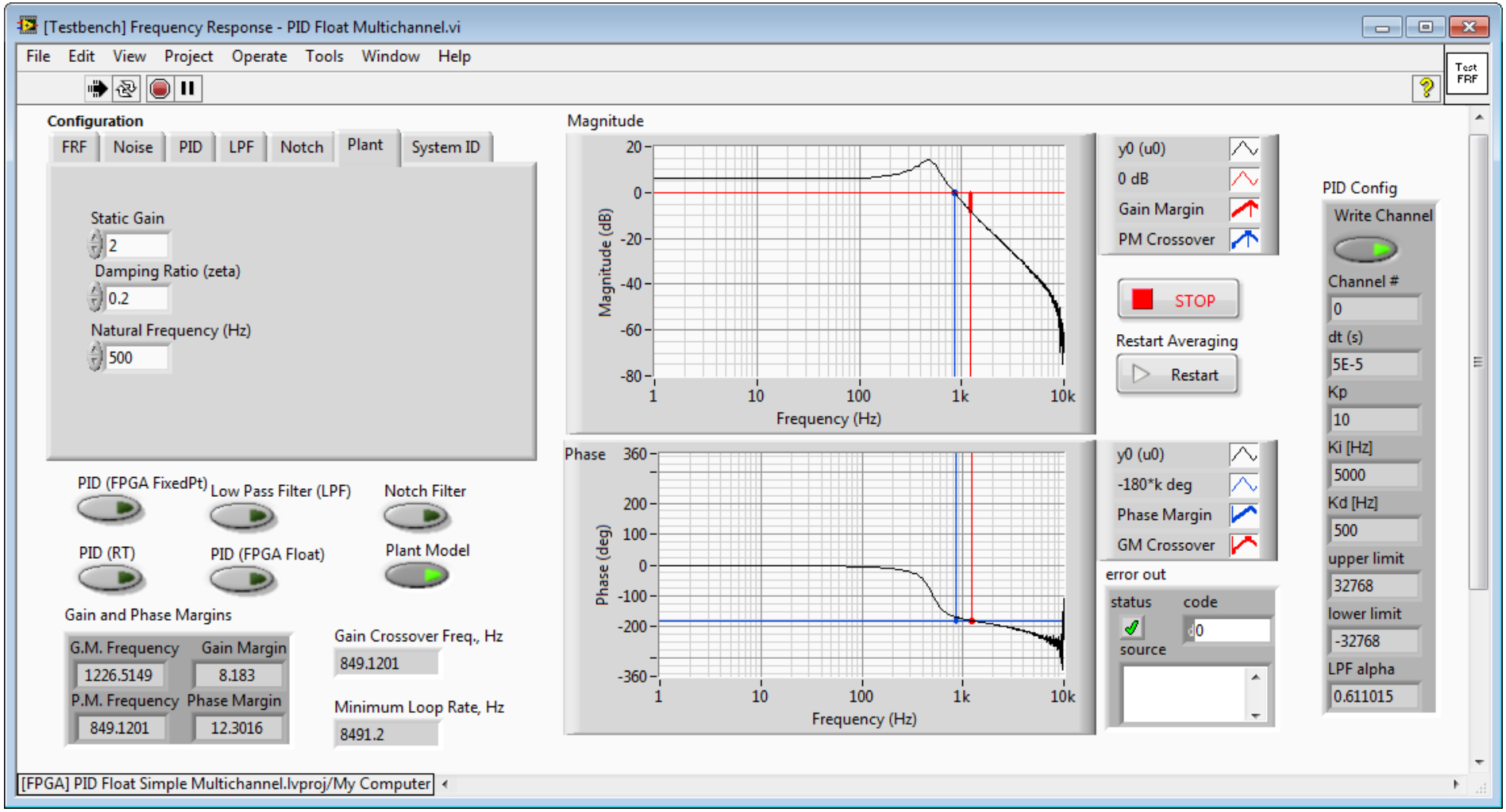
Open Loop Frequency Response
Second Order Systems (Mass-Spring-Damper)

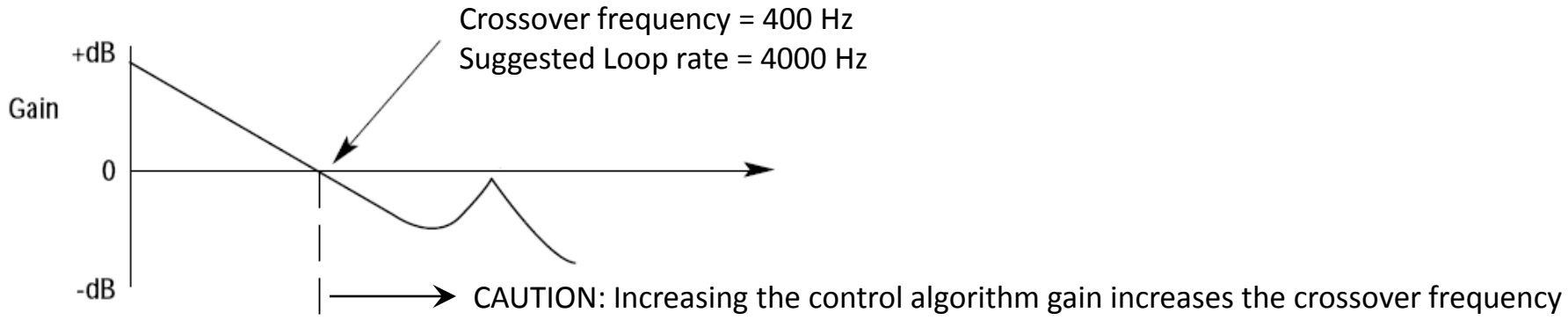


Using Frequency Response for Stability Analysis

- Gain Margin and Phase Margin
  - Must be positive for a stable system
  - The larger they are, the more stable the system will be
- To guarantee stability under all conditions:
  - Must make sure gain is less than 1 at all frequencies at which the phase is greater that -180 degrees

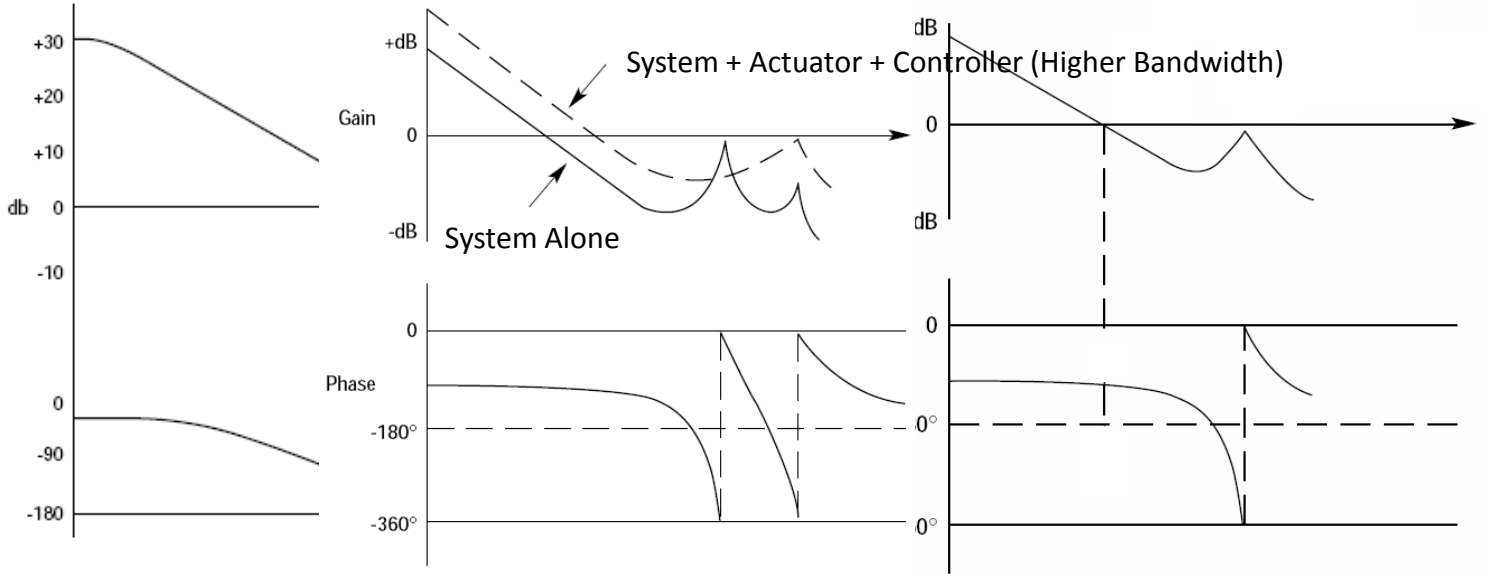
What can you learn from the frequency response?

- Loop Rate Requirements
  - How fast the control system need to be
- Rule of thumb
  - The control loop should be at least ten times faster than the gain crossover frequency of the system (minimum 2X faster)

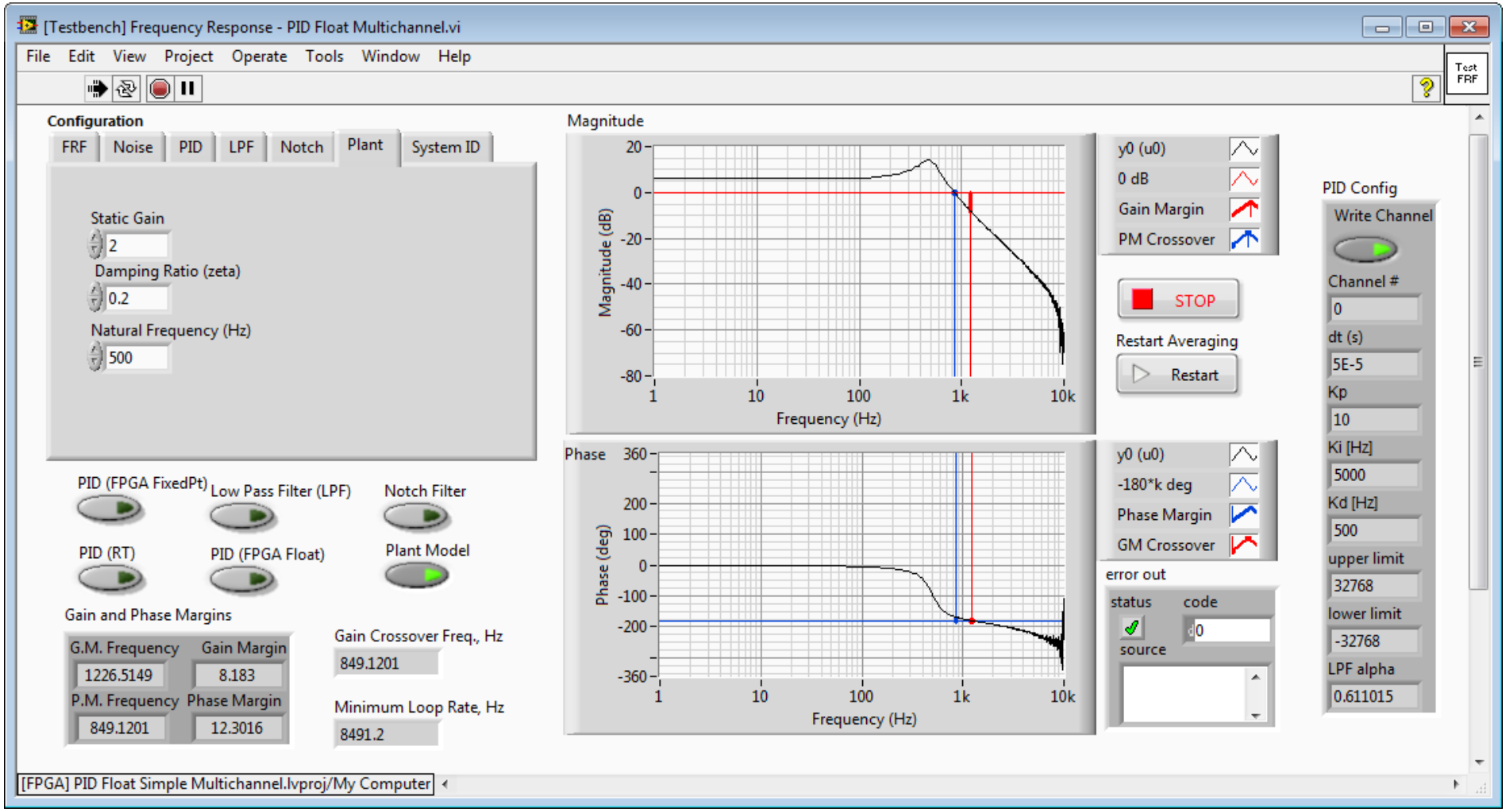


How does the control algorithm effect the response?

- Stability
  - Adding a control compensator will effect the stability and response
    - The controller changes the gain and frequency response of the system



Demo: Understanding Control System Frequency Response

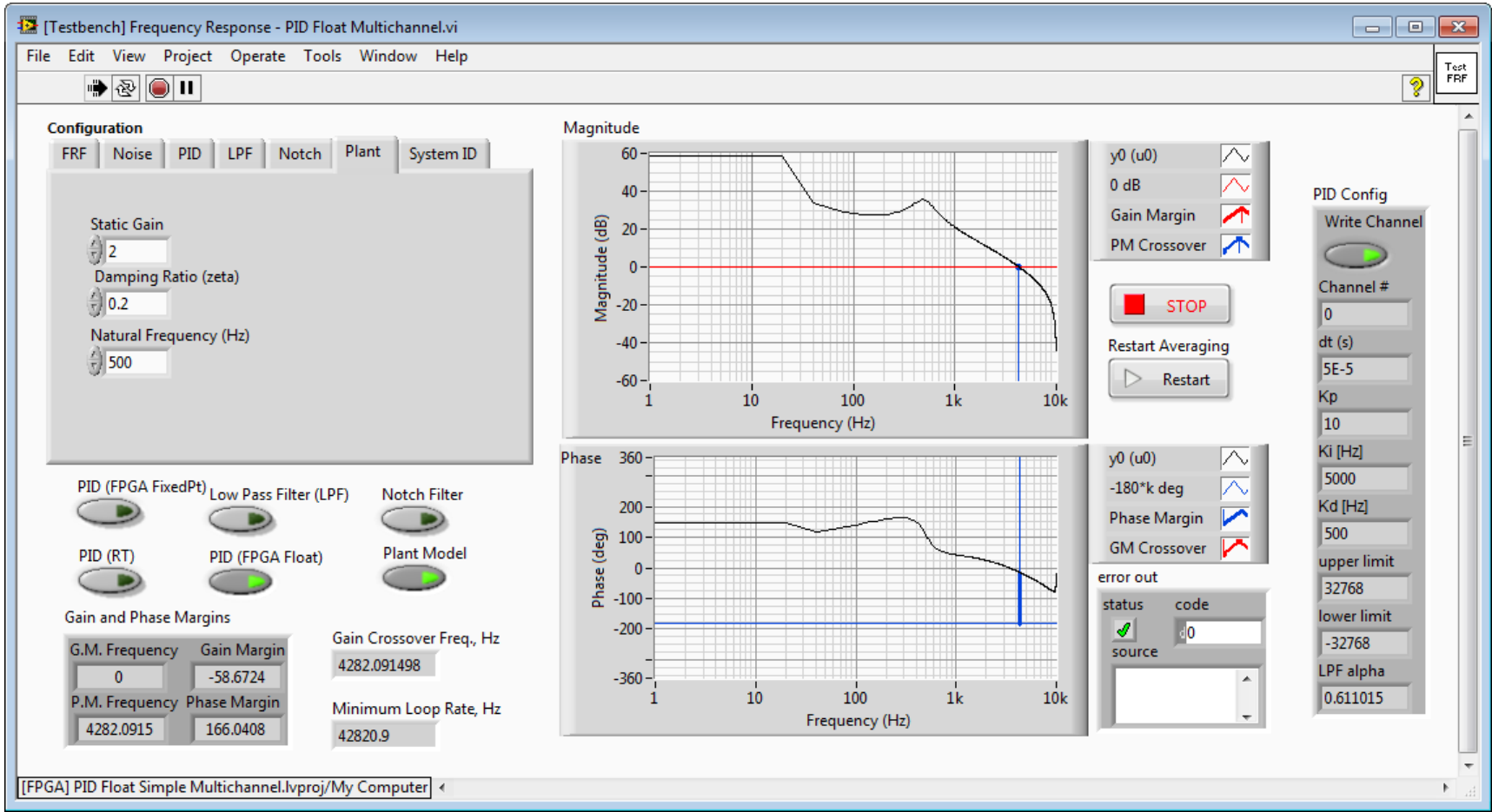


Frequency Response Analysis

Second Order Plant + Multichannel Float PID IP Core (Series Connection): Frequency Response (Open Loop)

Observations:

1. Note the smooth FRF out to Nyquist (10 kHz). System is stable with respect to gain margin. Note the phase never crosses -180 degrees. The gain is extremely small at high frequency (-58.7 db)
2. Gain crossover frequency of 4282 Hz suggests a minimum control loop rate of 42,820 Hz. (By adding this high gain control compensator, the bandwidth of the system has increased significantly, necessitating a fast control system for stable control.)
3. To be stable, the phase of the system must be greater than -180 degrees at this P.M. frequency. In this case, the phase margin is 166 degrees.



Why floating point?

- Problem: Discrete time simulations become numerically unstable as two or more poles approach the edge of the unit circle and overlap.

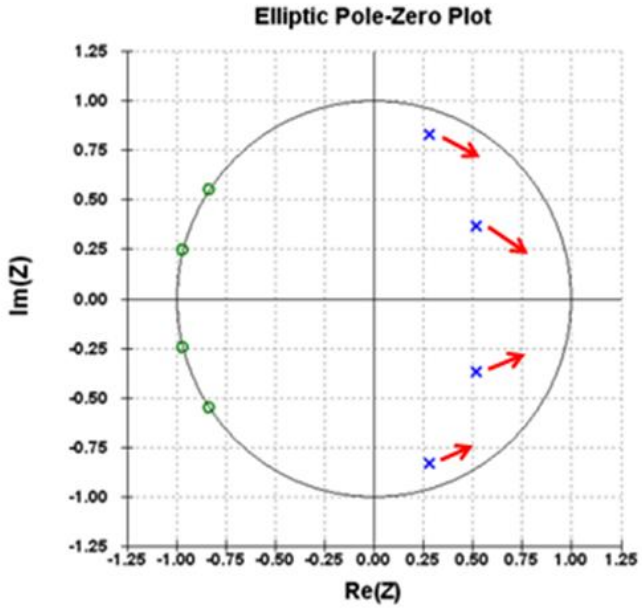


Figure 11. Increasing the sampling rate pushes the poles closer to the stability boundary.

Why floating point?

Problem: Linear discrete time solvers go numerically unstable if a pole reaches the edge of the unit circle or two poles overlap.

RLC Circuit Example (2nd order):

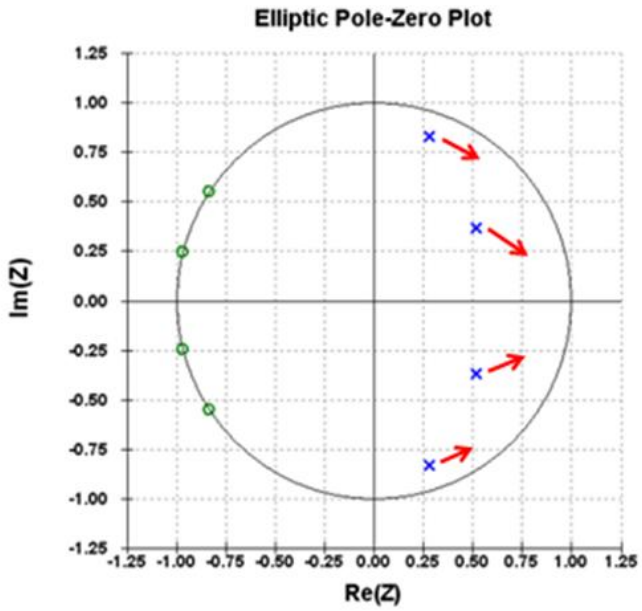
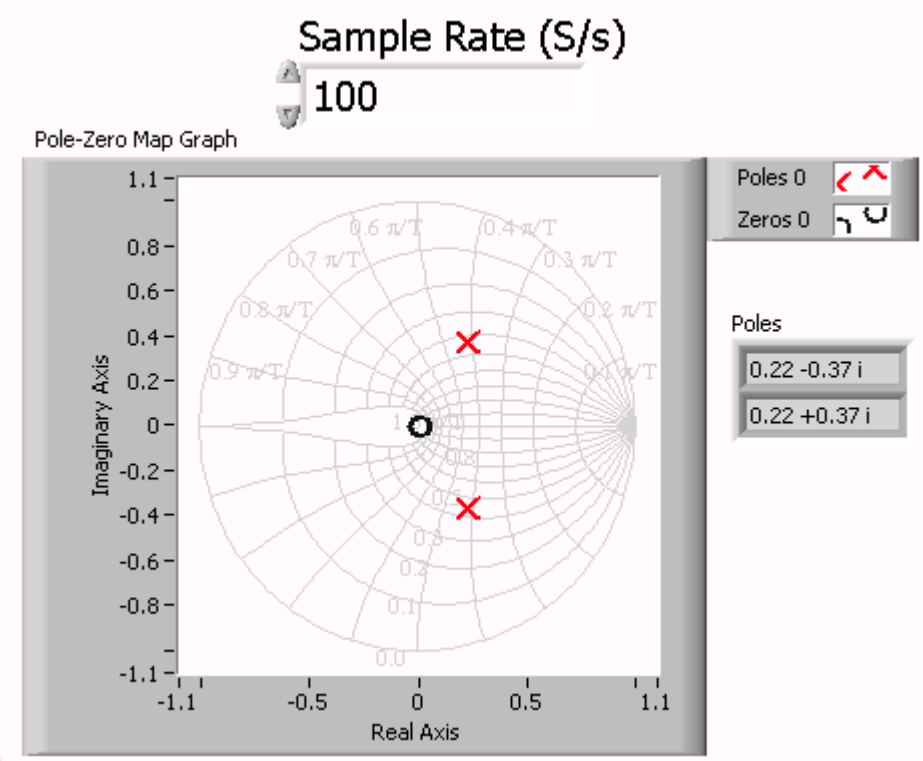


Figure 11. Increasing the sampling rate pushes the poles closer to the stability boundary.



NATIONAL INSTRUMENTS

Why floating point?

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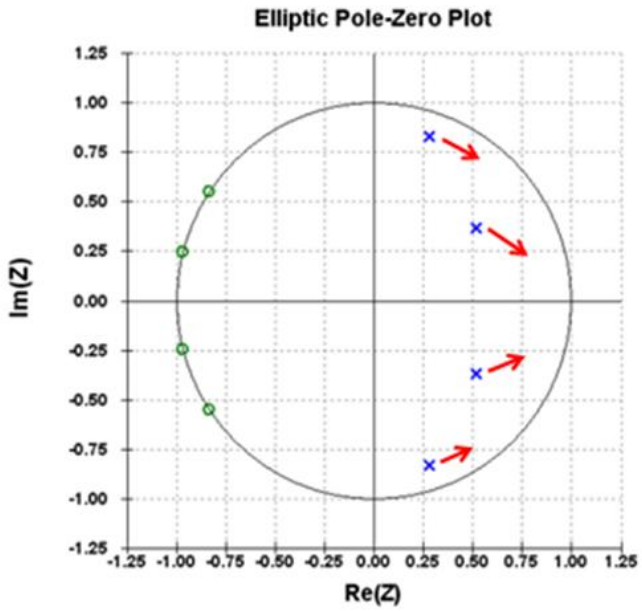
RLC Circuit Example (2nd order):



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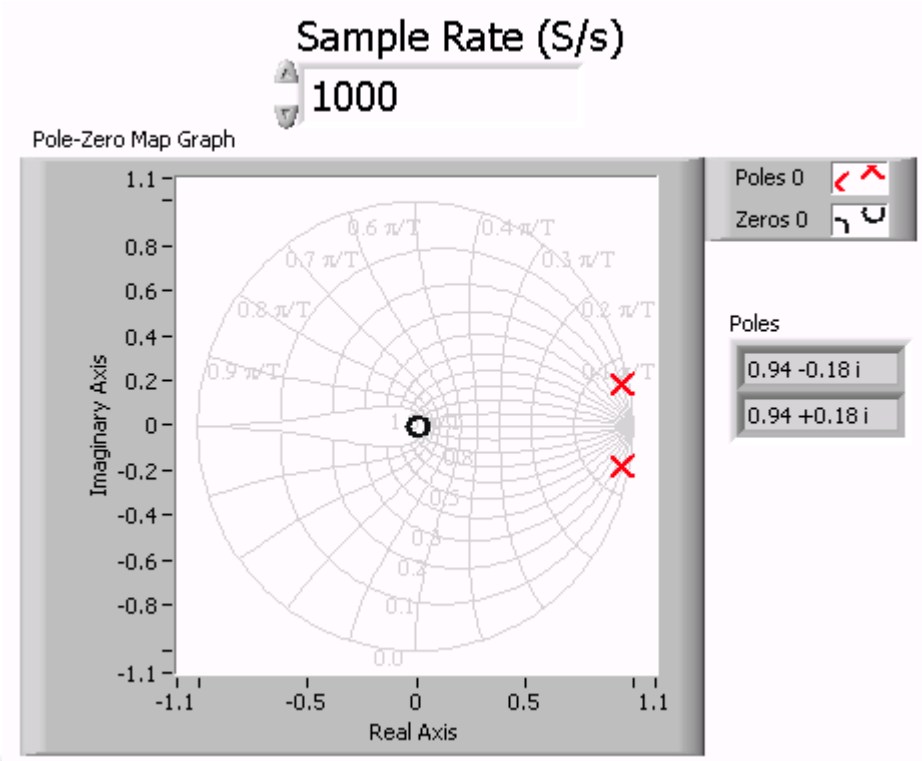

NATIONAL INSTRUMENTS

Why floating point?

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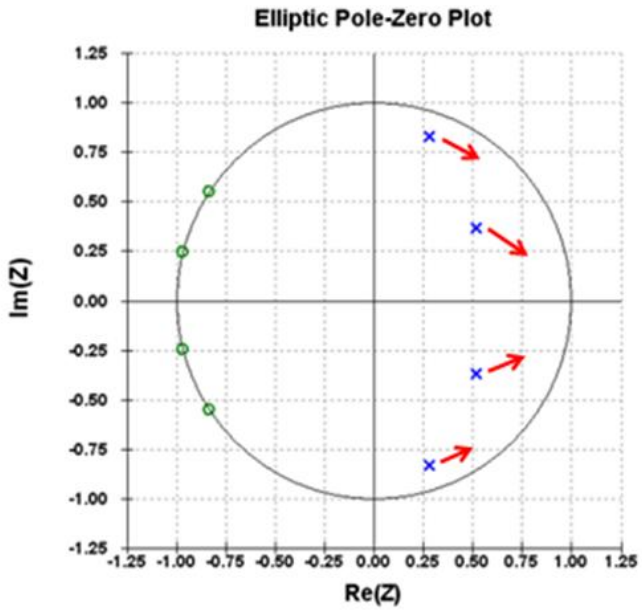

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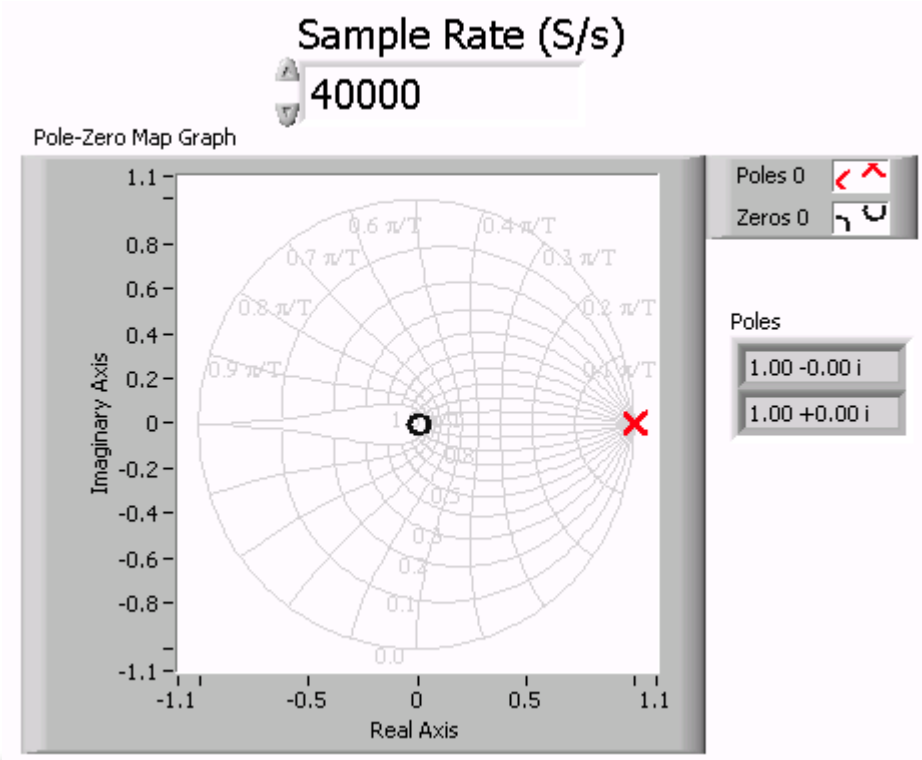
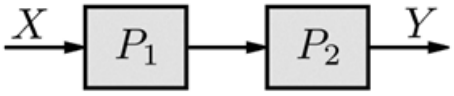


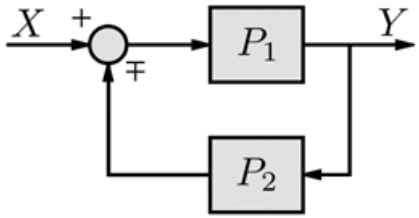
NATIONAL INSTRUMENTS

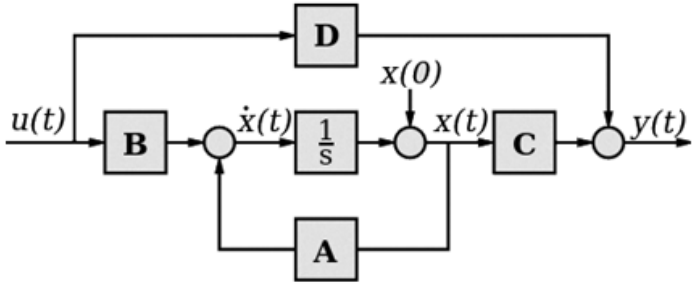
Why floating point?

- Fixed point algorithms connected in cascaded or feedback paths may be individually stable but become numerically unstable when connected
  - Violates CS principal of modular design

The simplest common interconnections of transfer functions are shown below (series connection, feedback loop, state-space connection, etc.). More complex control algorithms and simulations are constructed using a variety of interconnections (more information).

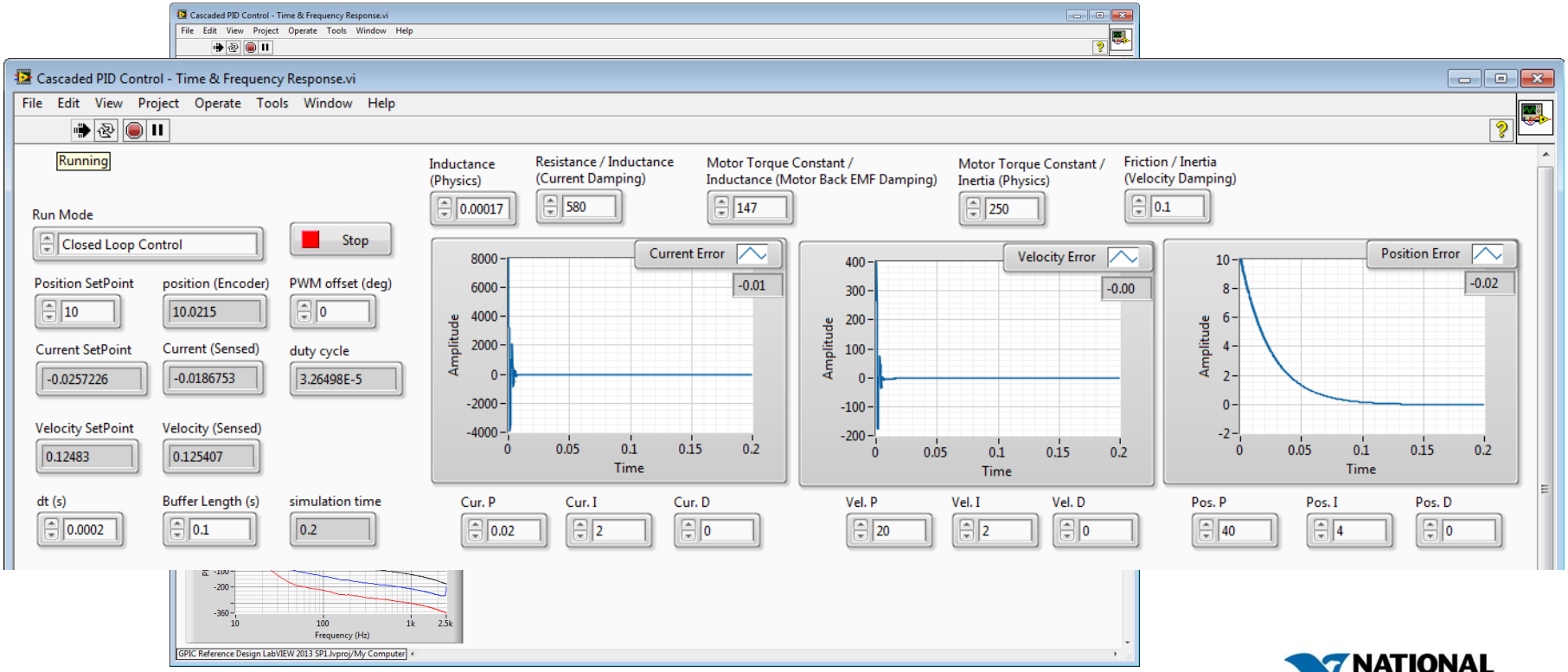






[Module 3, Exercise 5]
PID Control Tutorial

Understanding cascaded PID control, time constants and frequency response



NATIONAL INSTRUMENTS

NI Power Electronics Control Design V Training Workshop

Workshop Agenda

1. Power Electronics
2. NI Design V Toolchain
3. Training Kits & Reference Design
4. The NI LabVIEW RIO Approach
5. Hands On Modules 1-3
6. Case Studies & Latest Releases

Hands-On Exercises

Module 1: Single Phase Power Conversion

1. Configuring your NI RIO Embedded System
2. Understand the GPIC Reference Design App.
3. Half-Bridge DC-to-AC Inverter Control
4. Pulse Width Modulation Logic
5. Sine-Triangle Pulse Width Modulation
6. Comparing Simulated vs. Experimental Results

Module 2: Three Phase Grid Synchronized Inverter Control

1. Understanding 3-Phase Power and the PLL
2. 3-Phase DC-to-AC Inverter Control
3. Comparing Simulated vs. Experimental Results
4. Grid Synchronized Inverter Control

Module 3: AC Induction Motor Control

1. Understanding the 3-Phase AC Induction Motor
2. Sine-Triangle AC Induction Motor Control
3. Comparing Simulated vs. Experimental Results
4. Voltage-over-Frequency Control
5. PID Control Tutorial

Module 4: Power Electronics Real-Time HIL Simulation

1. LabVIEW FPGA Floating Point Math Palette
2. Transfer Function and State-Space Modeling
3. Single-Phase Inverter HIL (Transfer Function)
4. Three-Phase Inverter HIL (State-Space)
5. AC Induction Motor HIL (Custom)
6. Automatic Multisim-to-FPGA Conversion HIL

Case Studies

Two years after project start

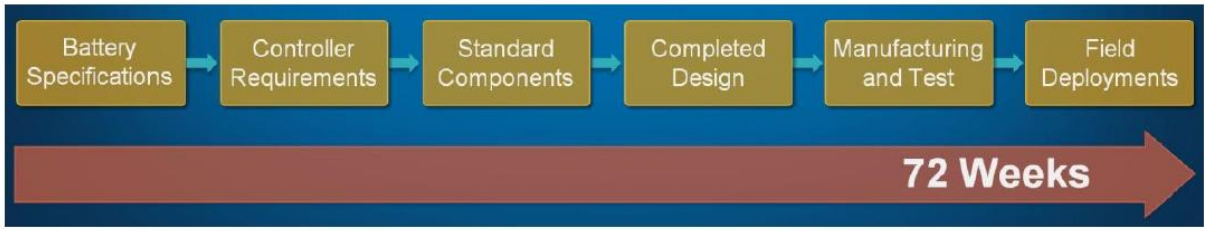
In the meantime **hundreds of inverters** are running in PV power plants.
Thanks to code reusability for cheaper controllers, the costs could be reduced.

Running power plants

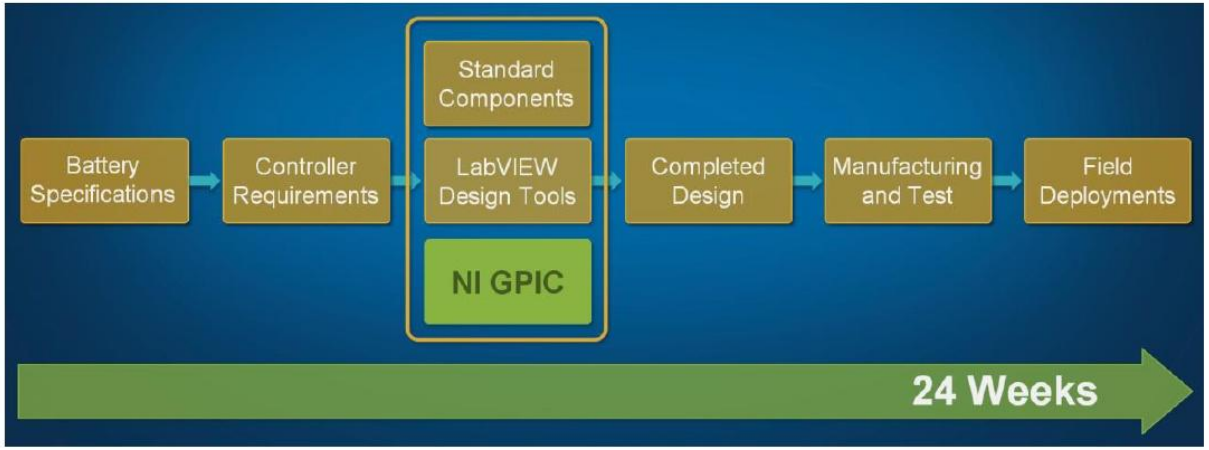
Project	Installation	Location	Ambient
A La Shan	20 MW	Inner Mongolia	Desert
Xie Tie Shan	20 MW	Qinghai/Tibet (plateau)	3600 m over sea, High altitude
Yu Men	20 MW	Gansu	Desert
Chinese Medicine Greenhouse	30 MW	Shandong	Lage scale roof top
Dun Huang	20 MW	Gansu	Dessert
Le Ping	19 MW	Jiangxi	Lage scale roof top
Han Chuan	5 MW	Hubei	Lage scale roof top

Dynapower

- Reduced development time from 72 to 24 weeks
- Allowed power engineers to program without a software engineer in the middle
- Tool chain gives 90 percent confidence factor in first design



In the past, the Dynapower development cycle was a traditional embedded design process involving a full custom DSP board, text-based programming and simulation models.



The new Dynapower development cycle is based on the NI GPIC hardware and NI LabVIEW RIO graphical system design process, yielding a 3X reduction in development time.

- Integrated AC Breaker with Shunt Trip
- Integrated DC Disconnect
- Integrated DC Pre-Charge
- Integrated DC Input Fuses
- DynaCloud™ - cloud-based remote monitoring and diagnostics

Available Options

- Integrated Transformer
- Black Start
- Revenue Grade Power Meter
- AC Pre-Charge Circuit - permits MPS-100 to be used as a DC voltage source

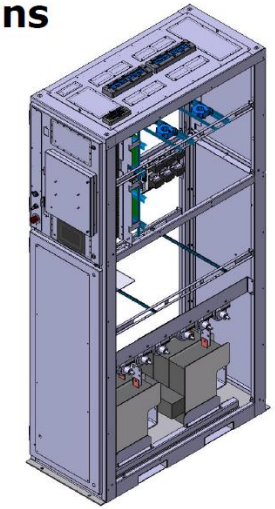
Having provided over 50% of the domestic grid-tied power electronics for battery energy systems the Dynapower Energy Management team brings an unchallenged level of expertise and unrivaled knowledge base to our customers.

Dynapower's engineering team has designed and delivered energy storage systems globally including Asia, North America, Oceania and Australia of systems sized from 25 kW to 36,000 kW.

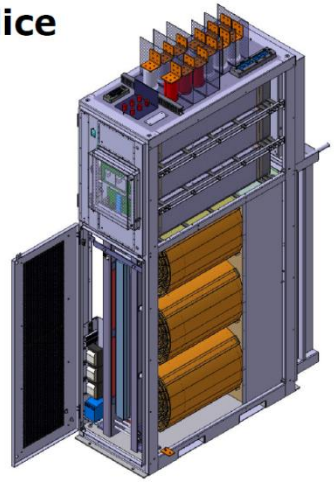
www.dynapower.com

15 MW Modular Multilevel Inverter

Mains

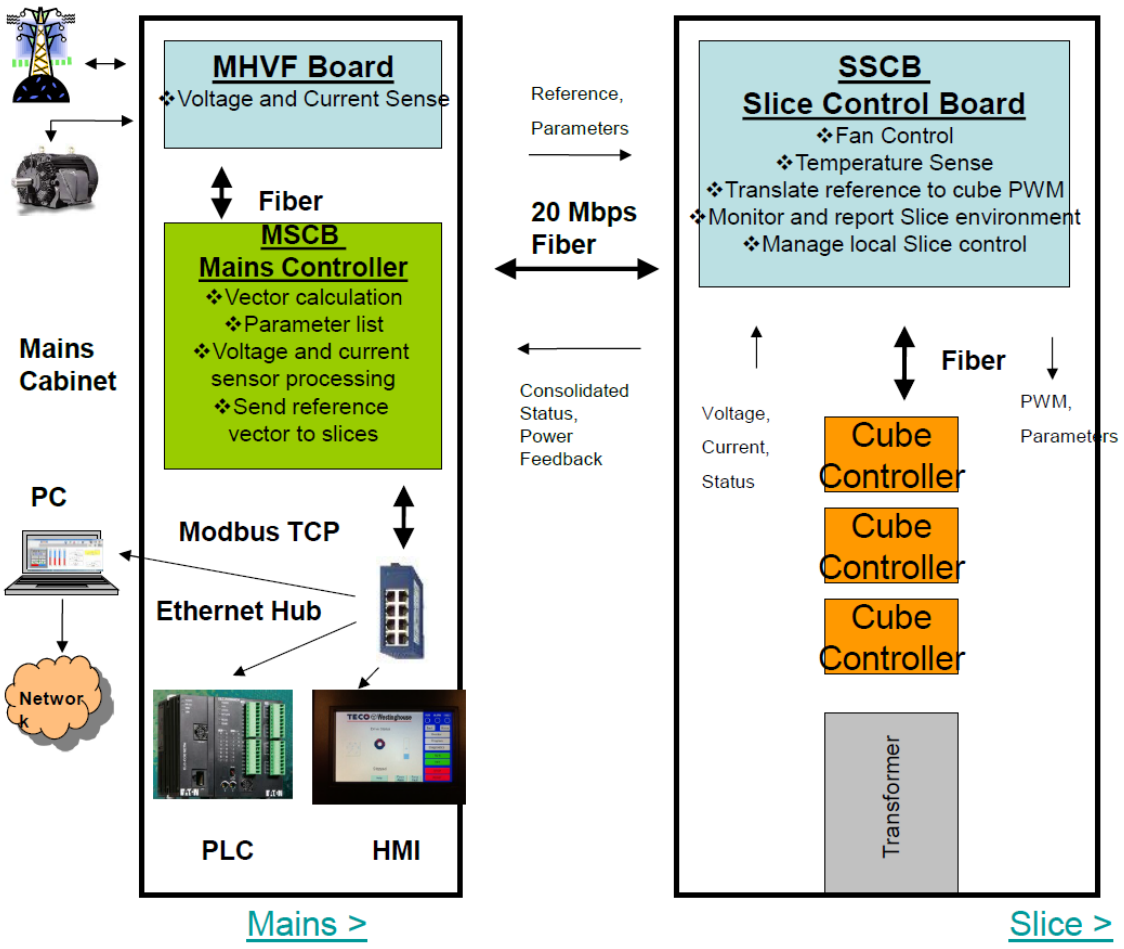


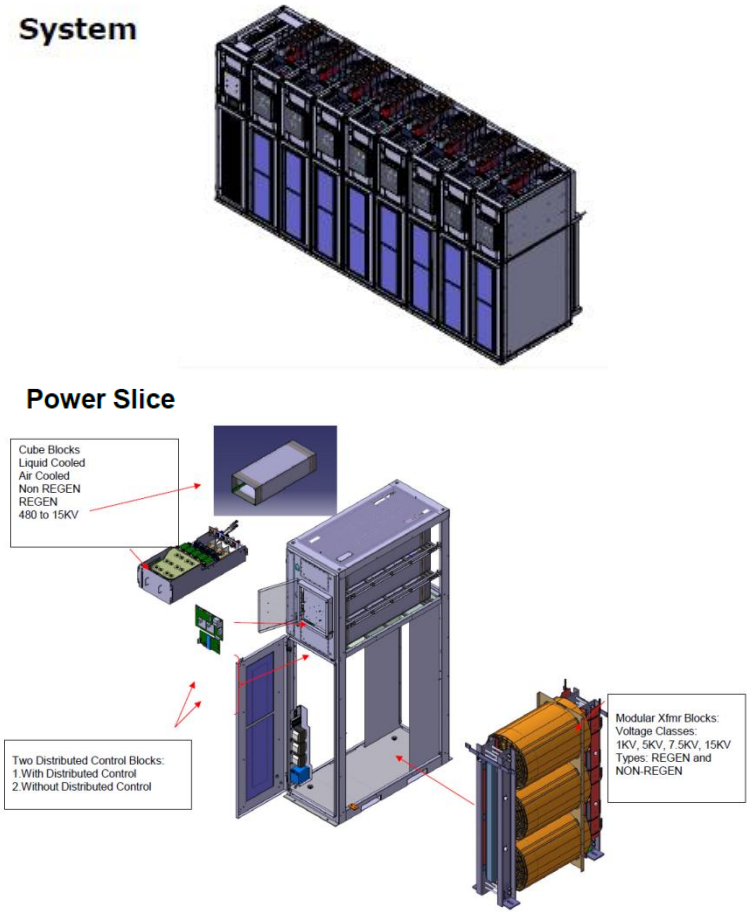
Slice



69 NI sbRIO-9606's

Cyber-Physical System:
Modular Blocks Combine to Make Larger Control System



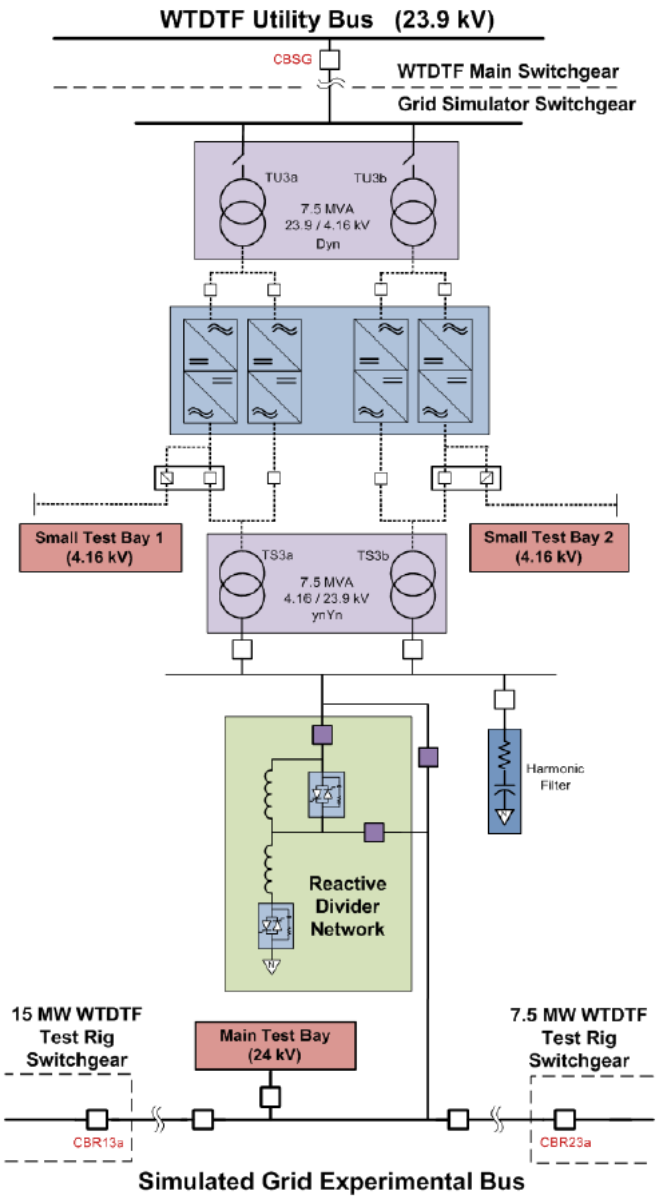


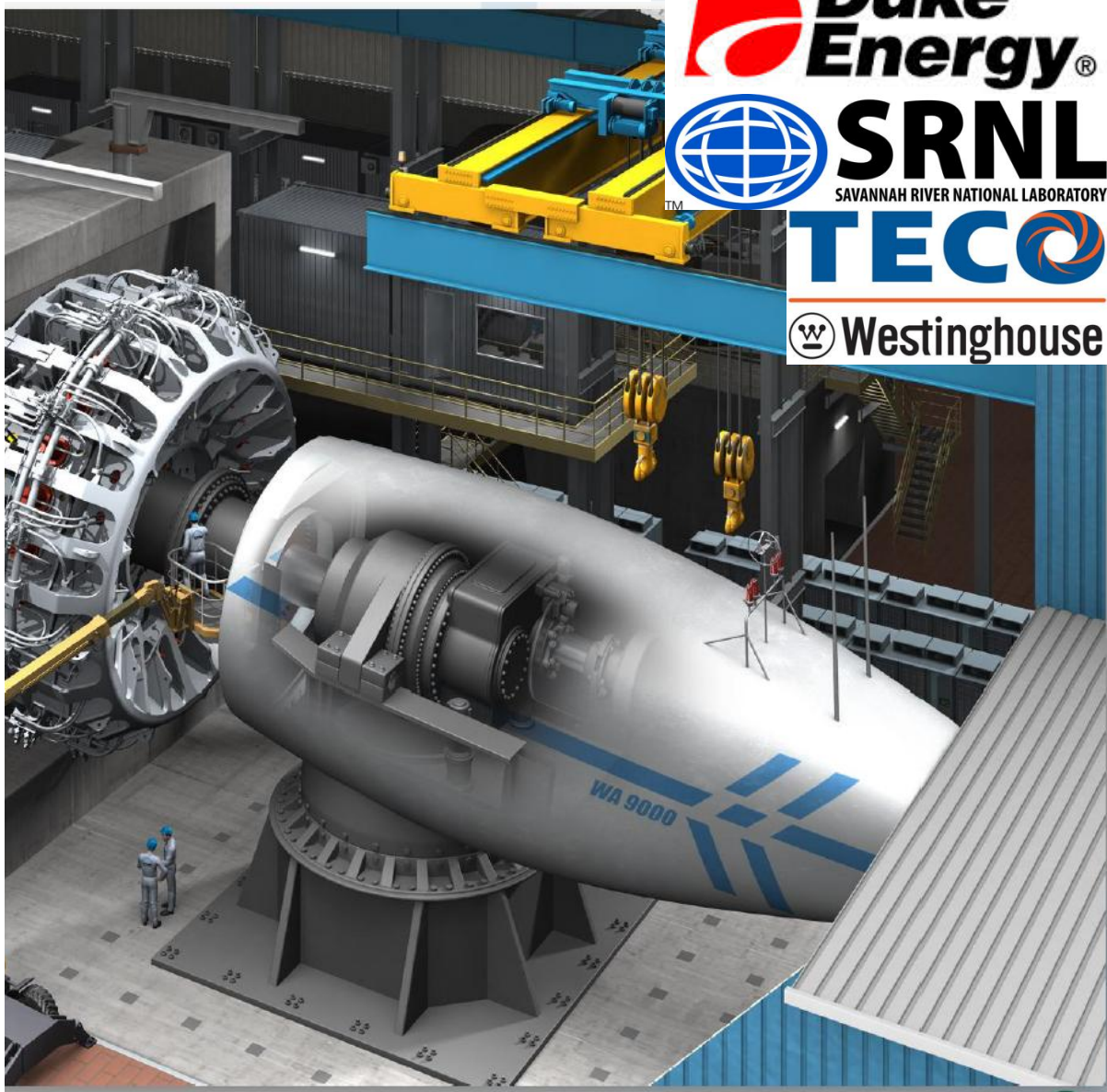
Key Enabler: FPGA-to-FPGA isochronous communication & time synchronization

TECO Westinghouse

15 MW 15 MW Duke Energy eGRID Simulator

Facility Single Line Diagram





CLEMSON UNIVERSITY

Duke Energy®

SRNL
SAVANNAH RIVER NATIONAL LABORATORY

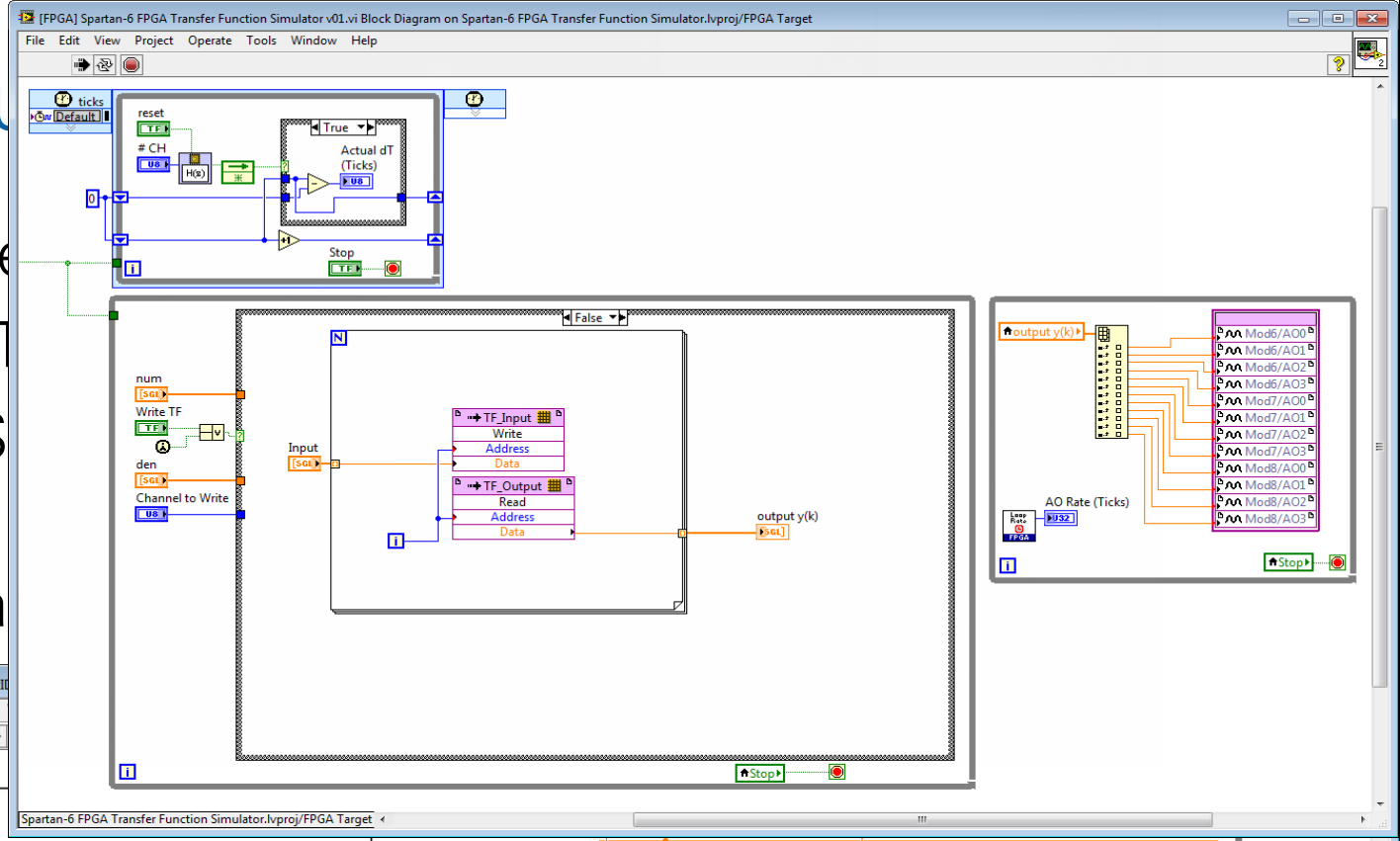
TECO

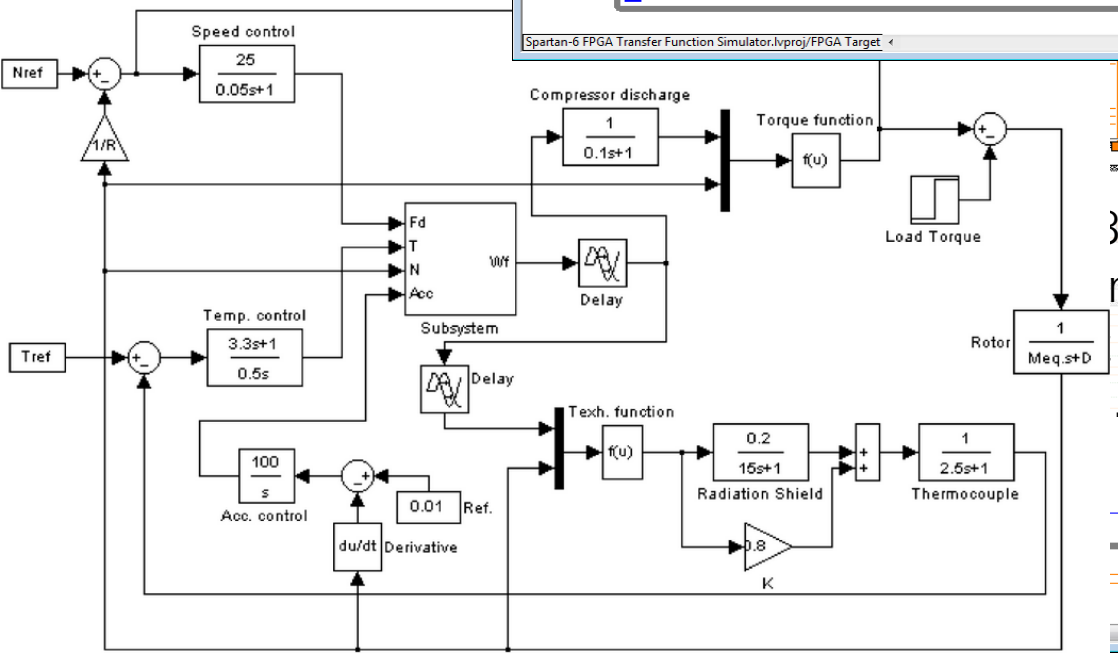
Westinghouse

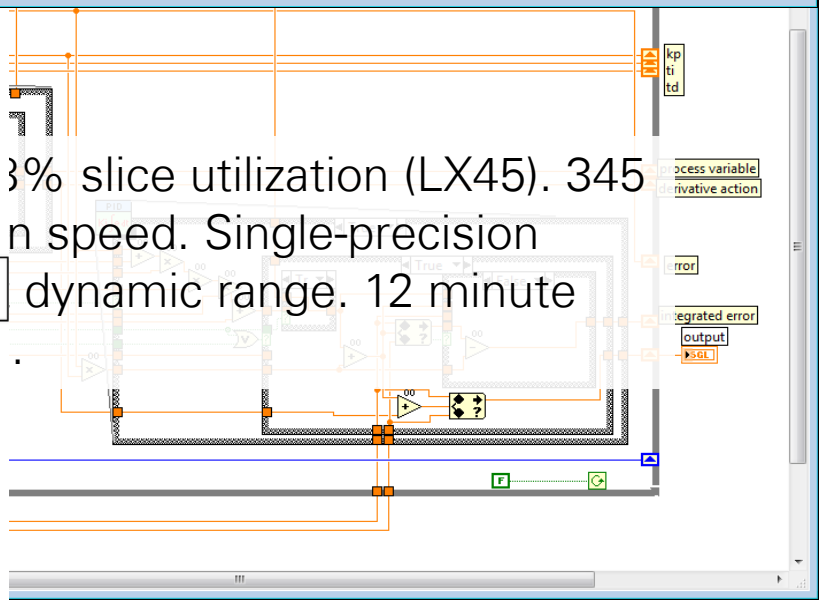
Latest Releases

New Resou

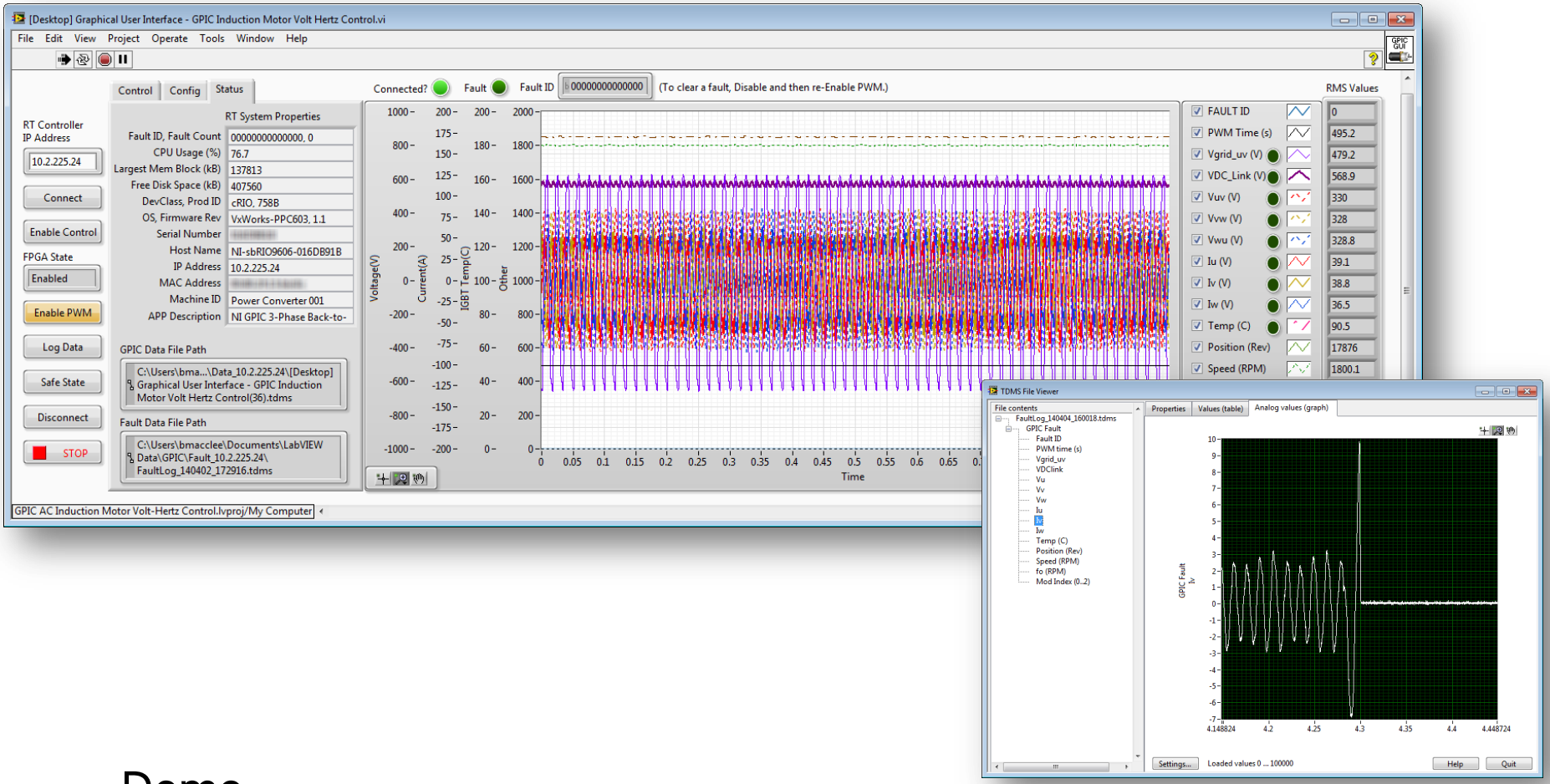
1. NI GPIC Re
2. Hands-on T
3. Updated S
   PCB
4. FPGA Floa
5. Transfe





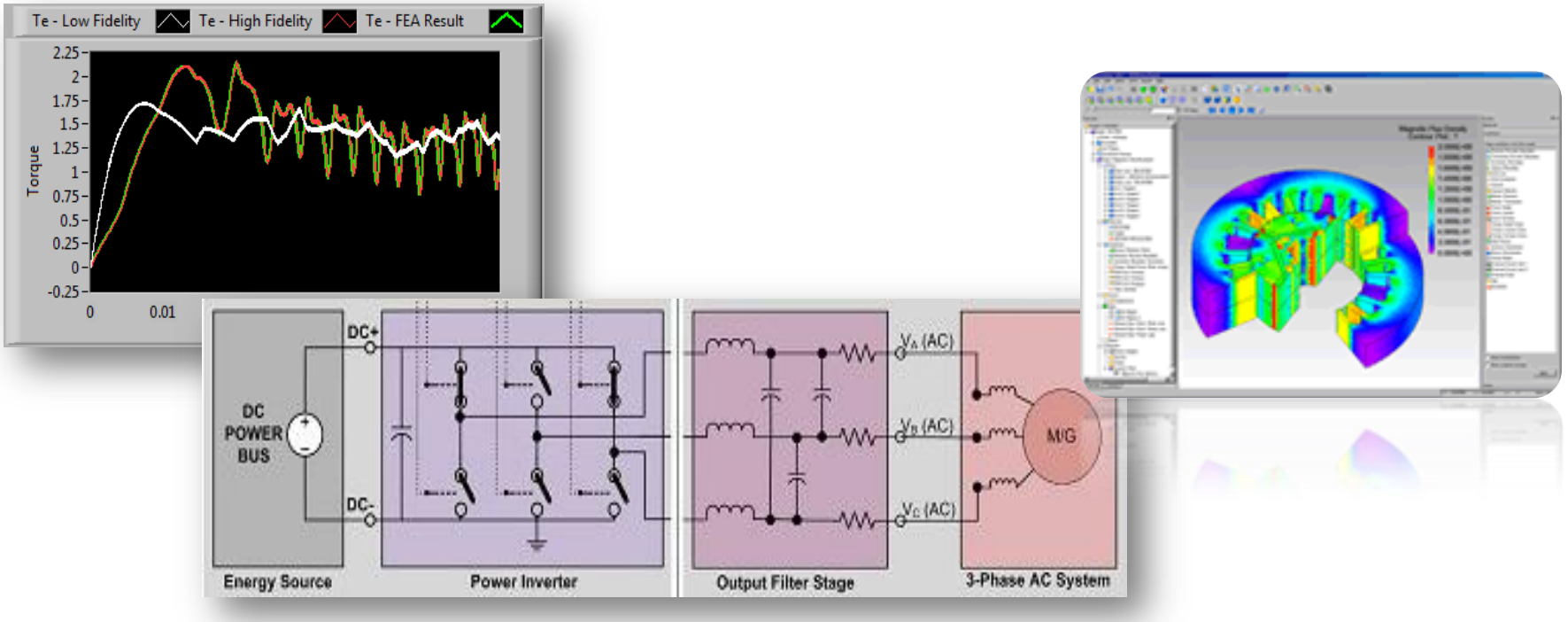


3% slice utilization (LX45). 345
n speed. Single-precision
dynamic range. 12 minute



Demo

GPIC REFERENCE DESIGN



NATIONAL INSTRUMENTS

NEW ULTRA-FAST, FPGA-BASED, FLOATING-POINT TOOLS FOR REAL-TIME POWER SYSTEM SIMULATION AND ADVANCED CONTROL

Key Enablers

3. A new palette of floating point IP cores for LabVIEW FPGA available with resource optimized (control oriented) and speed optimized (simulation oriented) cores.

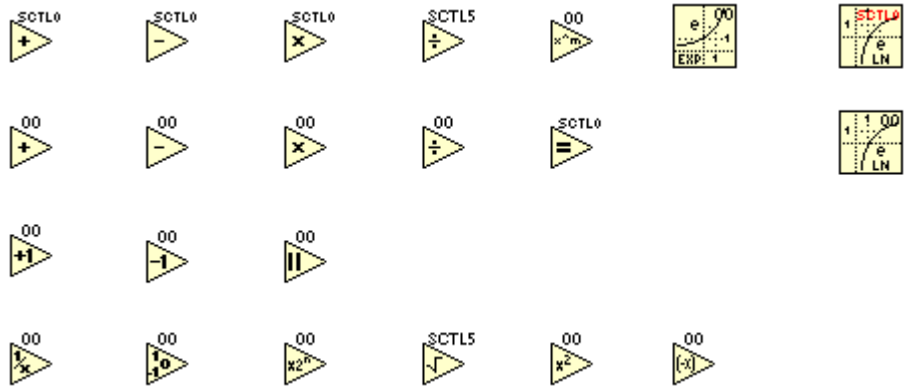
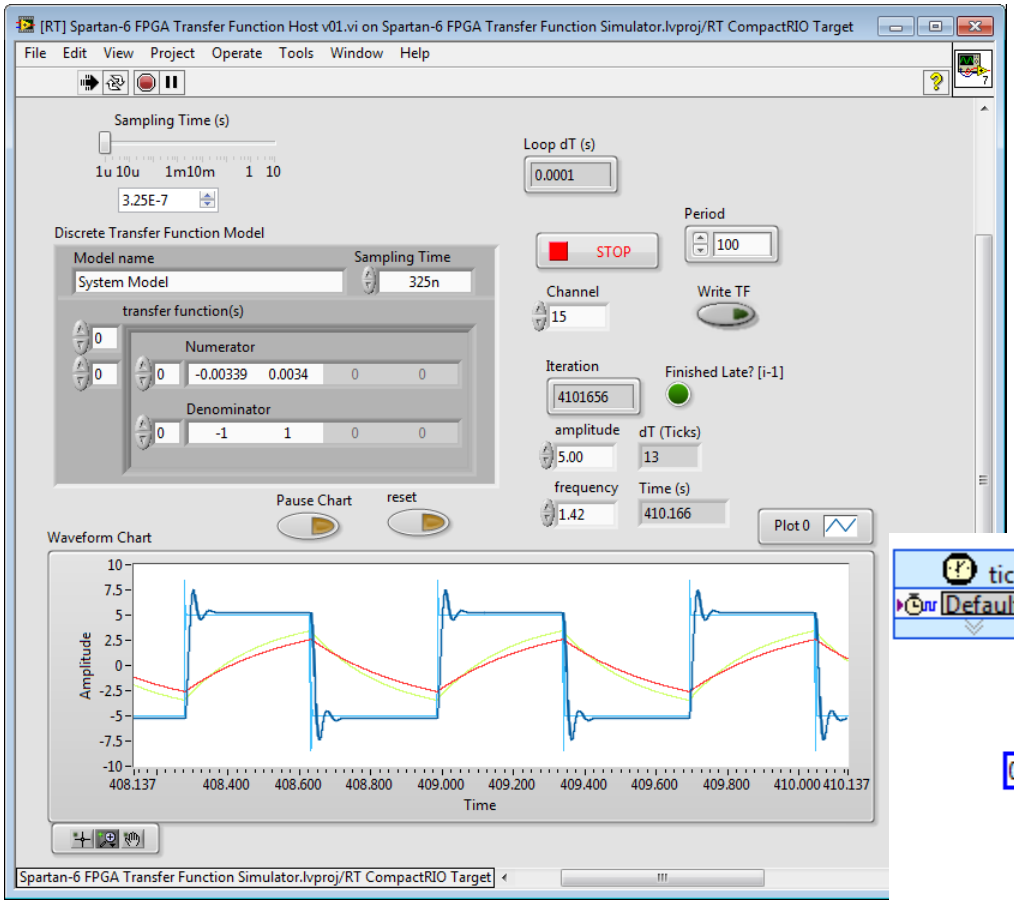
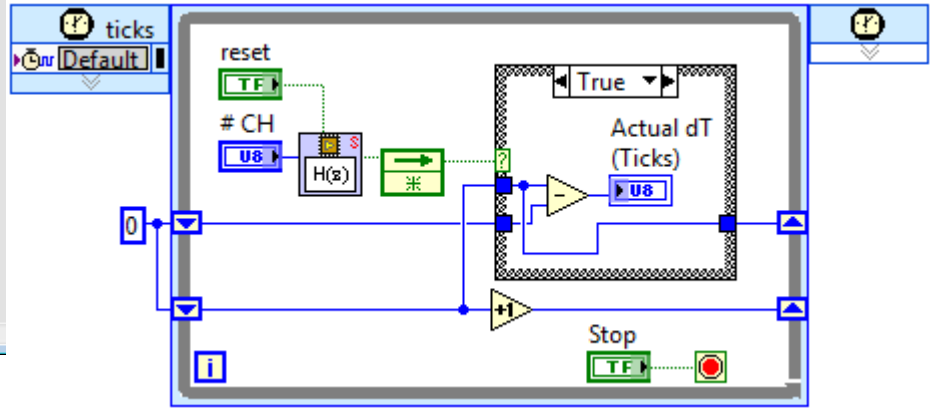


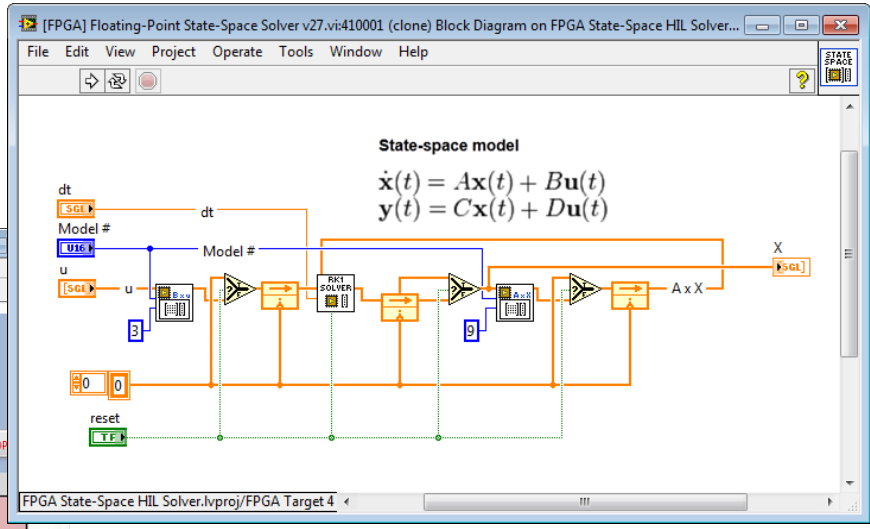
Figure 3. LabVIEW FPGA graphical floating point palette cores include arithmetic and transcendental math functions in resource optimized (ending in 00) and speed optimized (ending in SCTL) versions

Multichannel Transfer Function Solver (6.6 MHz/ch)





Multichannel State-Space Solver (3 MHz/ch)



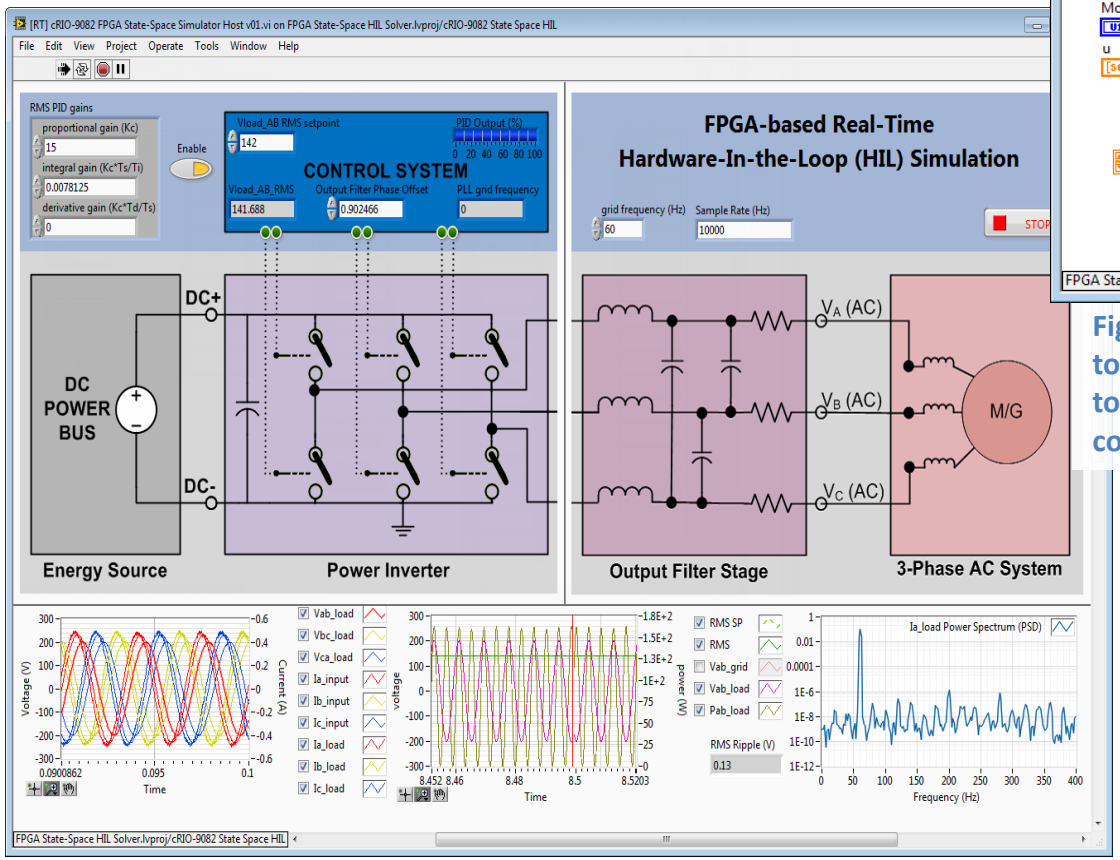


Figure 2. Using open, high level graphical programming tools, advanced algorithms can be automatically compiled to heterogeneous FPGA hardware like this floating point IP core for a 9x9 state space solver which executes at 1.9 MHz

Key Enablers

4. Technology to automatically convert electric circuit, power electronics and power system models to graphical floating point solvers for ultra-high speed heterogeneous FPGA hardware.

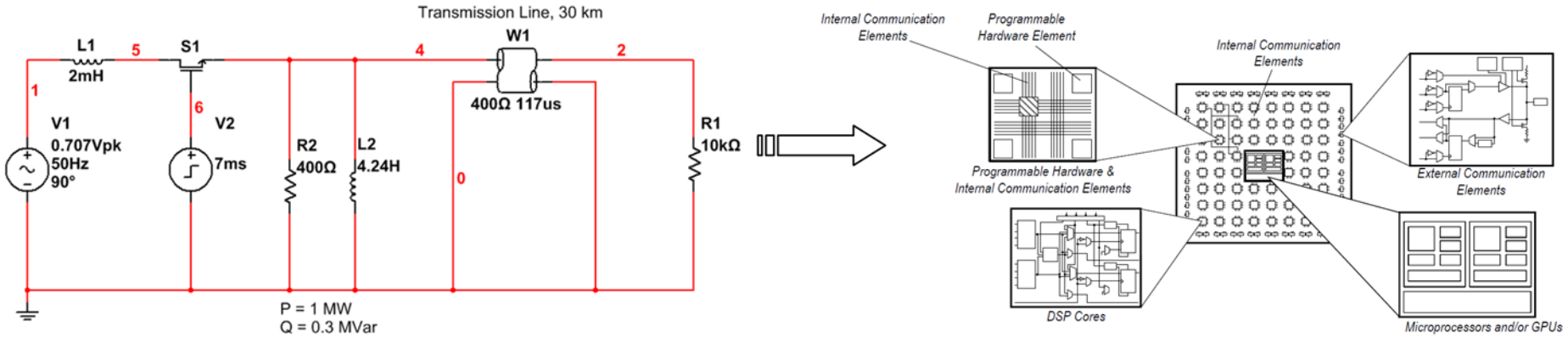


Figure 4. Automatic Multisim to LabVIEW FPGA conversion enables this power system model to be simulated at 2 MHz speeds using heterogeneous FPGA hardware

Key Enablers

5. Technology to automatically convert finite element analysis (FEA) results to high fidelity, ultra-high speed real-time electric motor and inverter drive simulations.

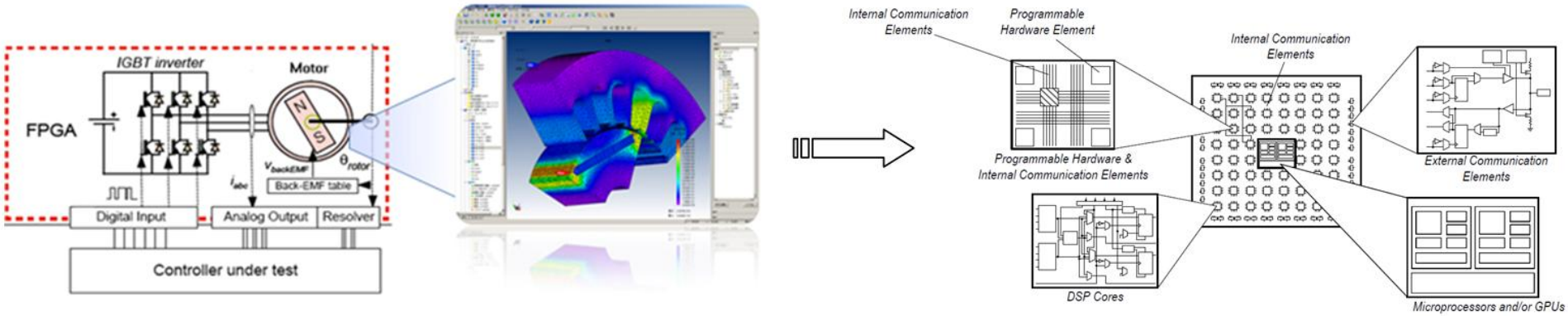
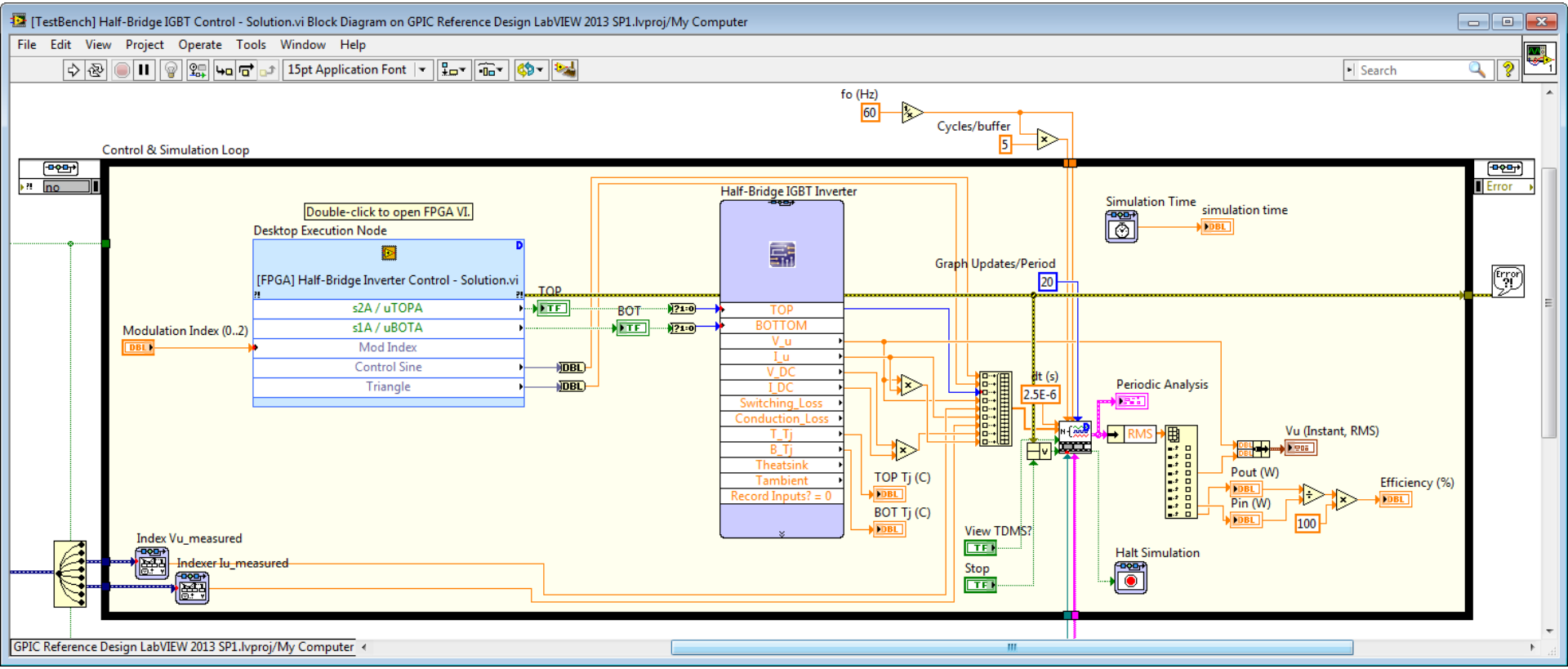


Figure 5. National Instruments has partnered with JSOL Corporation to enable the ability to export JMAG and JMAG-RT FEA models for PMSM and SRM machines to special high-fidelity, high speed solvers for heterogeneous FPGA hardware

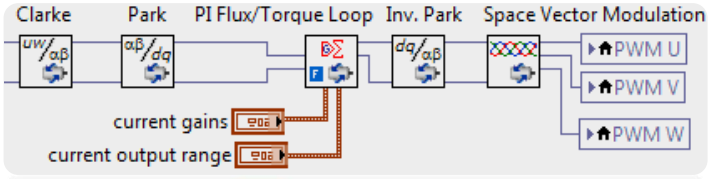
GRAPHICAL CO-SIMULATION WITH NI LABVIEW FPGA & MULTISIM (AUTO-VARIABLE TIMESTEP CO-SIMULATION)

- NATIONAL INSTRUMENTS



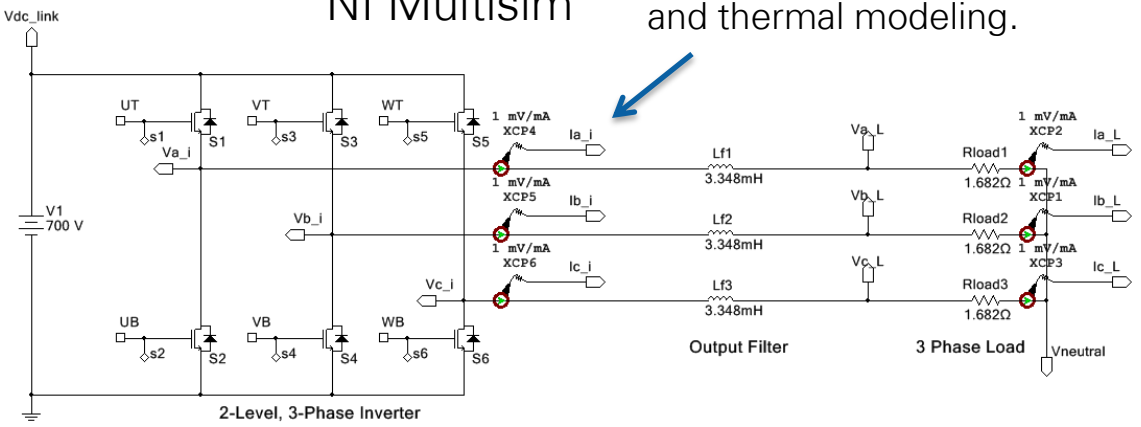
AUTO-VARIABLE TIMESTEP FPGA CO-SIMULATION

NI LabVIEW FPGA



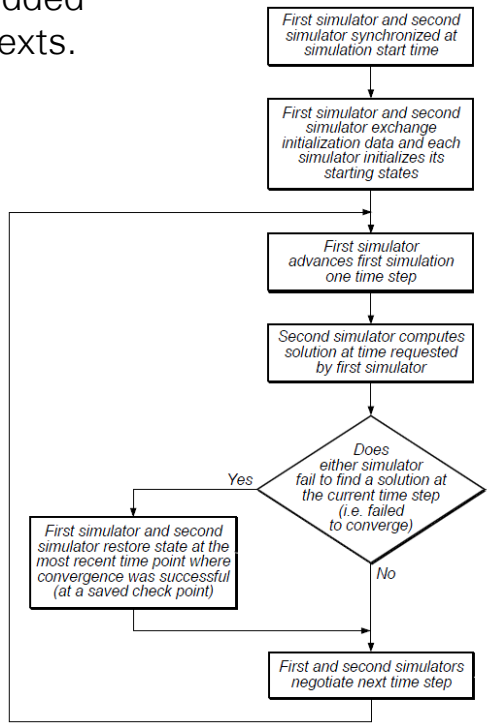
NI Multisim

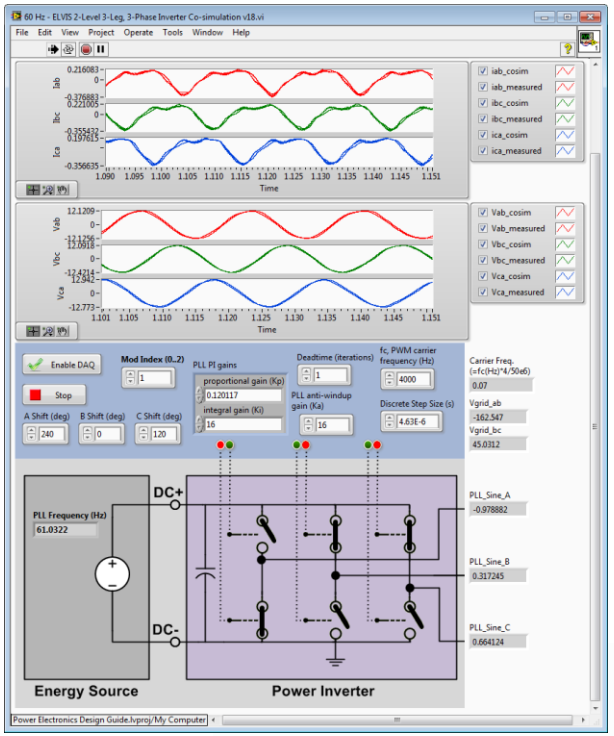
High fidelity switched power, switching/conduction loss and thermal modeling.



Identical behavior and timing of digital embedded software in simulation and deployment contexts.

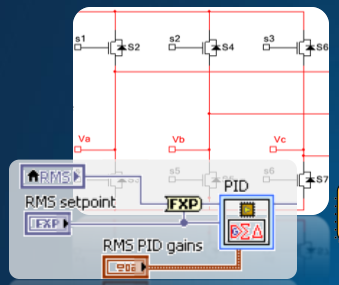
- Auto-variable timestep FPGA co-simulation technology enables accurate simulation of closed loop interaction between the FPGA and switched-mode power system





NATIONAL INSTRUMENTS

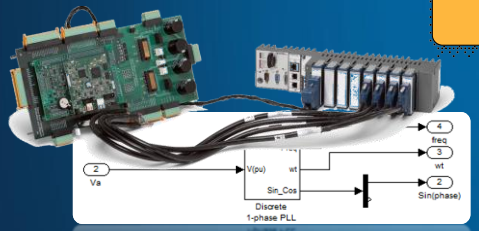
Graphical Co-Simulation (Multisim, LabVIEW FPGA)



Deployed System Management & Remote Monitoring

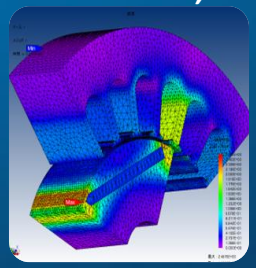
Full Power HIL Simulation

Rapid Control Prototyping (CompactRIO, Veristand)

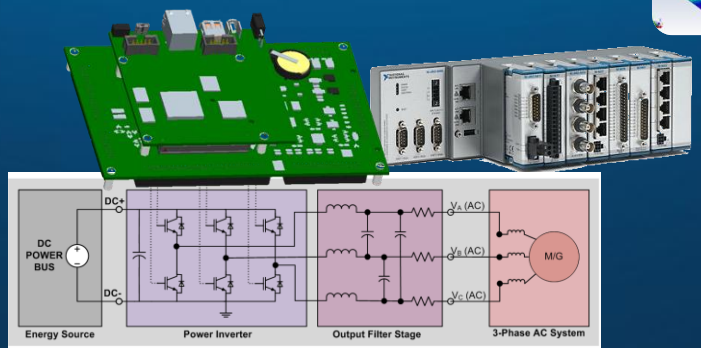


Design
Test Cells
Prototype
HIL Testing
Deploy

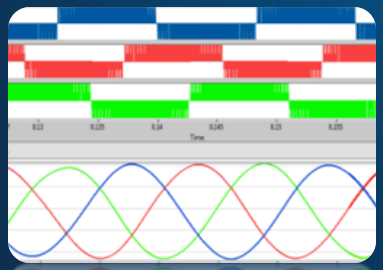
Real-Time HIL Simulation (StarSim, FPGA Motor Sim, FPGA TF/SS Solvers)



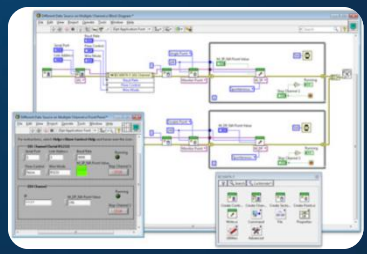
Commercial Deployment (General Purpose Inverter Controller)



Power Measurement Suite (IEC EN 61000, 50160, …)



Utility Networking (IEC-61850, DNP3, …)



Next Steps

Training & Development Assistance

Hardware & Software Pricing

- GPIC Evaluation Kit ($1495)
- GPIC OEM Kits
  - OEM Quantity 1
  - OEM Quantity 20
- Software ($10k-$21k)
  - NI Developer Suite
  - NI LabVIEW Real-Time
  - NI LabVIEW FPGA
  - NI Circuit Design Suite
  - NI Control Design & Simulation
  - NI Power Electronics IP Library (Softmotion)
  - NI Electrical Power Measurement Suite
- Mating Connector Board
  - Free templates available on ni.com/powerdev
  - Free hardware design review with NI R&D
  - Manufacture directly or through PCB house

Training & Development Assistance

- Training Options
  - Self-Paced Online Training (SPOT) – Free
  - Power Electronics Design Guide - Free
  - Regional courses – $3100 per week
    - 1 year training membership $6,210 per person
  - Custom on-site courses - $12,500 per week (multiple people)
- Support
  - Phone & e-mail support - Free
  - Dedicated discussion forum for GPIC questions – Free
  - Periodic conference calls to review progress / open issues - Free
- Development Assistance Options
  - Hardware design review for mating board – Free
  - Work space in Austin next to NI Systems Engineers – Free up to two weeks
  - Remote or on-site development assistance
    - Systems Engineer: $6000-$9200 per week
    - Travel: $500 airfare + $250/day per diem ($1750 per week)
- Alliance Partner Network
  - Provide a turnkey solution
  - Options for taking ownership of code

Training & Jump-Start Assistance Plan

- Self-Paced Online Training (SPOT)
  - LabVIEW Core 1 (3 days), Core 2 (2 days), Multisim (2 days)
  - Time Commitment: 1-2 weeks
  - Cost: Free
- Customized on-site course
  - LabVIEW Real-Time (2 days), LabVIEW FPGA (3 days), Power Electronics Design Guide
  - Time Commitment: 1 week
  - Cost: $12,500 (max)
- Development Assistance
  - On-site development assistance
    - Time Commitment: One week with Senior Systems Engineer
    - Cost: $9200 + $1750 (travel) =$10,950
  - Remote development assistance
    - Time Commitment: One week with Senior Systems Engineer
    - Cost: $9200
  - Work space in Austin next to NI Systems Engineers
    - Time Commitment: 1-2 weeks
    - Cost: Free
- Summary
  - Time Commitment
    - 2 weeks for SPOT training
    - 1 week of custom on-site training
    - 2 weeks of development assistance
  - Cost: $32,650

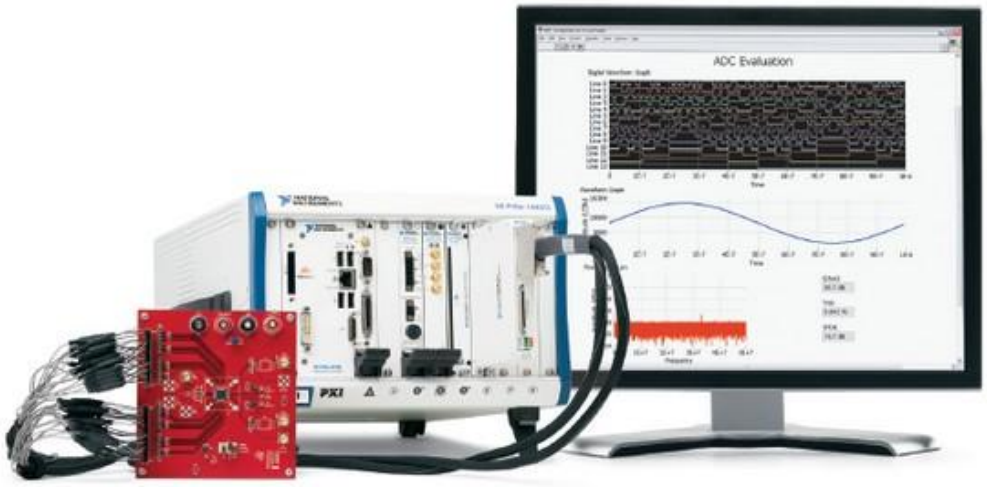
NI LabVIEW for CompactRIO Developer's Guide

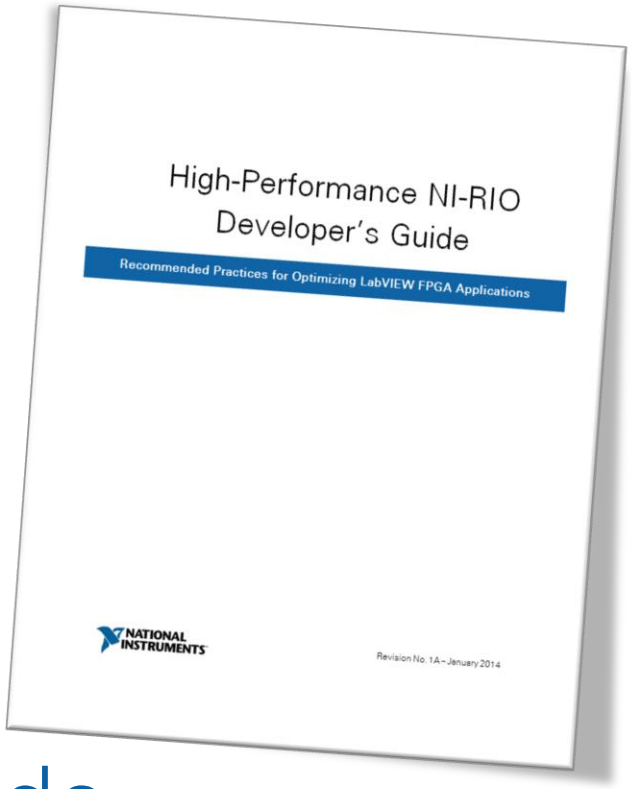
http://www.ni.com/compactriodevguide/

NI LabVIEW High-Performance FPGA Developer's Guide

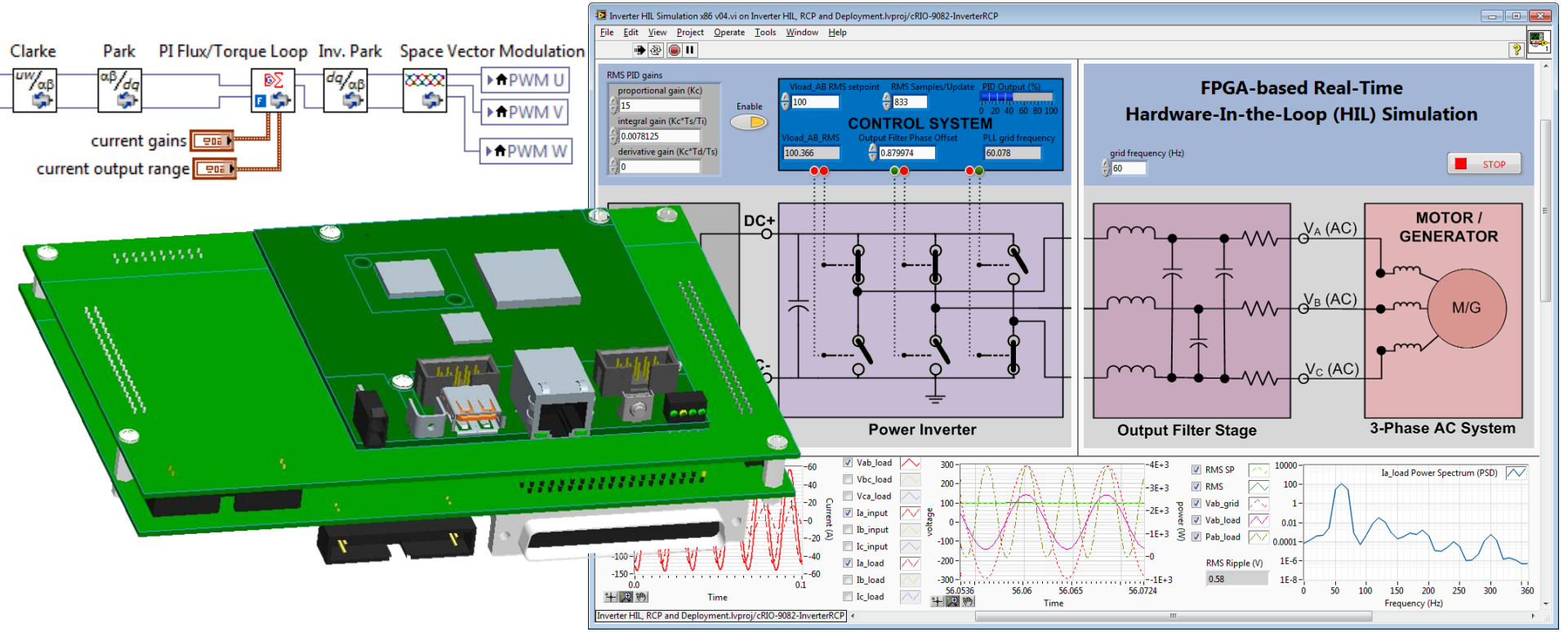
LabVIEW High-Performance FPGA Developer's Guide

- LabVIEW single-cycle Timed Loop programming
- Throughput, latency, and resource optimization techniques
- HDL and third-party IP integration
- Data transfer mechanisms





ni.com/hprioguide



NEXT STEP

JOIN THE DEVELOPER COMMUNITY AT NI.COM/POWERDEV

NATIONAL INSTRUMENTS