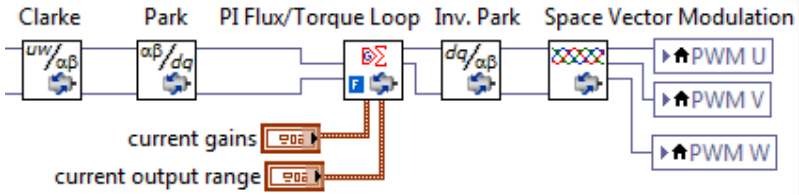
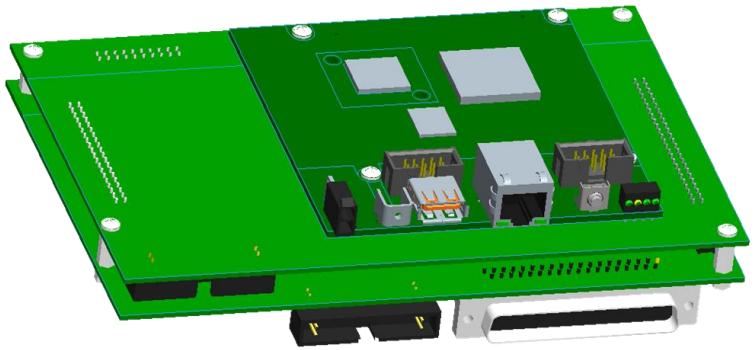
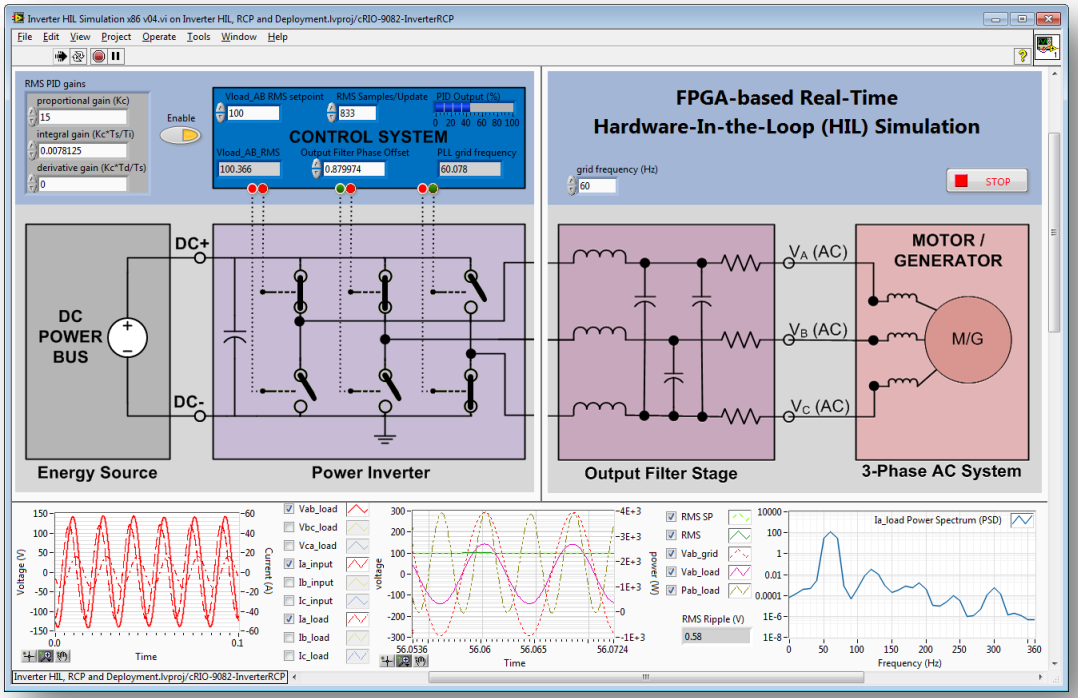
NI Power Electronics Graphical System Design

Control Platform Guide







Brian MacCleery – Principal Product Manager for Clean Energy Technology, National Instruments, Member IEEE

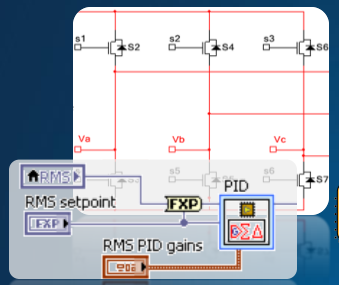
TOPICS

Click to navigate

NI Vision for Power Electronics

Click to navigate

Graphical Co-Simulation
(Multisim, LabVIEW FPGA)



Design

Test Cells

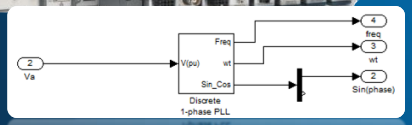
Prototype

HIL Testing

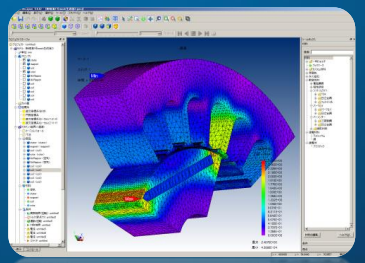
Deploy

Power Electronics Testing
(Bloomy Energy, PXI)

Rapid Control Prototyping
(Multicore CompactRIO, SIT)

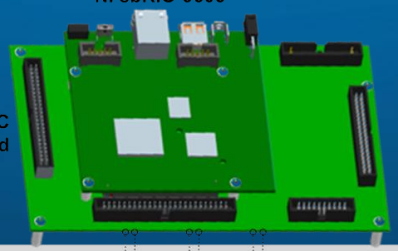


Real-Time HIL Simulation
(JMAG, KGC, SET, FlexRIO, Veristand)

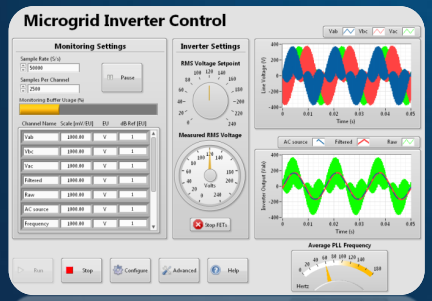


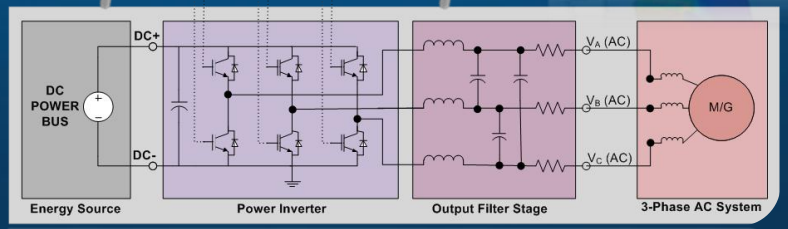
NI sbRIO-9606

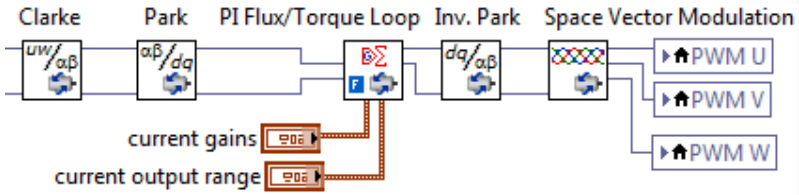
NI GPIC
Mezzanine Card

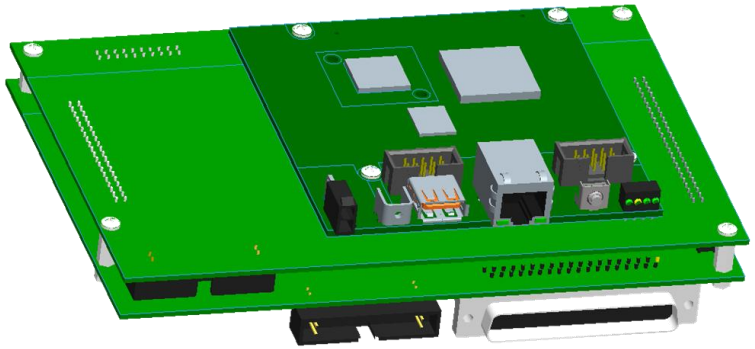


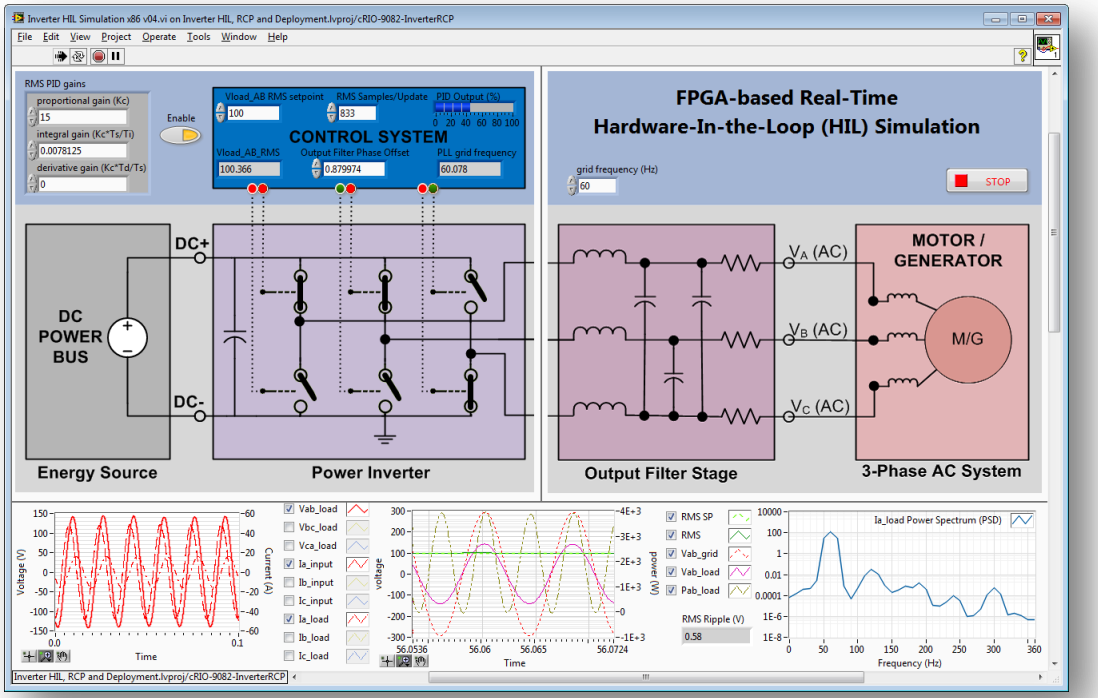
Commercial Deployment
(General Purpose Inverter Controller)







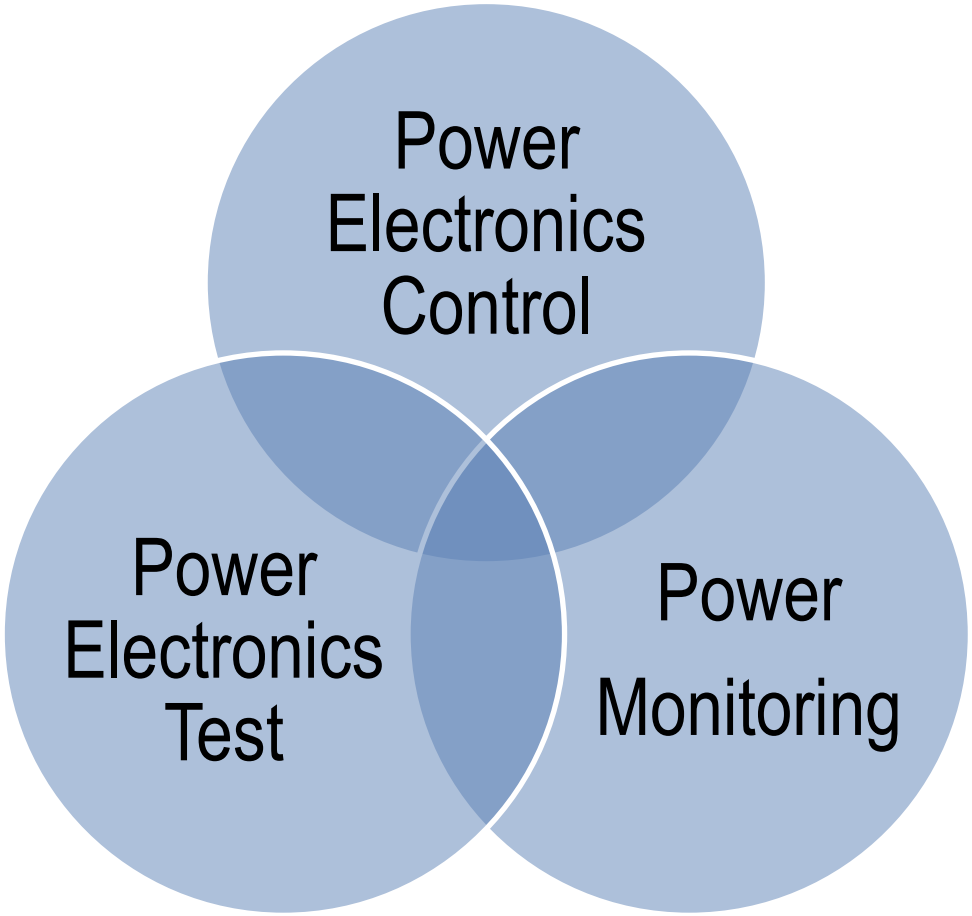




NATIONAL INSTRUMENTS

NI VISION FOR POWER ELECTRONICS

NI Role in Power Electronics



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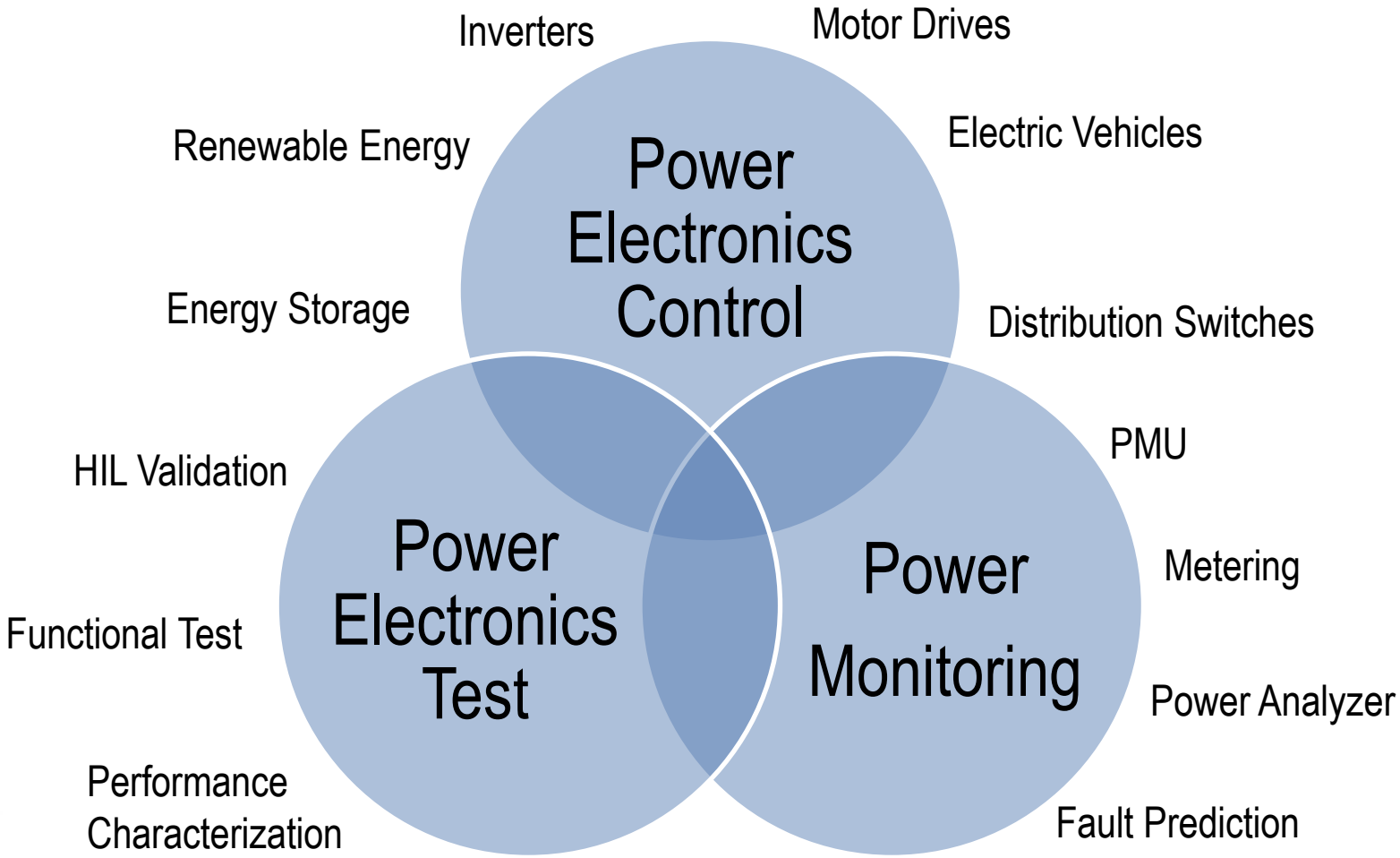
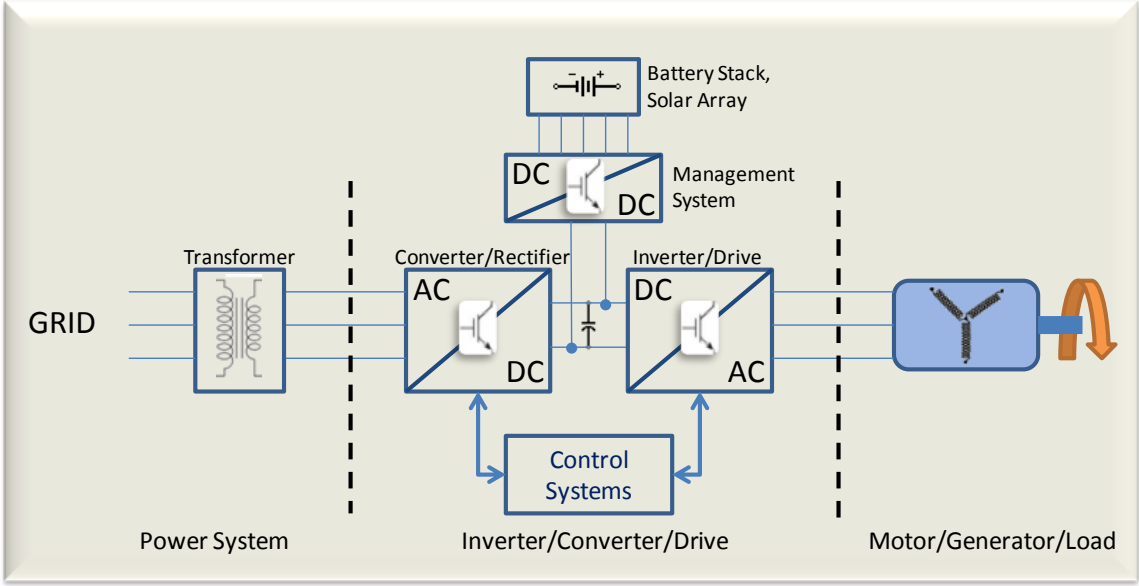
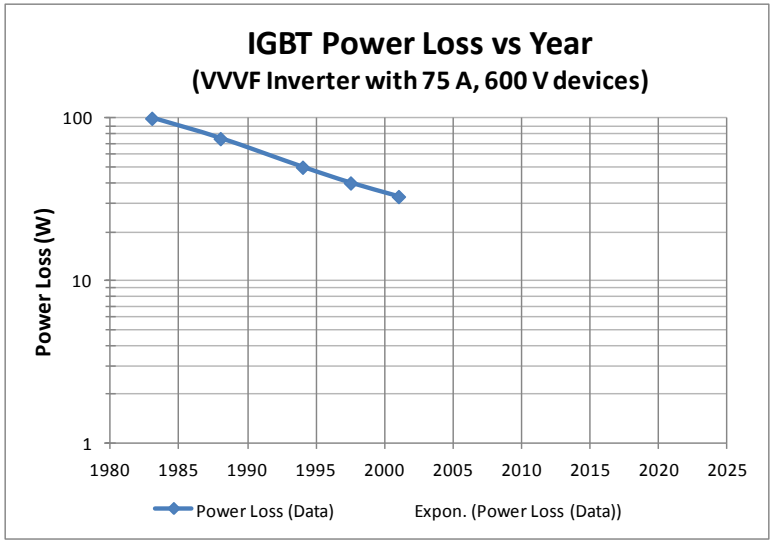


Smart Grid Power Electronics



- Grid tied solar inverters (unidirectional DC>AC inverter)
- Wind turbine power converters (unidirectional AC>DC>AC converter)
- Utility scale energy storage systems (bidirectional AC-DC-AC converter)
- Electric and hybrid electric vehicles, automobiles, trains, agricultural equipment (bidirectional DC-AC converter)
- Industrial medium voltage power supplies (unidirectional DC>DC converter)
- Medium voltage motor drives and pumps (unidirectional or bidirectional AC-DC-AC converter)

The Power Electronics Renaissance



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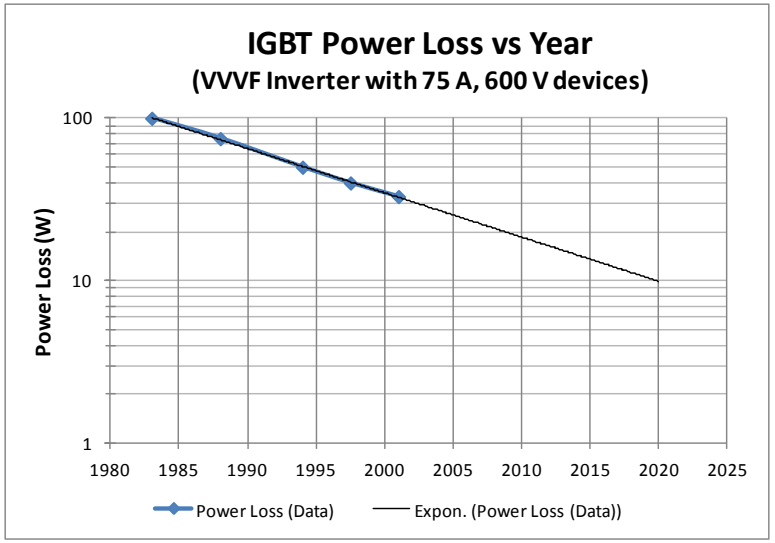

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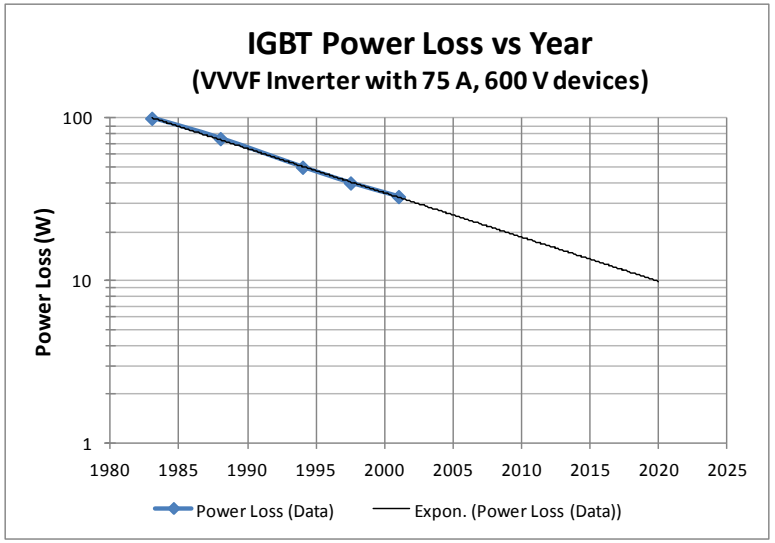
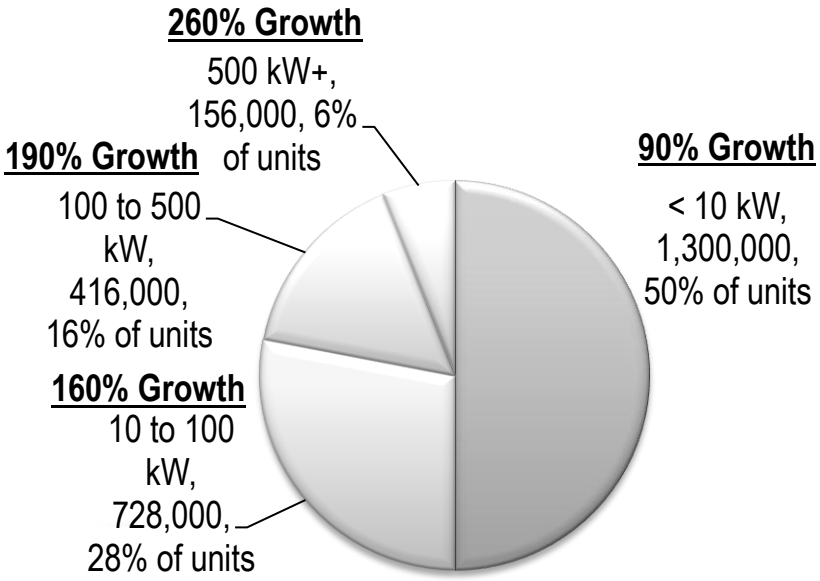
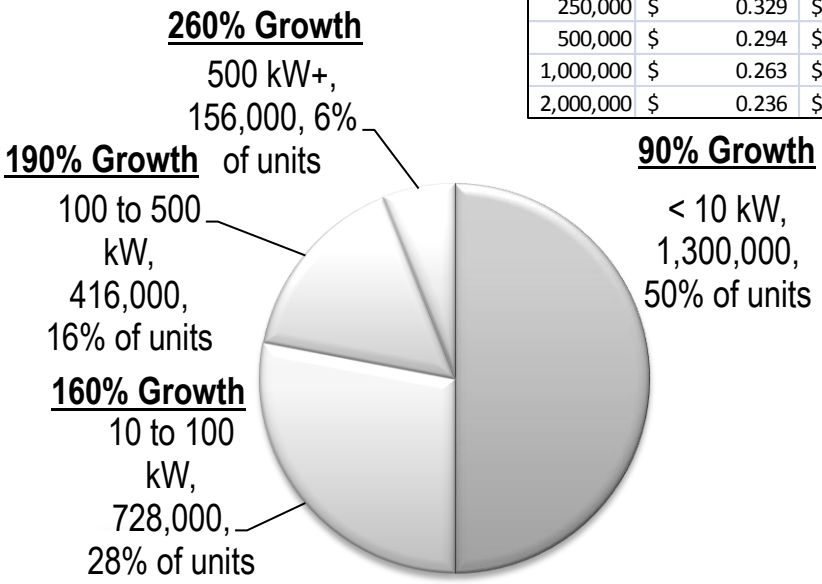




2010 INVERTER UNITS AND GROWTH RATE BY INVERTER SIZE (kW)

The Power Electronics Renaissance

Inverter Size (W)	AVG Retail $/W Continuous	AVG Inverter Retail Price
1	$ 2.400	$ 2.40
150	$ 1.077	$ 161
7,800	$ 0.572	$ 4,462
15,000	$ 0.515	$ 7,729
30,000	$ 0.461	$ 13,835
50,000	$ 0.425	$ 21,249
100,000	$ 0.380	$ 38,037
250,000	$ 0.329	$ 82,126
500,000	$ 0.294	$ 147,010
1,000,000	$ 0.263	$ 263,155
2,000,000	$ 0.236	$ 471,060



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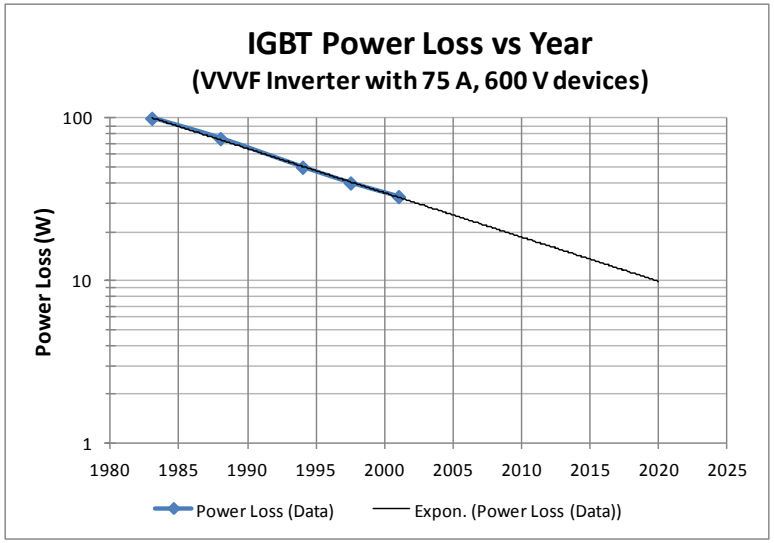

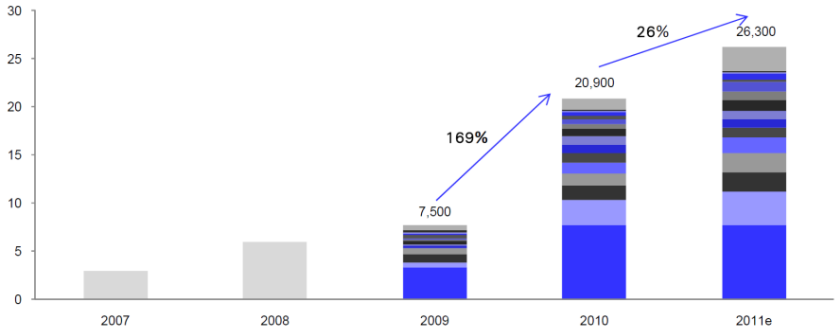

INVERTER SHIPMENTS (MWp)

The Power Electronics Renaissance

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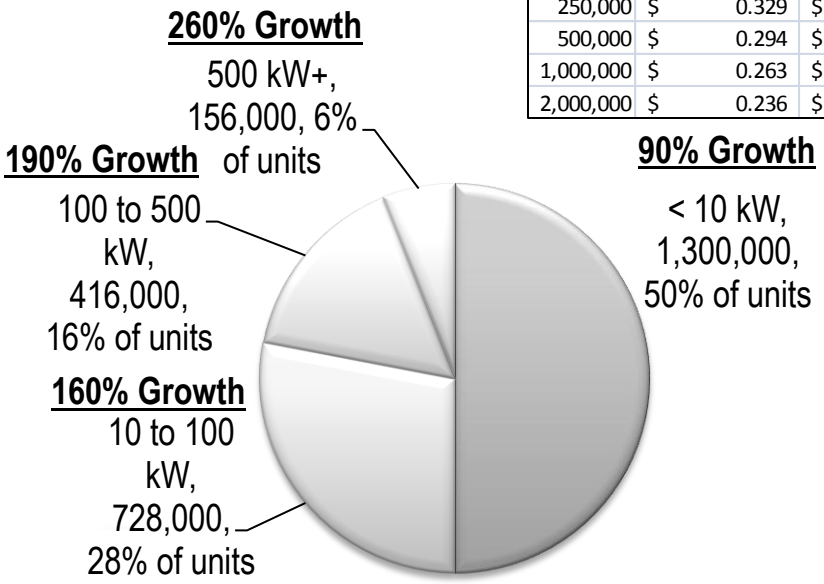

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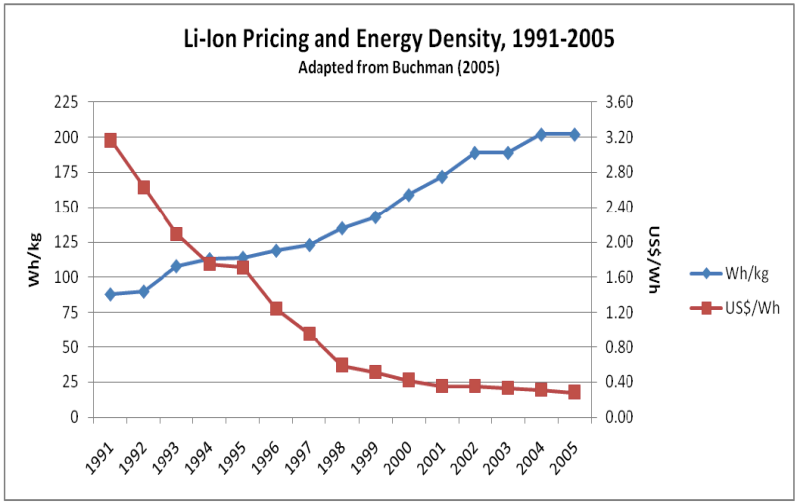
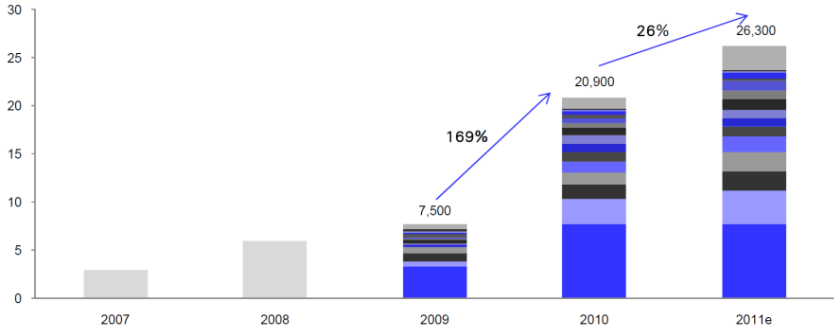


Figure 11: Historical Prices and Specific Energy Trends for Li-Ion Batteries



INVERTER SHIPMENTS (MWp)

The Power Electronics Renaissance

"Since the industrial revolution I do not know of a single financial push towards a solitary focus as large as renewable energy outside of war."- Glenn A. Knierim, Ph.D. of Infinity Physics

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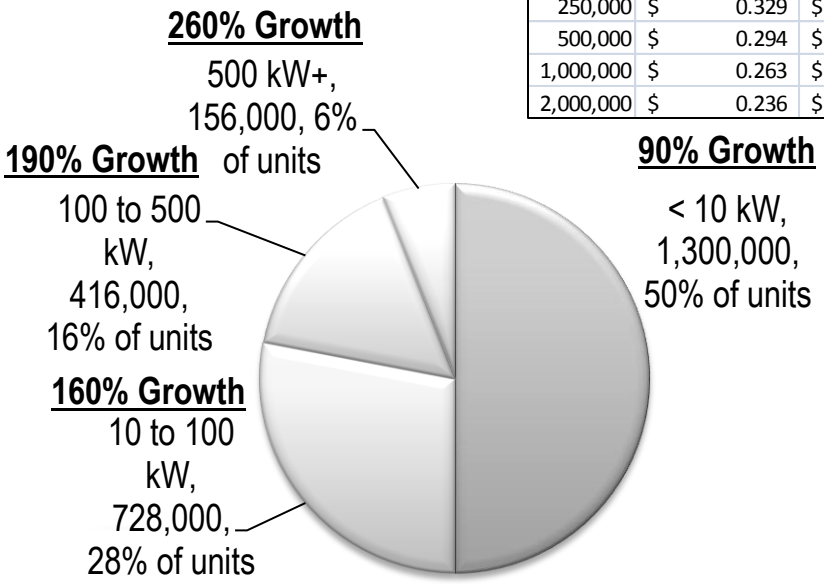

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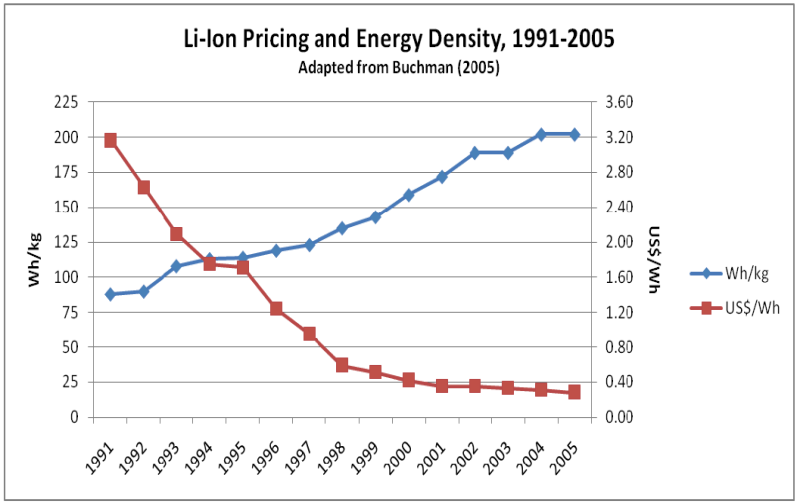

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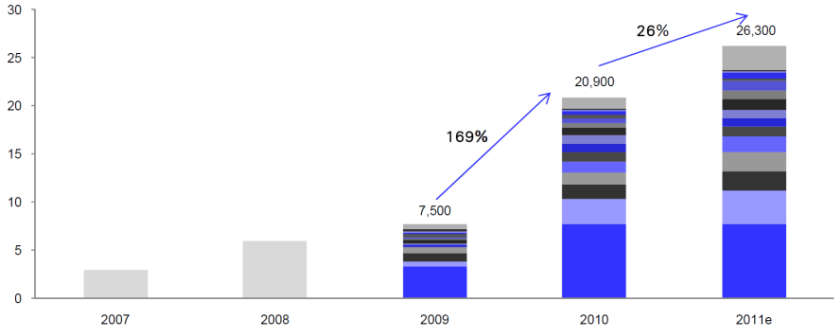

INVERTER SHIPMENTS (MWp)

PE Design Goals & Tradeoffs

- Optimize for multiple design goals simultaneously, including:
  - Energy efficiency
  - Cost
  - Component lifetime
  - Systematic reliability

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  - …

PE Design Goals & Tradeoffs

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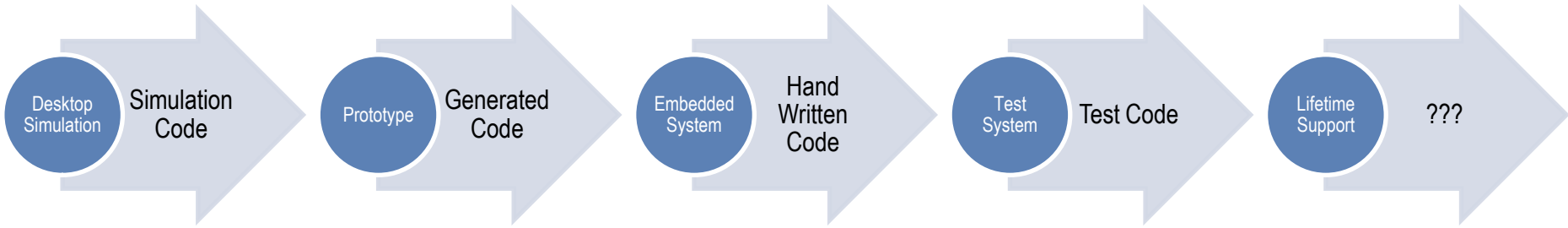
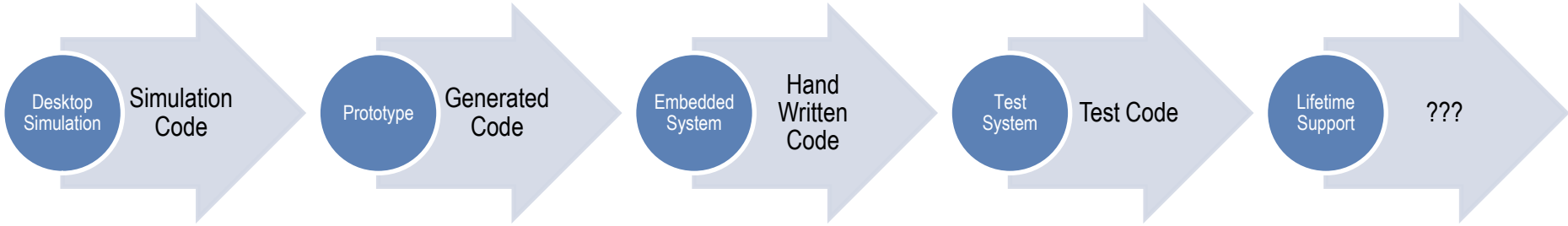
What's the problem?



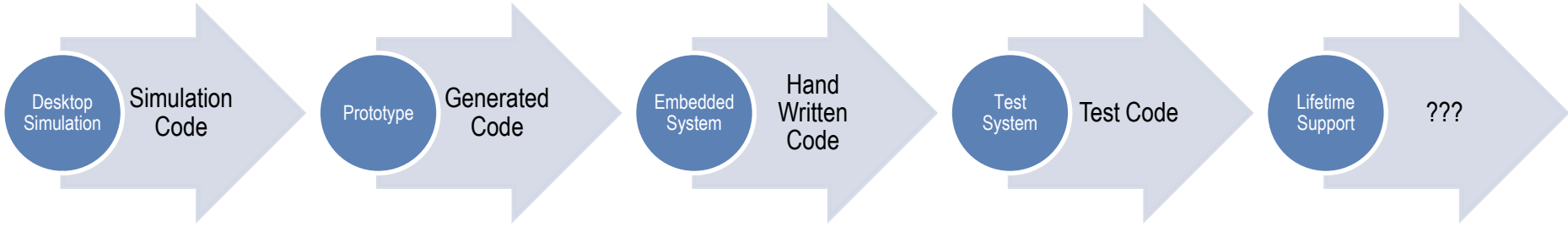
What's the problem?

1. Unidirectional software development path



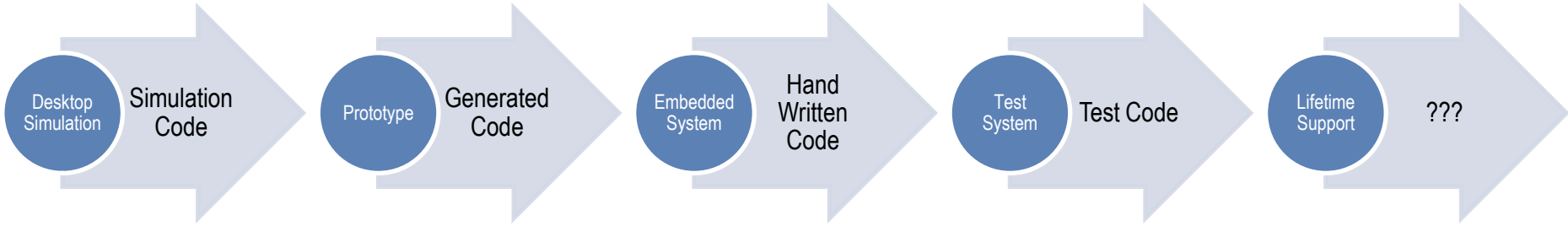
What's the problem?

1. Unidirectional software development path
2. "Dirty code"



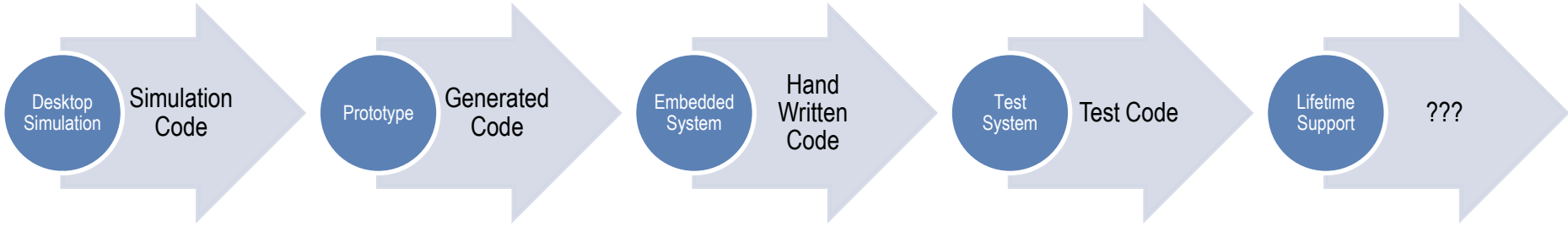
What's the problem?

1. Unidirectional software development path
2. "Dirty code"
3. "Throw it over the wall" engineering

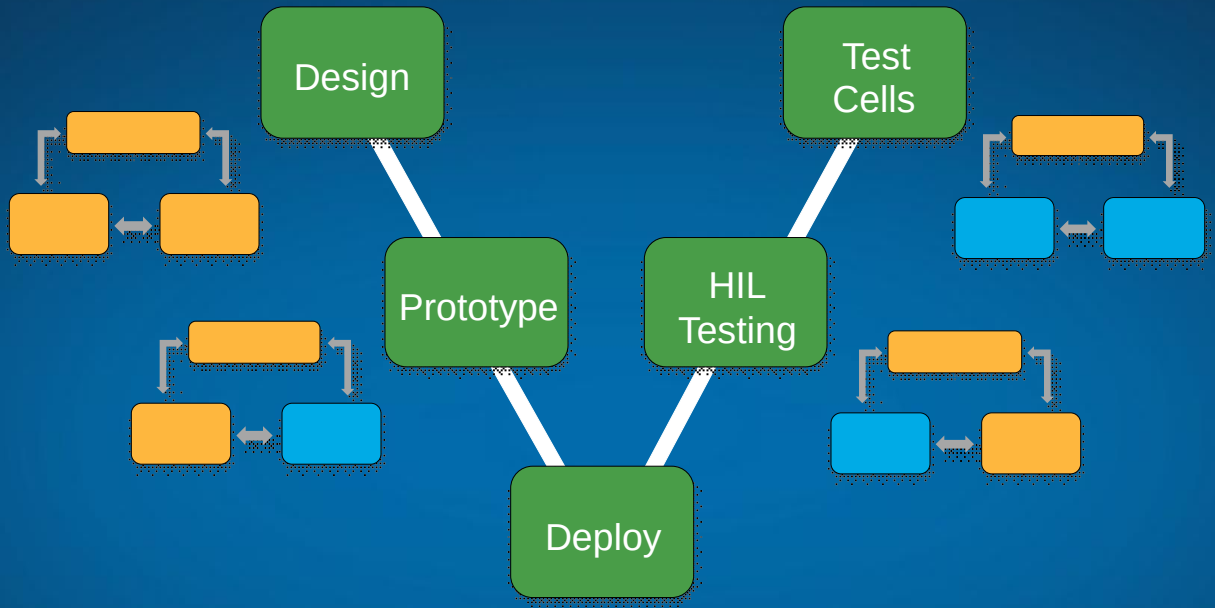


What's the problem?

1. Unidirectional software development path
2. "Dirty code"
3. "Throw it over the wall" engineering
4. Missing real-time test tools



NI Vision for Power Electronics



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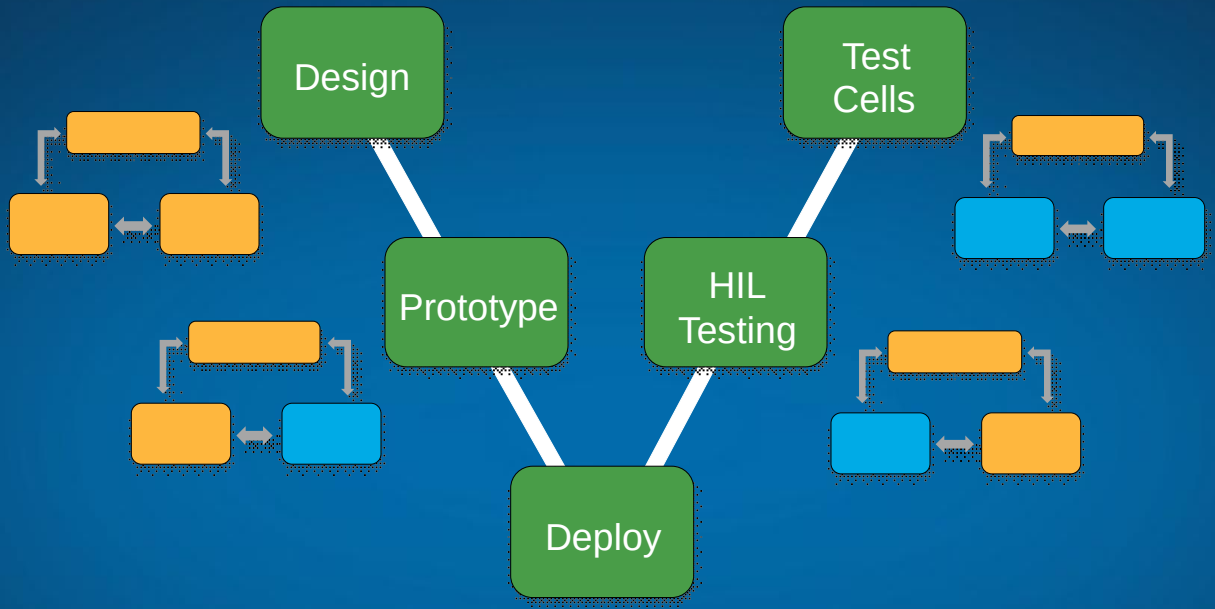
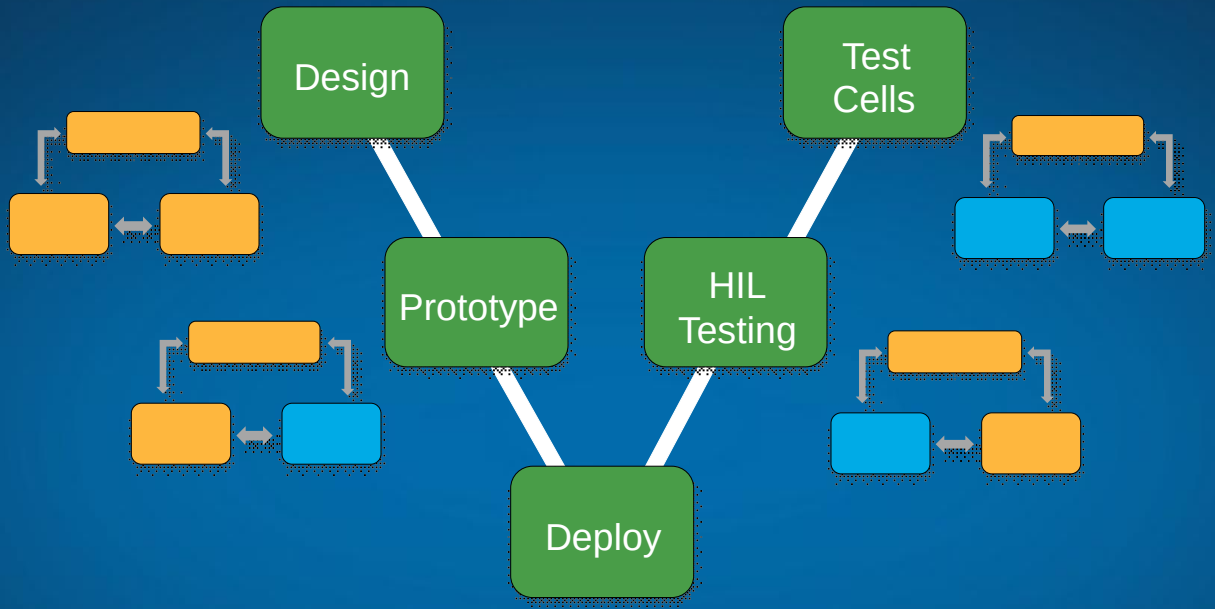


Make energy an information technology

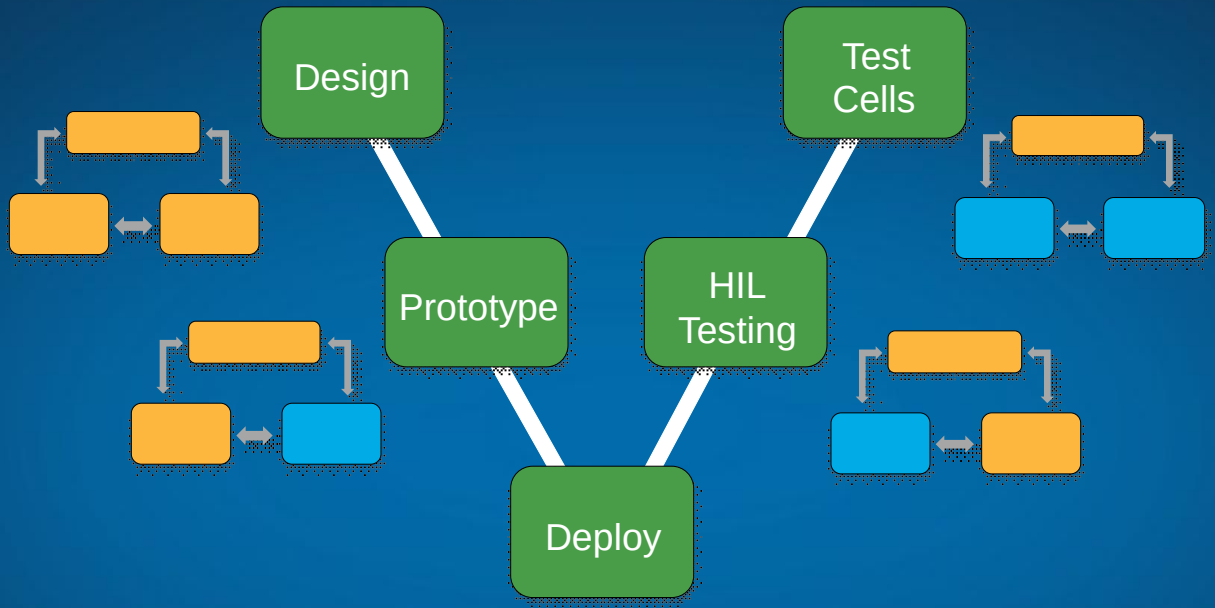
NI Vision for Power Electronics



Make energy an information technology

Enable complete software re-use

NI Vision for Power Electronics

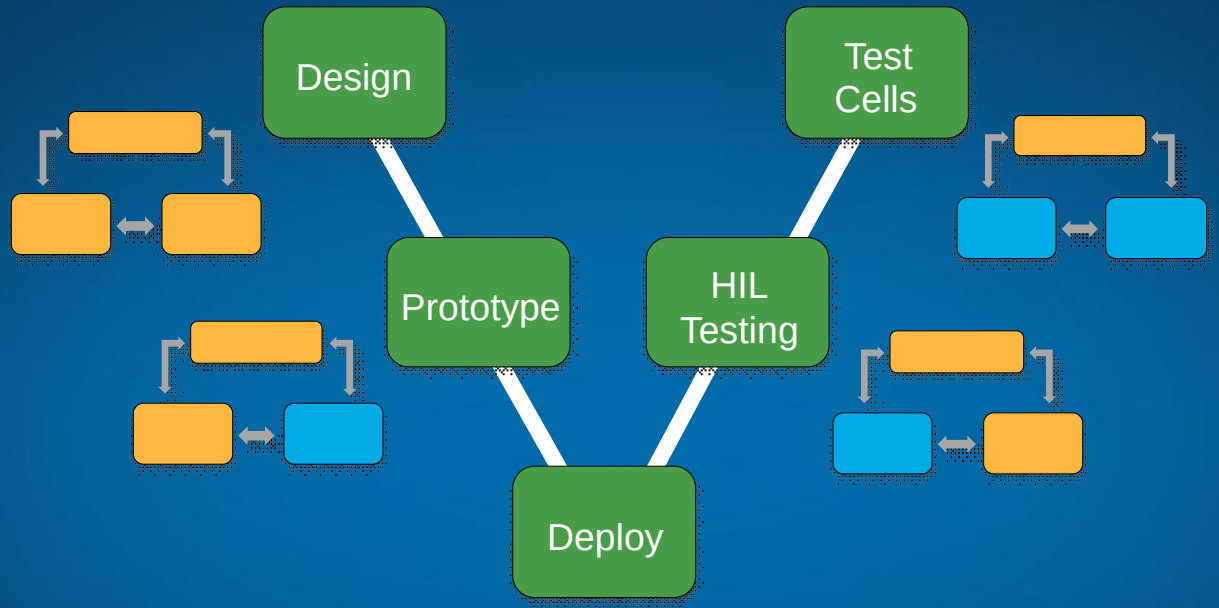


Make energy an information technology

Enable complete software re-use

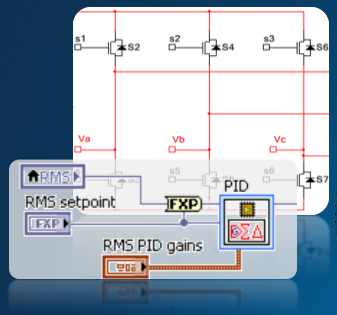
Enable multi-criteria design optimization

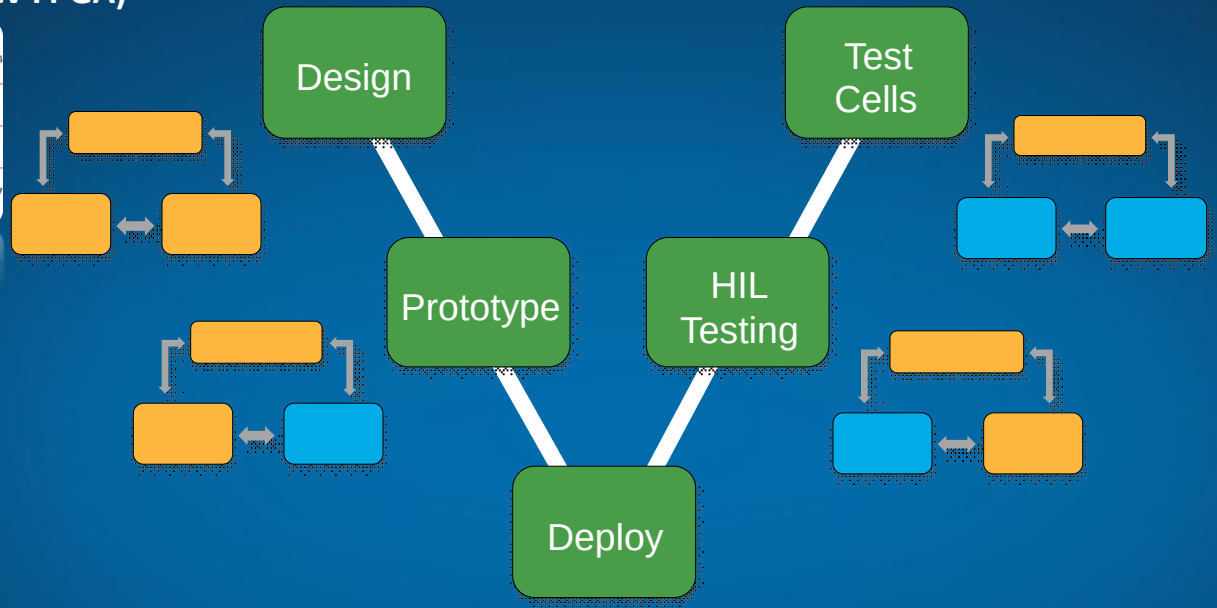
NI Vision for Power Electronics



NI Vision for Power Electronics

Graphical Co-Simulation (Multisim, LabVIEW FPGA)





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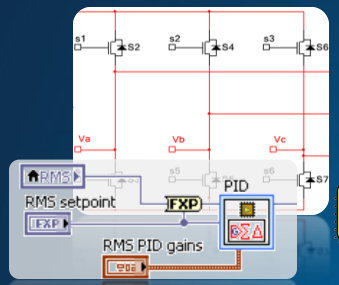
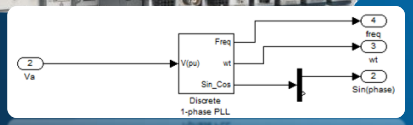
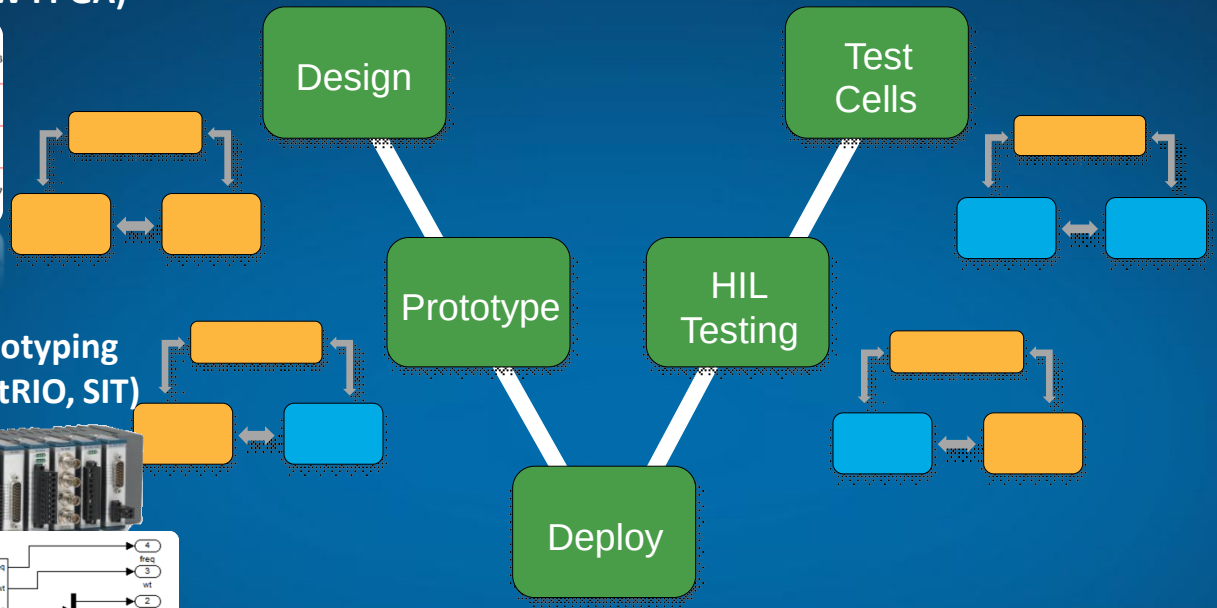


Rapid Control Prototyping (Multicore CompactRIO, SIT)





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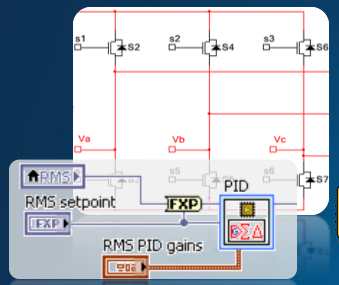

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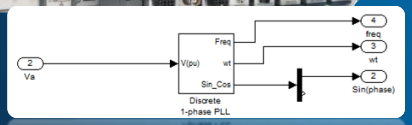

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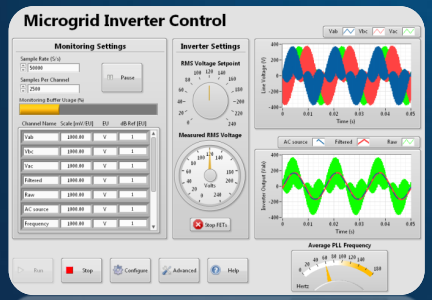
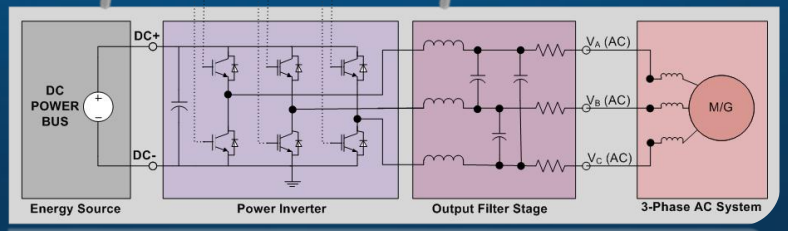


NI sbRIO-9606

NI GPIC Mezzanine Card



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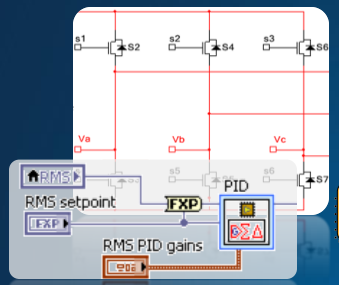

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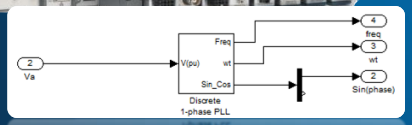
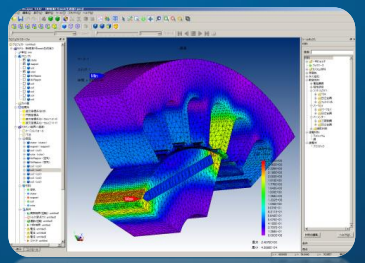
HIL Testing

Deploy

Rapid Control Prototyping
(Multicore CompactRIO, SIT)

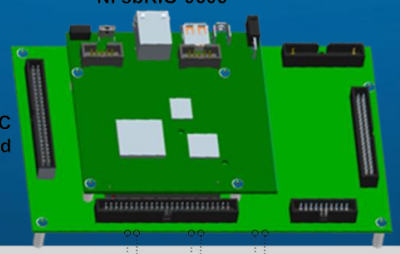


Real-Time HIL Simulation
(JMAG, KGC, SET, FlexRIO, Veristand)

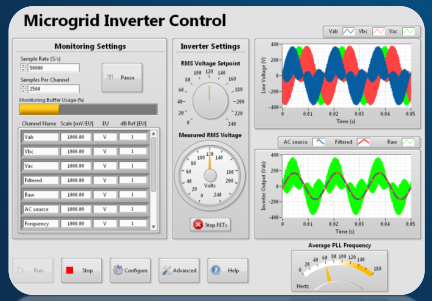


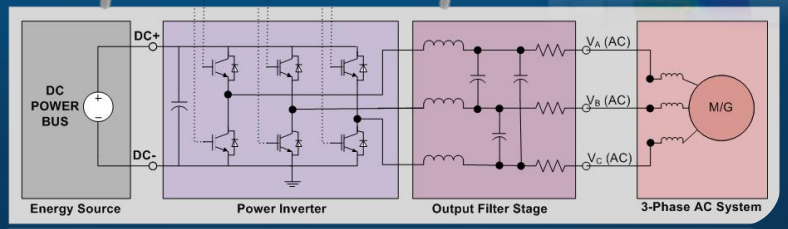
NI sbRIO-9606

NI GPIC
Mezzanine Card



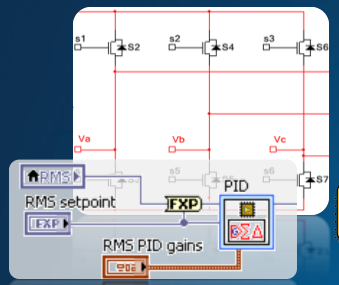
Commercial Deployment
(General Purpose Inverter Controller)





NI Vision for Power Electronics

Graphical Co-Simulation
(Multisim, LabVIEW FPGA)



Design

Test Cells

Prototype

HIL Testing

Deploy

Rapid Control Prototyping
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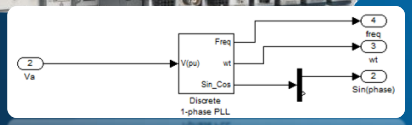

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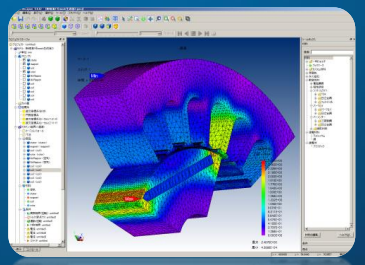

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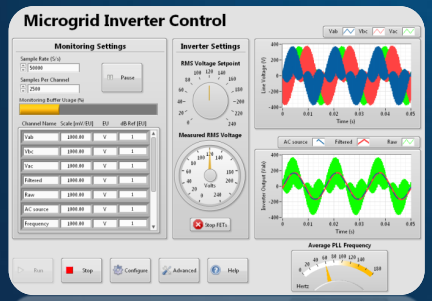

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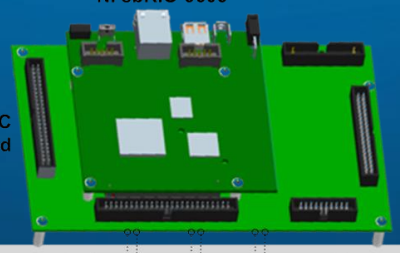

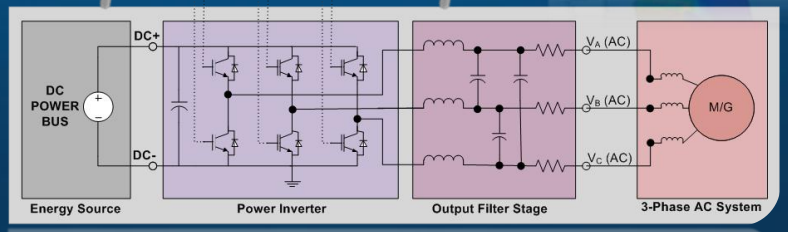

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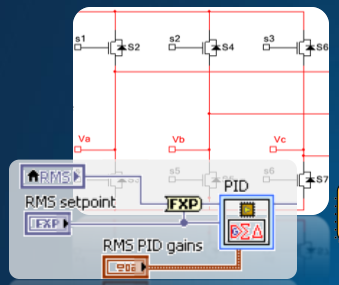

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(Bloomy Energy, PXI)

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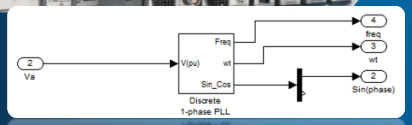

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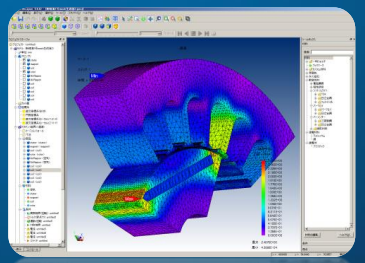

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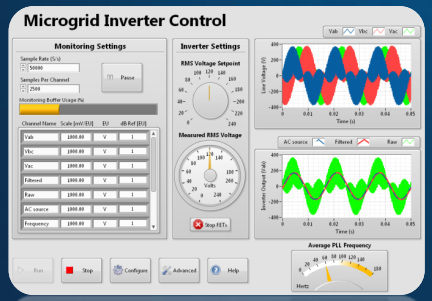

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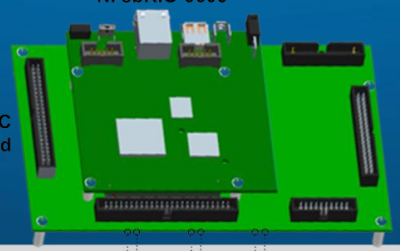

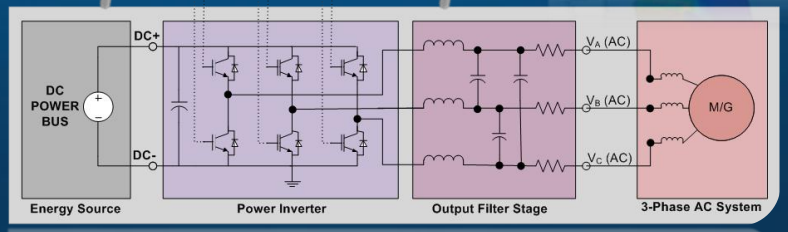

A New Platform and Methodology for System-Level Design of Next-Generation FPGA-based Digital SMPS

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1. Co-simulation tool must capture coupled dynamics between FPGA and power system

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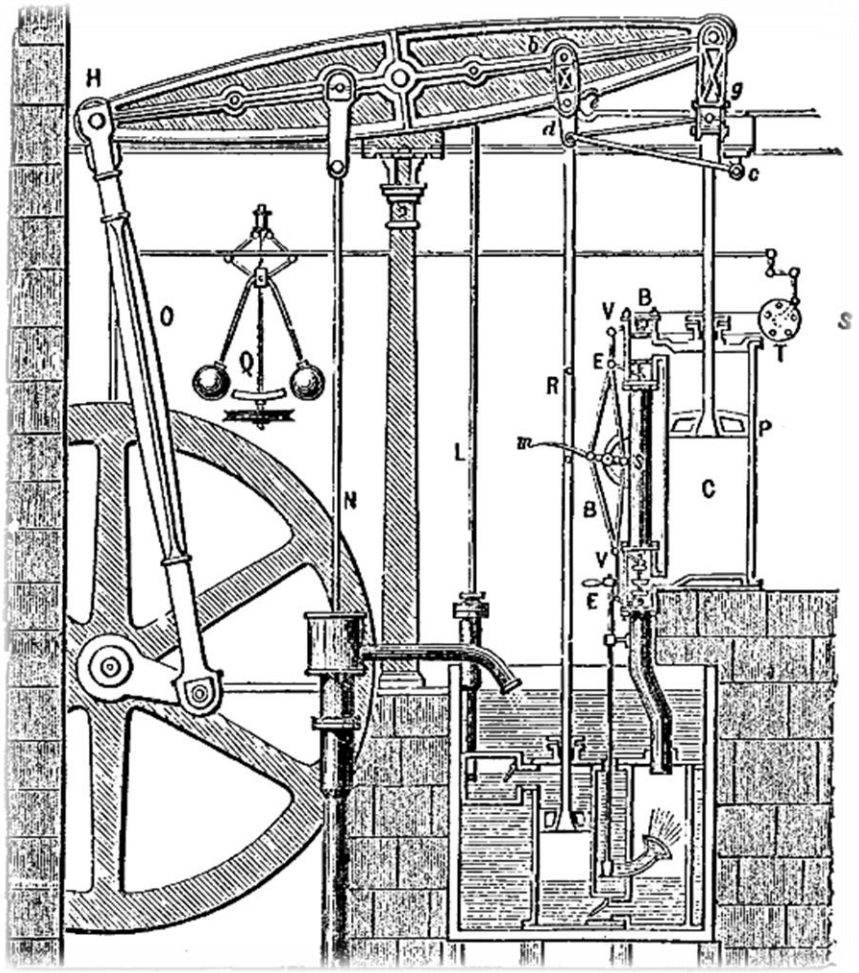
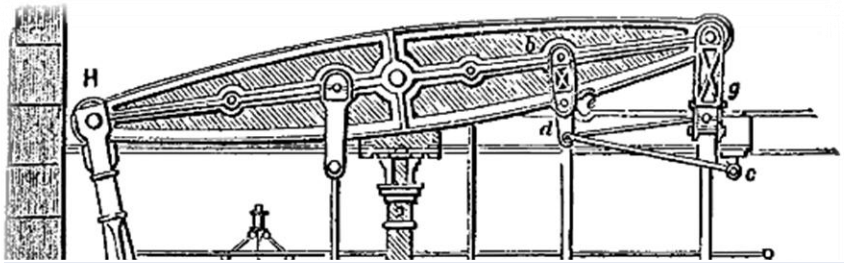
6. Tool must target pre-validated COTS control boards suitable for high volume commercial deployment
7. Tool should also be suitable for developing fast FPGA-based HIL simulators for comprehensive validation of production control system

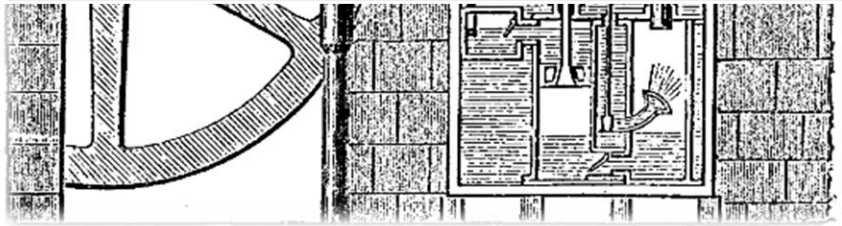
Is energy an information technology?



Is energy an information technology?



Is it digitized and digitally controlled?	
Is it networked?	
Is it improving at exponential rates?	
Can you model and simulate it?	



Making energy an information technology

Making energy an information technology

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Analog Hardware → Digital Software

SENSING

Making energy an information technology

Analog Hardware → Digital Software

SENSING

PROCESSING

Making energy an information technology

Analog Hardware → Digital Software

SENSING

PROCESSING

CONTROL

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Making energy an information technology

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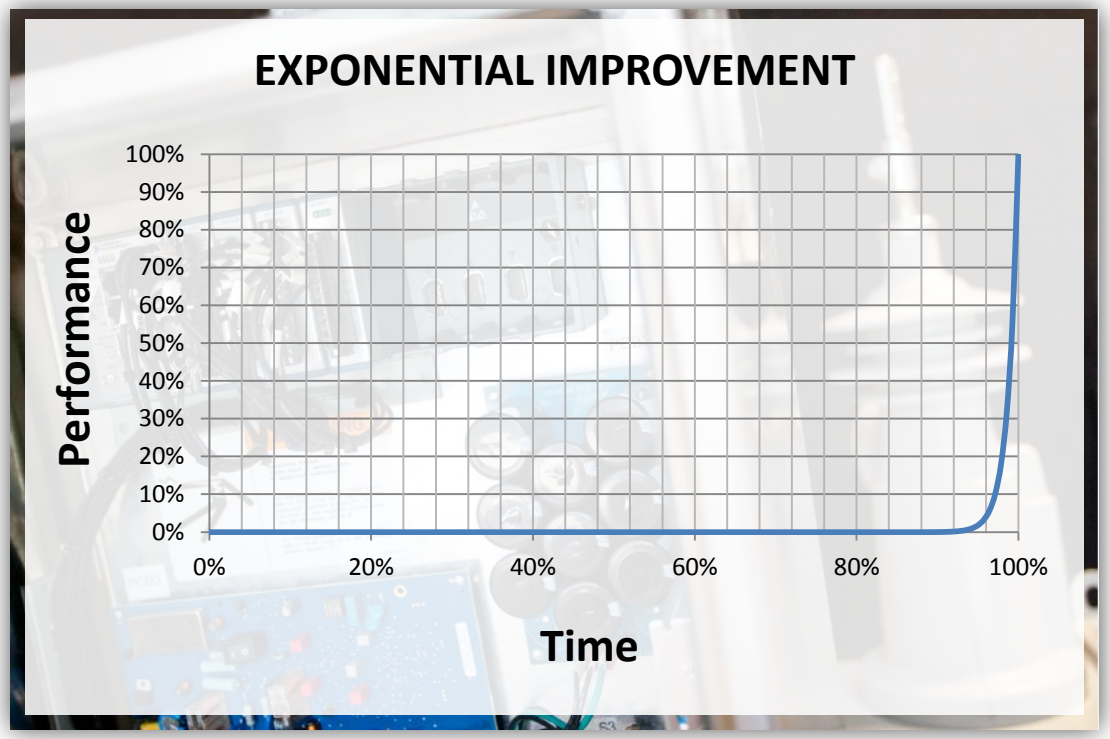
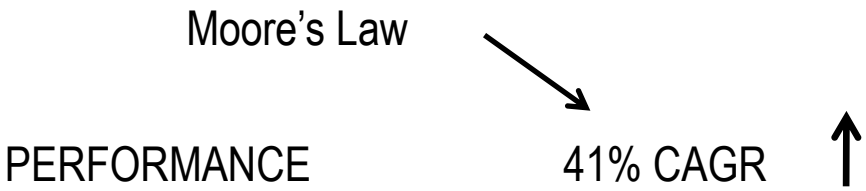


Price-performance

Price-performance

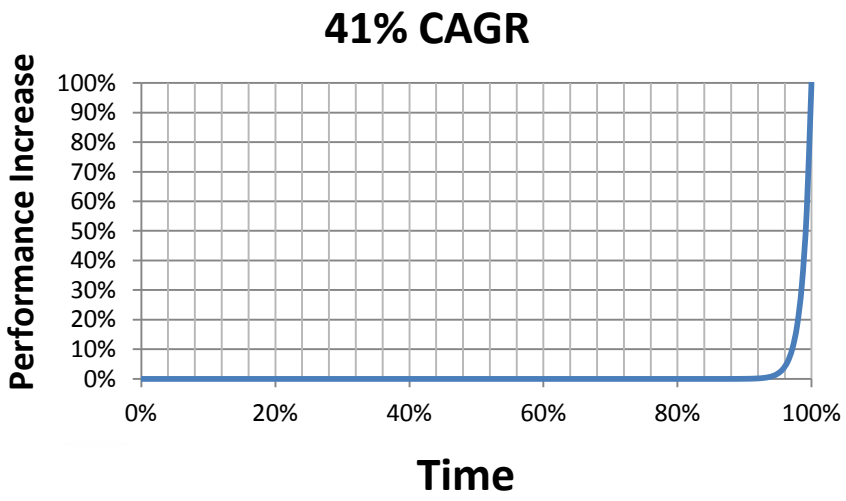


Price-performance

Moore's Law

PERFORMANCE

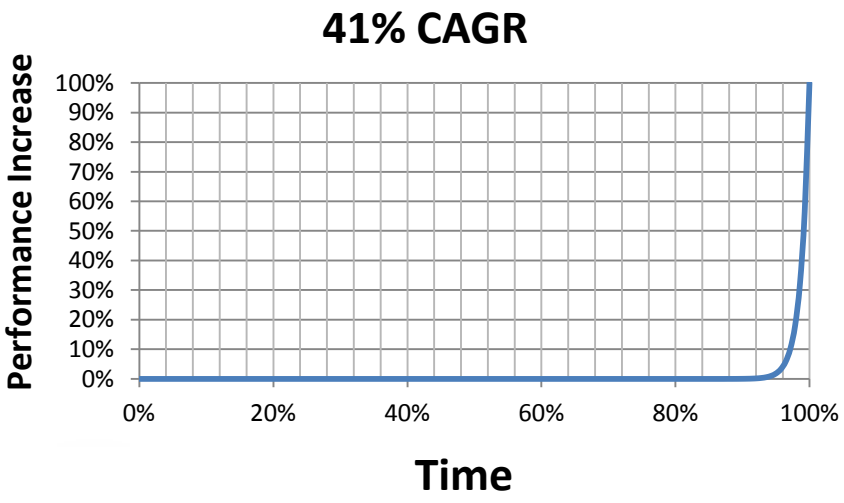
41% CAGR

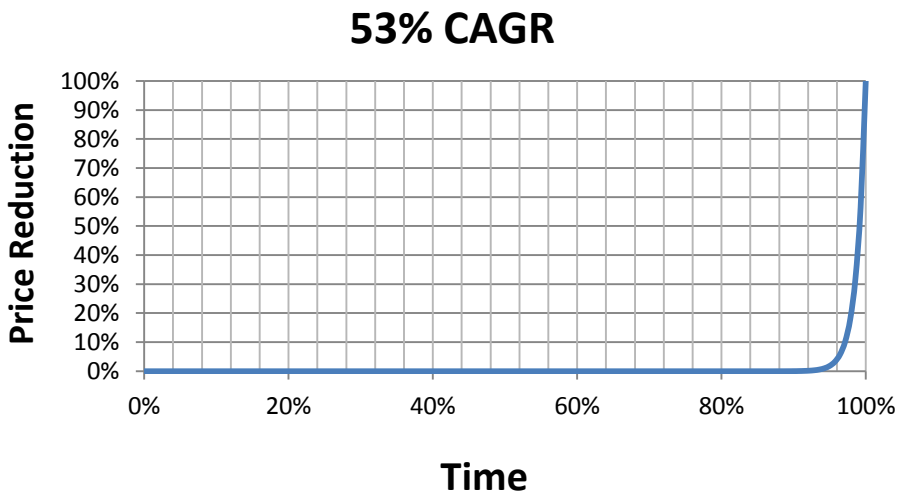


Price-performance

Moore's Law

PERFORMANCE	41% CAGR ↑
PRICE	53% CAGR ↓

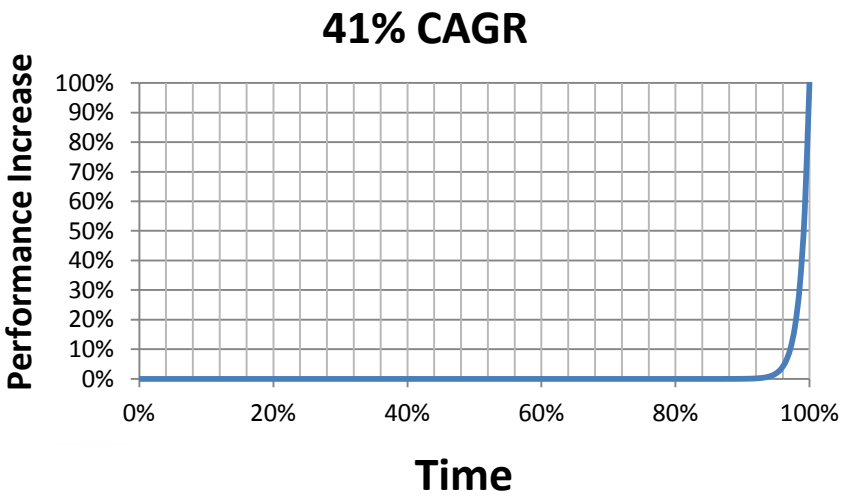


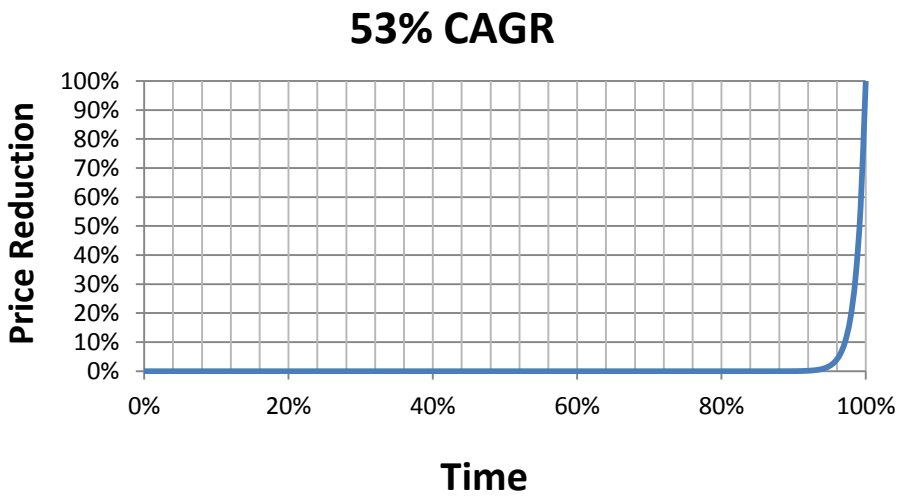


Price-performance

Moore's Law

PRICE-PERFORMANCE = $\frac{\text{PERFORMANCE}}{\text{PRICE}}$ = $\frac{\text{41\% CAGR}}{\text{53\% CAGR}}$

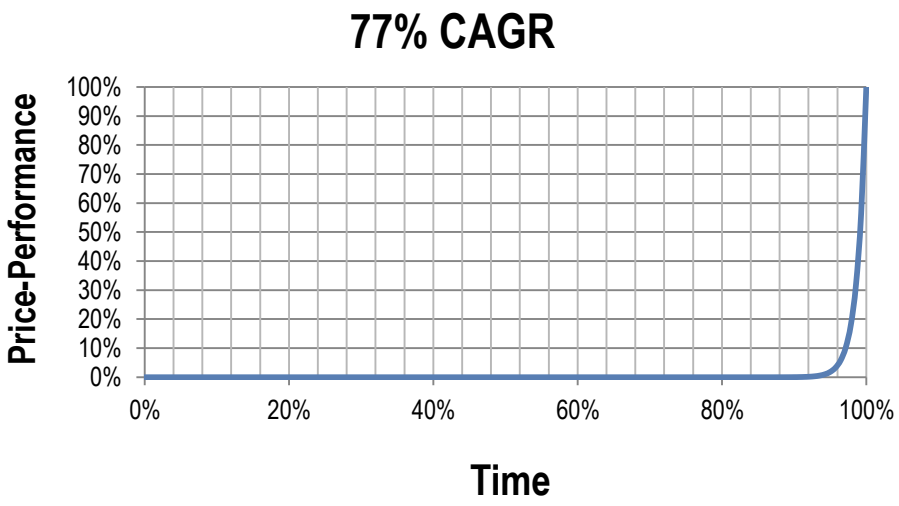




Price-performance

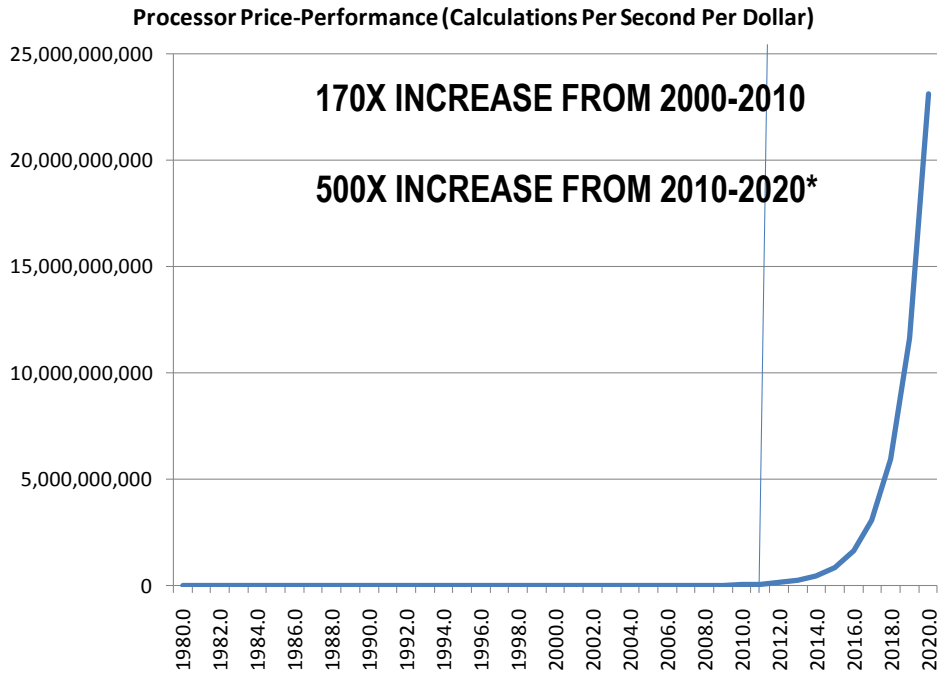
Moore's Law

$$\text{PRICE-PERFORMANCE} = \frac{\text{PERFORMANCE}}{\text{PRICE}} \qquad \frac{\text{41\% CAGR}}{\text{53\% CAGR}} = \text{77\% CAGR (11 MONTHS)}$$



Commercial off the shelf technology (COTS)

- Leverage commercial off the shelf technology for exponentially increasing price-performance
- Don't fall off the Moore's law curve

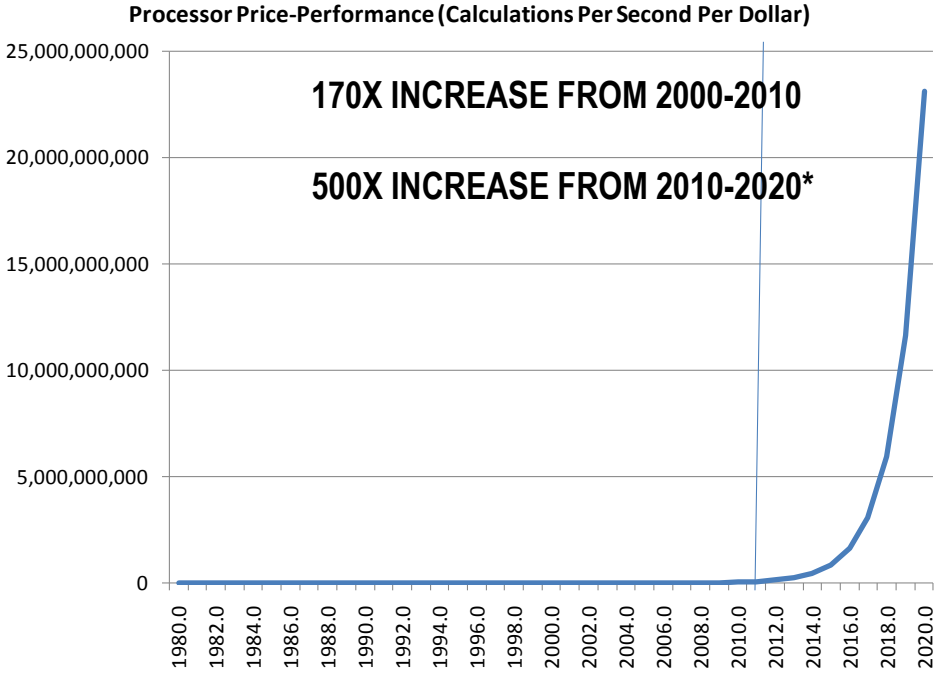


Moore's Law for
Processors and FPGAs

* Projected

Commercial off the shelf technology (COTS)

- Moore's Law is a double edged sword: Keeping a full custom design "on the curve" will be increasingly expensive. Parts will go end-of-Life (EOL) faster than ever.
- NI has a long history of keeping our customers "on the curve", delivering exponentially increasing price-performance, and delivering a platform with long term hardware/software compatibility



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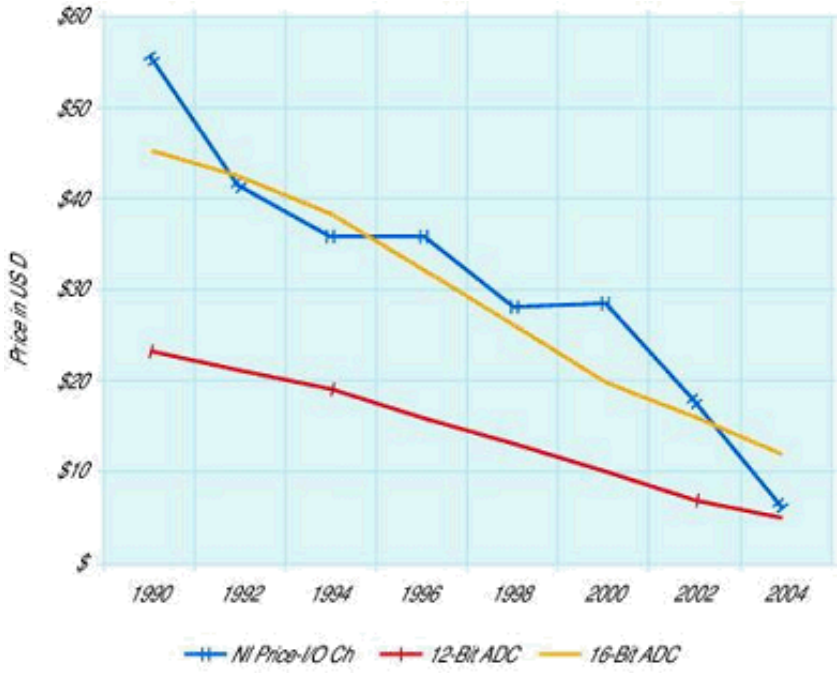


Moore's Law for analog to digital converters (ADCs)- historical

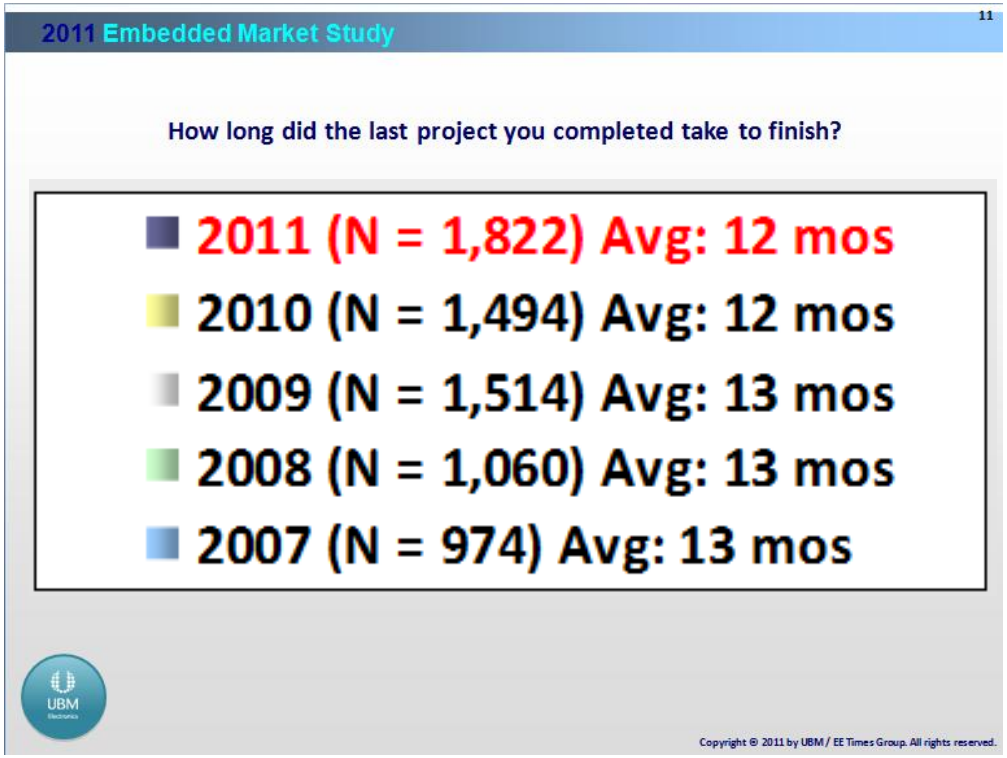
* Projected

Full custom development time is not improving: 12-13 months since 2007

UBM Electronics

2011
EMBEDDED MARKET STUDY

EE Times
Learn today. Design tomorrow. ESD Embedded Systems Design
Learn today. Design tomorrow. ESC Embedded.com
The Official Site of the Embedded Development Community



Images courtesy UBM / EE Times Group

Full custom development cost & risk is not improving: 2009-2011 data

- Average of 15 engineers/project:
  - 7 software engineers (± 1.9 standard deviation)
  - 5 hardware engineers (± 0.6 standard deviation)
  - 3 firmware engineers (± 0.8 standard deviation)
- 57% of projects finished late (no change from 2009-2011):
  - 43% of all projects finished on or ahead of schedule
- What will be your greatest technology challenges next year (managers only):
  1. Integrating new technology or tools
  2. Managing code size/complexity
  3. Building higher quality development process

Source: UBM / EE Times Group

The new era of chip level design

Graphical Programming → Desktop Test Bench → Compilation → Synthesis → Place & Route → Deployment

The new era of chip level design

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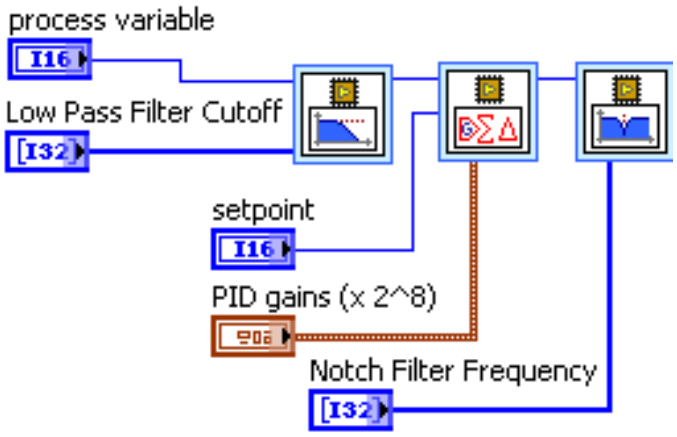

LabVIEW FPGA

The new era of chip level design

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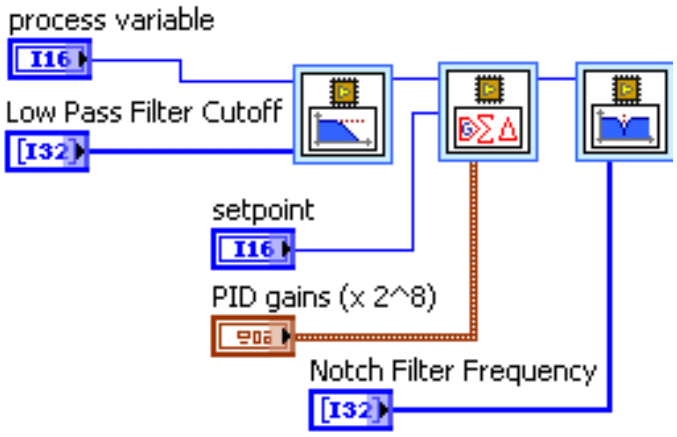

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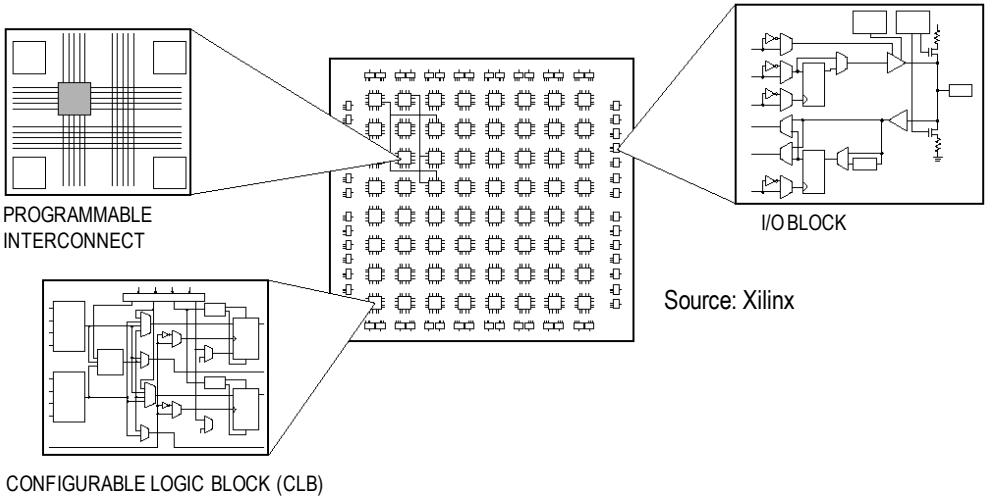
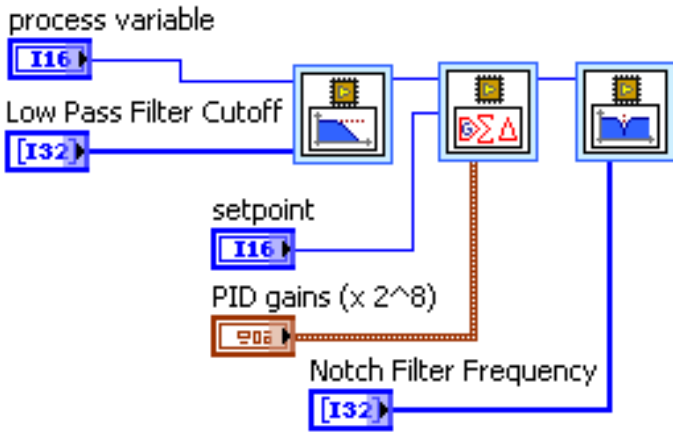


Reconfigurable I/O (RIO) Hardware

The new era of chip level design

"You are Fab-ulous"

Graphical Programming → Desktop Test Bench → Compilation → Synthesis → Place & Route → Deployment



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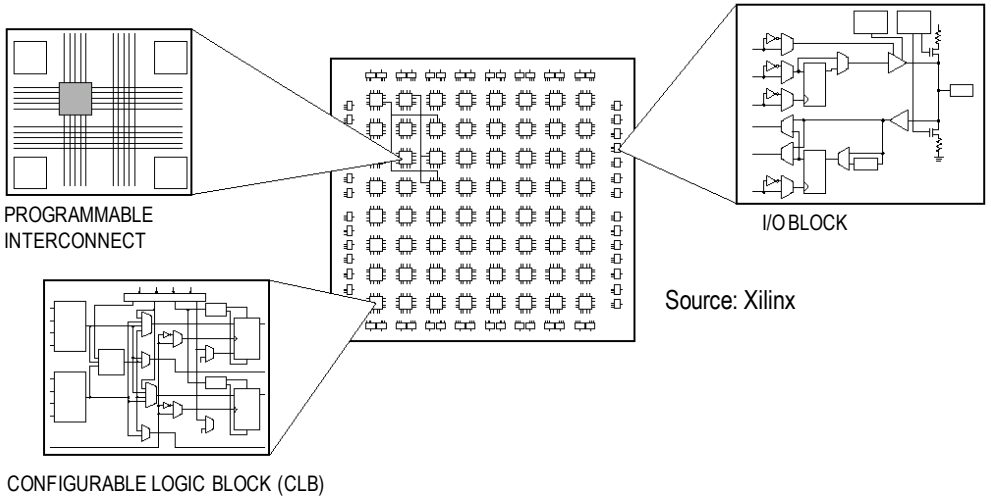
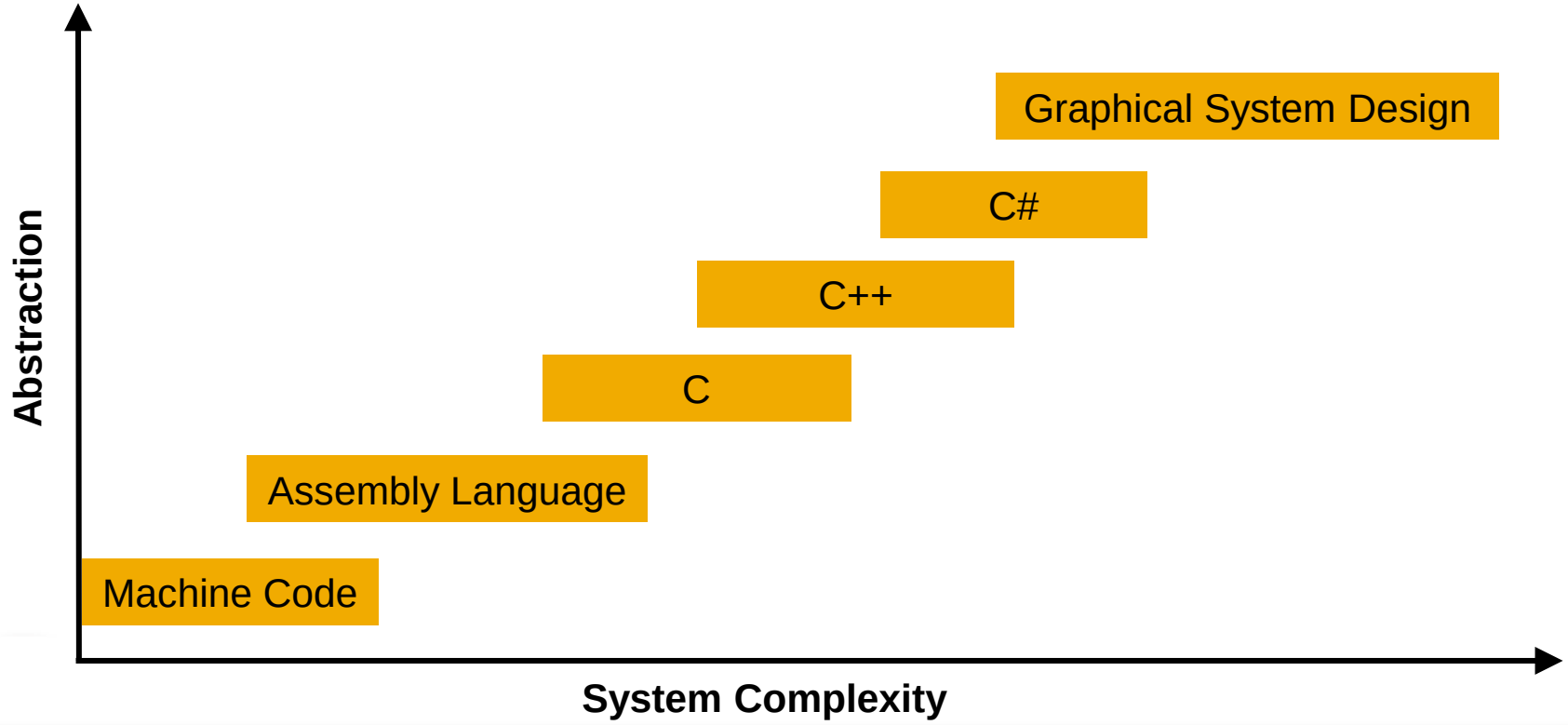


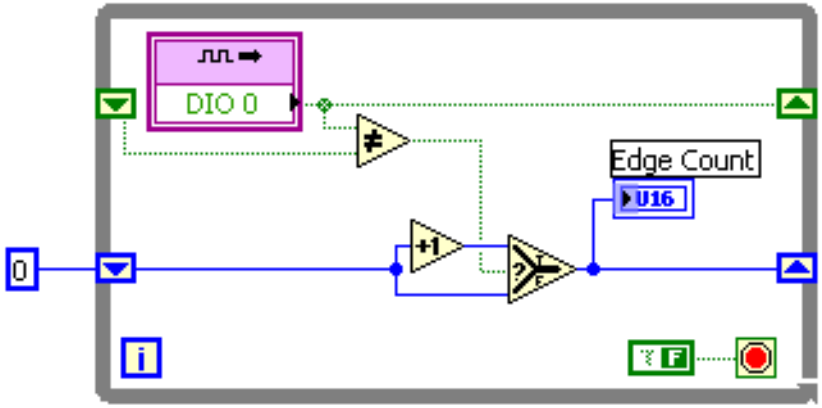
Reconfigurable I/O (RIO) Hardware

Automated Engineering

- 90% of engineering work should be automated



LabVIEW FPGA vs VHDL



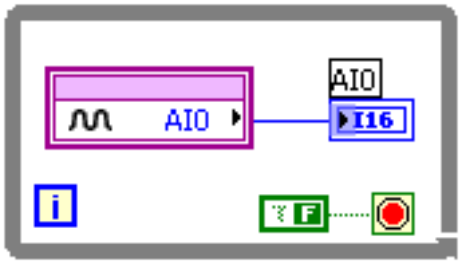

```
-- First we sychronize the asynchronous digital input to our clock
-- by inserting two flip flops.
SynchronizationFFs:
process( aReset, Clk )
begin
  if aReset then
    cDigitalInput_ms <= false;
    cDigitalInput <= false;
  elsif rising_edge(Clk) then
    cDigitalInput_ms <= aDigitalInput;
    cDigitalInput <= cDigitalInput_ms;
  end if;
end process SynchronizationFFs;

-- Then we keep track of what the digital input was on the previous
-- clock cycle by inserting another flip flop
PreviousDigitalInputFF:
process( aReset, Clk )
begin
  if aReset then
    cPrevDigitalInput <= false;
  elsif rising_edge(Clk) then
    cPrevDigitalInput <= cDigitalInput;
  end if;
end process PreviousDigitalInputFF;

-- Then we have a little combinatorial logic to detect a rising edge
cRisingEdgeDetected <= cDigitalInput and not cPrevDigitalInput;

-- And finally we have a register that increments when that rising
-- edge is detected.
CounterRegister:
process( aReset, Clk )
begin
  if aReset then
    cCountReg <= (others=>'0');
  elsif rising_edge(Clk) then
    if cRisingEdgeDetected then
      cCountReg <= cCountReg + 1;
    end if;
  end if;
end process CounterRegister;
cCount <= cCountReg;

end rtl;
```

Counter

Analog I/O

Streaming

LabVIEW FPGA vs VHDL



Counter

Analog I/O

Streaming

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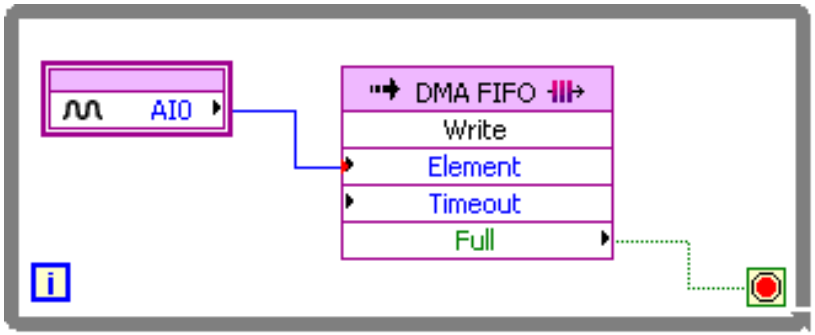
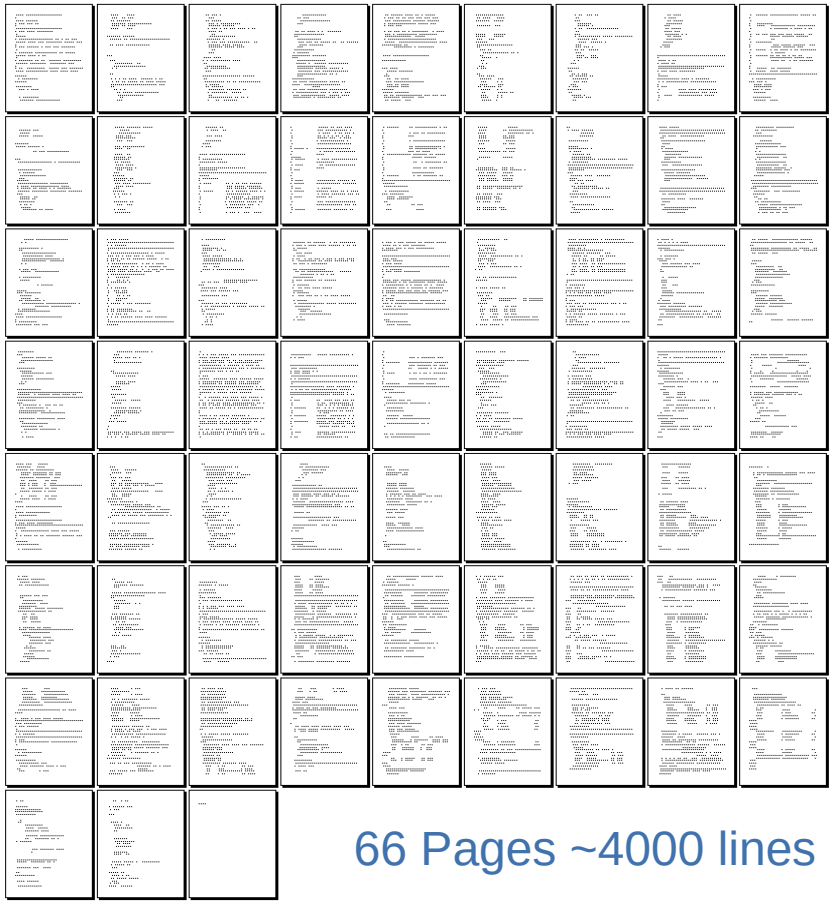
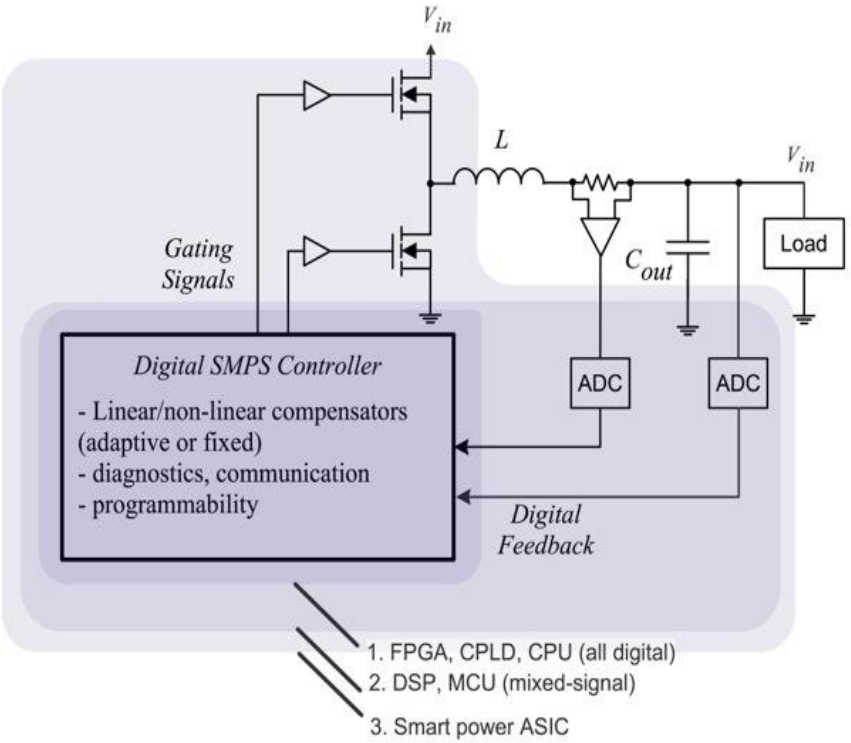


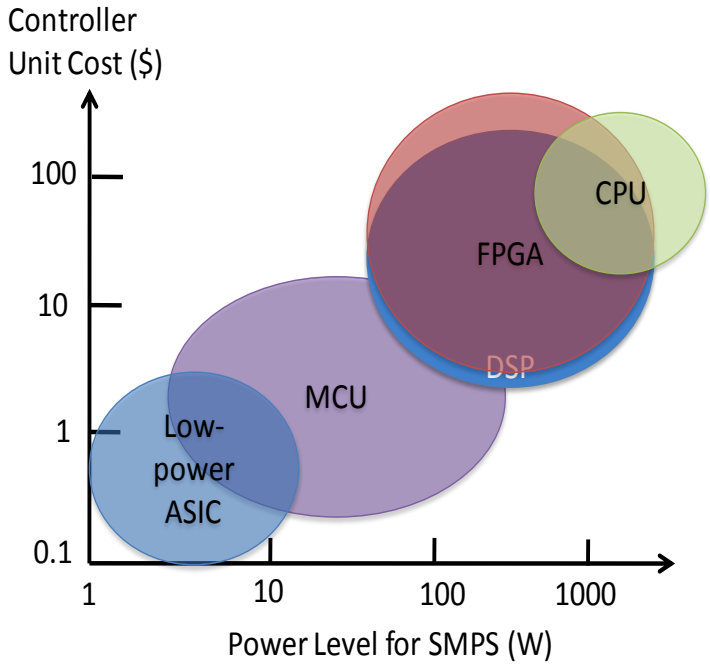


66 Pages ~4000 lines

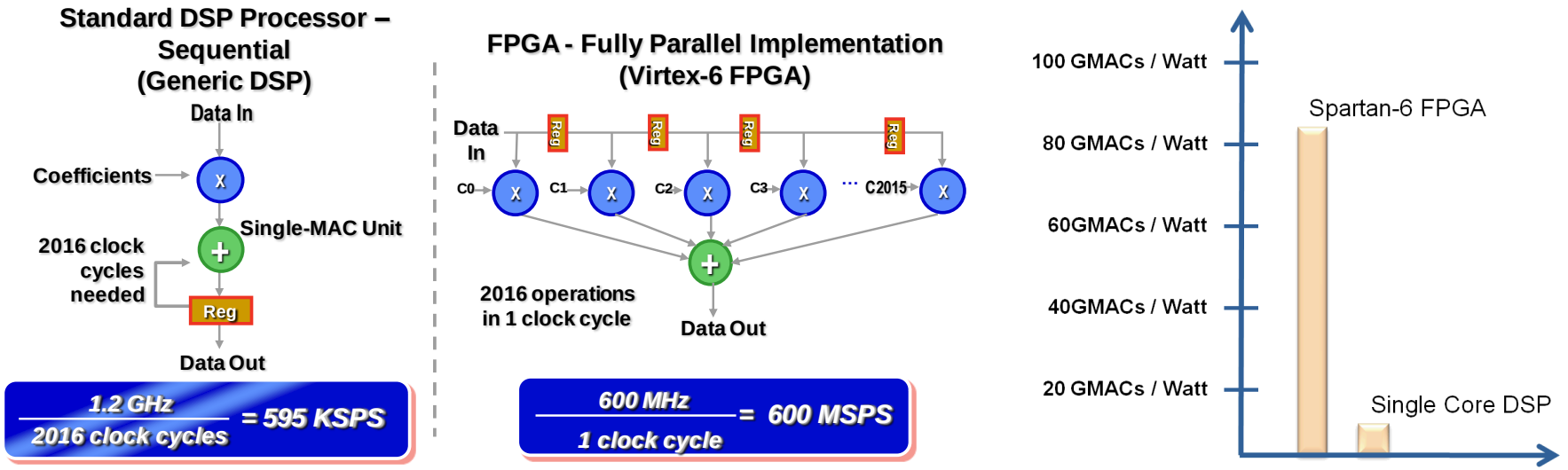
Counter **Analog I/O** **Streaming**

Spectrum of suitable control targets for high volume mass production





Modern FPGAs utilize hard-core DSP processing elements integrated in fabric



Modern FPGAs utilize hard-core DSP processing elements, integrated within the reconfigurable computing fabric to yield 1^9 to 1^{12} fixed-point multiply-accumulate (MAC) operations per second, often at a lower cost per MAC and lower power dissipation per MAC compared to processors and DSPs [5]. The lowest cost FPGAs on the market have now reached the ~ $5 range in high-volume, which makes them attractive not only for proof-of-concept research prototypes but also for mass-produced converters and motor drives in the several-hundred-watt range and above.

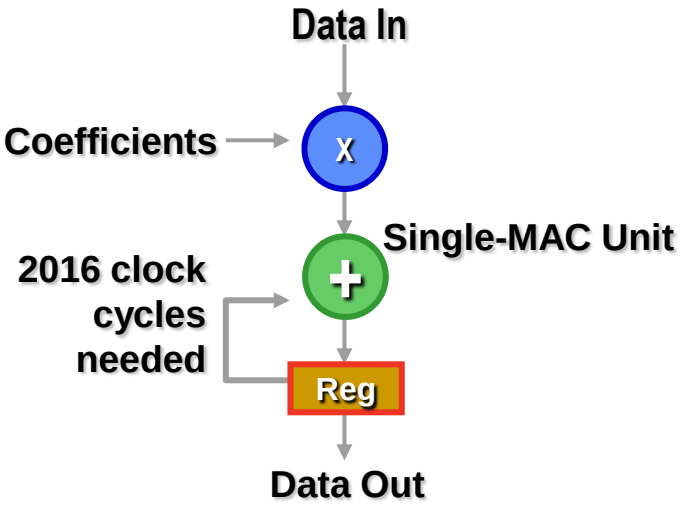
Modern FPGAs are often lower cost per MAC compared to single-core processors and DSPs

Part	Description	DSP Performance	MACs/$*
DSP A	32-bit, 100 MHz, fixed pt	100 MMACs	6.48e6
DSP B	300 MHz, fixed pt	600 MMACs	6.98e6
Xilinx Spartan-6 LX45 FPGA	FPGA, 250 MHz, fixed pt, 58 DSP48A1 multipliers	22,600 MMACs (250 MHz) 4,600 MMACs (40 MHz)	5.58e8 8.85e7

* Multiply-accumulate (MAC) operations per dollar

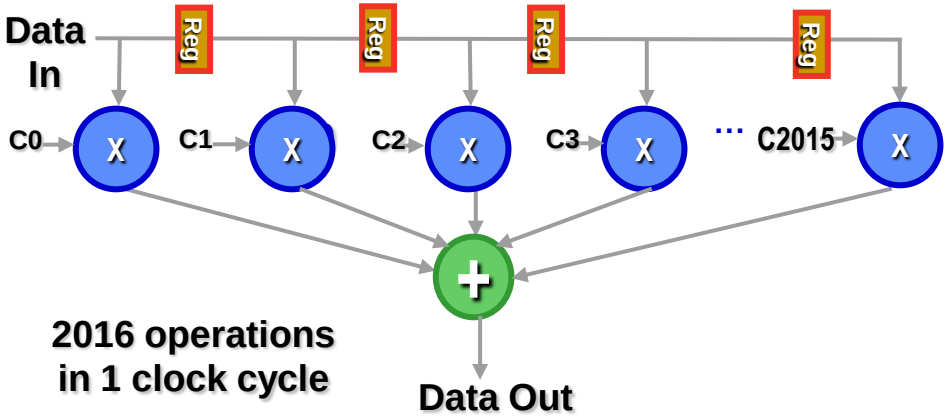
Sequential vs. Parallel DSP Processing

Standard DSP Processor – Sequential (Generic DSP)



$$\frac{1.2\ \text{GHz}}{2016\ \text{clock cycles}} = 595\ \text{KSPS}$$

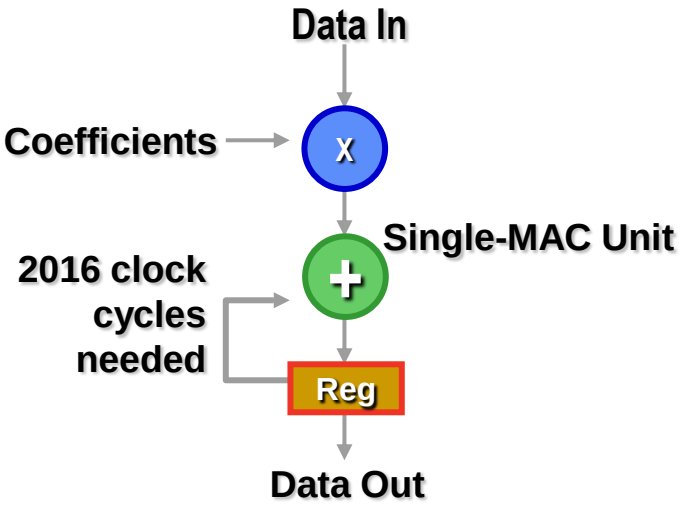
FPGA - Fully Parallel Implementation (Virtex-6 FPGA)



$$\frac{600\ \text{MHz}}{1\ \text{clock cycle}} = 600\ \text{MSPS}$$

Sequential vs. Parallel DSP Processing

Standard DSP Processor – Sequential (Generic DSP)



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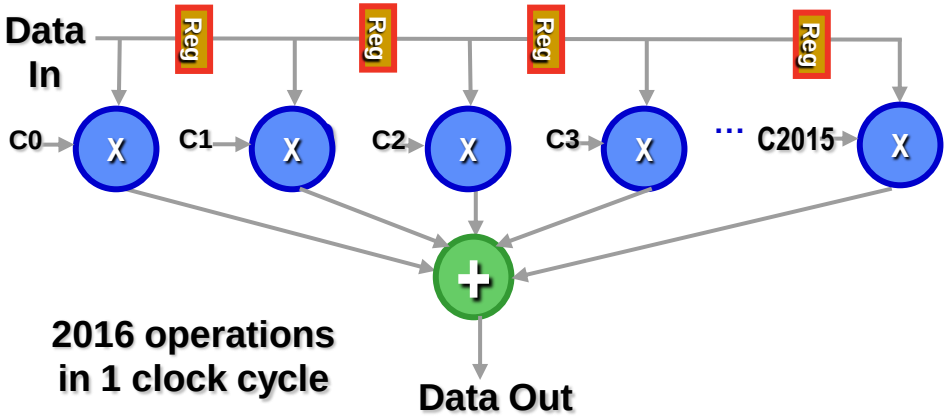
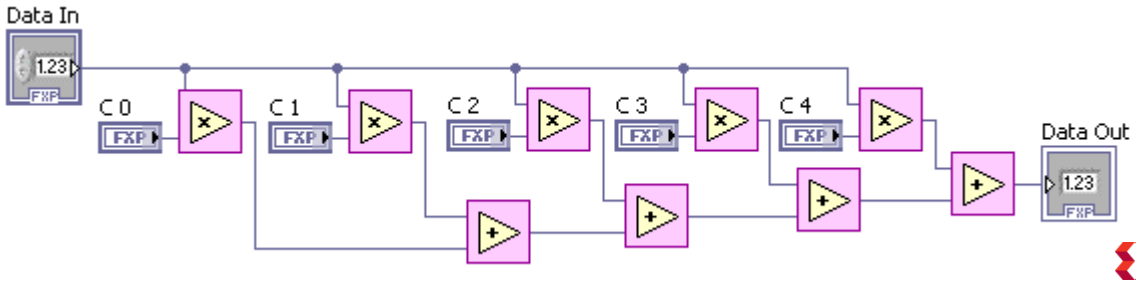
FPGA - Fully Parallel Implementation (Virtex-6 FPGA)



$$\frac{600\ \text{MHz}}{1\ \text{clock cycle}} = 600\ \text{MSPS}$$

NI LabVIEW FPGA

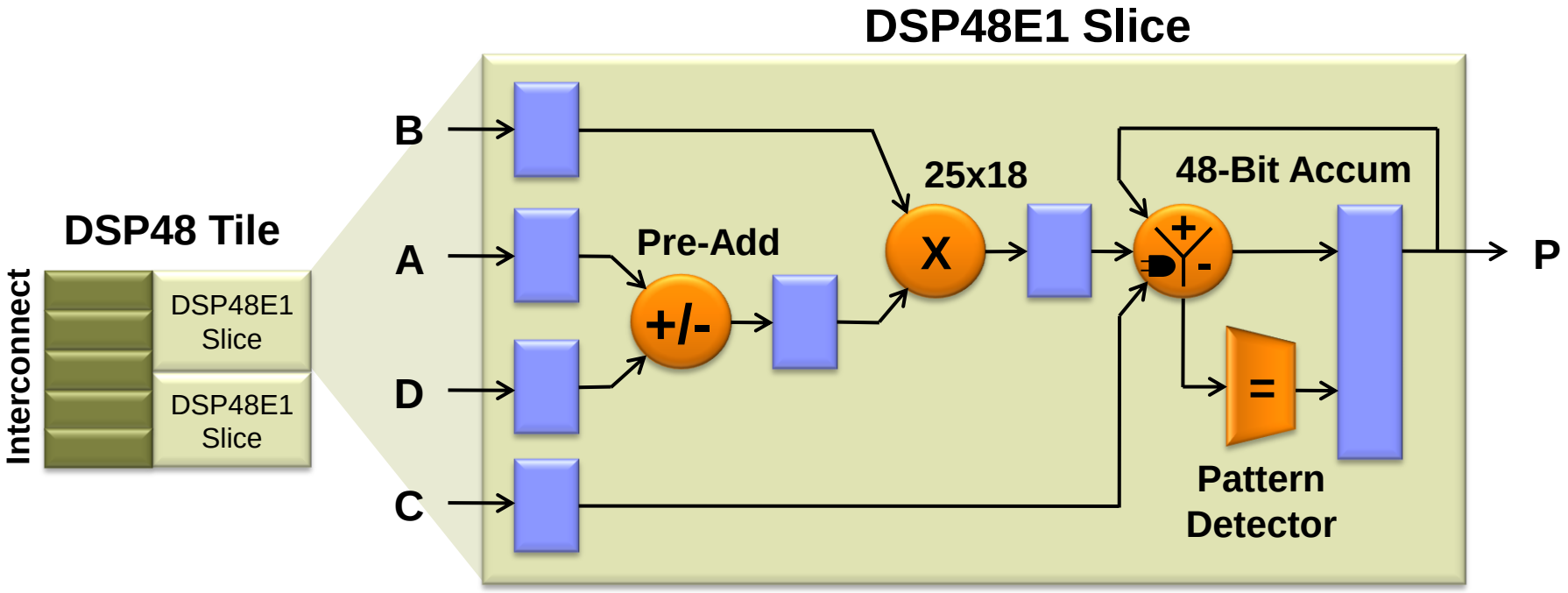
- High Level Programming
- True Parallel Execution



XILINX

DSP Performance through the DSP48E1 Slice

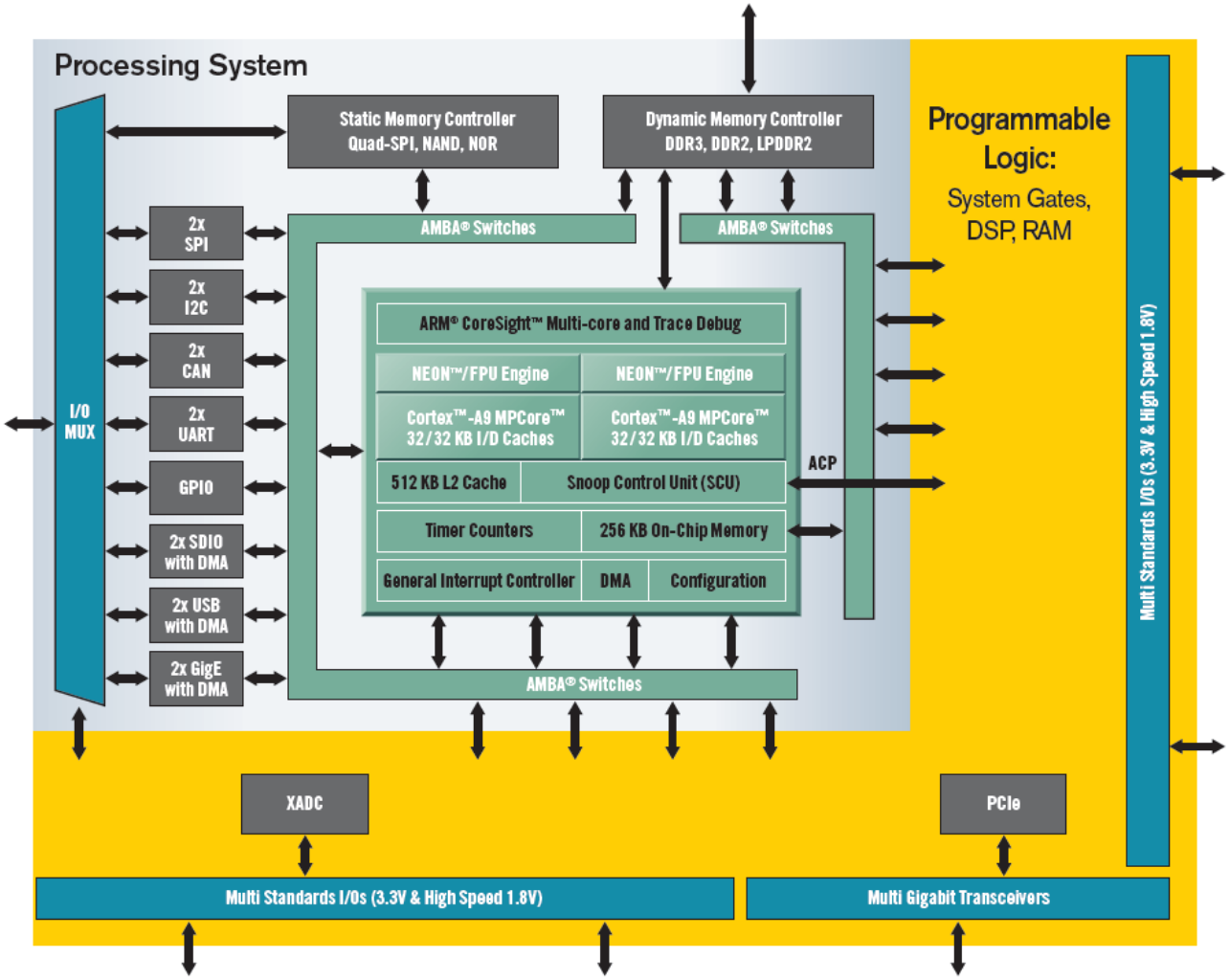
Virtex-6, Artex-7, Kintex-7, Virtex-7



- **2 DSP48E1 Slices / Tile**
- **Input Flexibility through 5 Shared interconnect**
- **638 MHz Fmax**
  - 20% faster than competing FPGAs

The Next Paradigm: Floating Point Processors Integrated in FPGA Fabric

ZYNQ EXTENSIBLE PROCESSING PLATFORM



The Next Paradigm: Floating Point Processors Integrated in FPGA Fabric

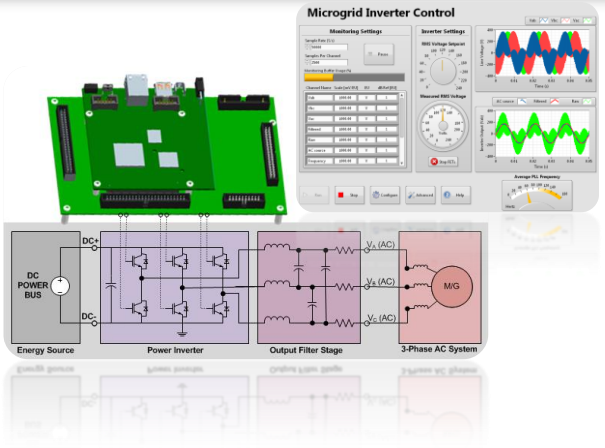
ZYNQ EXTENSIBLE PROCESSING PLATFORM

Zynq-7000 Product Table (Software View)

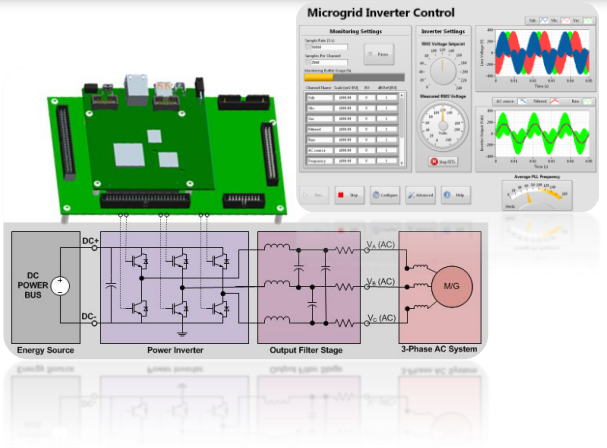
	Device Name	Z-7010	Z-7020	Z-7030	Z-7045
	Part Number	XC7Z010	XC7Z020	XC7Z030	XC7Z045
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™			
	Processor Extensions	NEON™ and Single/Double Precision Floating Point			
	Maximum Frequency	800 MHz			
	L1 Cache	32 KB Instruction, 32 KB Data per processor			
	L2 Cache	512 KB			
	On-Chip Memory	256 KB			
	External Memory Support	DDR3, DDR2, LPDDR2			
	External Static Memory Support	2x QSPI-SPI, NAND, NOR			
	DMA Channels	8 (4 dedicated to Programmable Logic)			
	Peripherals	2x USB 2.0 (OTG) w/DMA, 2x Tri-mode Gigabit Ethernet w/DMA, 2x SD/SDIO w/DMA, 2x UART (2), 2x CAN2.0B, 2x I2C, 2x SPI, 4x 32b GPIO			
	Security	AES and SHA 256b for secure boot			
	Peripherals and Static Memory Multiplexed I/O[1]	54			
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave, 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts			
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix™-7 FPGA	Artix™-7 FPGA	Kintex™-7 FPGA	Kintex™-7 FPGA
	Programmable Logic Cells (Approximate ASIC Gates[3])	28K Logic Cells (~430K)	85K Logic Cells (~1.3M)	125K Logic Cells (~1.9M)	350K Logic Cells (~5.2M)
	Extensible Block RAM (# 36 Kb Blocks)	240KB (60)	560KB (140)	1,060KB (265)	2,180KB (545)
	Programmable DSP Slices (18x25 MACCs)	80	220	400	900
	Peak DSP Performance (Symmetric FIR)	58 GMACS	158 GMACS	480 GMACS	1080 GMACS
	PCI Express® (Root Complex or Endpoint)	—	—	Gen2 x4	Gen2 x8
	Agile Mixed Signal (AMS)/XADC	2x 12 bit, 1 MSPS ADCs with up to 17 Differential Inputs			
	Security	AES and SHA 256b for secure configuration			
	Multi-Standards 3.3V I/O[2]	100	200	250	350
	Serial Transceivers[2]	—	—	4	16

Notes:
1. Static memory interface combined with the usage of many peripherals could require more than 54 I/Os. A designer can use the Programmable Logic I/Os.
2. Total Number of I/O and Transceivers depends on package used.
3. Equivalent ASIC gate count is dependent of the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.
4. Preliminary product information. Subject to change. Please contact your Xilinx representative for the latest information.

High Level Goals



High Level Goals



Reduce your engineering cost, risk and development time	→ Profitability
Focus on your core competency and value (not DSP board design)	→ Product differentiation
Incorporate the latest technologies while reusing software investments	→ On-time delivery
Ship fully tested, supported commercial embedded systems	→ Product quality
Empower your control experts to do embedded development	→ Development efficiency

You are here

NATIONAL INSTRUMENTS

GREEN ENGINEERING

RE<

C

Measure it. (Understand the problem.)

Acquire

Analyze

Present

Green Engineering

Measure it. (Understand the problem.)

Acquire

Analyze

Present

Design

Prototype

Deploy

Fix it. (Create the solution.)

Green Engineering

Measure it. (Understand the problem.)

Acquire

Analyze

Present

Design

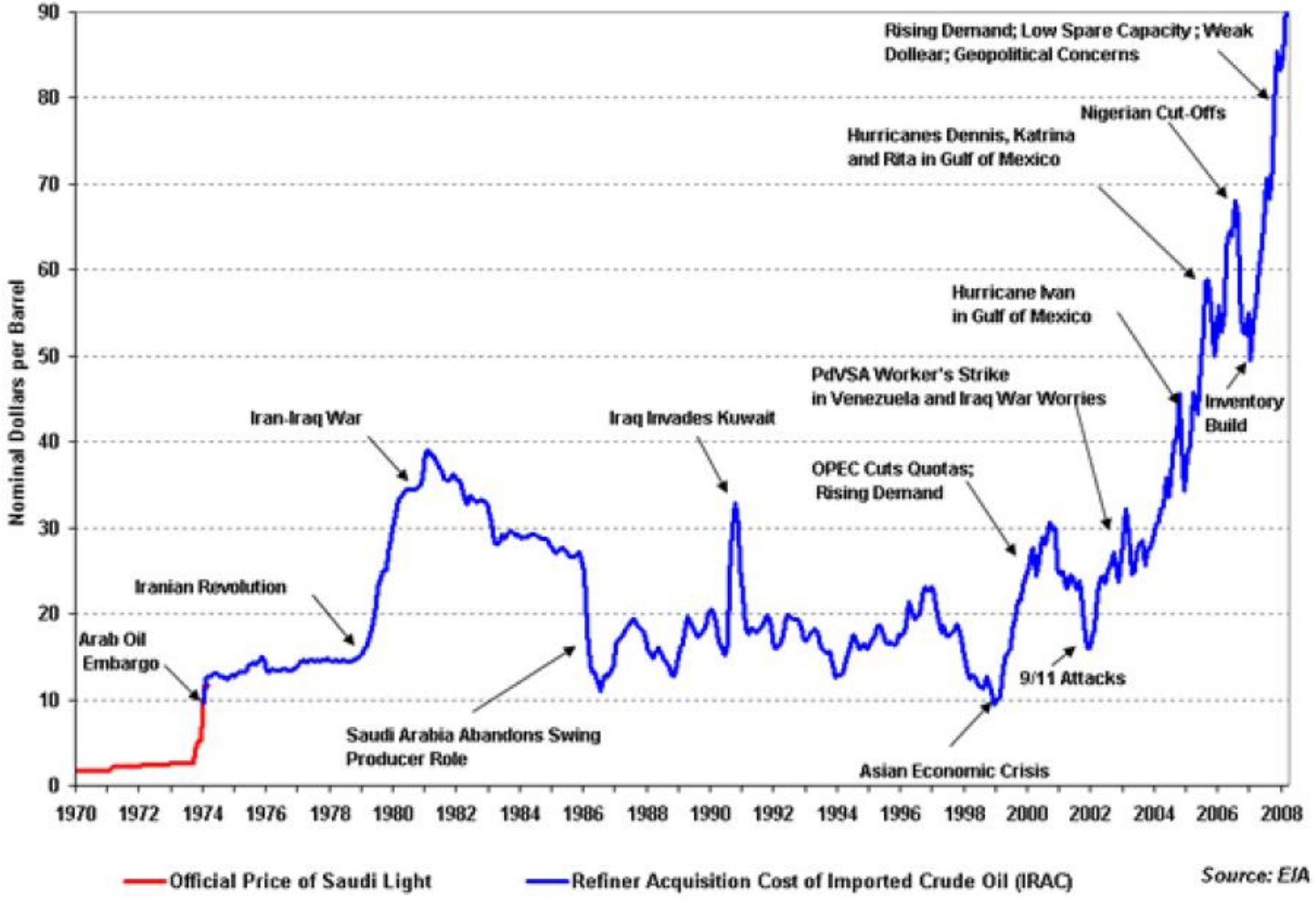
Prototype

Deploy

Fix it. (Create the solution.)

Green Engineering

The Largest Market Motivator



Source: "FreedomCAR and DOE Roadmap for Automotive Power Electronics," Laura Marlino, Oak Ridge National Laboratory (ORNL), March 2011

NATIONAL INSTRUMENTS

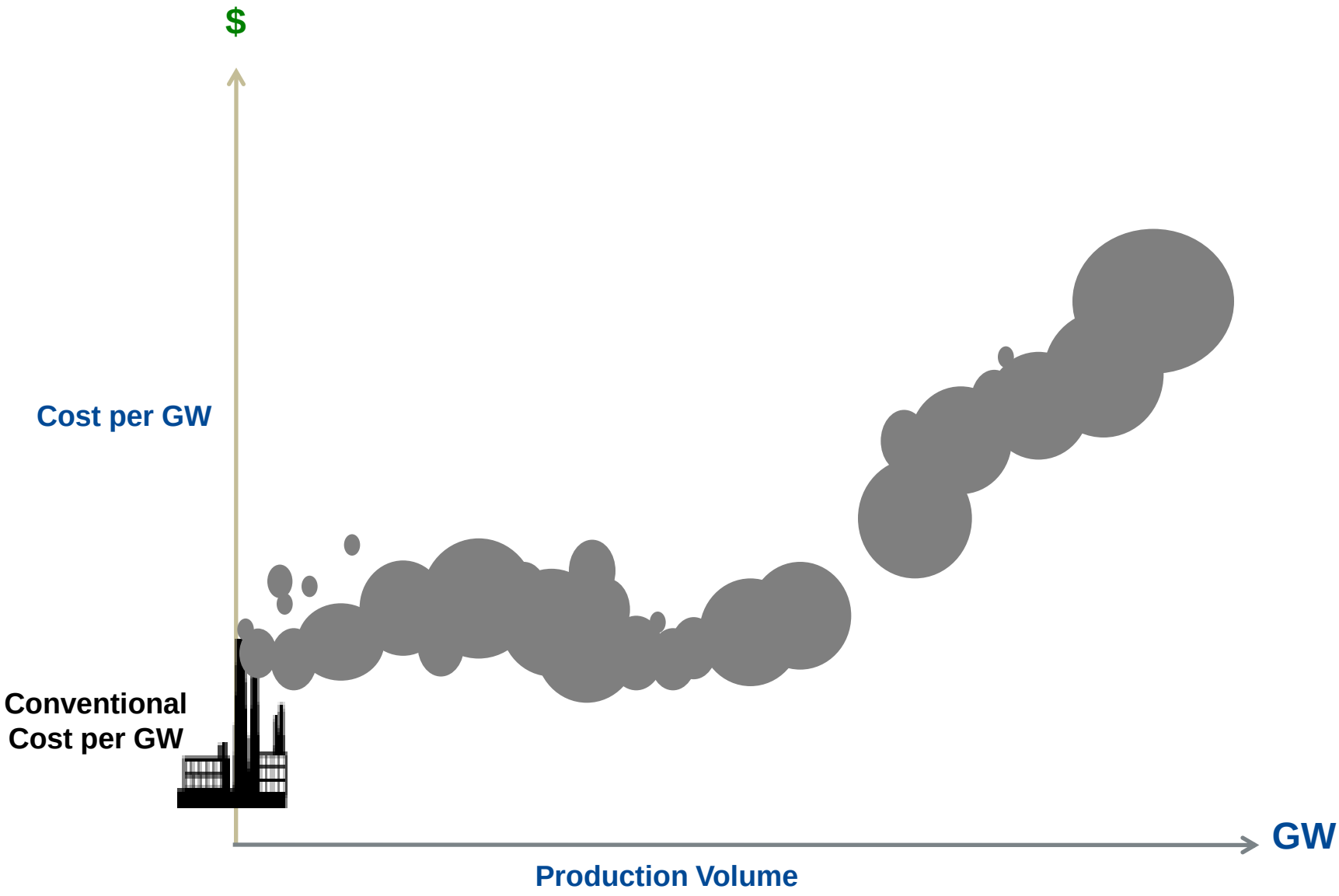
Renewable Energy is Abundant

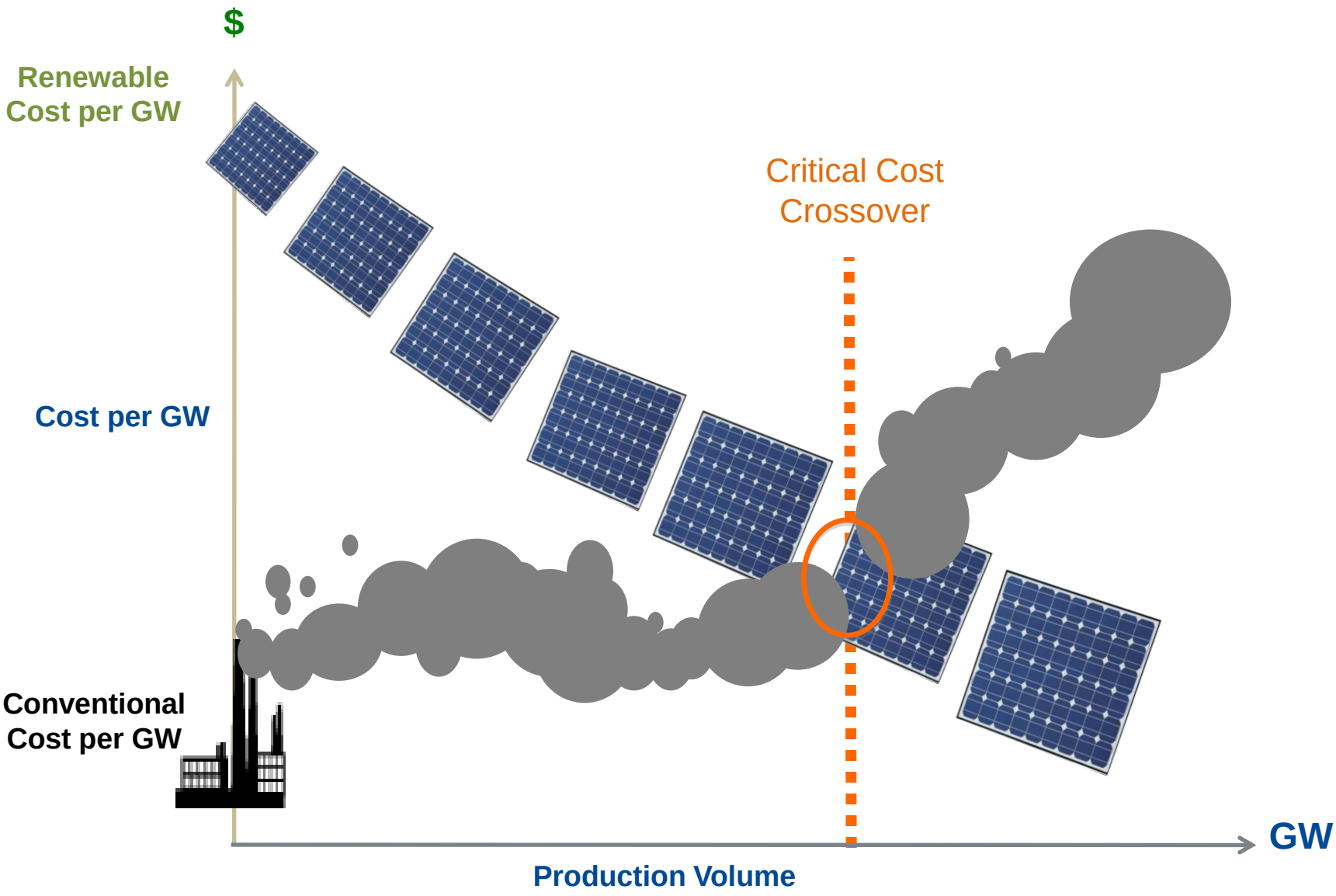
Human Demand: ~16 TW

Resource	Available (TW)	Ratio
Solar	86,000	5,375
Airborne Wind	3,000	187
Terrestrial Wind	870	54
Hydro	300	19
Ocean Thermal	100	6
Wave	8.7	4
Geothermal	3	2
Tidal	3.7	0.23

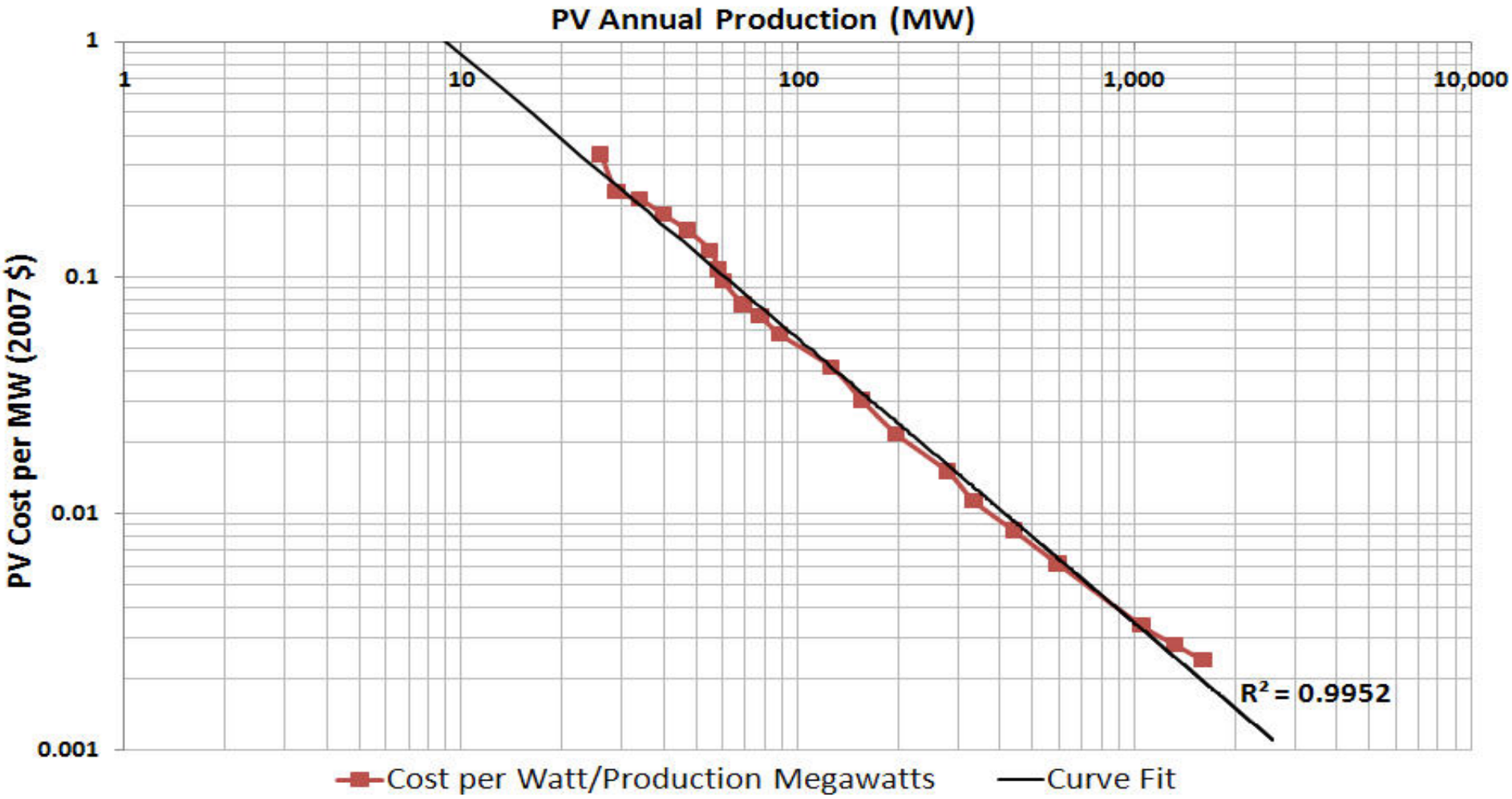
Data: “Quantifying global exergy resources,” Weston A. Hermann, 2005*
* Airborne wind data from alternate source.

NATIONAL INSTRUMENTS

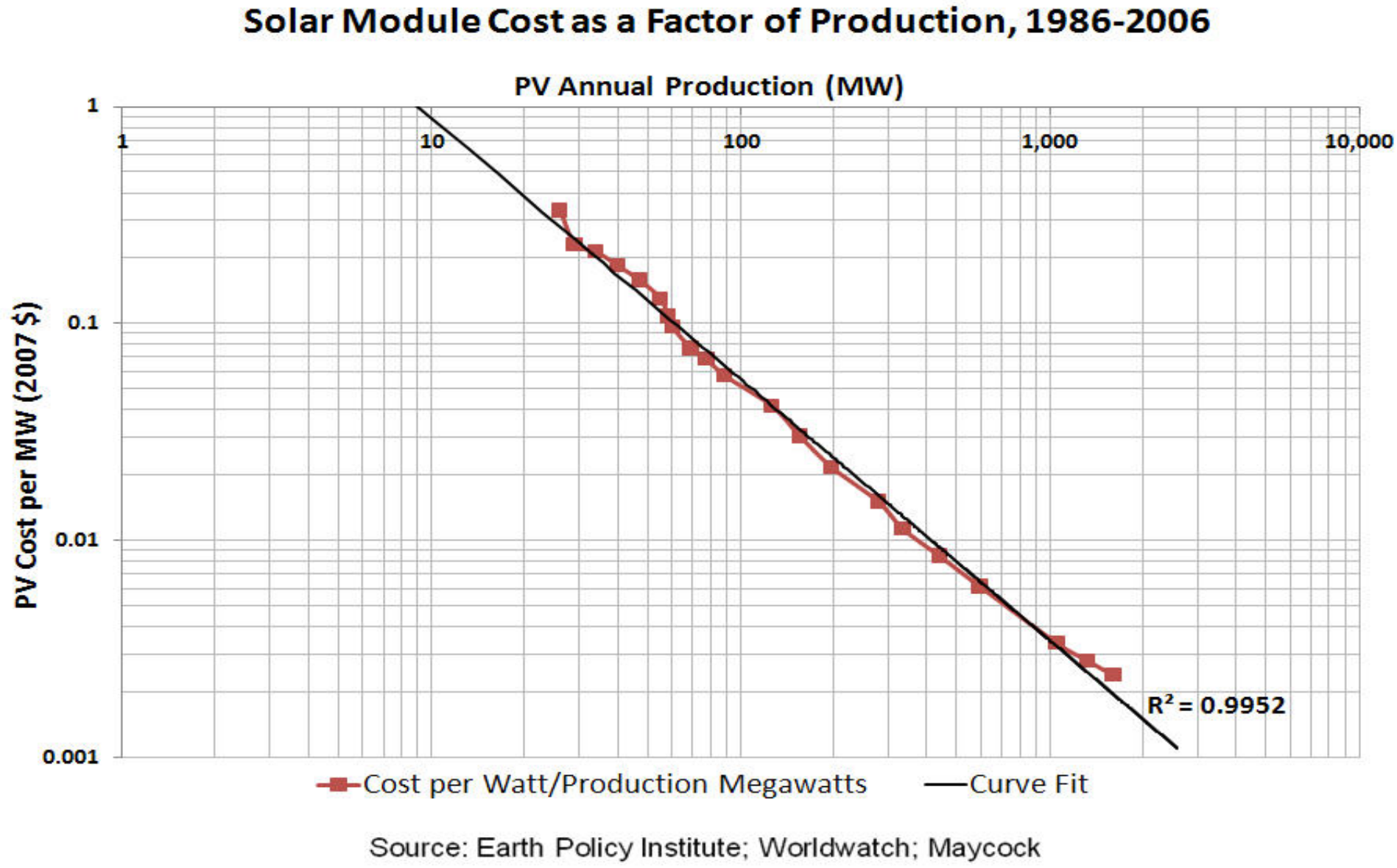

$
Cost per GW
Conventional
Cost per GW
GW
Production Volume


$
Renewable
Cost per GW
Critical Cost
Crossover
Cost per GW
Conventional
Cost per GW
GW
Production Volume

Solar Module Cost as a Factor of Production, 1986-2006



Source: Earth Policy Institute; Worldwatch; Maycock



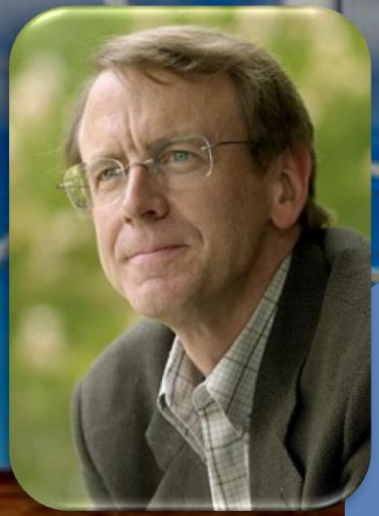
Cost per Watt = 14.26*(ANNUAL_PRODUCTION_GW*1000)^(-1.205)*ANNUAL_PRODUCTION_GW*1000

Energy is the World's Biggest Environmental Problem,

Energy is the World's Biggest Environmental Problem, Technological Challenge

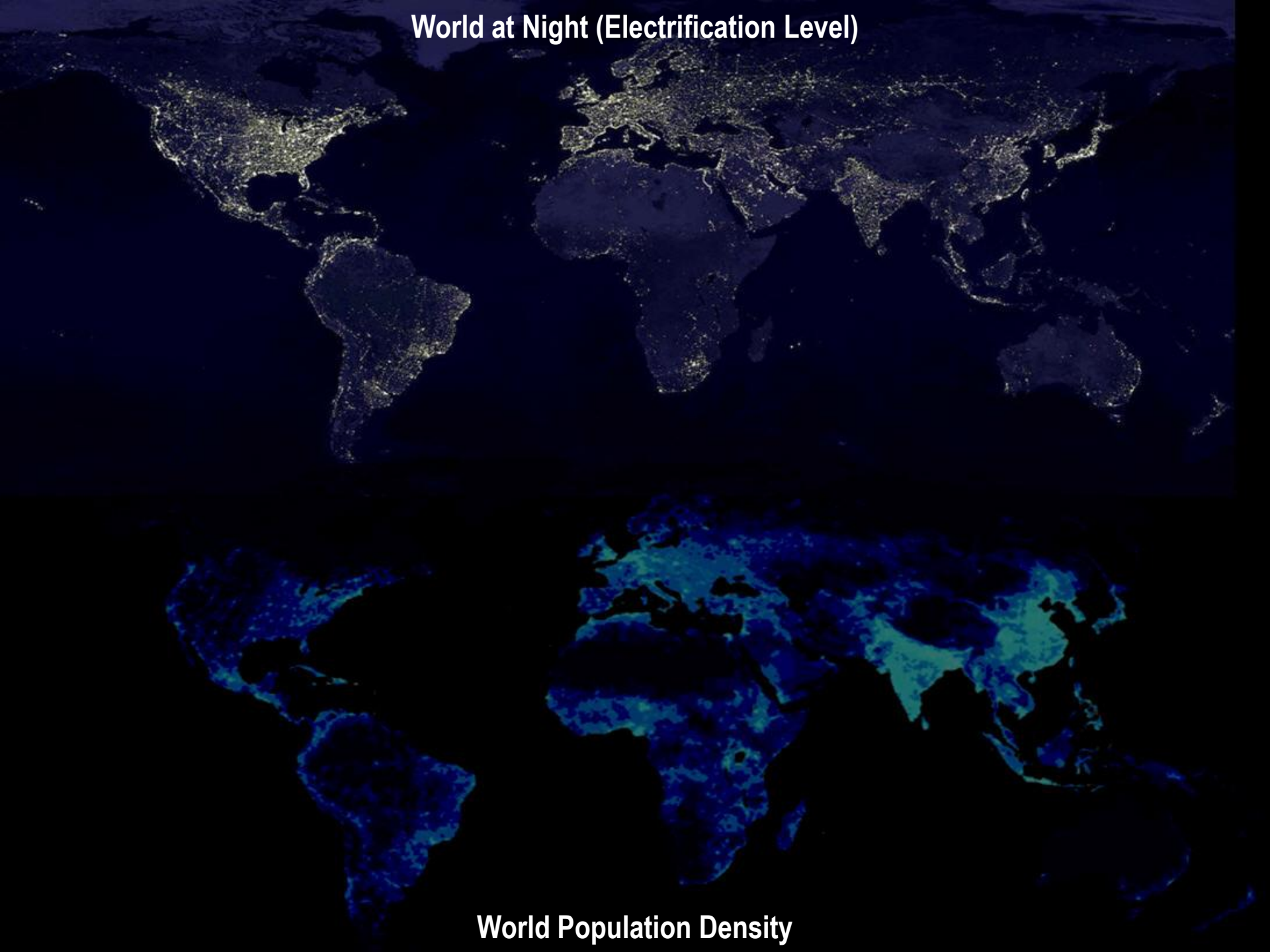
Energy is the World's Biggest Environmental Problem, Technological Challenge and Economic Opportunity

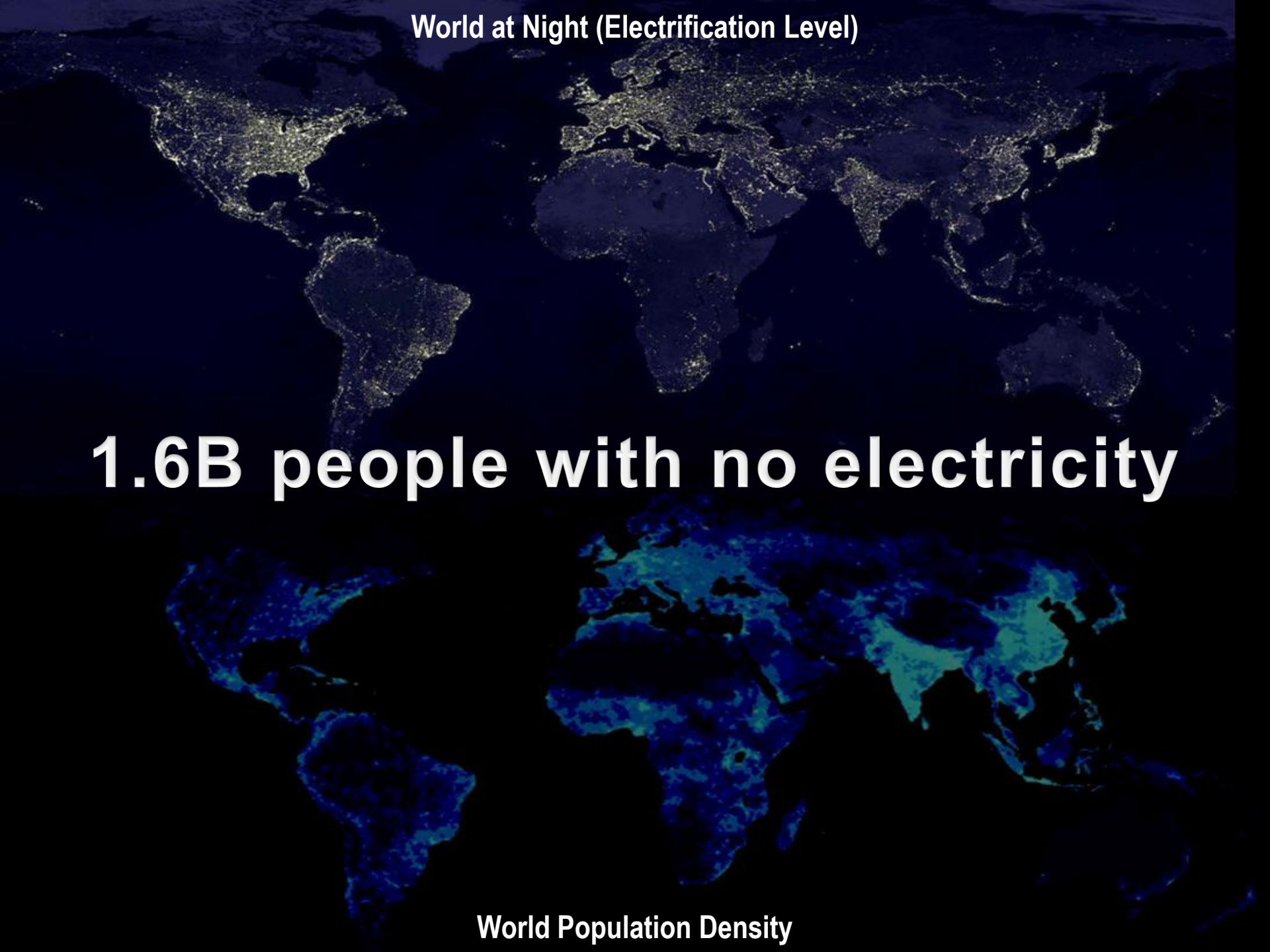
Energy is the World's Biggest Environmental Problem, Technological Challenge and Economic Opportunity



"The internet is a trillion-dollar economy. Energy is a 6-trillion-dollar economy – energy could be the largest economic opportunity of the 21st century."

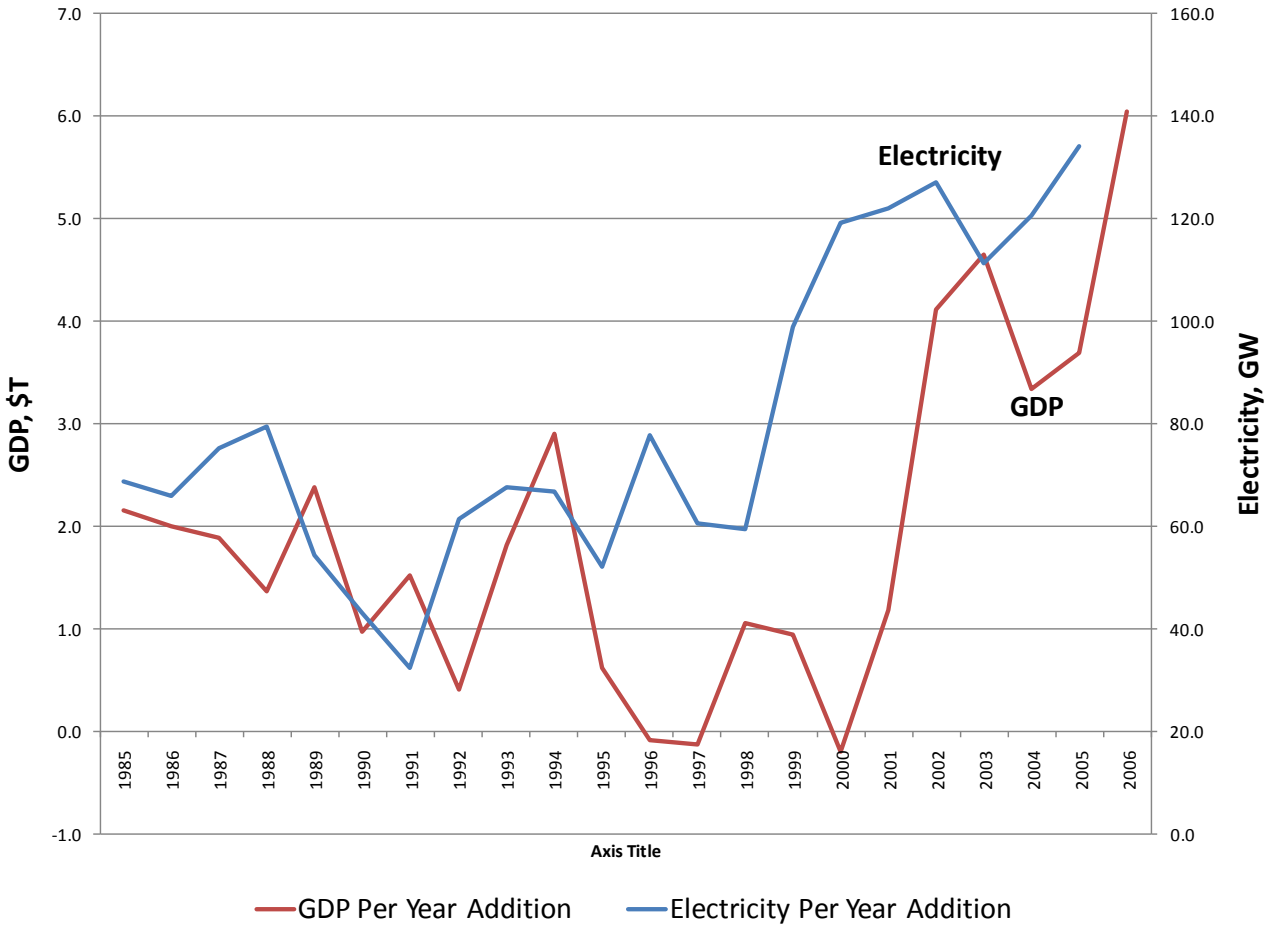
- John Doerr, Kleiner Perkins Caufield & Byers


World at Night (Electrification Level)
World Population Density


World at Night (Electrification Level)
1.6B people with no electricity
World Population Density

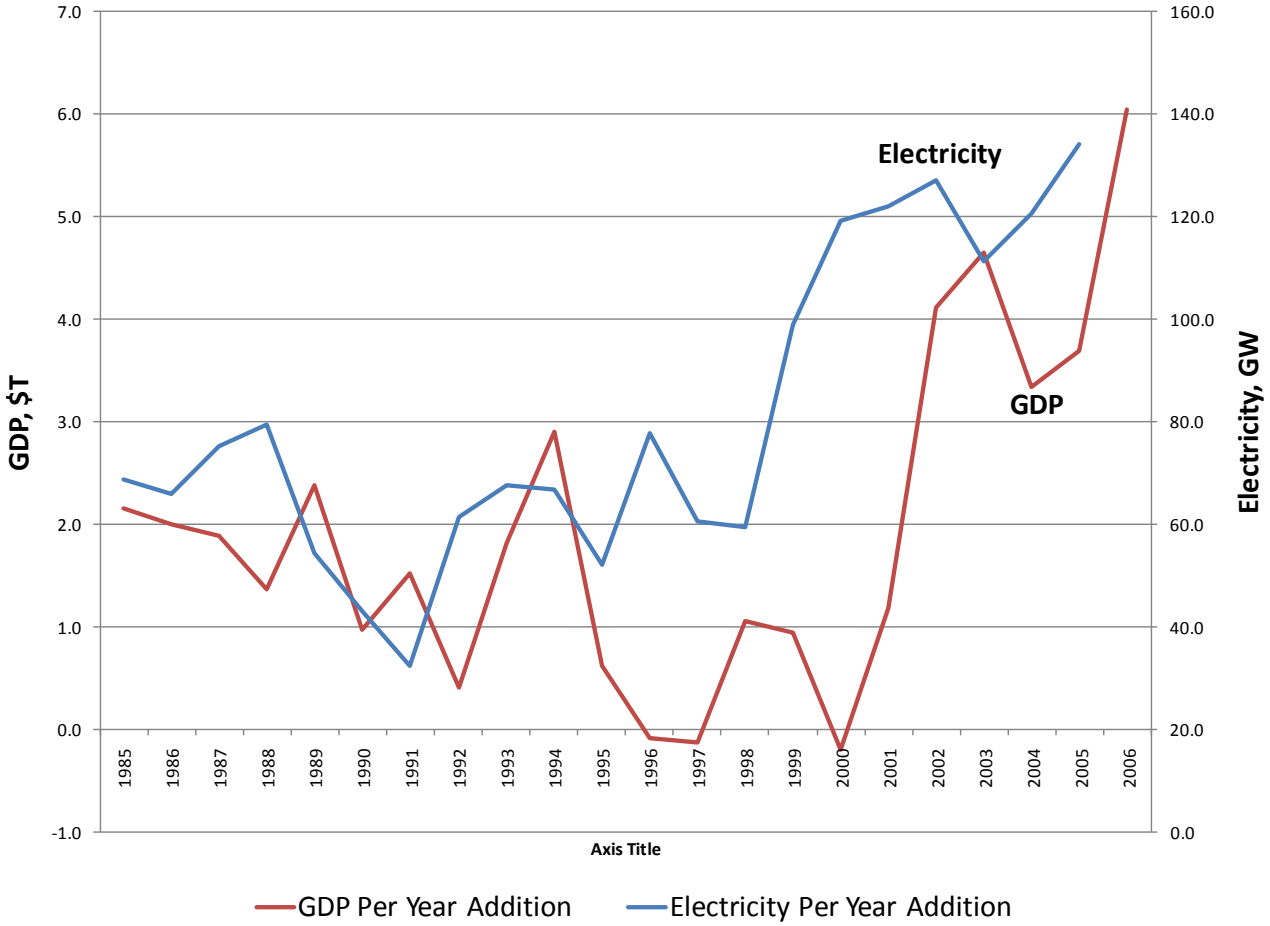

World at Night (Electrification Level)
“We’re going to need all the energy we can get”
World Population Density

Energy abundance causes economic growth



Sources: World Bank, U.S. Energy Information Administration

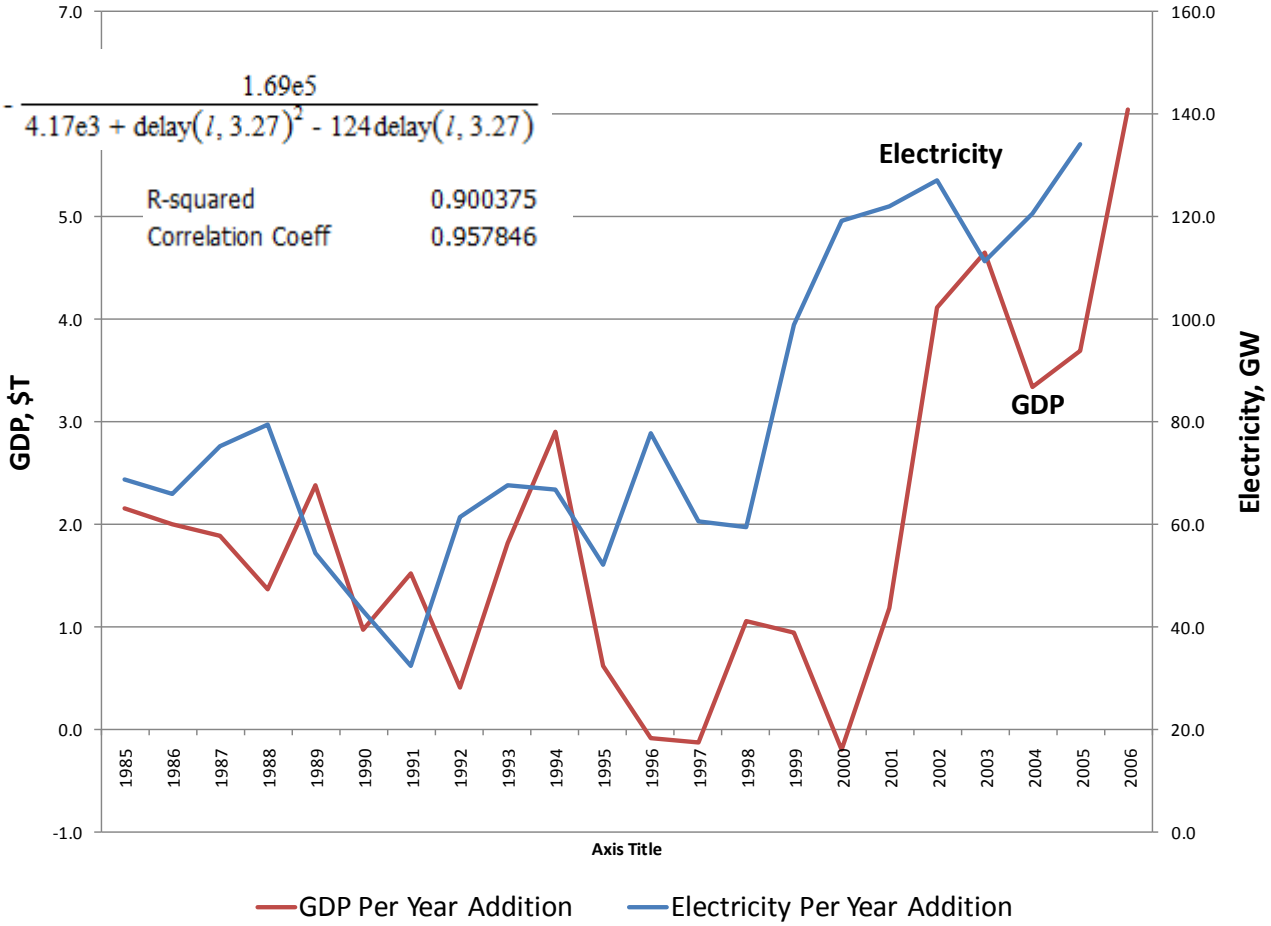
Energy abundance causes economic growth
Economic growth requires energy abundance



Sources: World Bank, U.S. Energy Information Administration

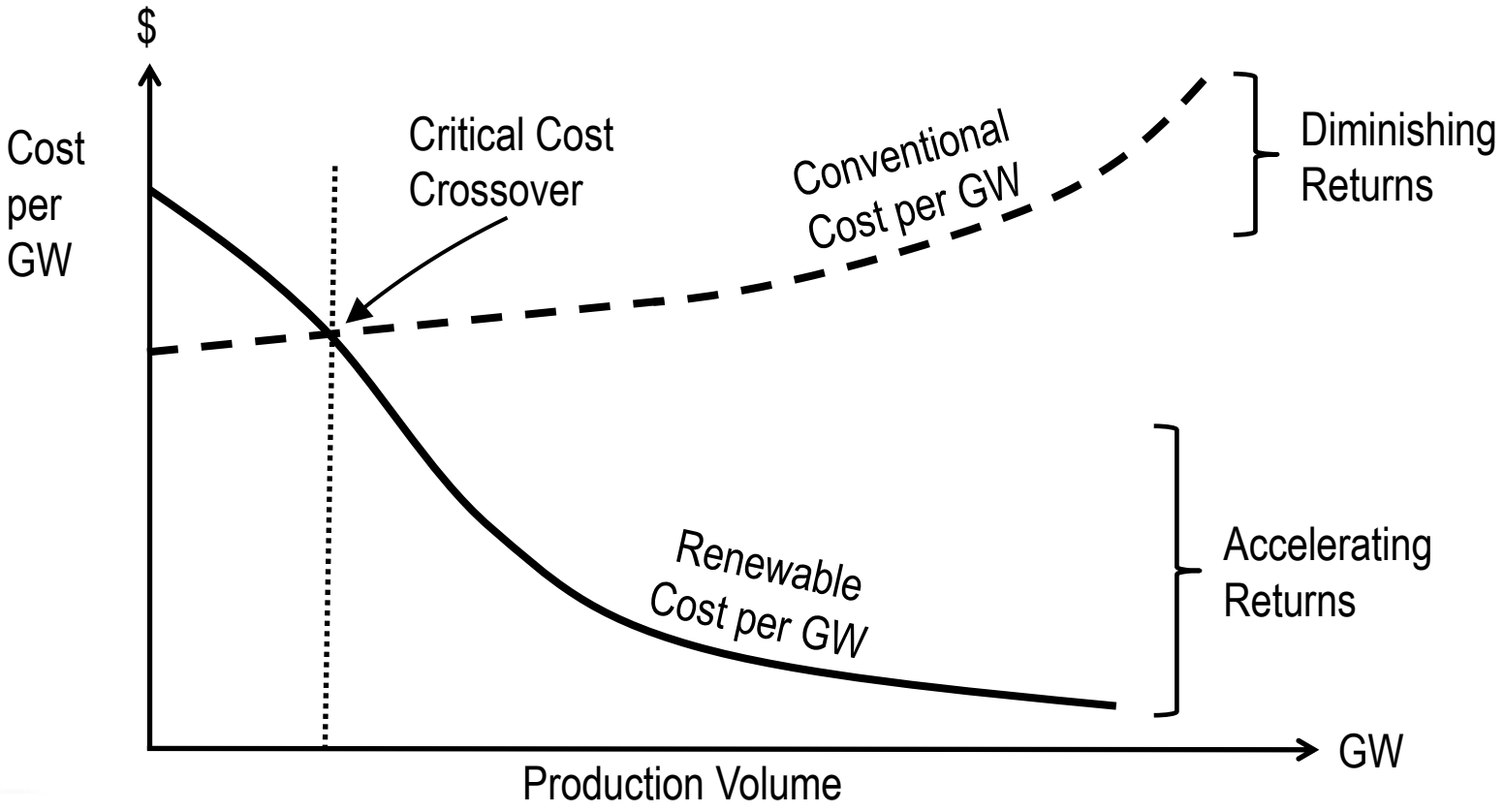
Energy abundance causes economic growth
Economic growth requires energy abundance

$$GDP = 521 - \frac{1.69e5}{4.17e3 + delay(I, 3.27)^2 - 124\,delay(I, 3.27)}$$

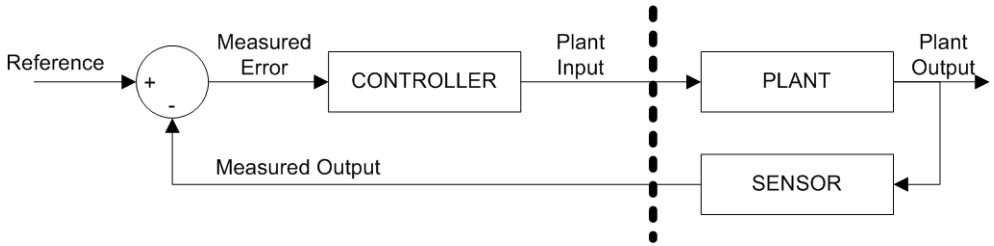


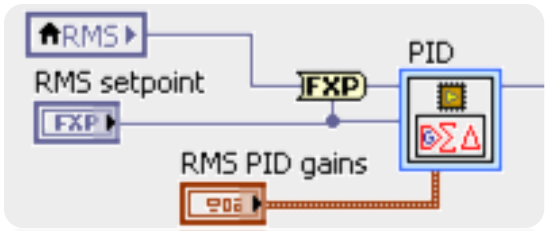
Sources: World Bank, U.S. Energy Information Administration

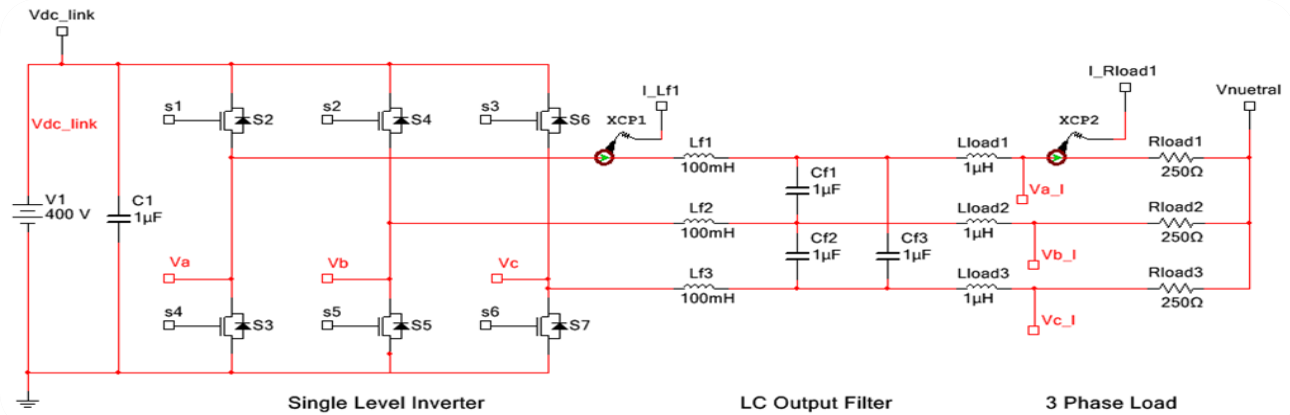
Renewable Returns



Read about "The Law of Renewable Returns"

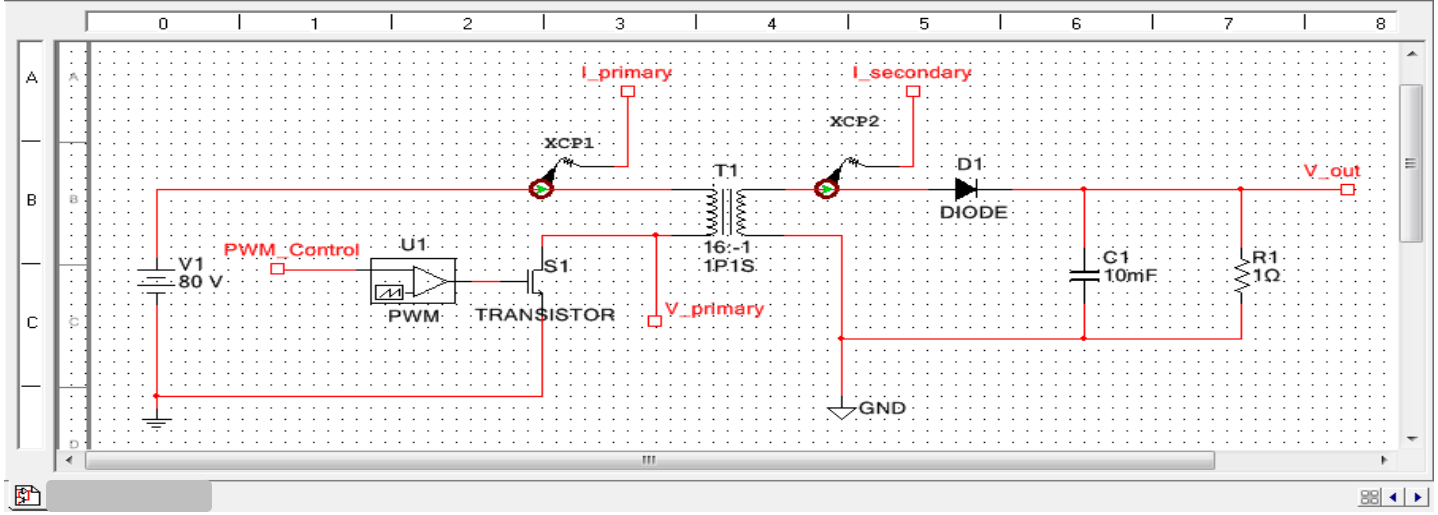


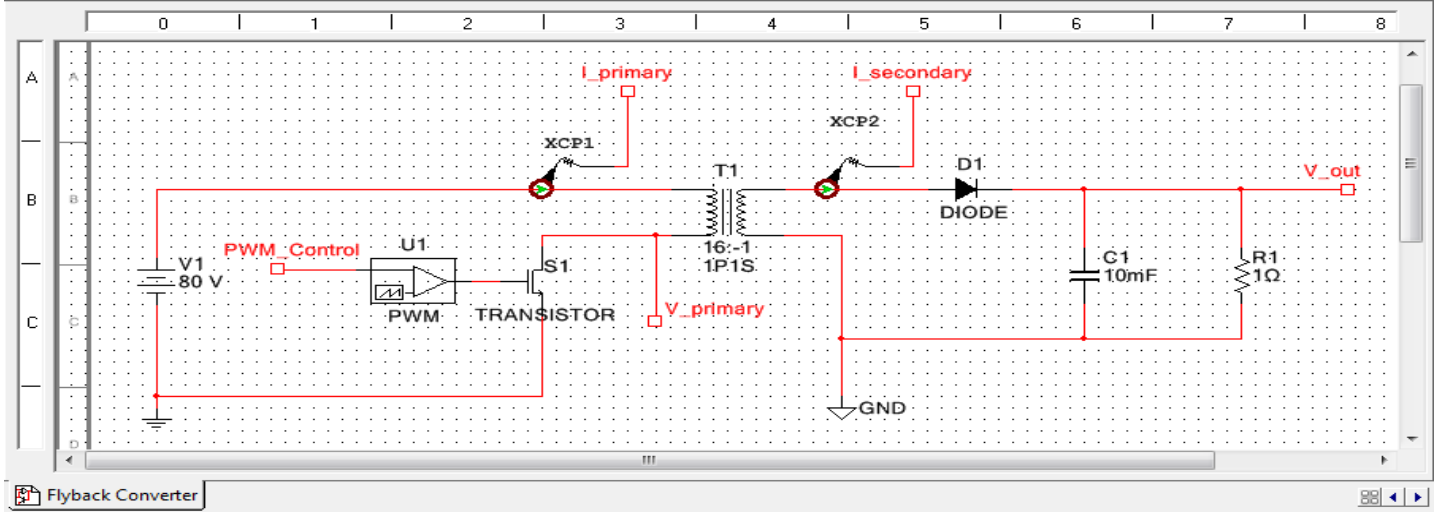




NATIONAL INSTRUMENTS

VARIABLE TIME-STEP GRAPHICAL CO-SIMULATION


I_primary
I_secondary
XCP1
XCP2
T1
D1
V_out
DIODE
V1
80 V
PWM_Control
U1
S1
16:-1
1P1S
C1
10mF
R1
1Ω
PWM
TRANSISTOR
V_primary
GND


I_primary
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XCP1
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80 V
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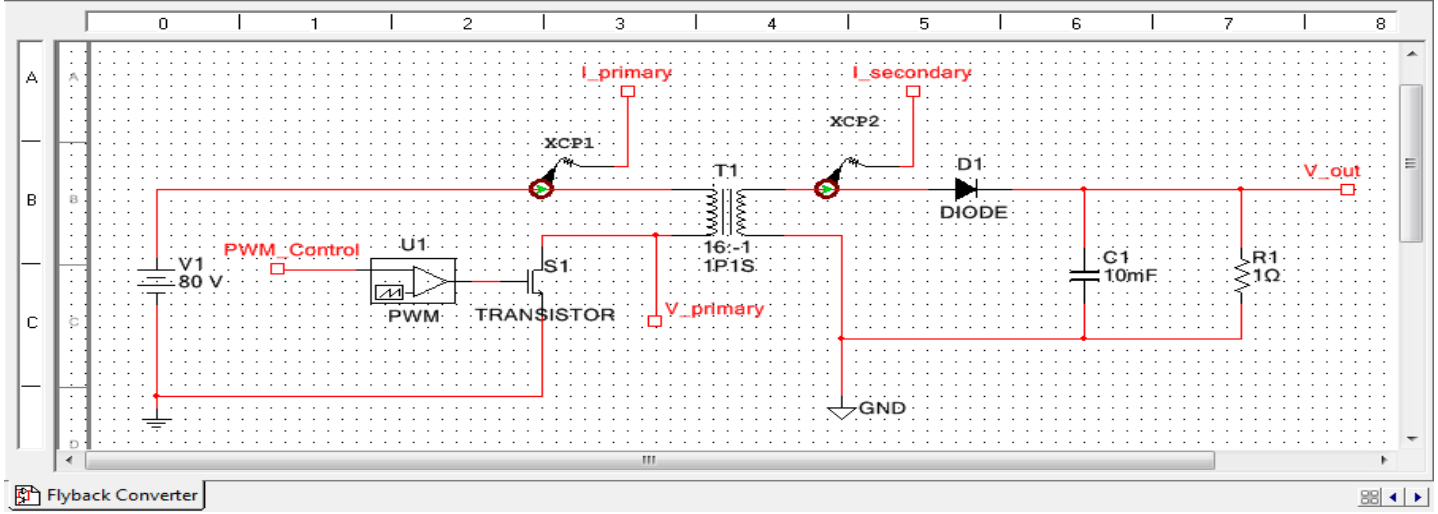
U1
S1
16:-1
1P1S
C1
10mF
R1
1Ω
PWM
TRANSISTOR
V_primary
GND
Flyback Converter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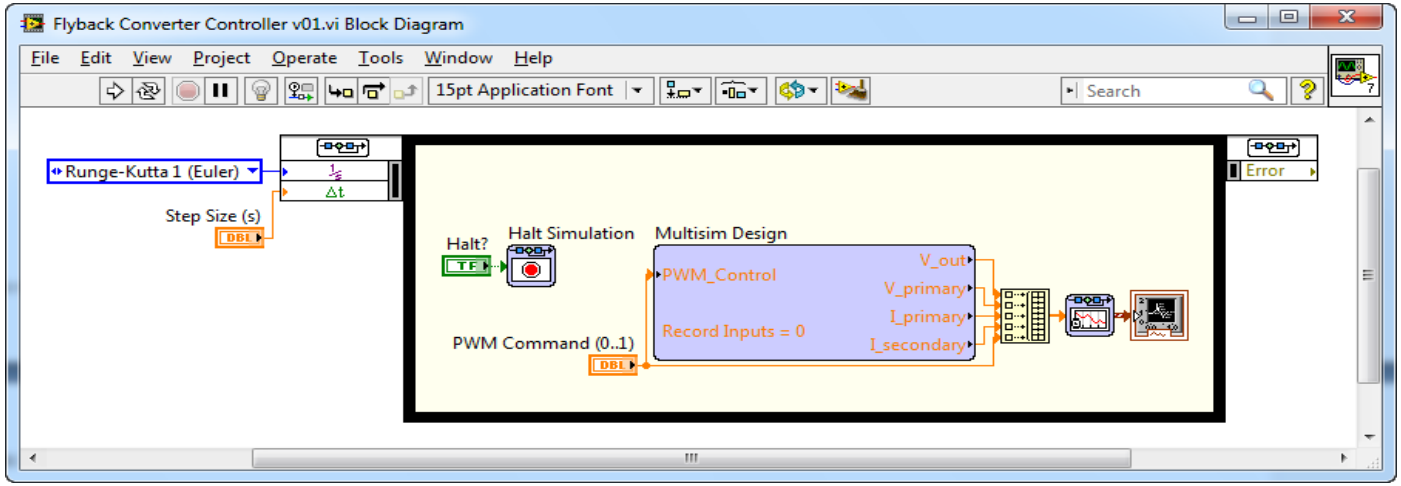
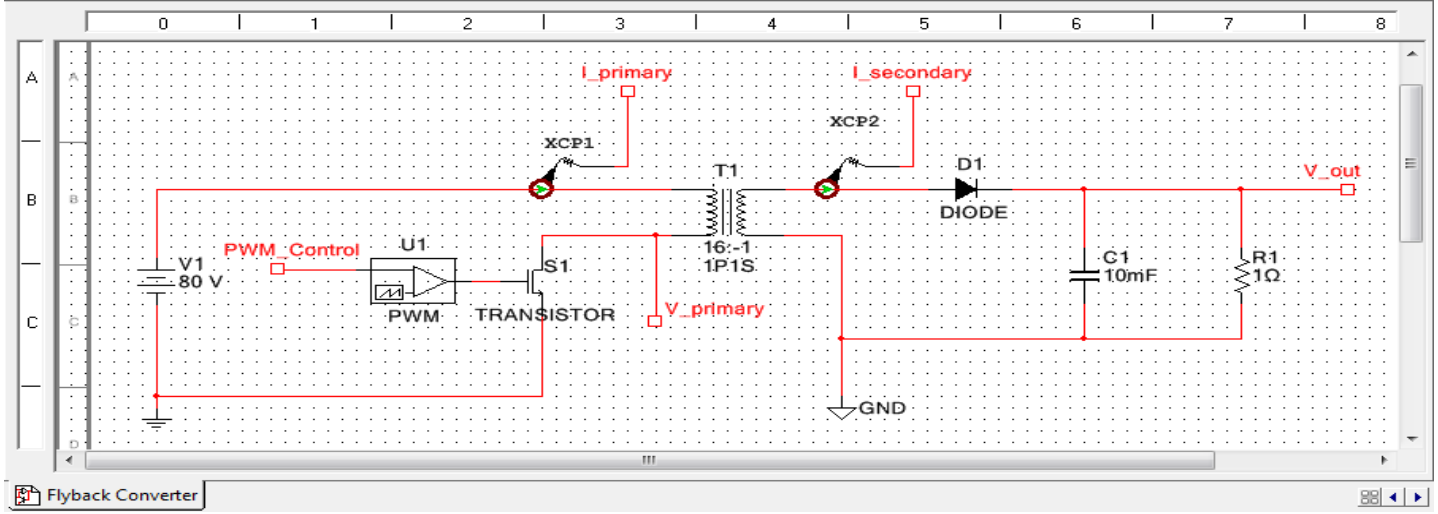
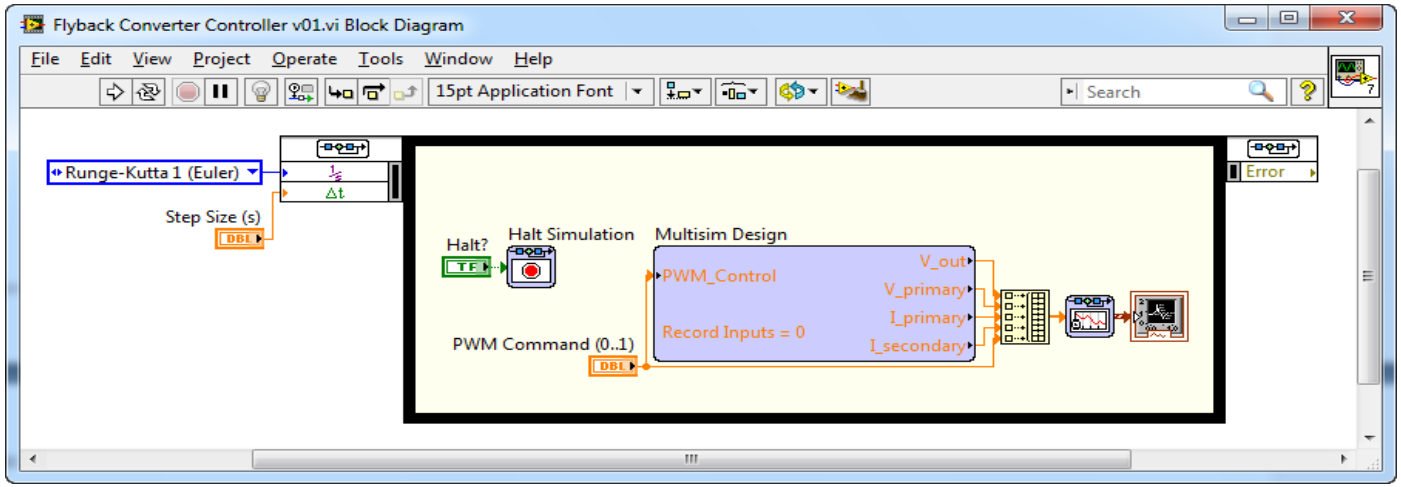

Flyback Converter Controller v01.vi Block Diagram
File Edit View Project Operate Tools Window Help
15pt Application Font
Search
Runge-Kutta 1 (Euler)
Step Size (s)
Halt?
Halt Simulation
Multisim Design
PWM_Control
Record Inputs = 0
V_out
V_primary
I_primary
I_secondary
PWM Command (0..1)
Error


I_primary
I_secondary
XCP1
XCP2
T1
D1
DIODE
V_out
PWM_Control
U1
V1
80 V
S1
16:-1
1P1S
C1
10mF
R1
1Ω
PWM
TRANSISTOR
V_primary
GND
Flyback Converter


Flyback Converter Controller v01.vi Block Diagram
File Edit View Project Operate Tools Window Help
15pt Application Font
Search
Runge-Kutta 1 (Euler)
Step Size (s)
Halt?
Halt Simulation
Multisim Design
PWM_Control
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V_out
V_primary
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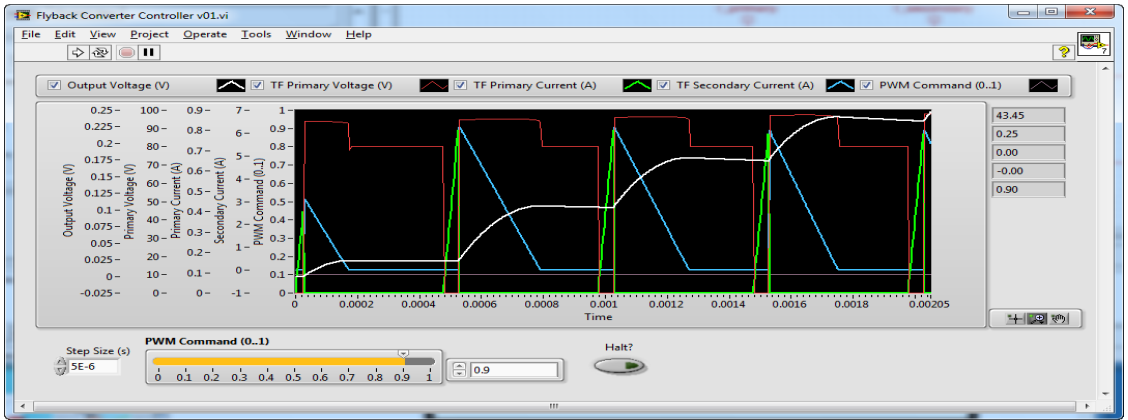
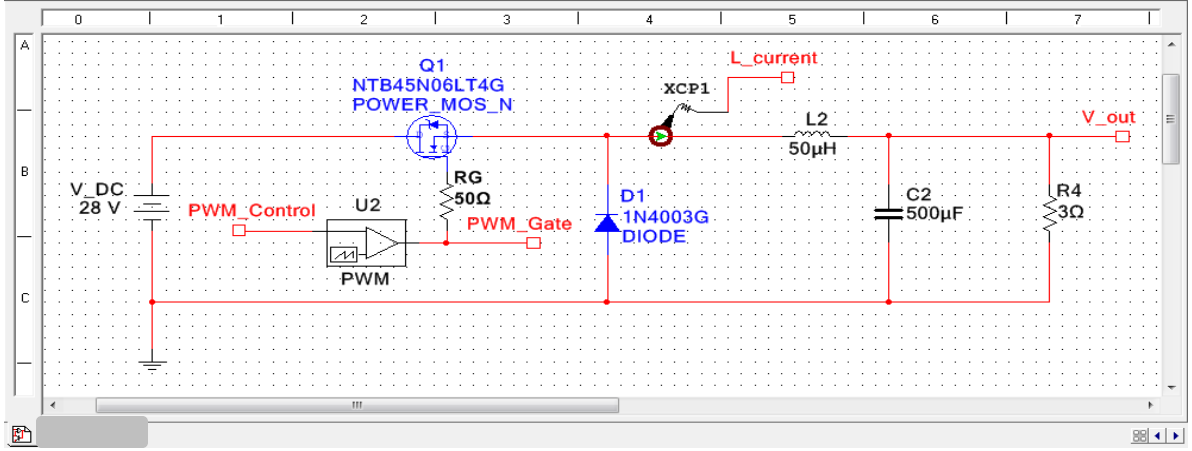
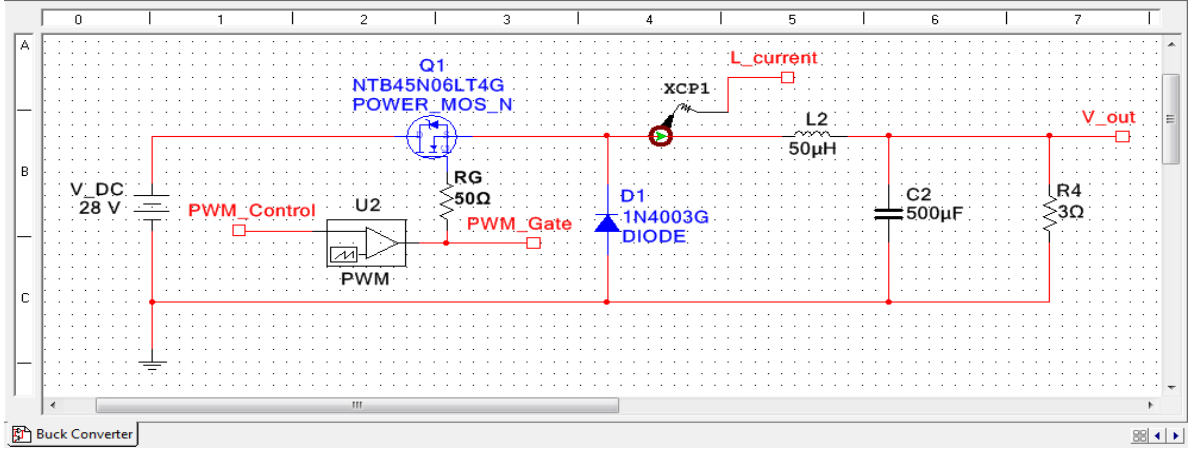
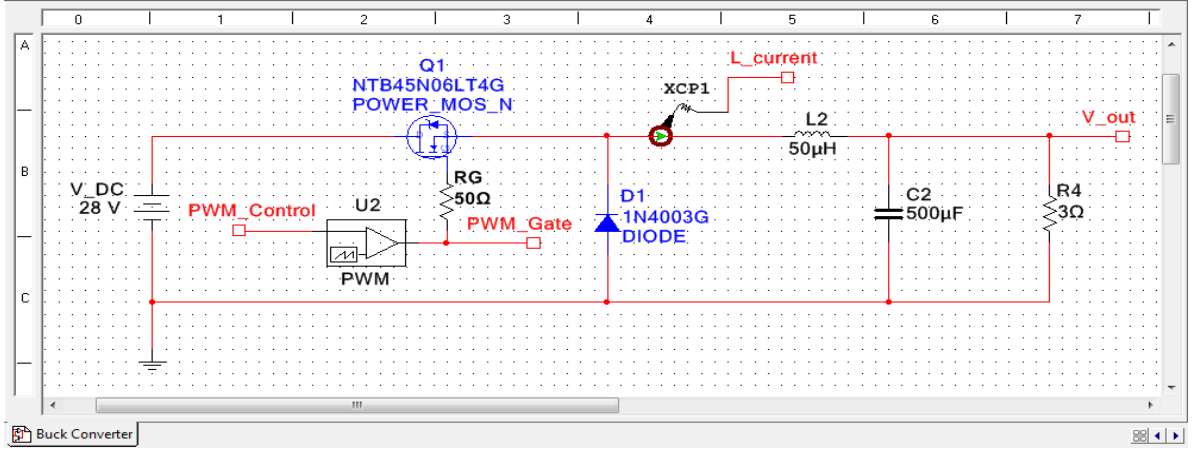
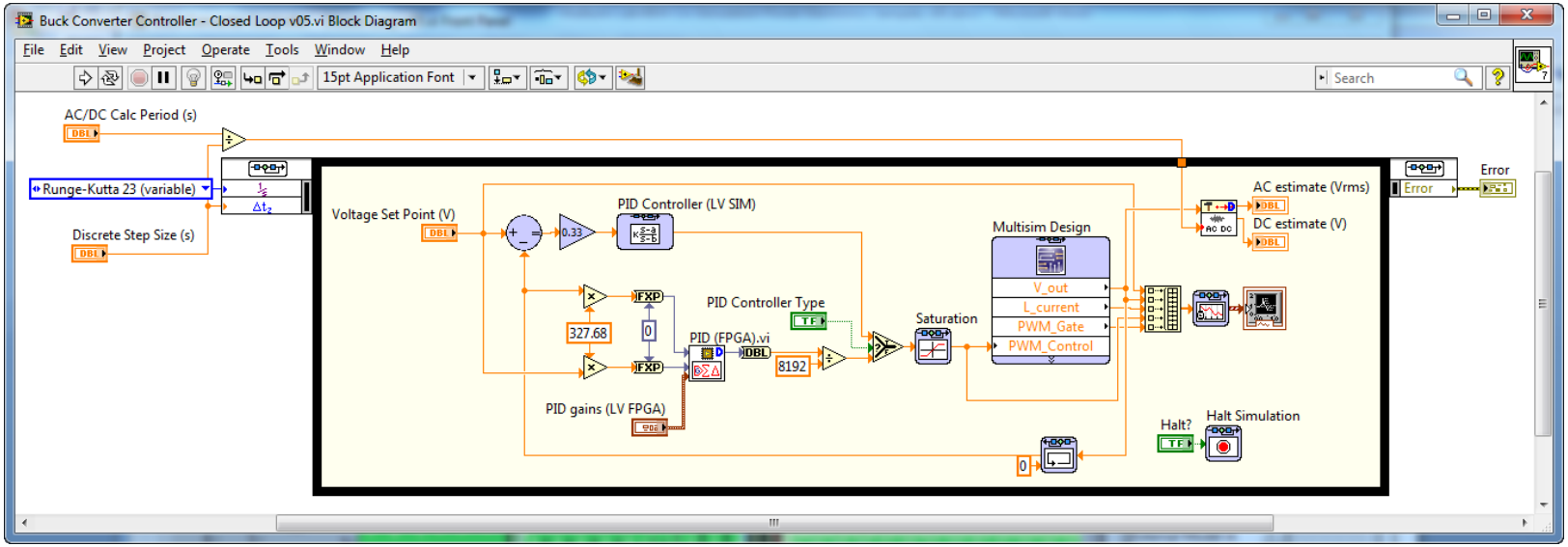
Error

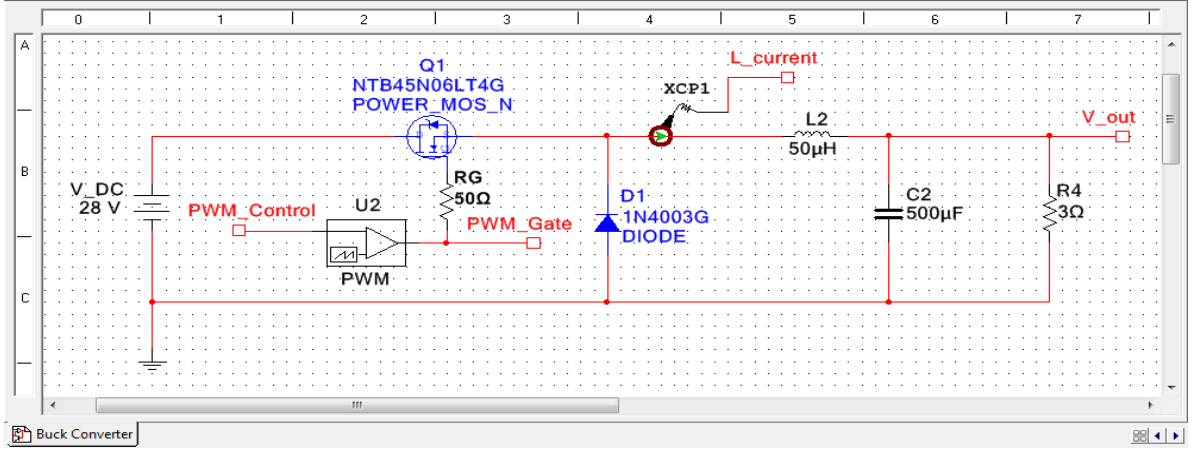

Flyback Converter Controller v01.vi
File Edit View Project Operate Tools Window Help
Output Voltage (V)
TF Primary Voltage (V)
TF Primary Current (A)
TF Secondary Current (A)
PWM Command (0..1)
Time
Step Size (s)
PWM Command (0..1)
Halt?

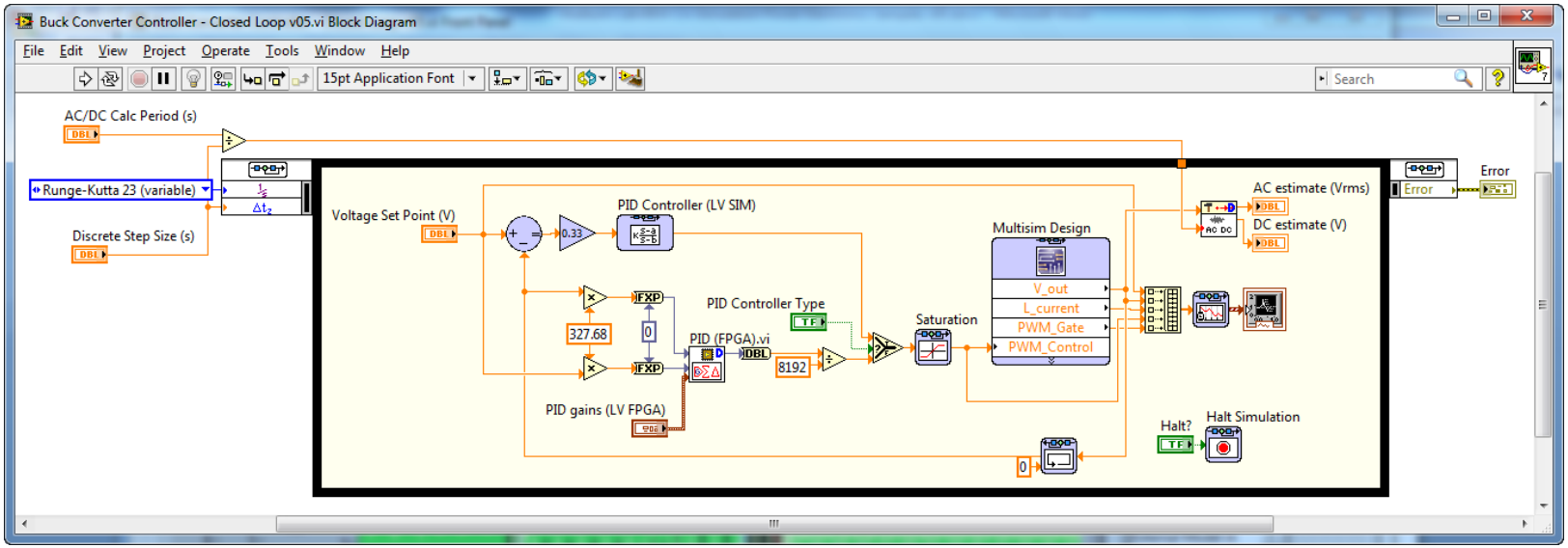

Q1
NTB45N06LT4G
POWER_MOS_N
L_current
XCP1
L2
50µH
V_out
RG
50Ω
V_DC
28 V
PWM_Control
U2
PWM_Gate
D1
1N4003G
DIODE
C2
500µF
R4
3Ω
PWM


Q1
NTB45N06LT4G
POWER_MOS_N
XCP1
L_current
L2
50µH
V_out
RG
50Ω
V_DC
28 V
PWM_Control
U2
PWM_Gate
D1
1N4003G
DIODE
C2
500µF
R4
3Ω
PWM
Buck Converter


Q1
NTB45N06LT4G
POWER_MOS_N
XCP1
L_current
L2
50µH
V_out
RG
50Ω
V_DC
28 V
PWM_Control
U2
PWM_Gate
D1
1N4003G
DIODE
C2
500µF
R4
3Ω
PWM
Buck Converter


Buck Converter Controller - Closed Loop v05.vi Block Diagram
File Edit View Project Operate Tools Window Help
15pt Application Font
Search
AC/DC Calc Period (s)
Runge-Kutta 23 (variable)
Discrete Step Size (s)
Voltage Set Point (V)
0.33
PID Controller (LV SIM)
327.68
PID Controller Type
PID (FPGA).vi
8192
PID gains (LV FPGA)
Saturation
Multisim Design
V_out
L_current
PWM_Gate
PWM_Control
AC estimate (Vrms)
DC estimate (V)
Error
Halt?
Halt Simulation


Q1
NTB45N06LT4G
POWER_MOS_N
XCP1
L_current
L2
50µH
V_out
RG
50Ω
V_DC
28 V
PWM_Control
U2
PWM_Gate
D1
1N4003G
DIODE
C2
500µF
R4
3Ω
PWM
Buck Converter


Buck Converter Controller - Closed Loop v05.vi Block Diagram
File Edit View Project Operate Tools Window Help
15pt Application Font
Search
AC/DC Calc Period (s)
Runge-Kutta 23 (variable)
Discrete Step Size (s)
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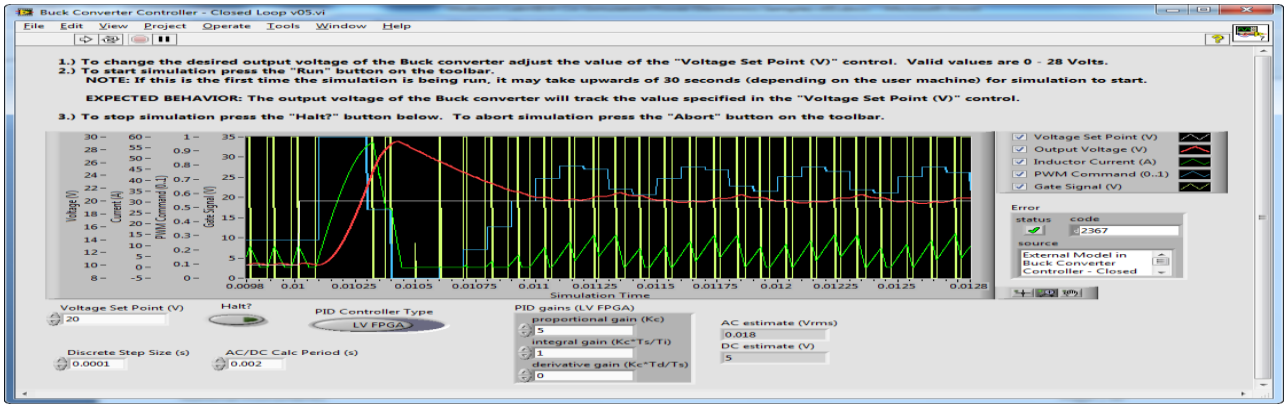
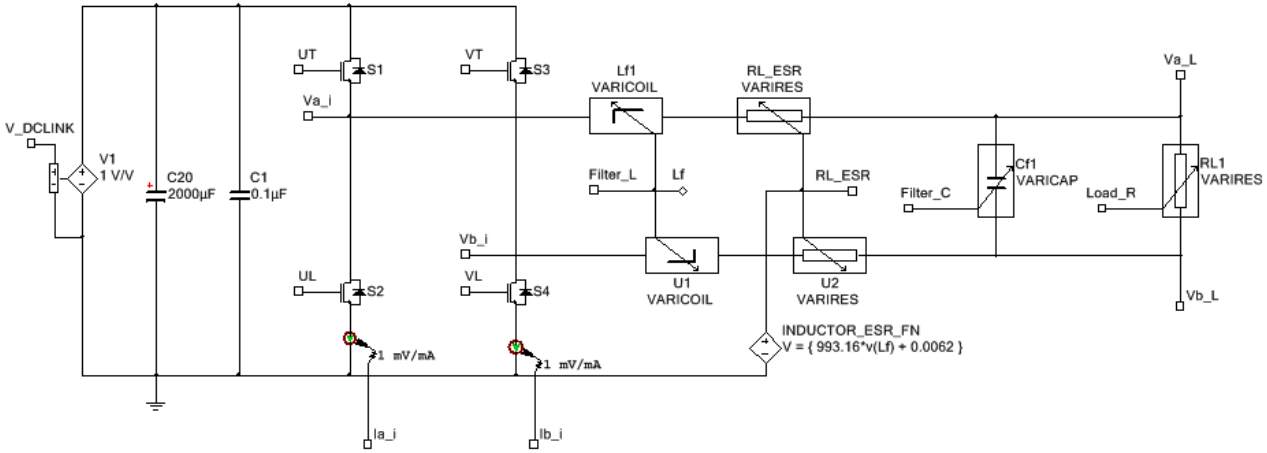
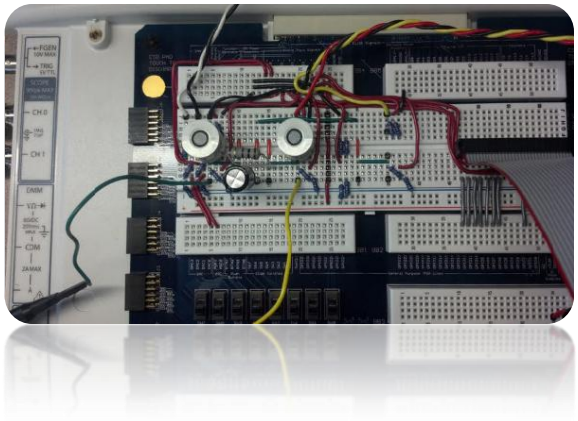
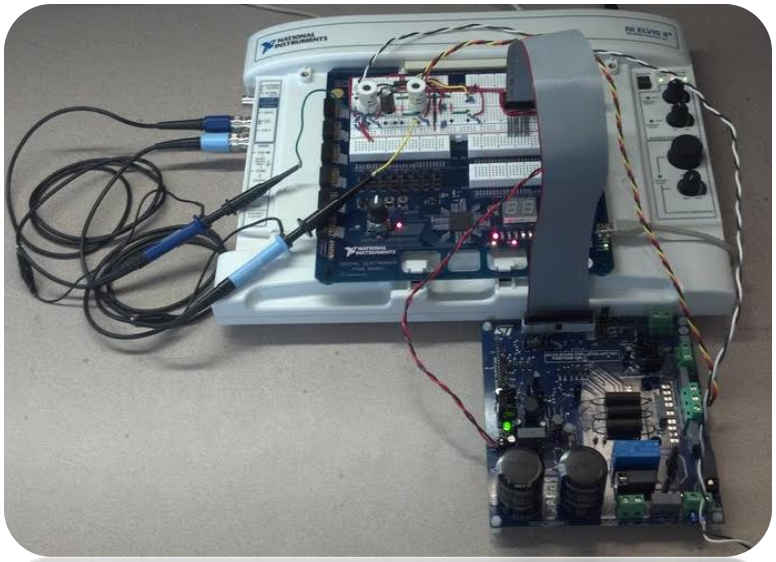
0.33
PID Controller (LV SIM)
327.68
PID Controller Type
PID (FPGA).vi
8192
PID gains (LV FPGA)
Saturation
Multisim Design
V_out
L_current
PWM_Gate
PWM_Control
AC estimate (Vrms)
DC estimate (V)
Error
Halt?
Halt Simulation

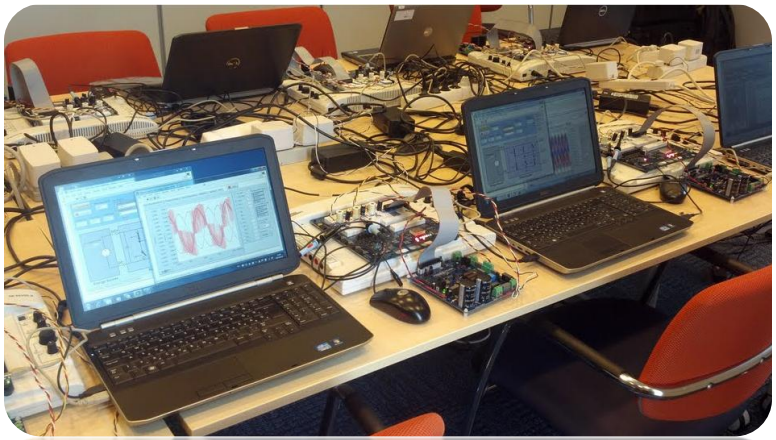

Buck Converter Controller - Closed Loop v05.vi
File Edit View Project Operate Tools Window Help
1.) To change the desired output voltage of the Buck converter adjust the value of the "Voltage Set Point (V)" control. Valid values are 0 - 28 Volts.
2.) To start simulation press the "Run" button on the toolbar.
NOTE: If this is the first time the simulation is being run, it may take upwards of 30 seconds (depending on the user machine) for simulation to start.
EXPECTED BEHAVIOR: The output voltage of the Buck converter will track the value specified in the "Voltage Set Point (V)" control.
3.) To stop simulation press the "Halt?" button below. To abort simulation press the "Abort" button on the toolbar.
Simulation Time
Voltage Set Point (V)
Output Voltage (V)
Inductor Current (A)
PWM Command (0..1)
Gate Signal (V)
Error
status
code
source
External Model in Buck Converter Controller - Closed
Voltage Set Point (V)
Halt?
PID Controller Type
LV FPGA
PID gains (LV FPGA)
proportional gain (Kc)
integral gain (Kc*Ts/Ti)
derivative gain (Kc*Td/Ts)
AC estimate (Vrms)
DC estimate (V)
Discrete Step Size (s)
AC/DC Calc Period (s)

H Bridge Single Phase Inverter: Co-Simulation vs. Physical Measurements

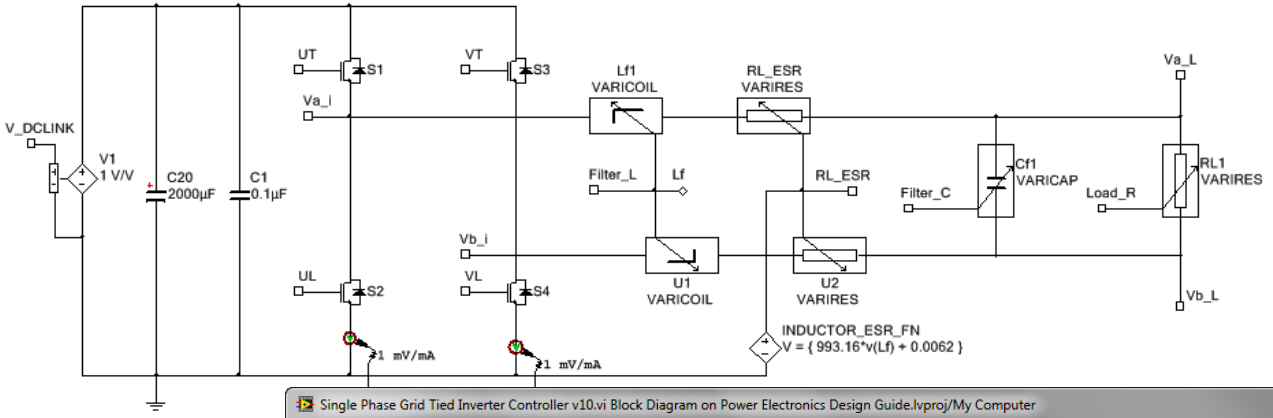


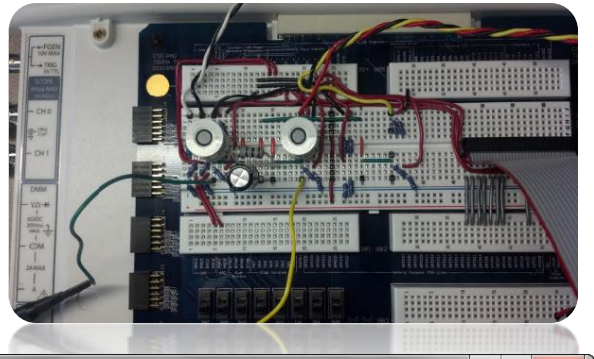


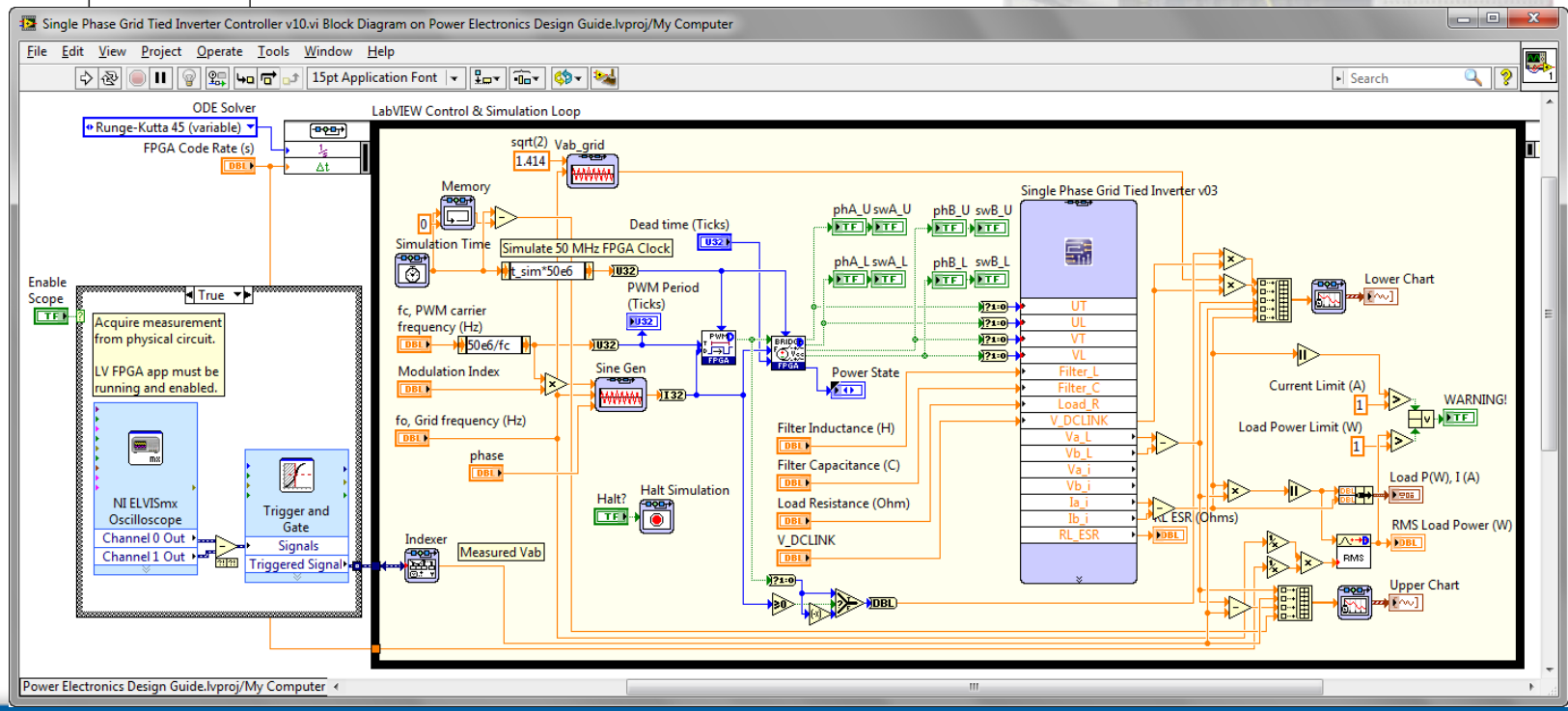




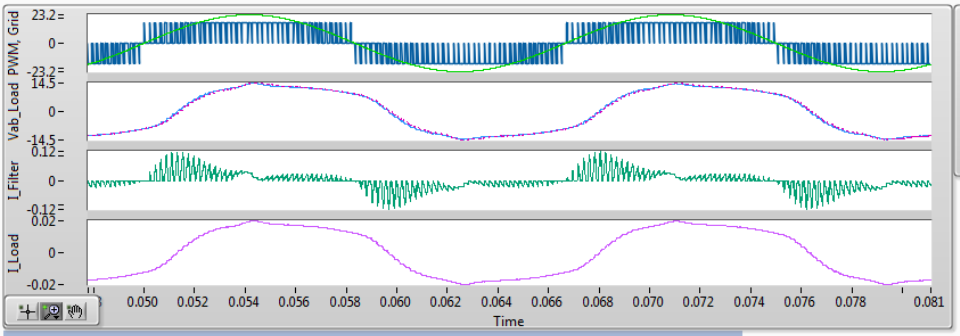
H Bridge Single Phase Inverter: Co-Simulation vs. Physical Measurements







H Bridge Single Phase Inverter: Co-Simulation vs. Physical Measurements



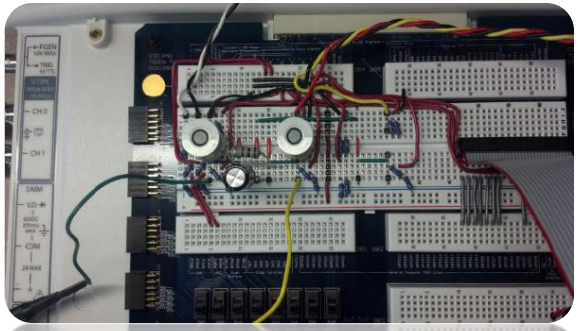
PWM_cosim
Vab_grid_cosim (V)
Vab_Load_cosim (V)
Vab_Load_measured (V)
I_filter_cosim (A)
I_load_cosim (A)

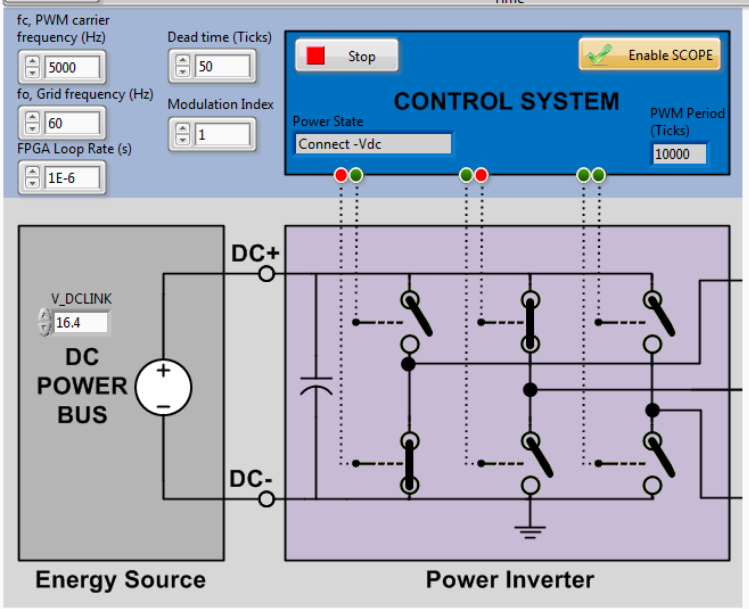
Available Capacitor Values (bi-polar):
0.1 uF
1 uF
4.7 uF
10 uF
100 uF
470 uF

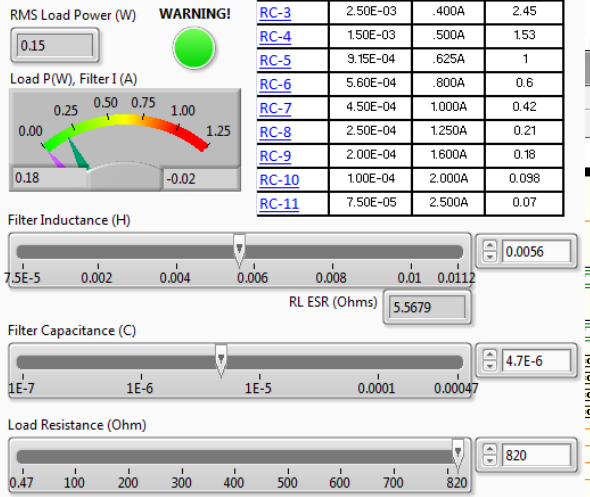
Available Resistor Values (1 W):
0.47 to 7.5 kOhm

Available Inductor Values:

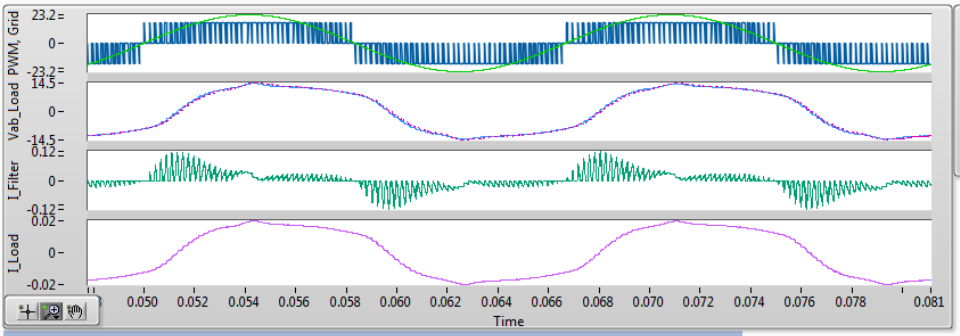
Type No.	Inductance	DC Rated Current	± 15% DC Resistance Ohms
RC-1	5.60E-03	.250A	6.1
RC-2	3.90E-03	.320A	3.9
RC-3	2.50E-03	.400A	2.45
RC-4	1.50E-03	.500A	1.53
RC-5	9.15E-04	.625A	1
RC-6	5.60E-04	.800A	0.6
RC-7	4.50E-04	1.000A	0.42
RC-8	2.50E-04	1.250A	0.21
RC-9	2.00E-04	1.600A	0.18
RC-10	1.00E-04	2.000A	0.098
RC-11	7.50E-05	2.500A	0.07







H Bridge Single Phase Inverter: Co-Simulation vs. Physical Measurements



PWM_cosim
Vab_grid_cosim (V)
Vab_Load_cosim (V)
Vab_Load_measured (V)
I_filter_cosim (A)
I_load_cosim (A)

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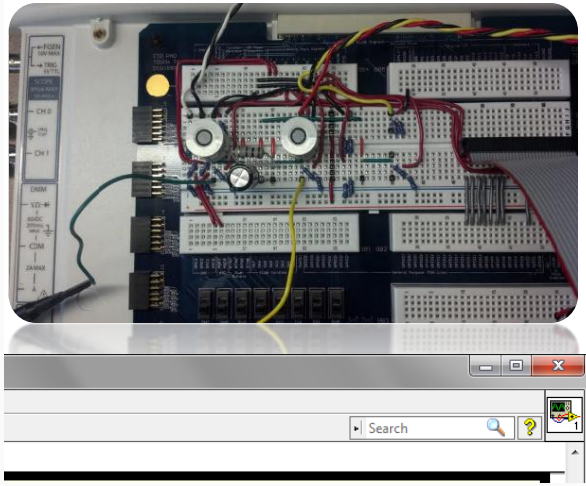
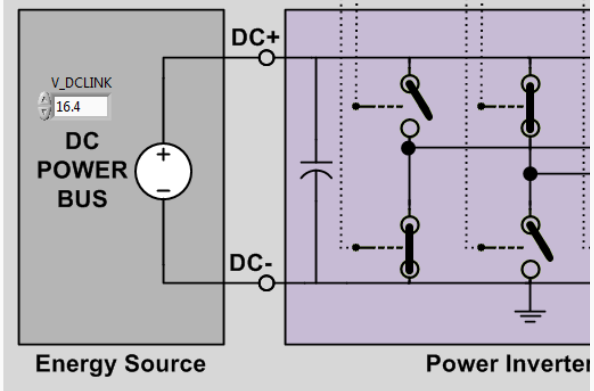
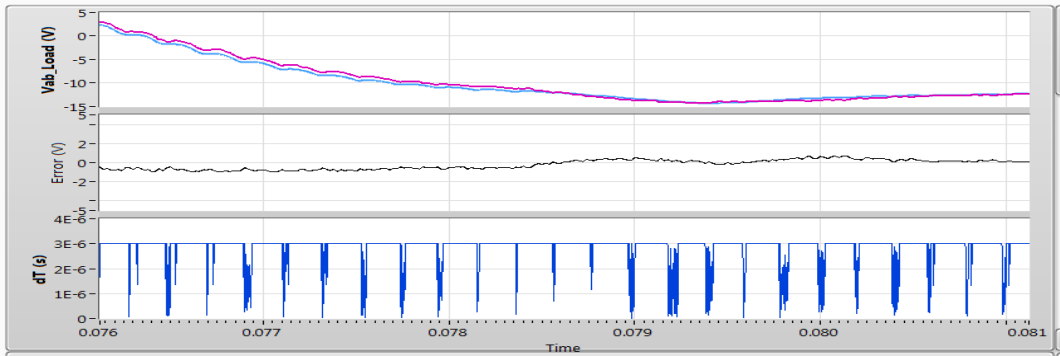
RC-5	9.15E-04	.625A	1
RC-6	5.60E-04	.800A	0.6
RC-7	4.50E-04	1.000A	0.42
RC-8	2.50E-04	1.250A	0.21
RC-9	2.00E-04	1.600A	0.18

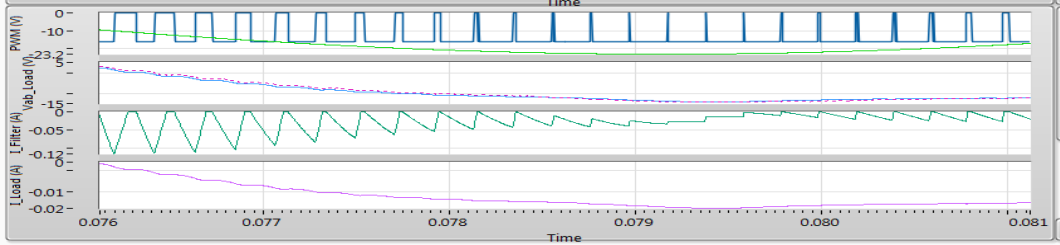


fc, PWM carrier frequency (Hz): 5000
Dead time (Ticks): 50
fo, Grid frequency (Hz): 60
Modulation Index: 1
FPGA Loop Rate (s): 1E-6
Stop
Enable SCOPE
CONTROL SYSTEM
Power State: Connect -Vdc
PWM Period (Ticks): 10000
RMS Load Power (W): 0.15
WARNING!
Load P(W), Filter I (A)

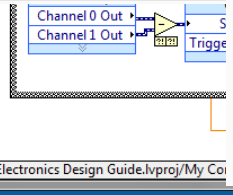




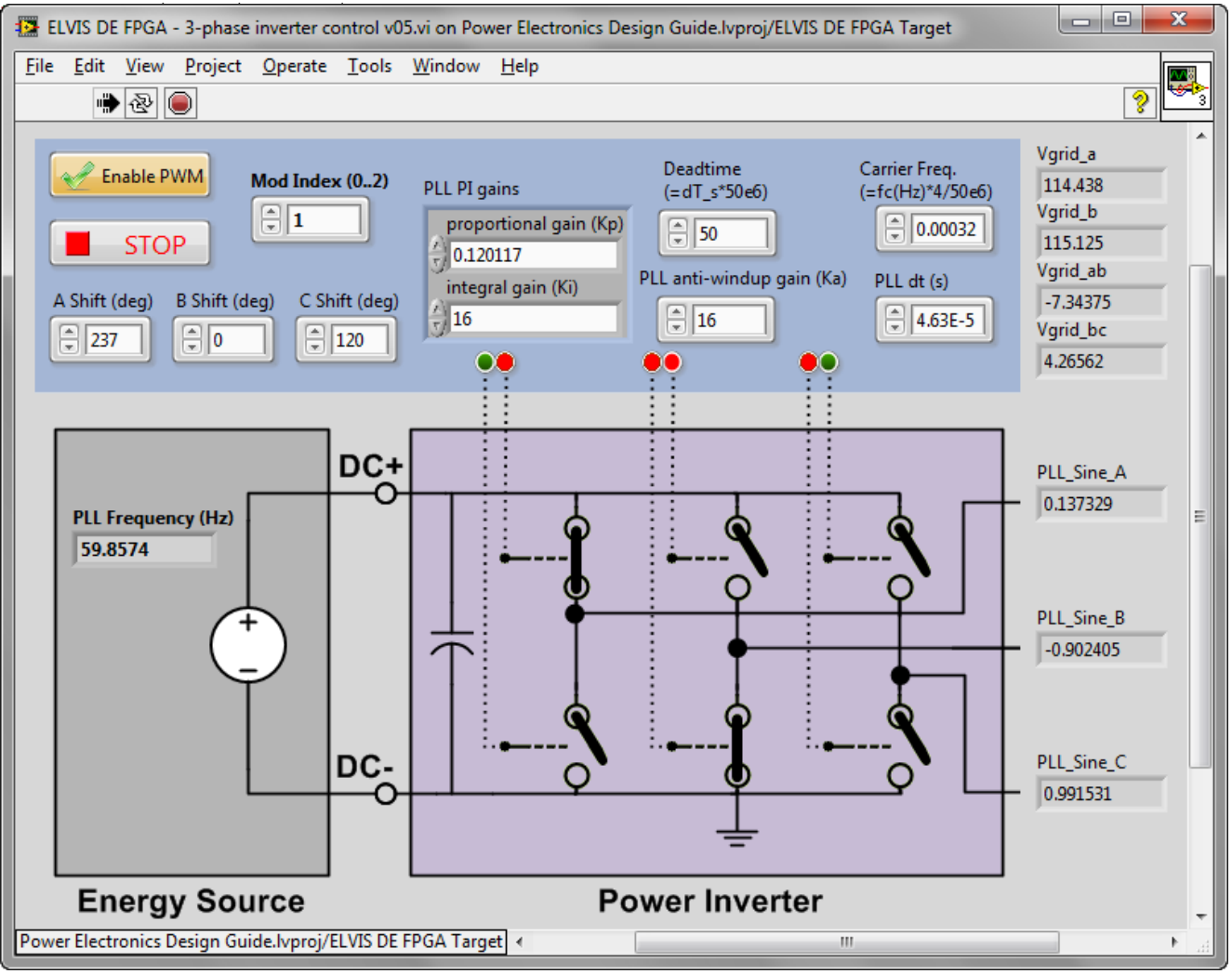
Vab_Load_cosim (V)
Vab_Load_measured (V)
Error (Cosim.-Meas.) (V)
Cosim. Timestep (s)

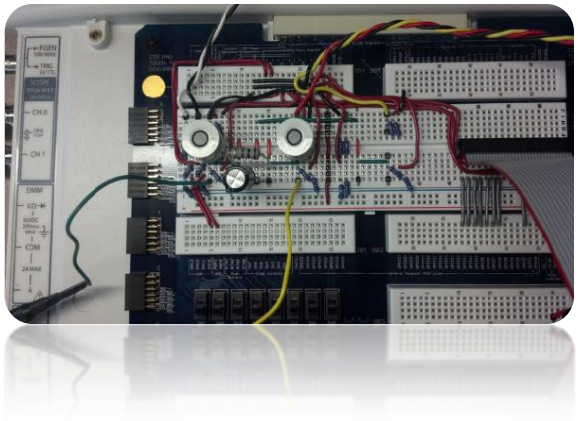


PWM_cosim
Vab_grid_cosim (V)
Vab_Load_cosim (V)
Vab_Load_measured (V)
I_filter_cosim (A)
I_load_cosim (A)



H Bridge Single Phase Inverter: Co-Simulation vs. Physical Measurements





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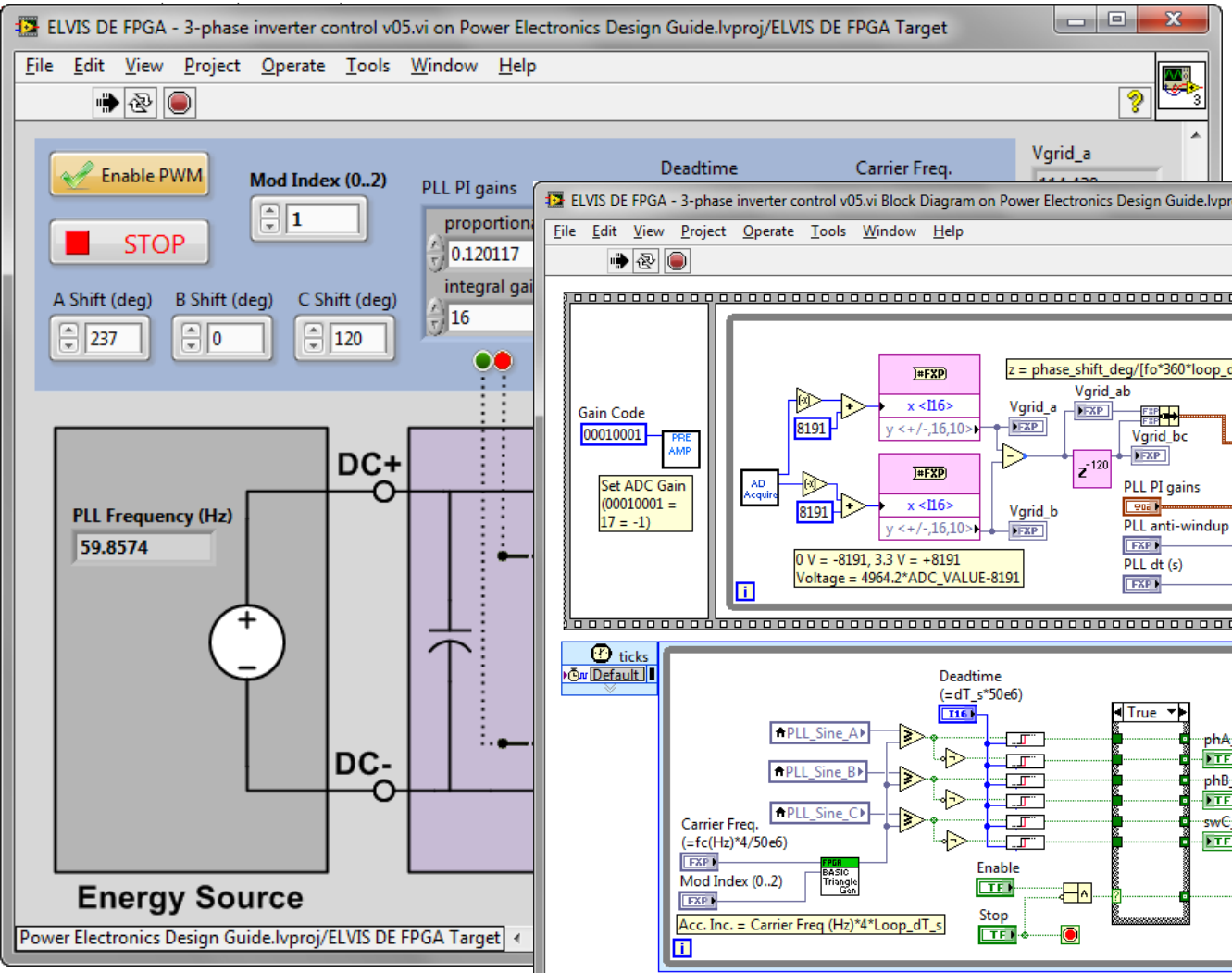
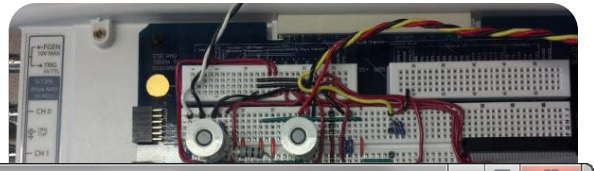
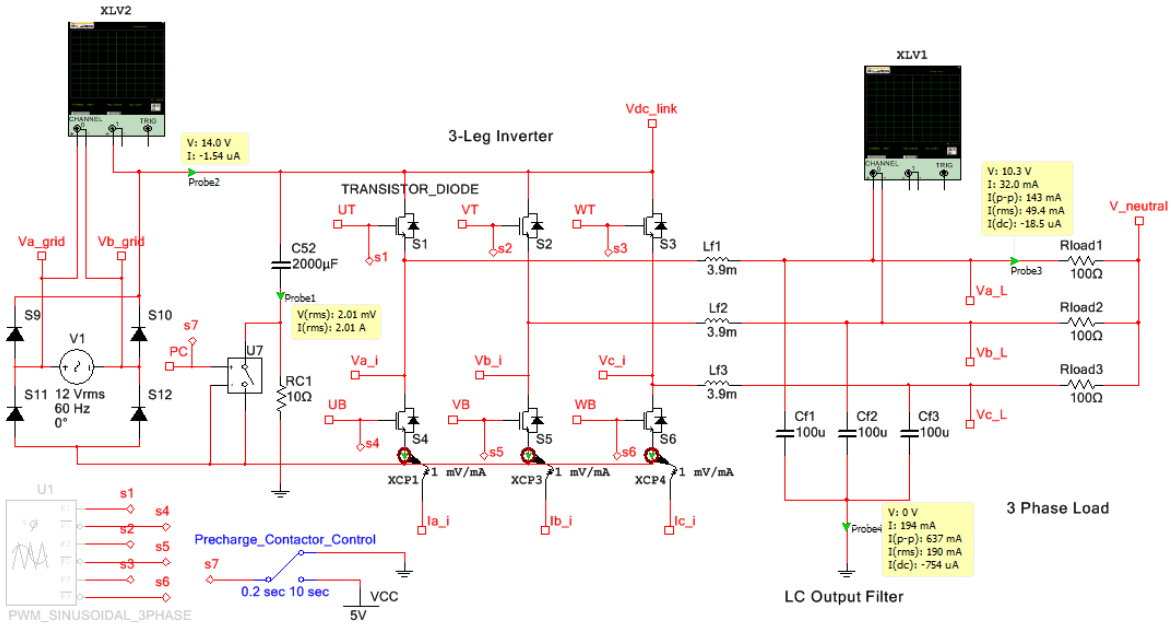
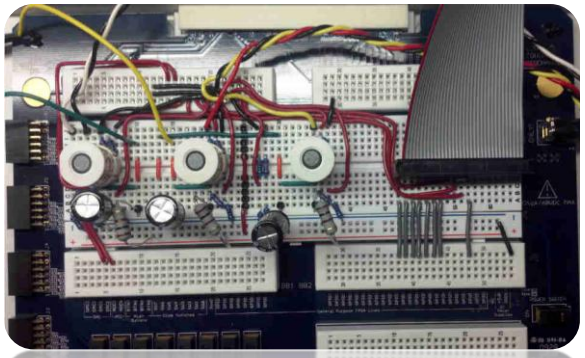
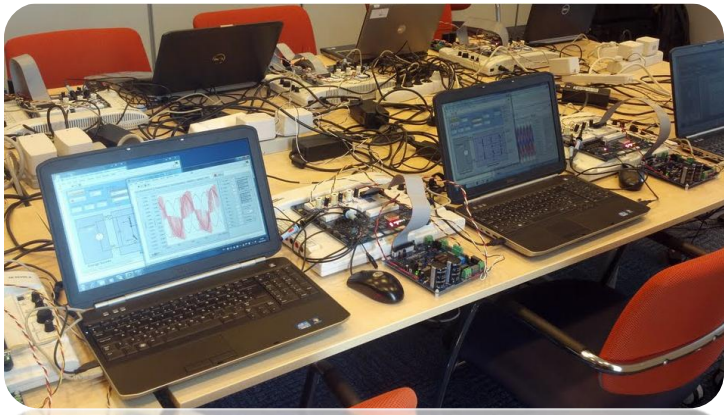


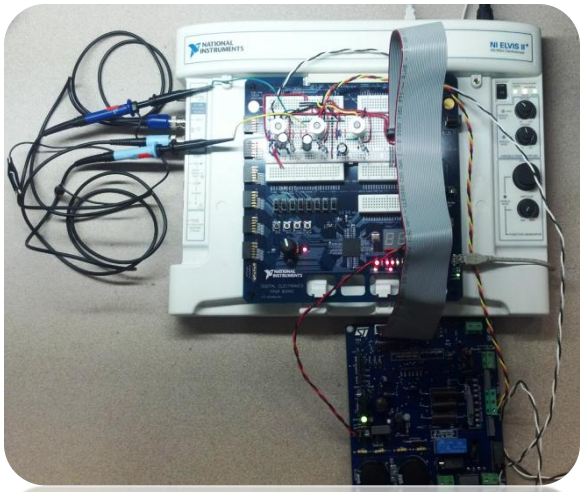


Three Phase Inverter: Co-Simulation vs. Physical Measurements

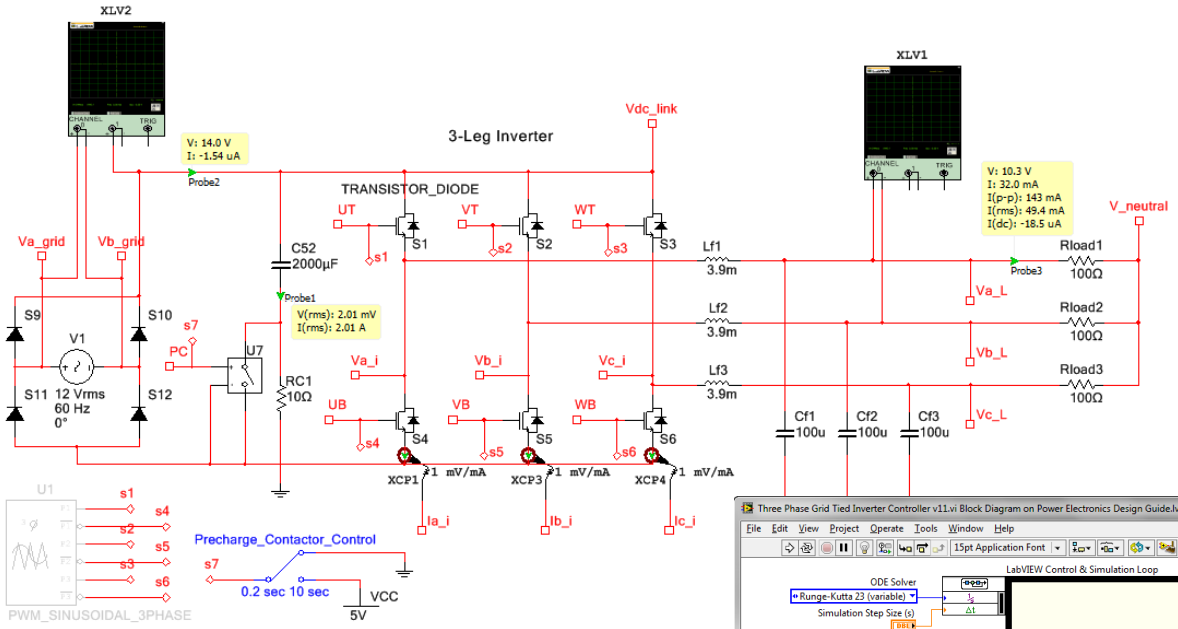


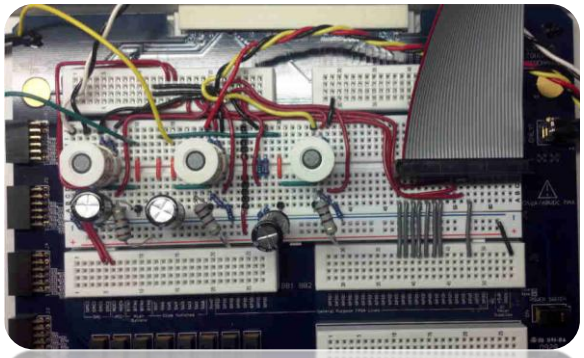


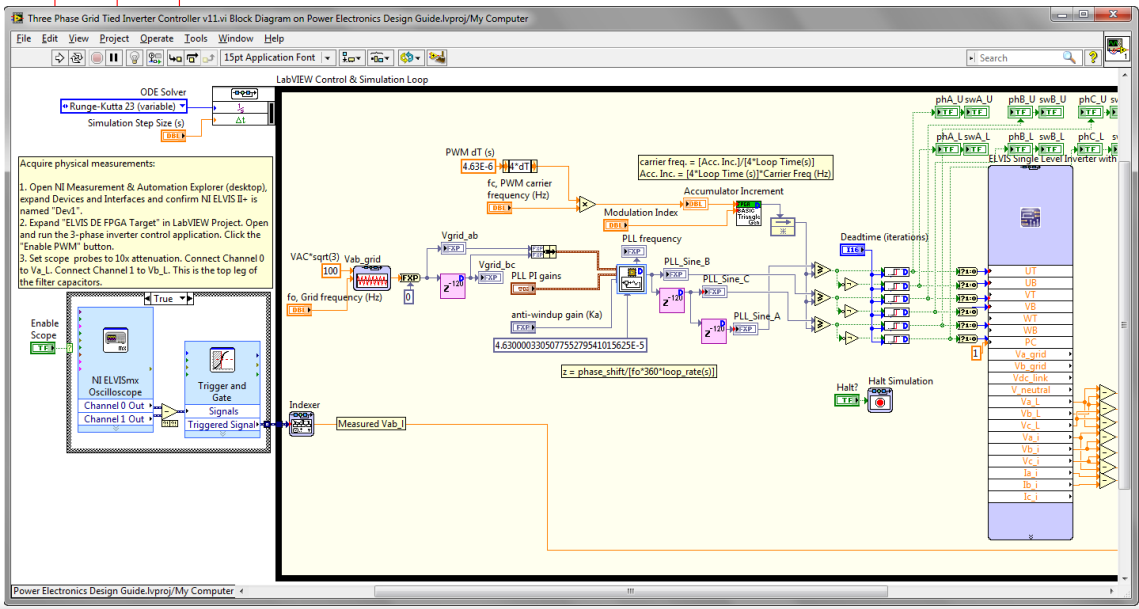




Three Phase Inverter: Co-Simulation vs. Physical Measurements

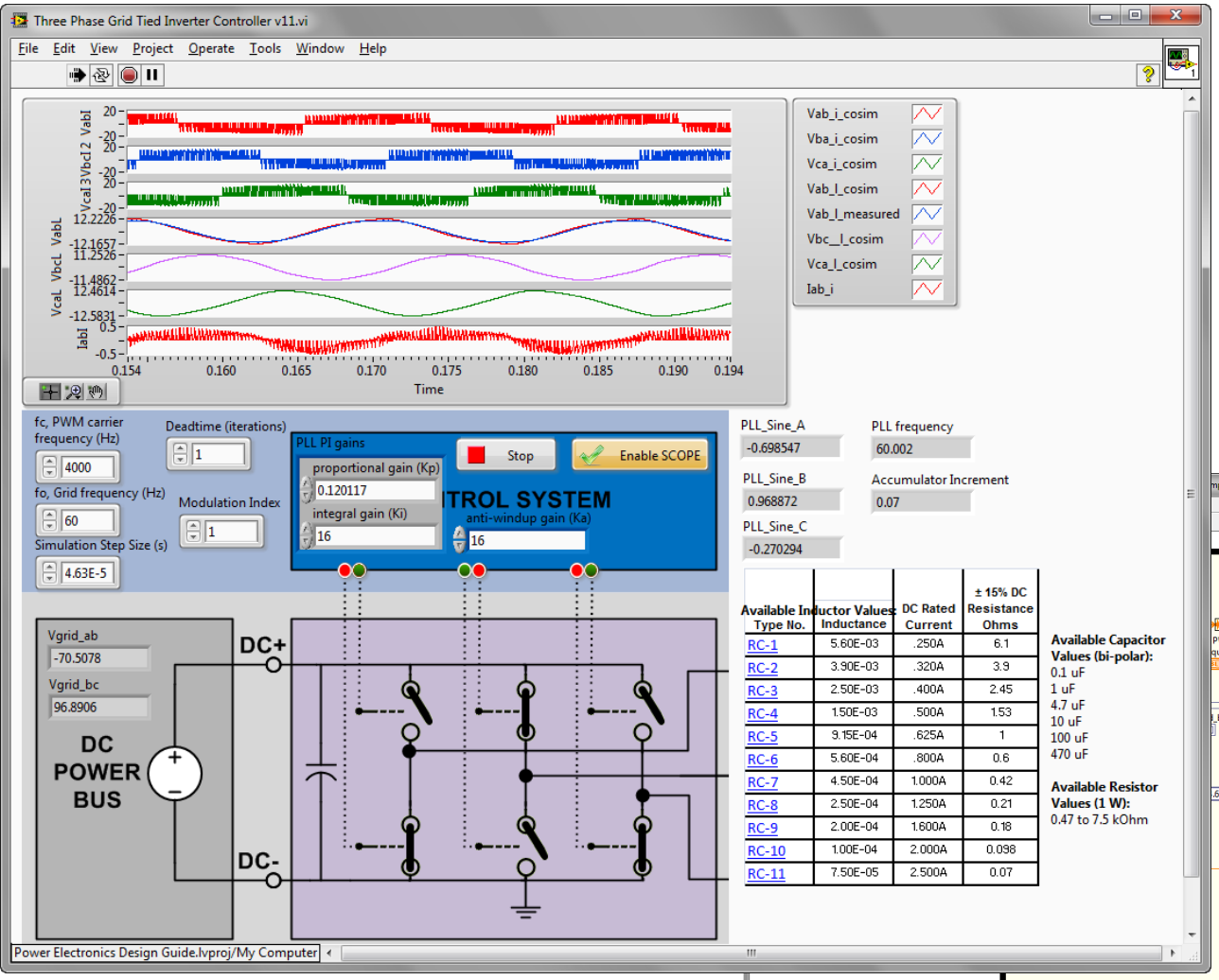






New Power Electronics Hands-on Experiential Learning System

Three Phase Inverter: Co-Simulation vs. Physical Measurements



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RC-8	2.50E-04	1.250A	0.21
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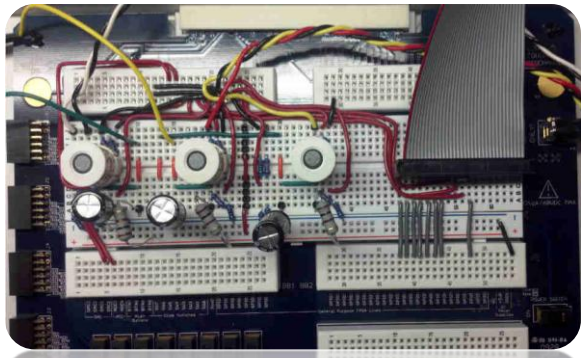
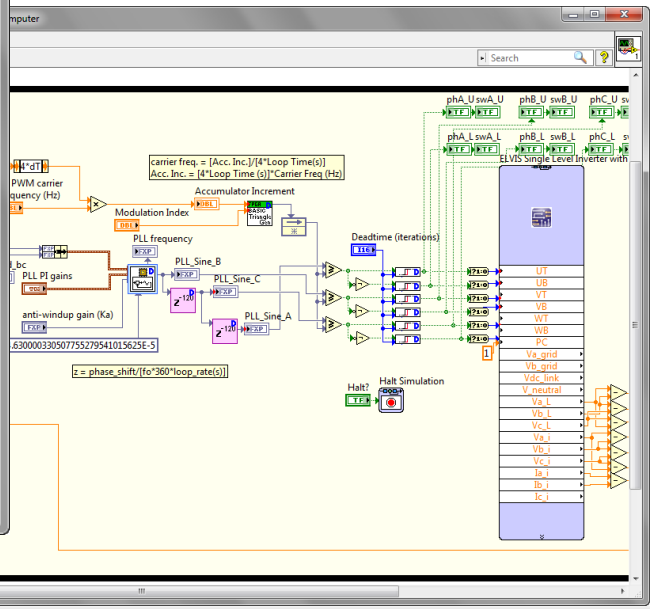
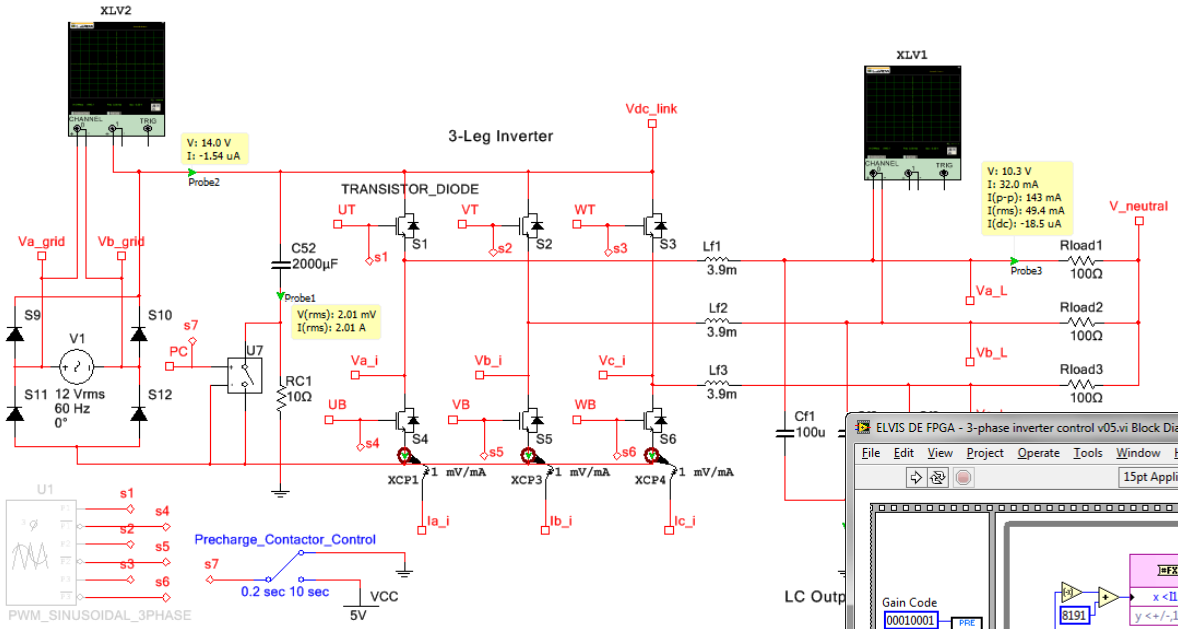
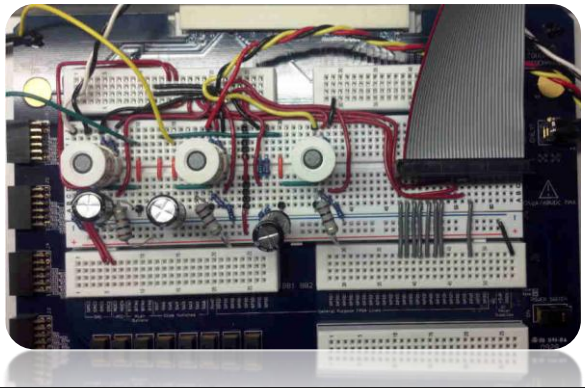
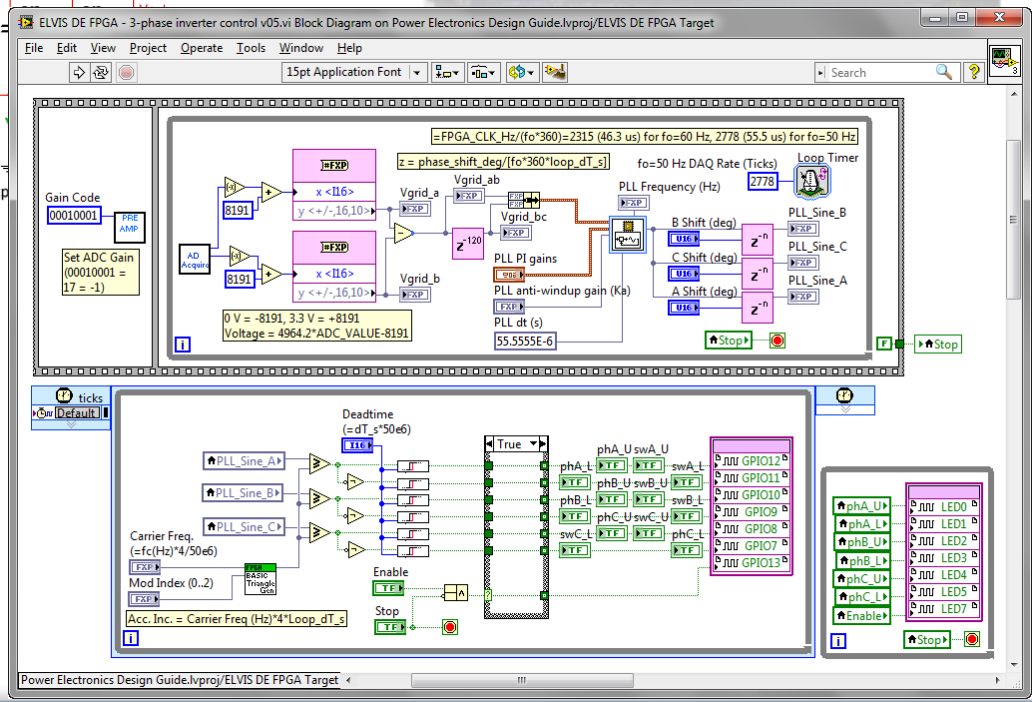




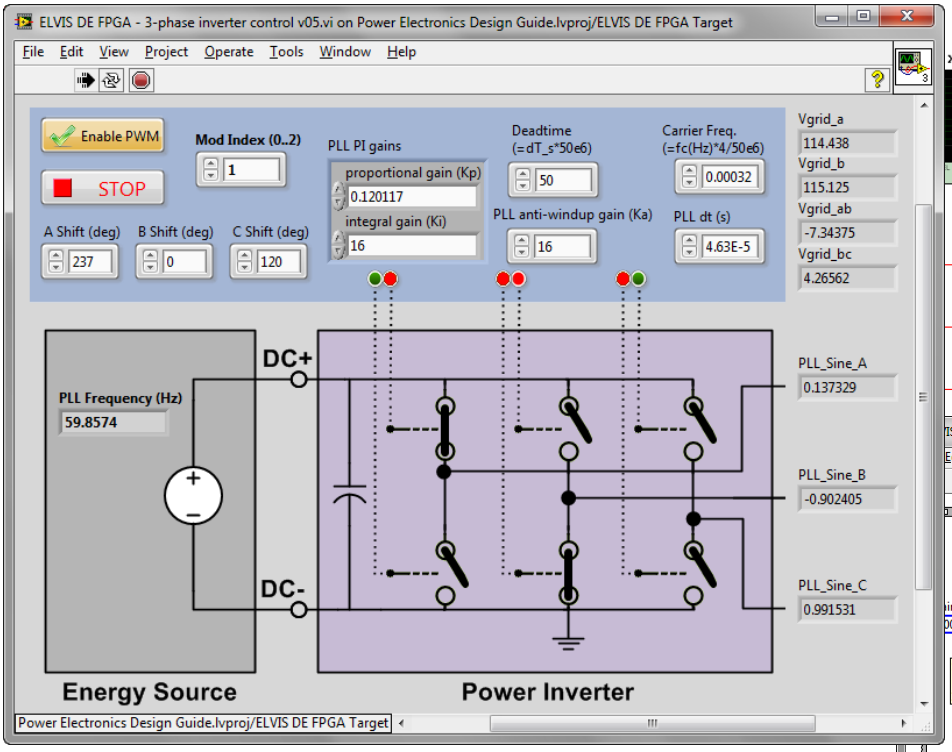
Three Phase Inverter: Co-Simulation vs. Physical Measurements

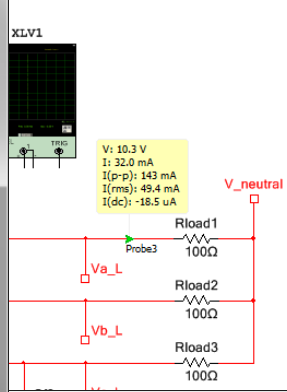


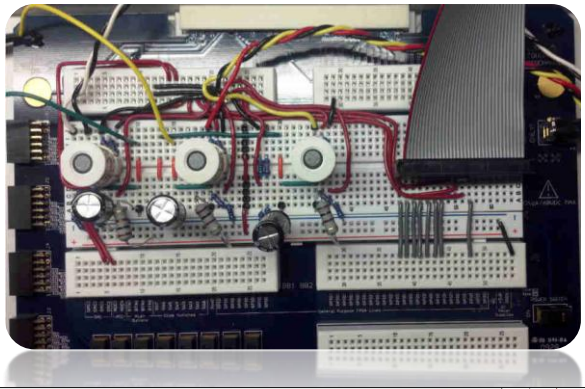


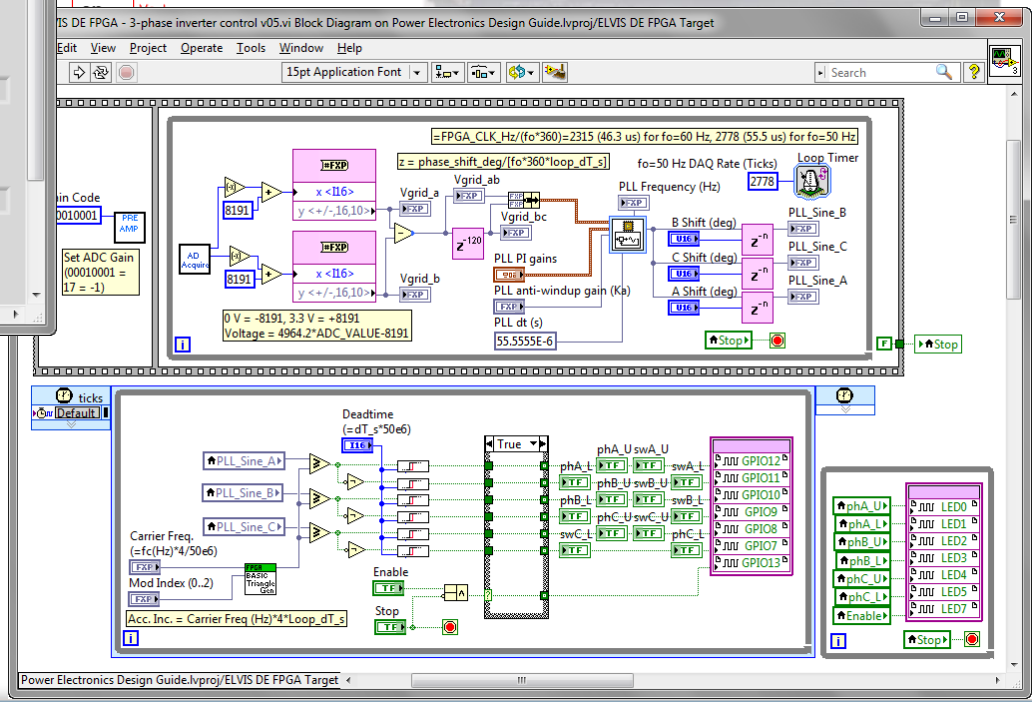


Three Phase Inverter: Co-Simulation vs. Physical Measurements

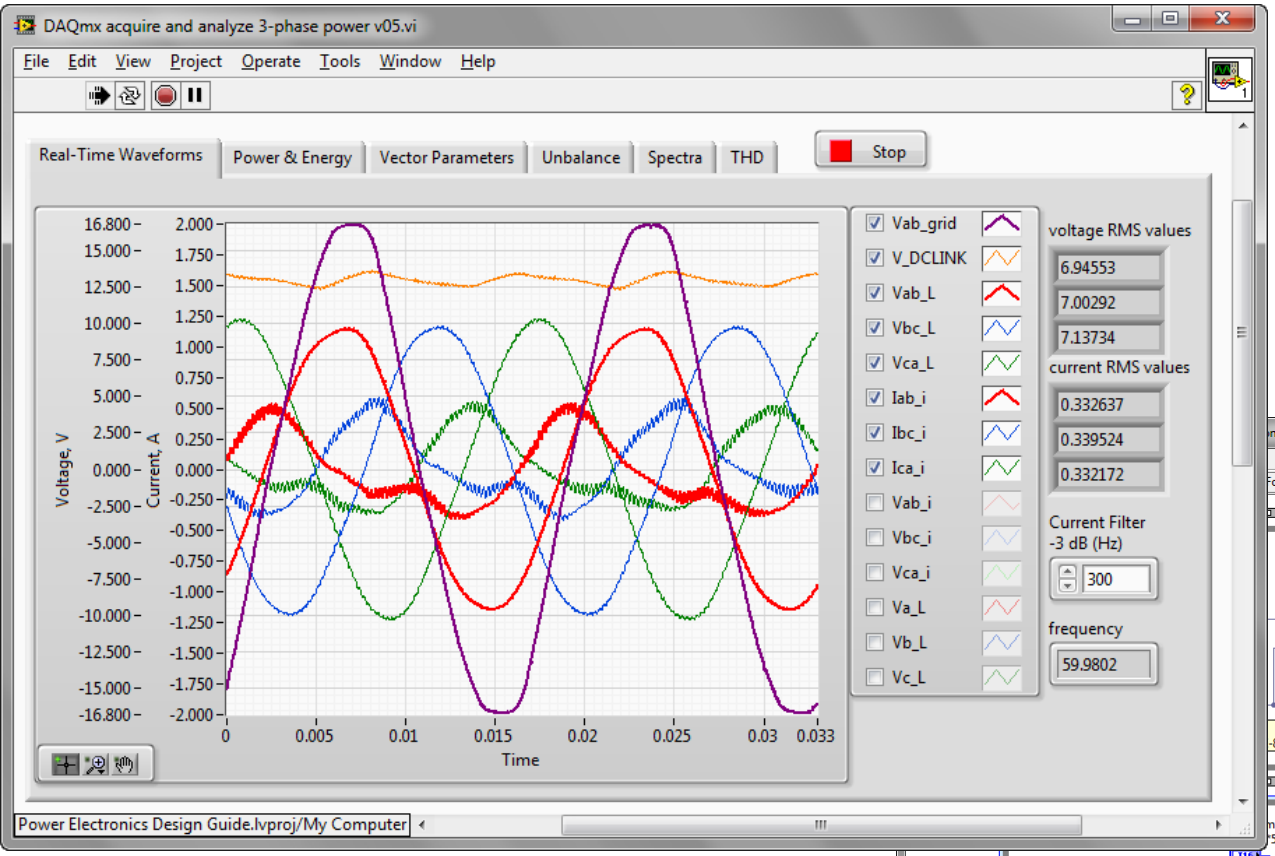


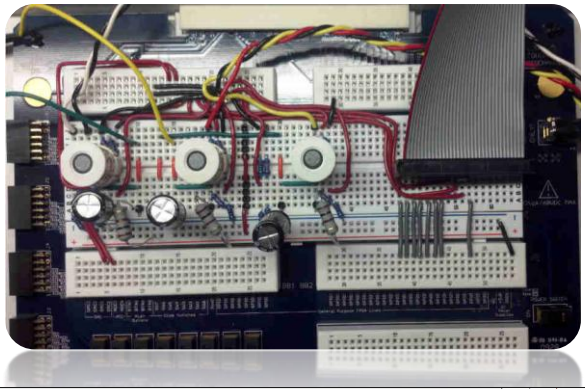


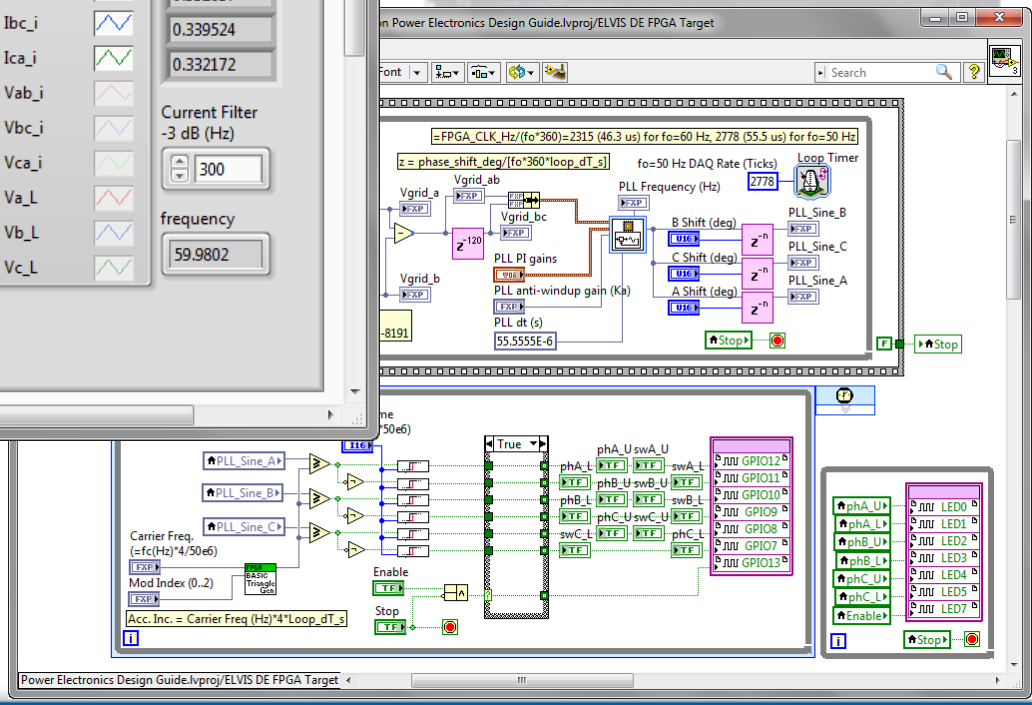




Three Phase Inverter: Co-Simulation vs. Physical Measurements







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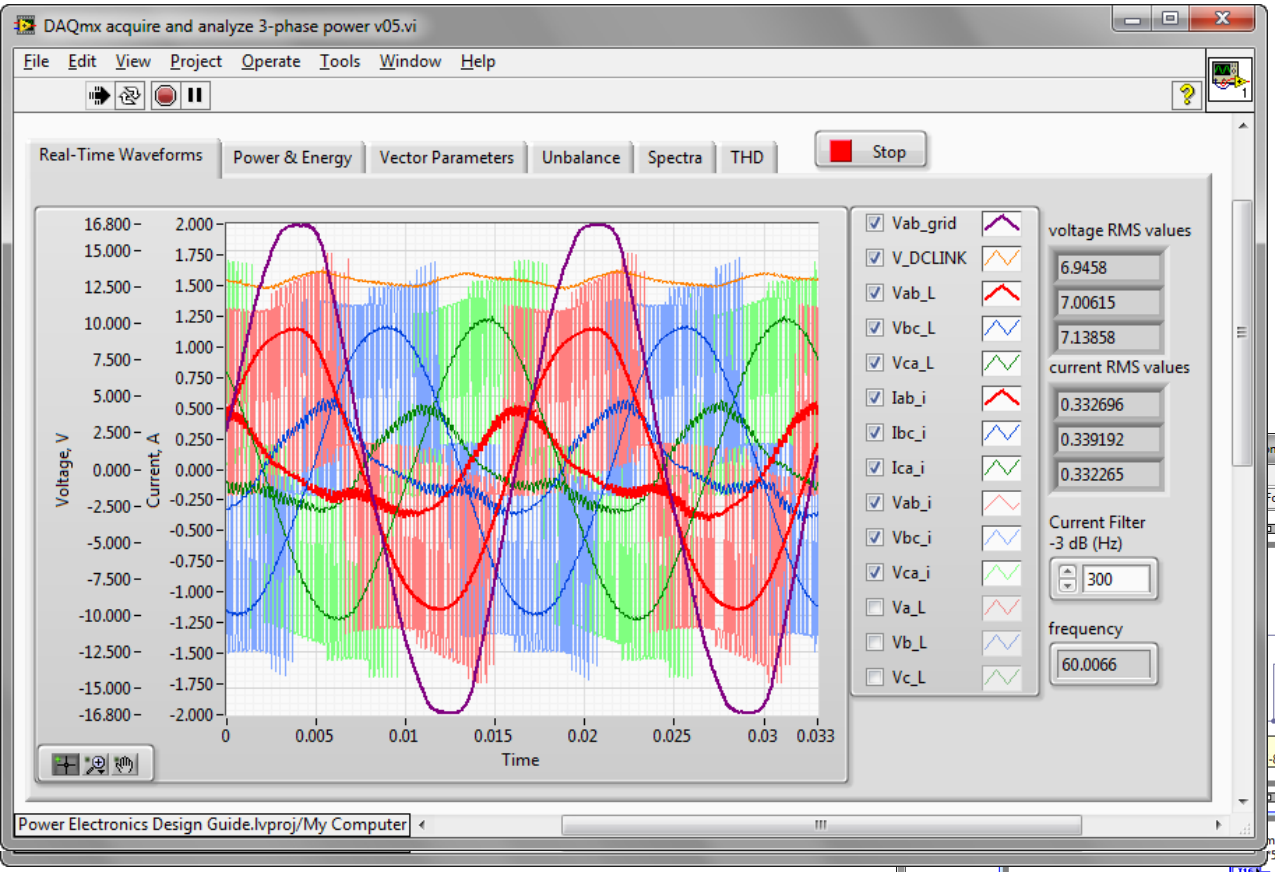

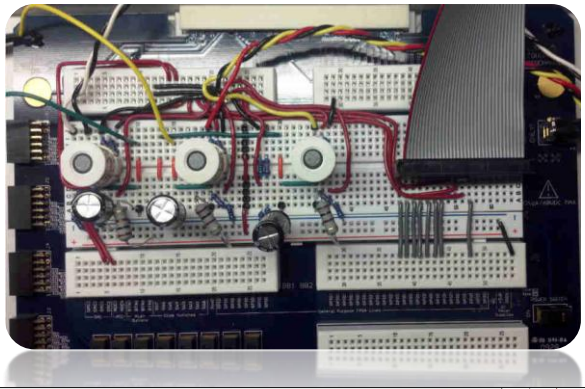

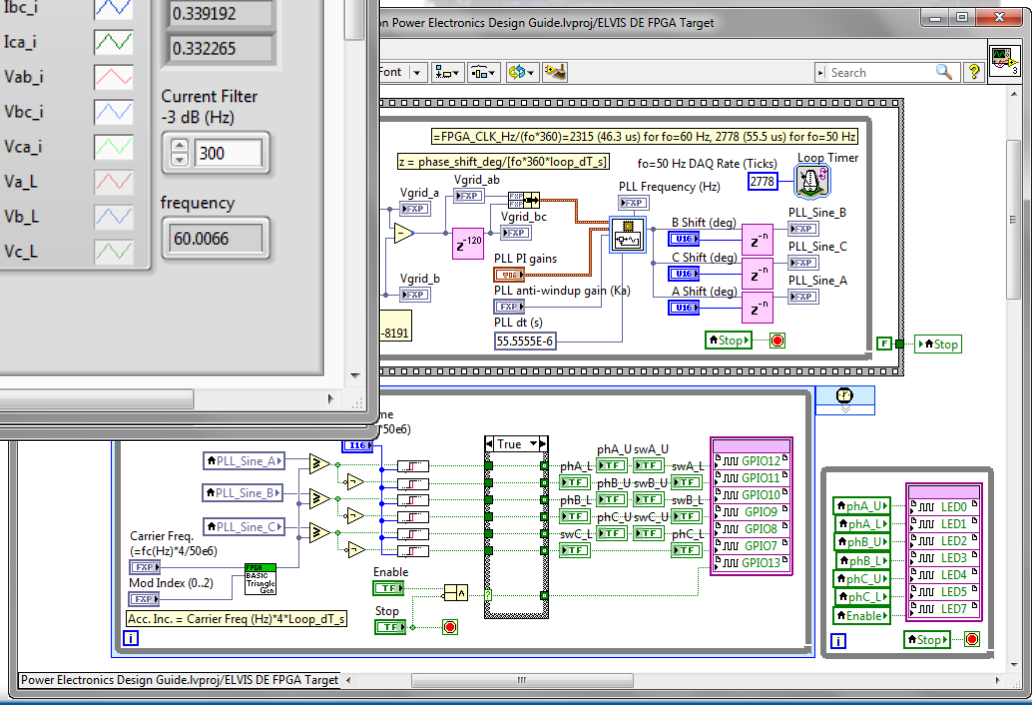

New Power Electronics Hands-on Experiential Learning System

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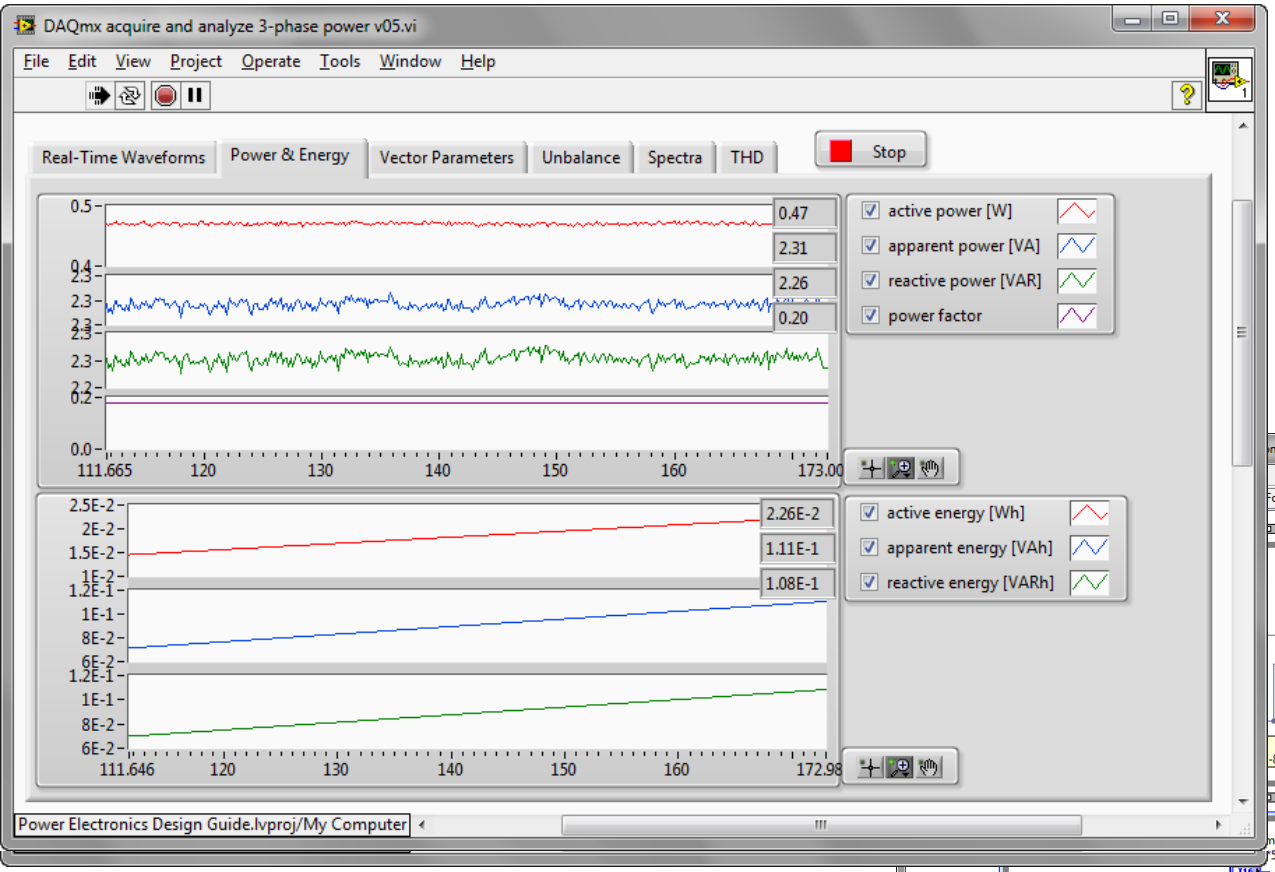

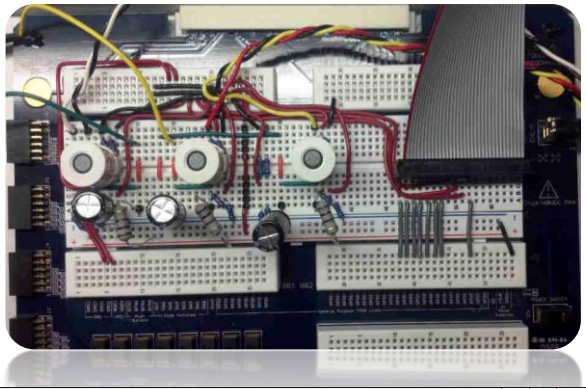

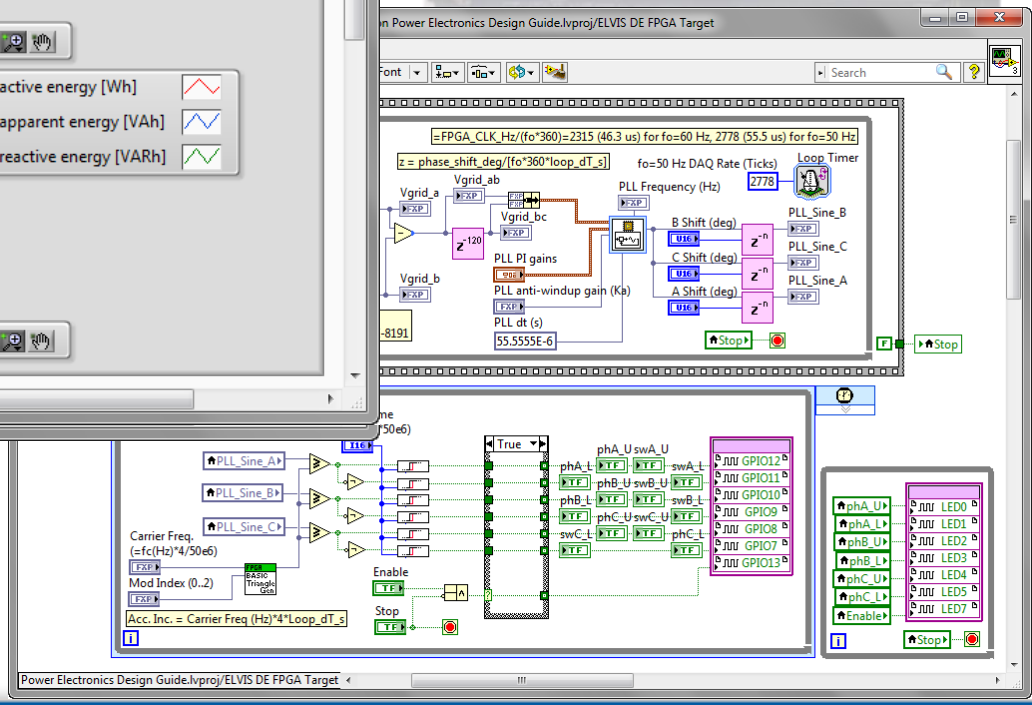

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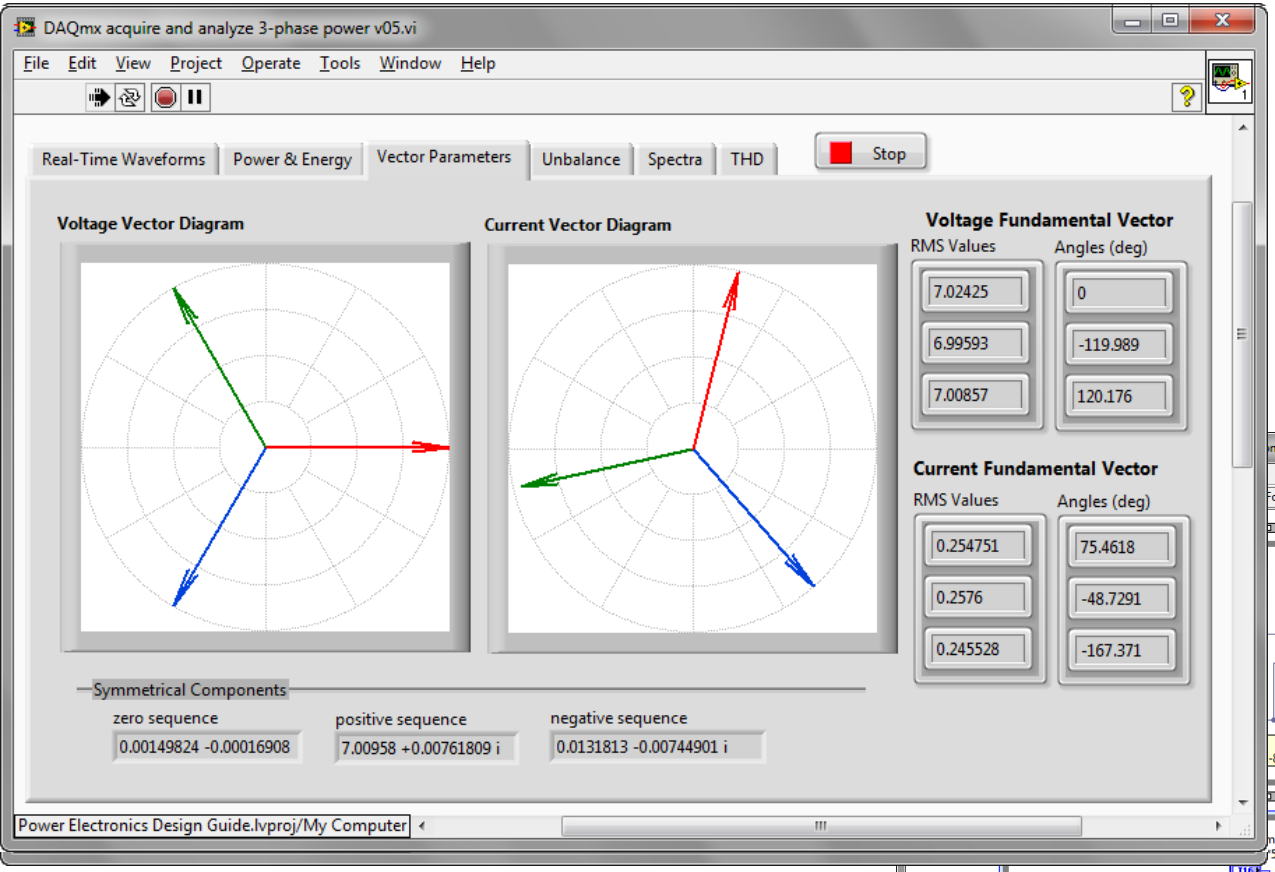

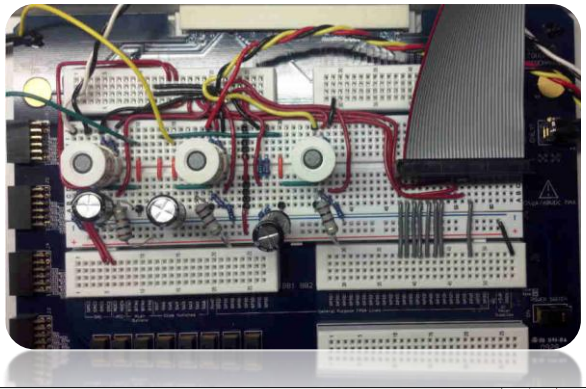

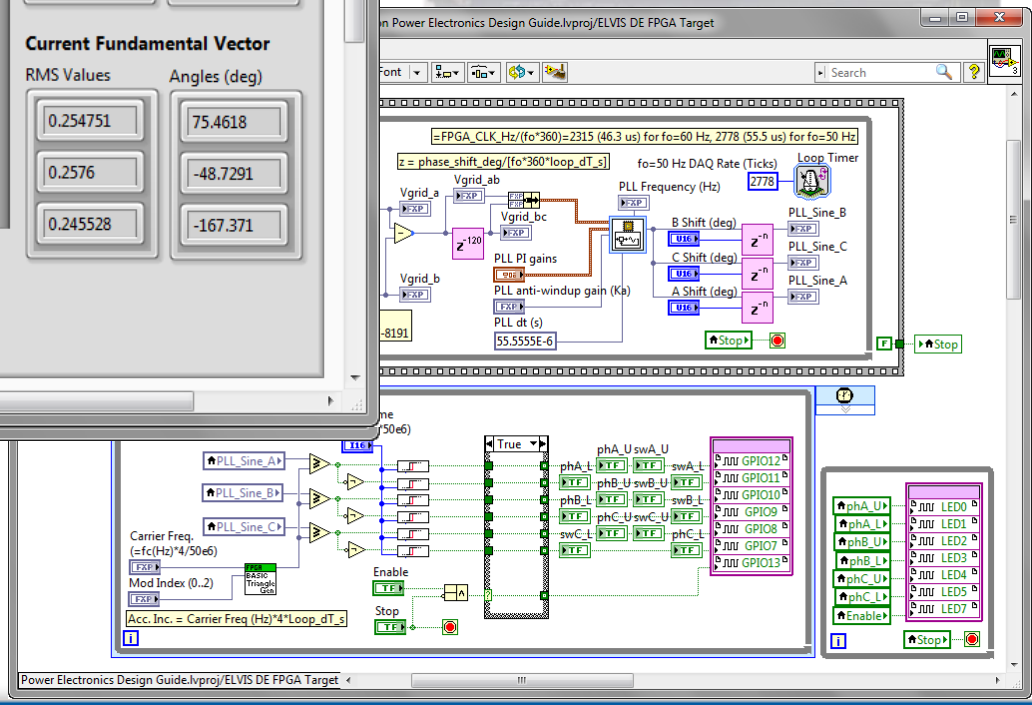

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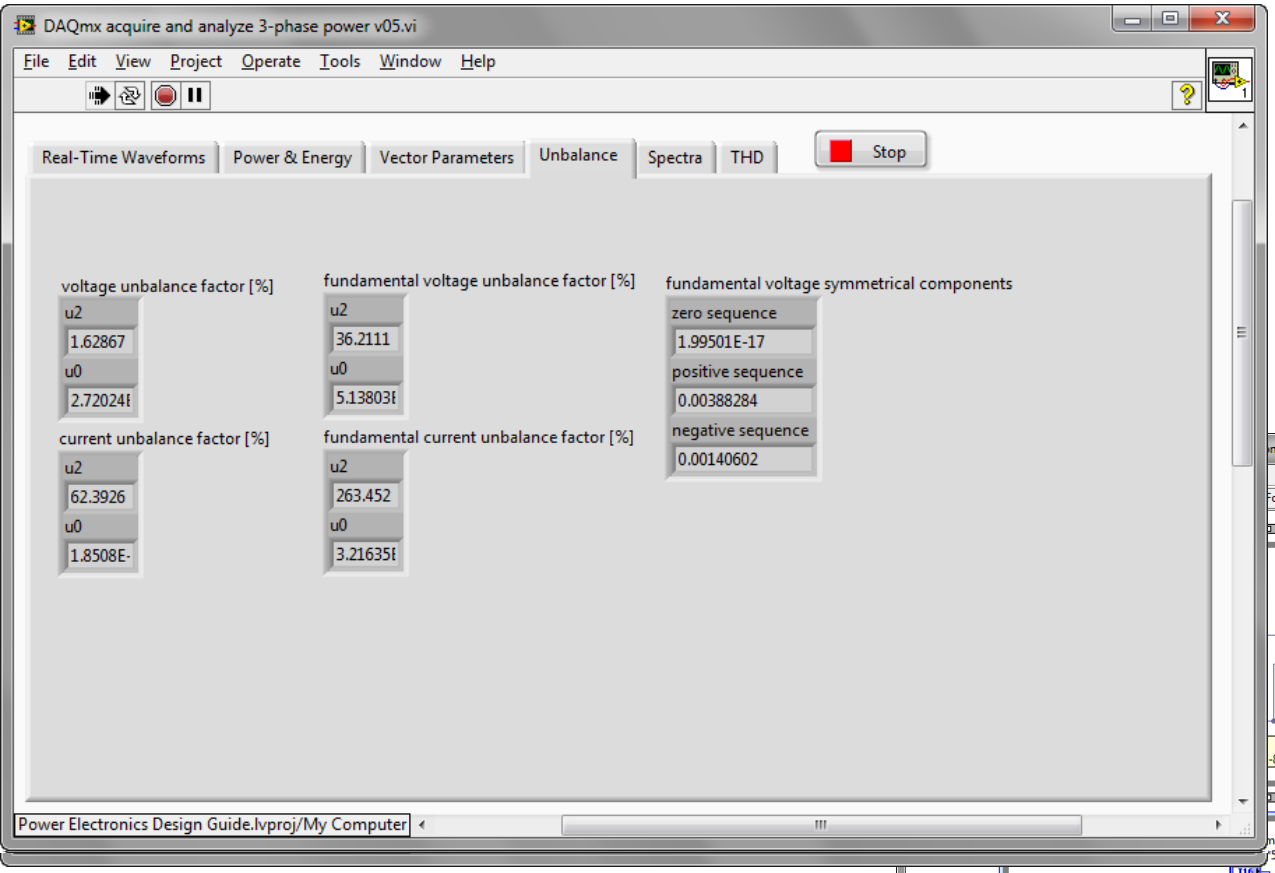

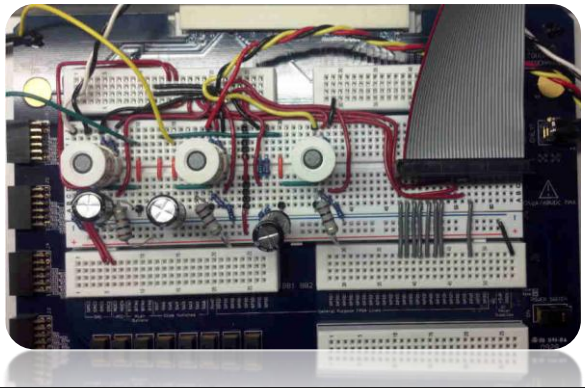

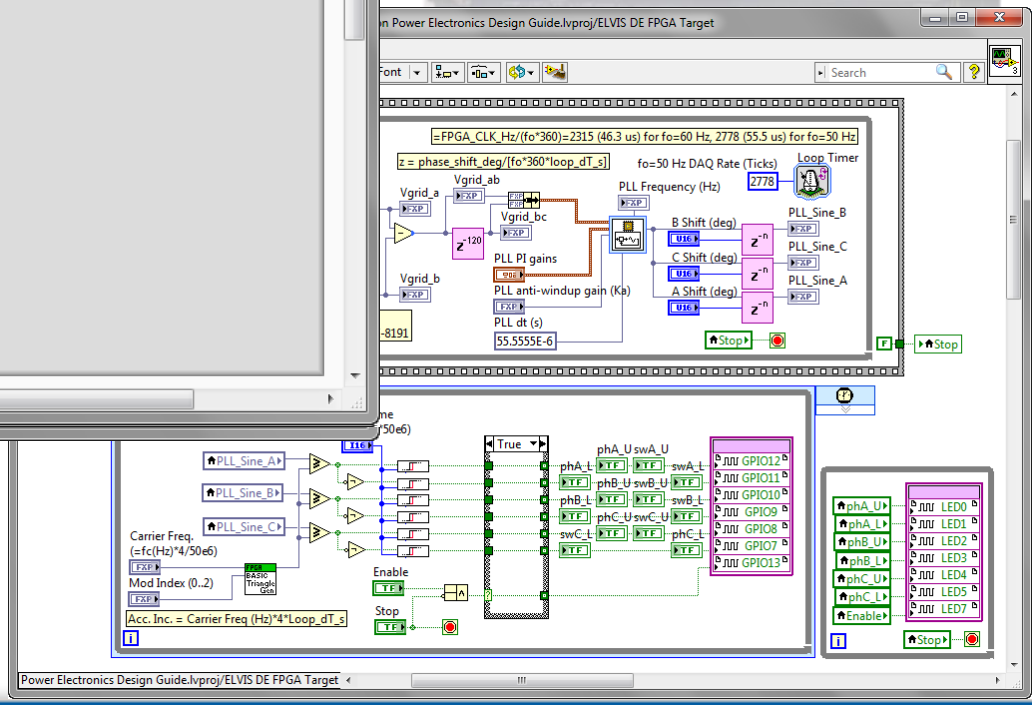

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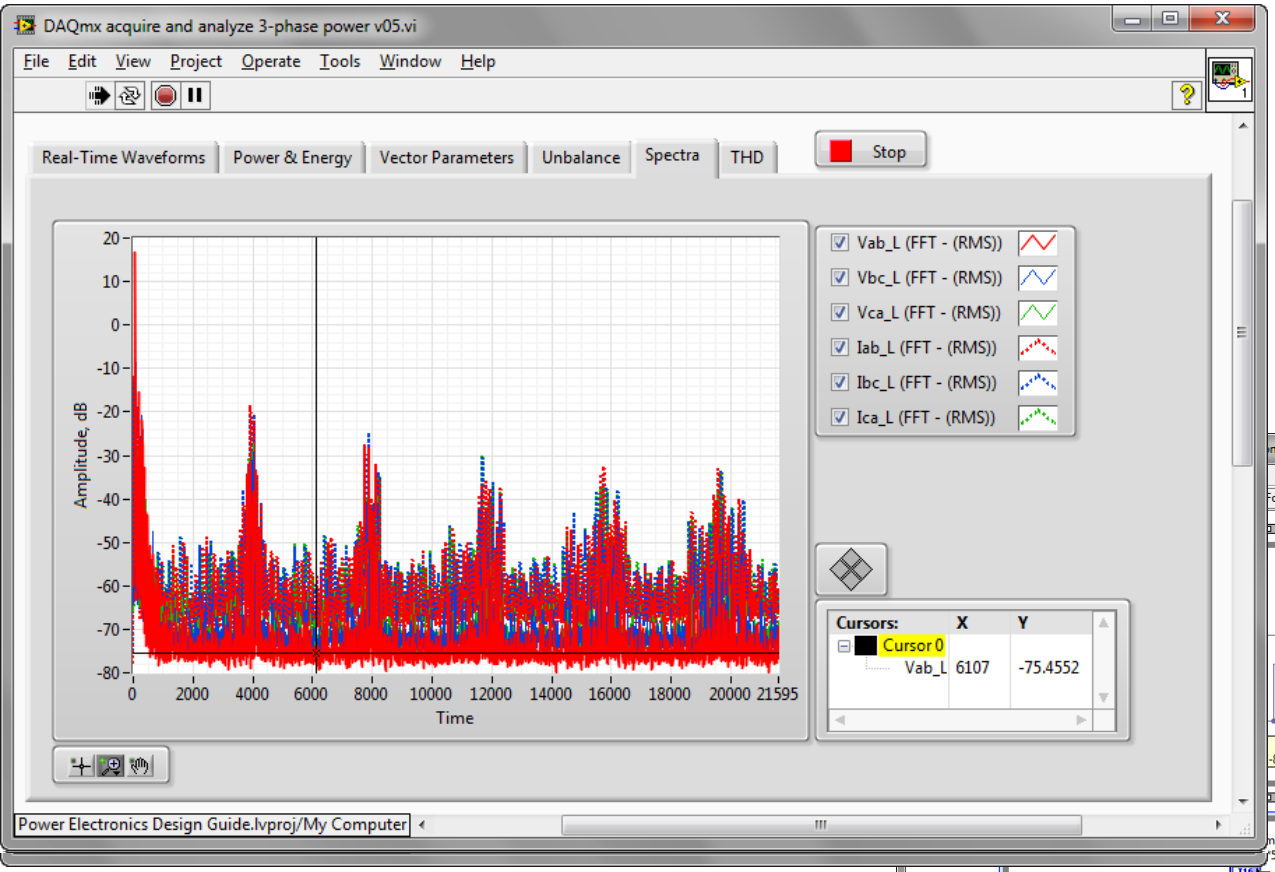

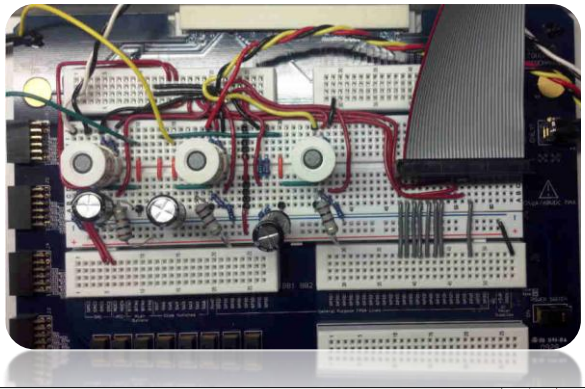

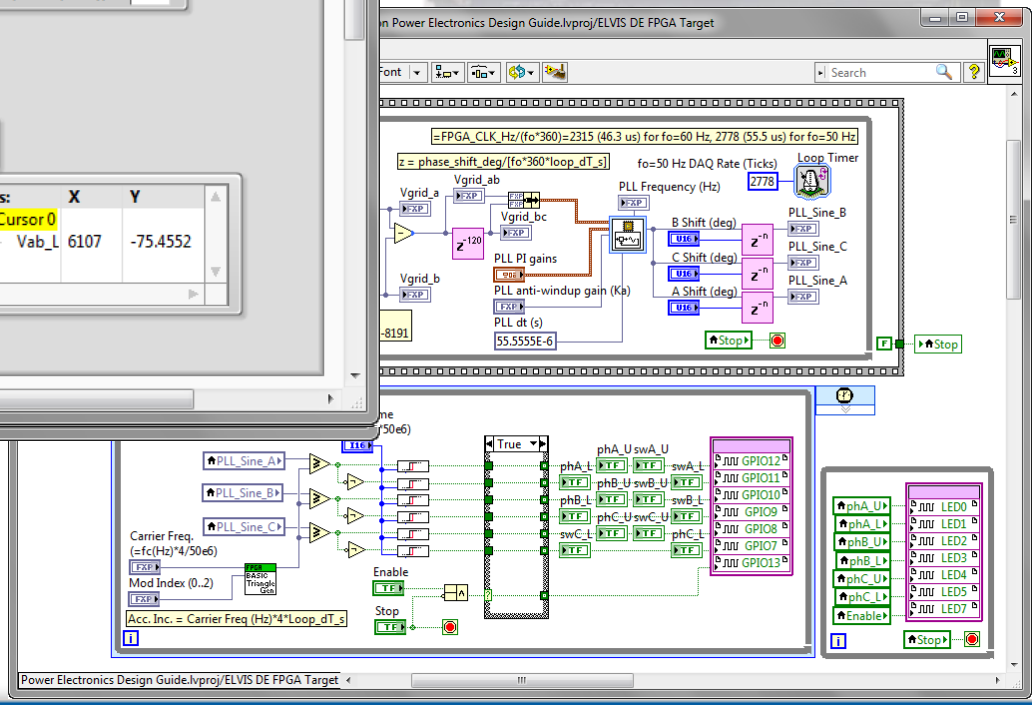

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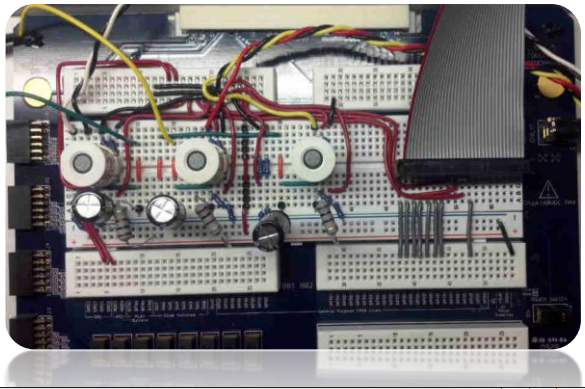

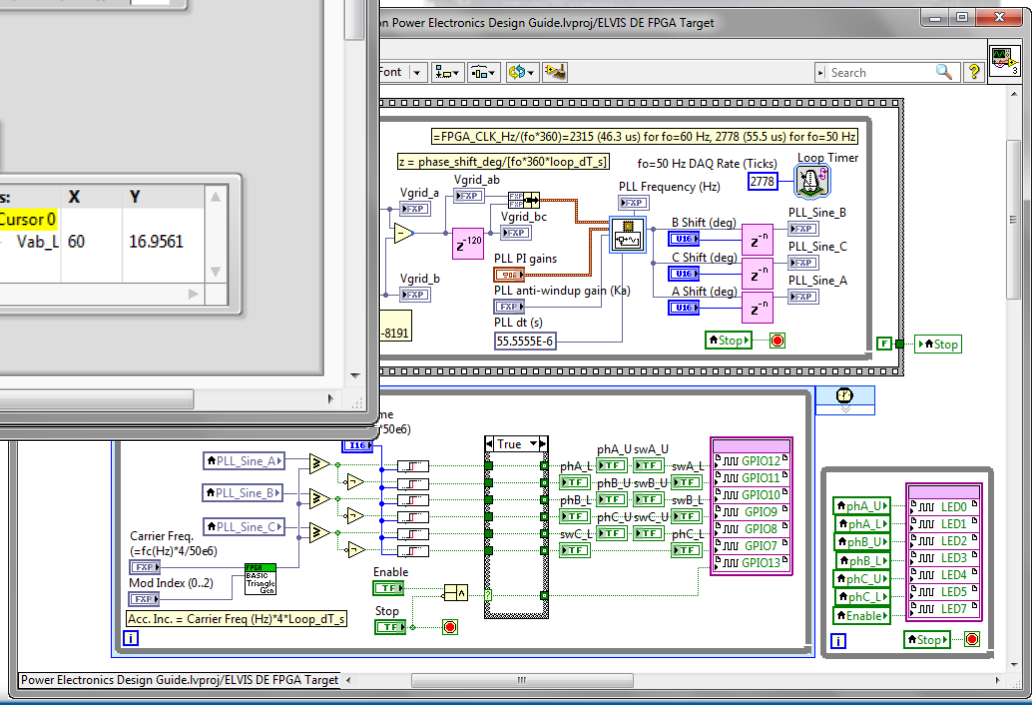

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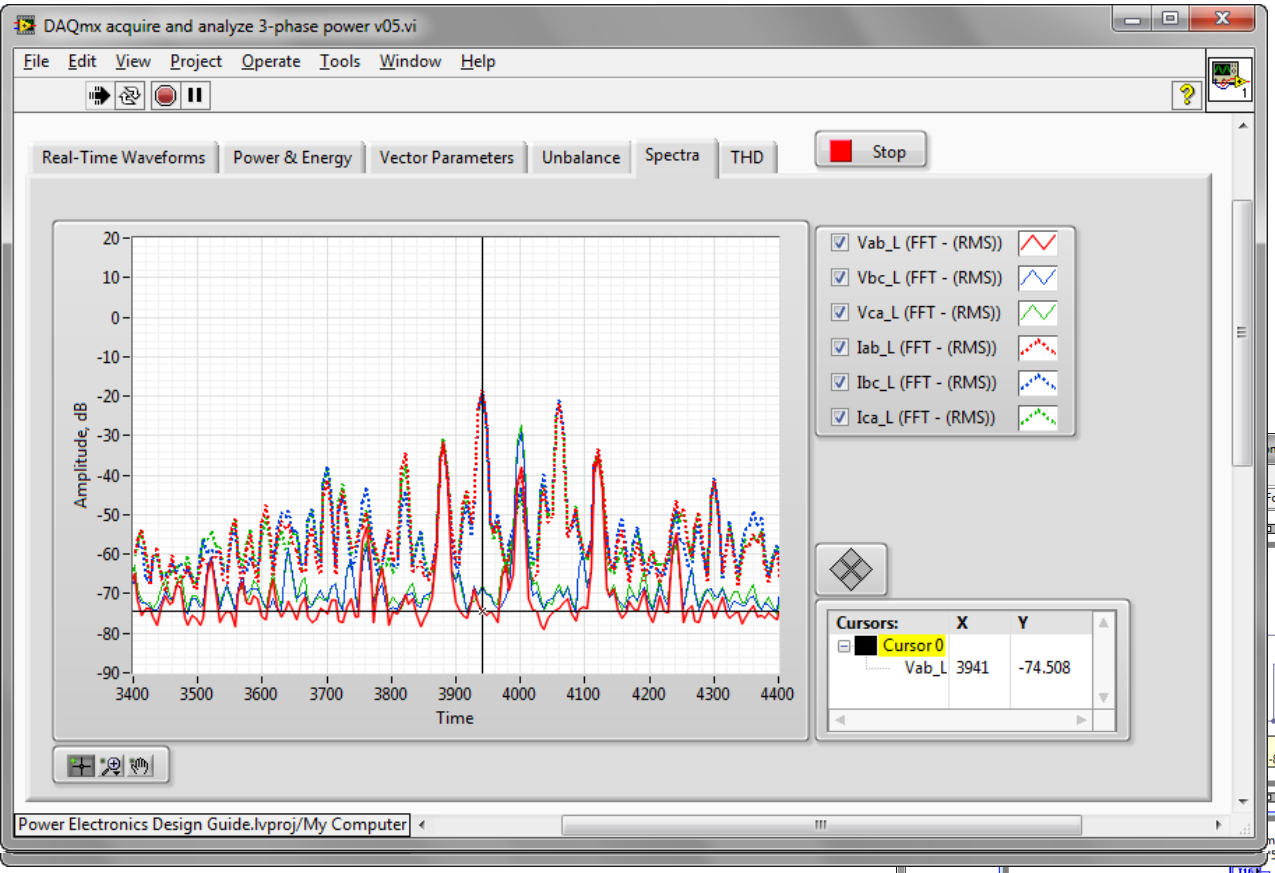

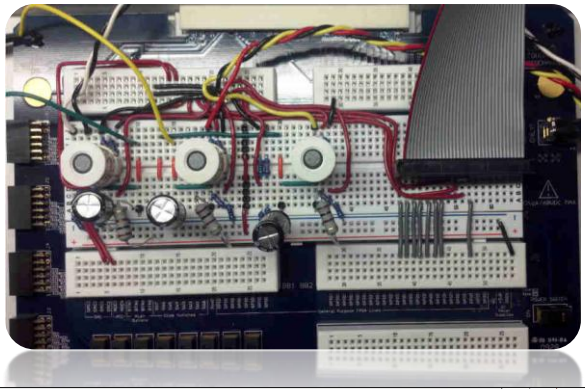

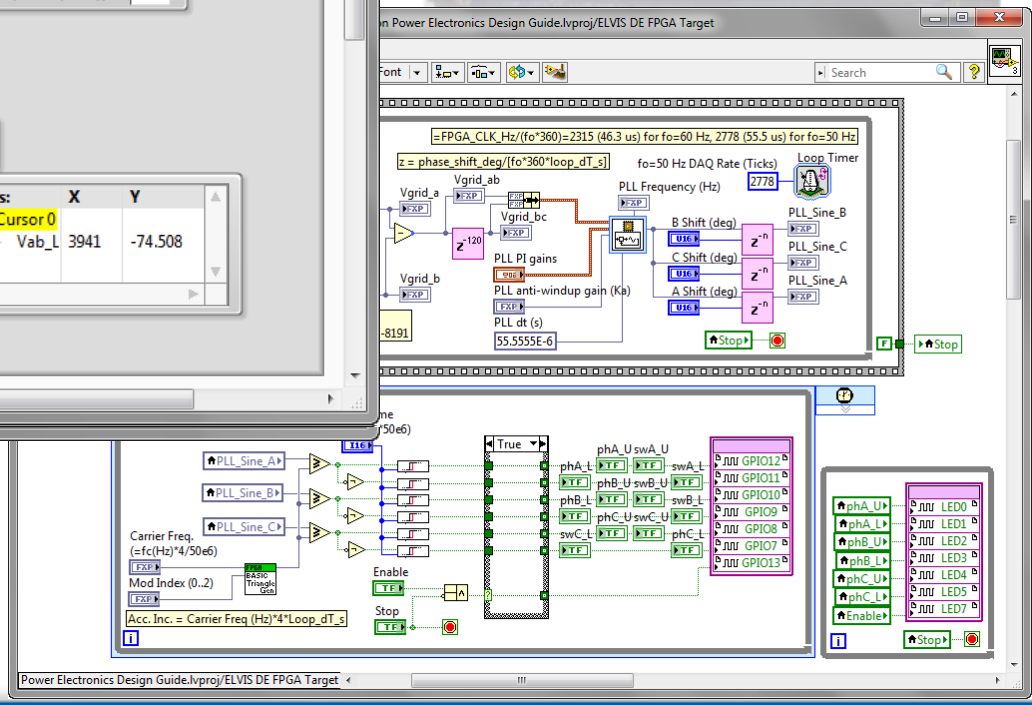

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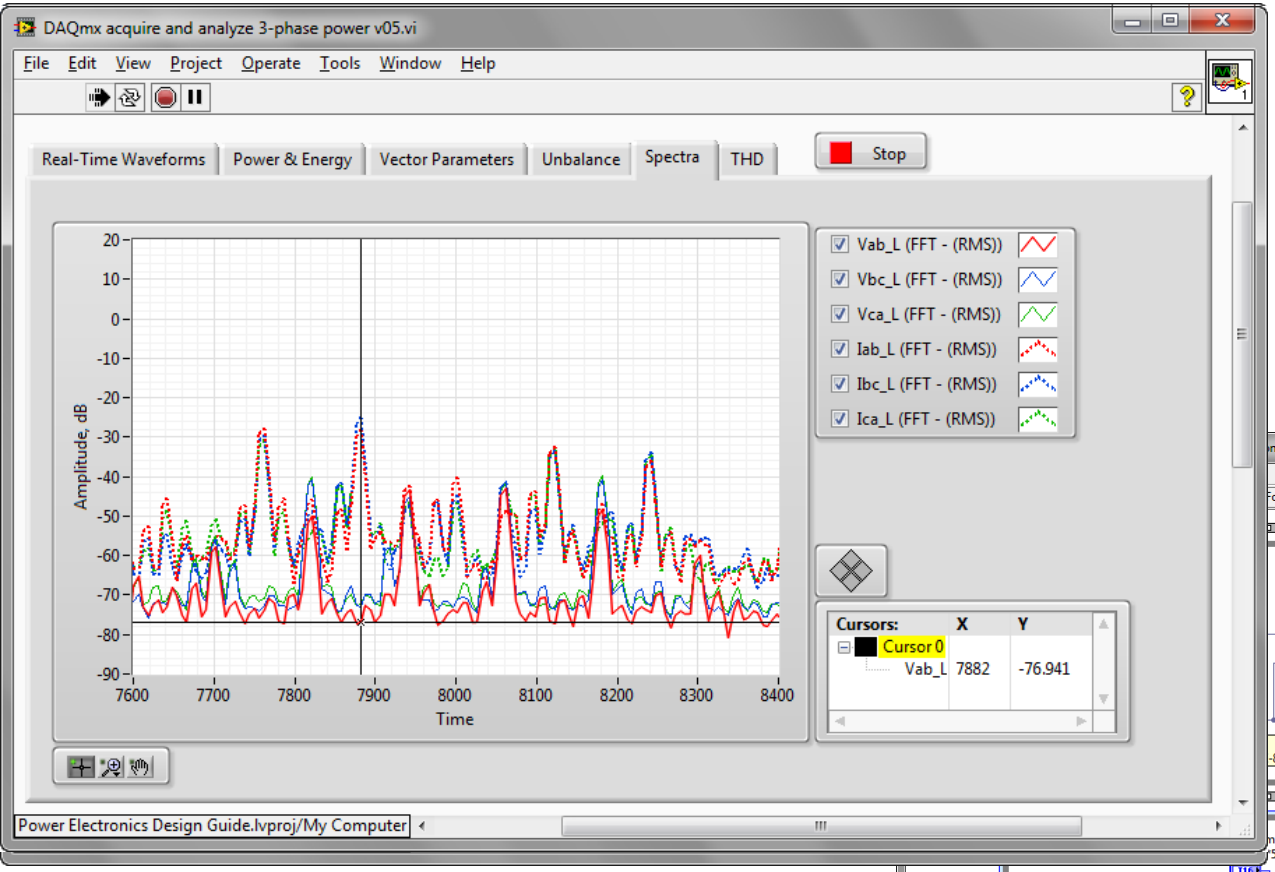

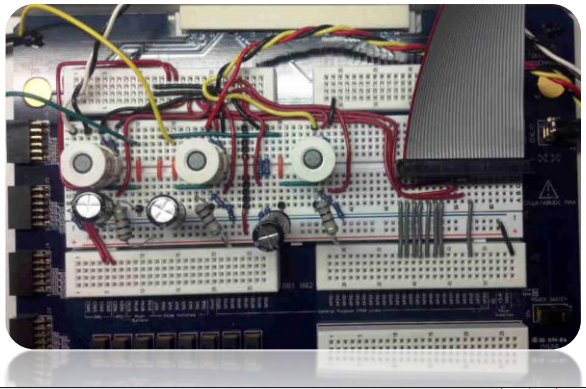

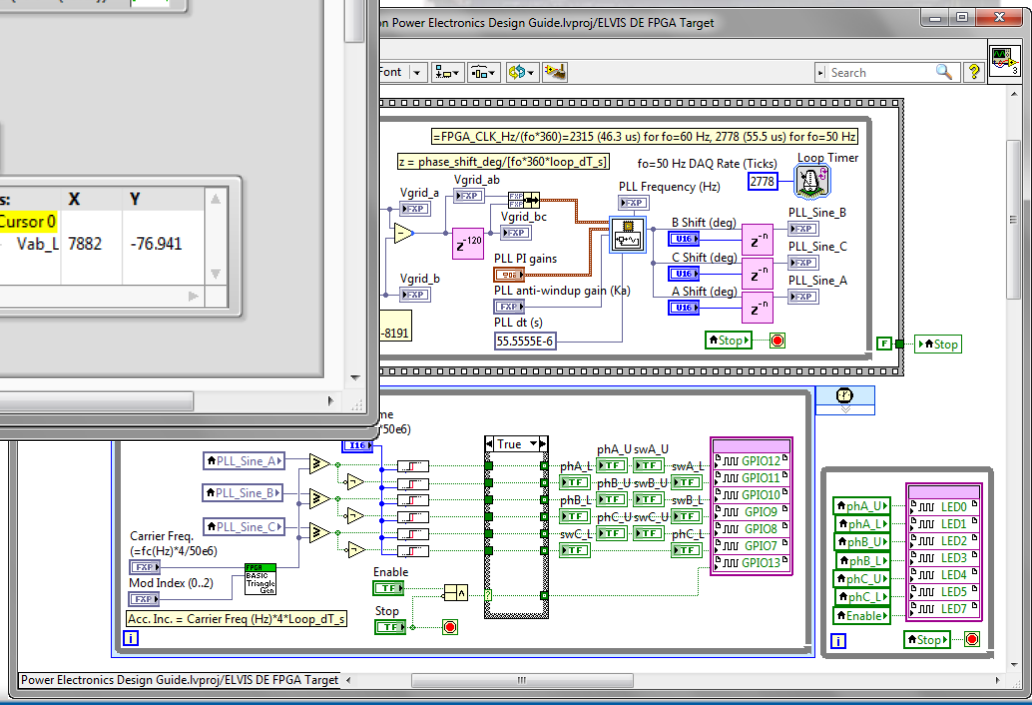

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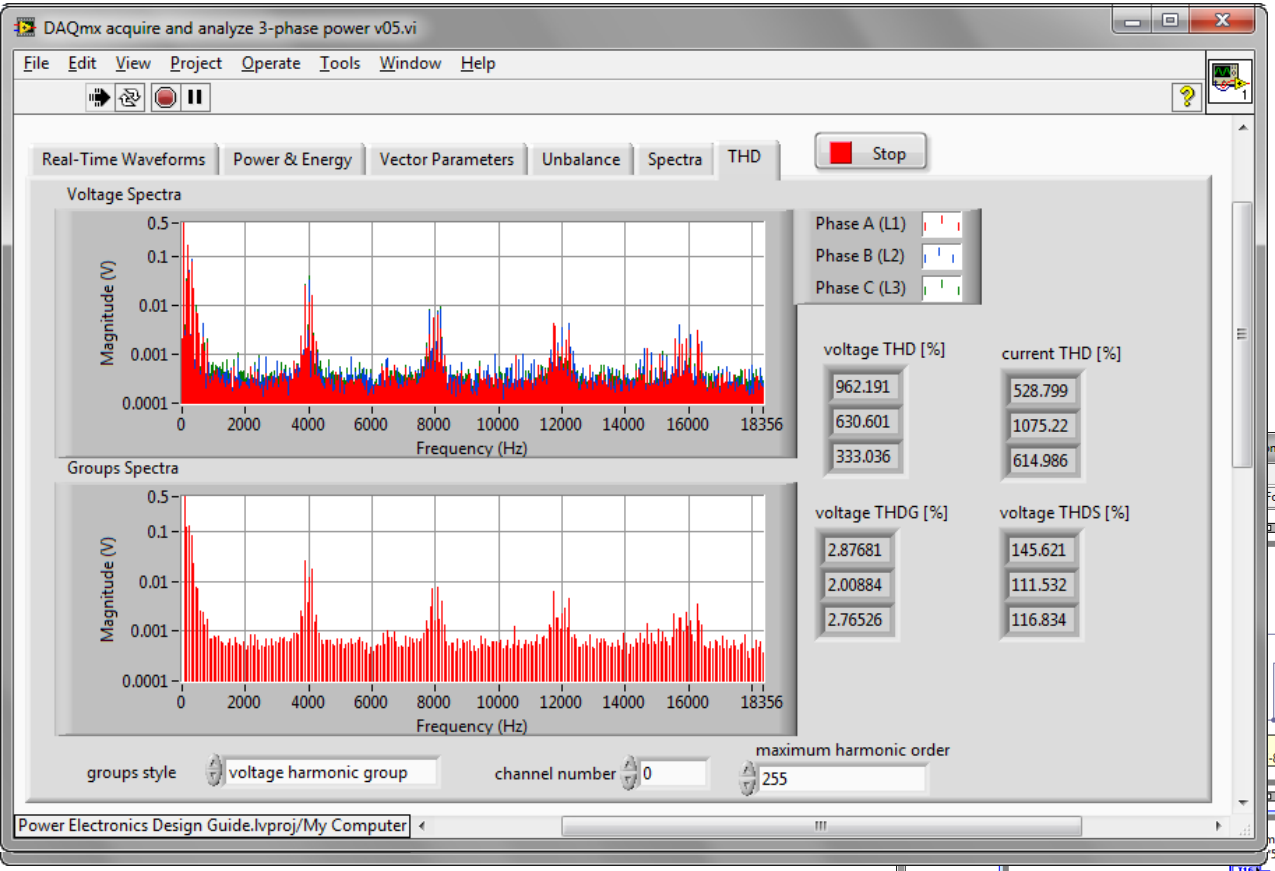
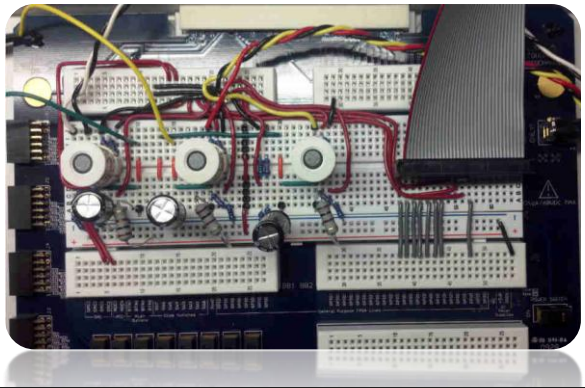
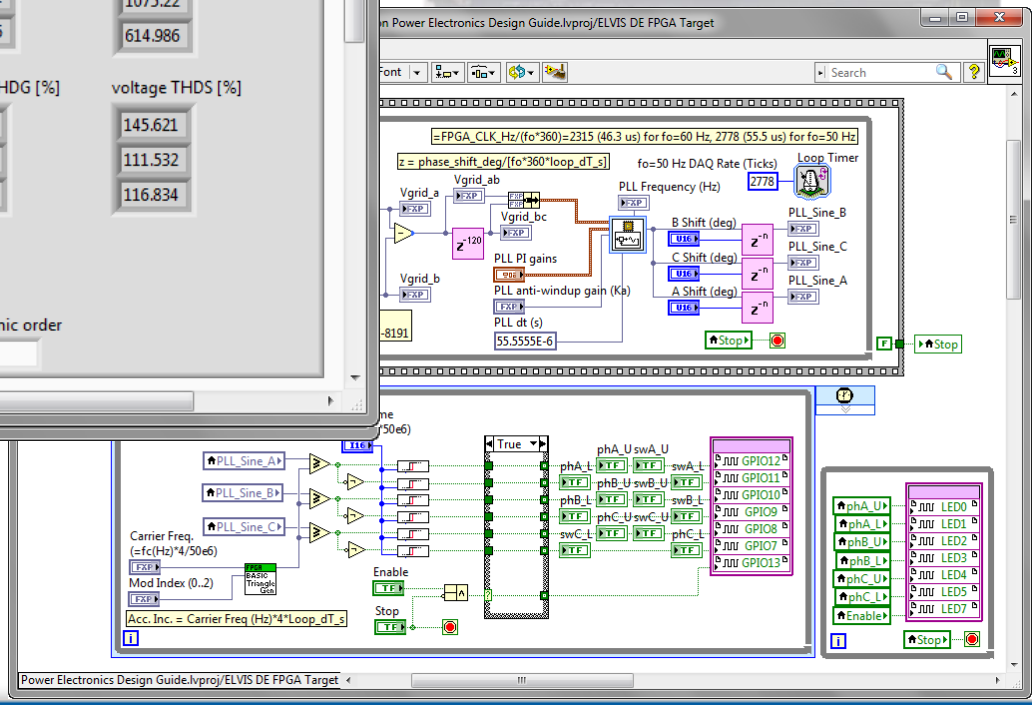
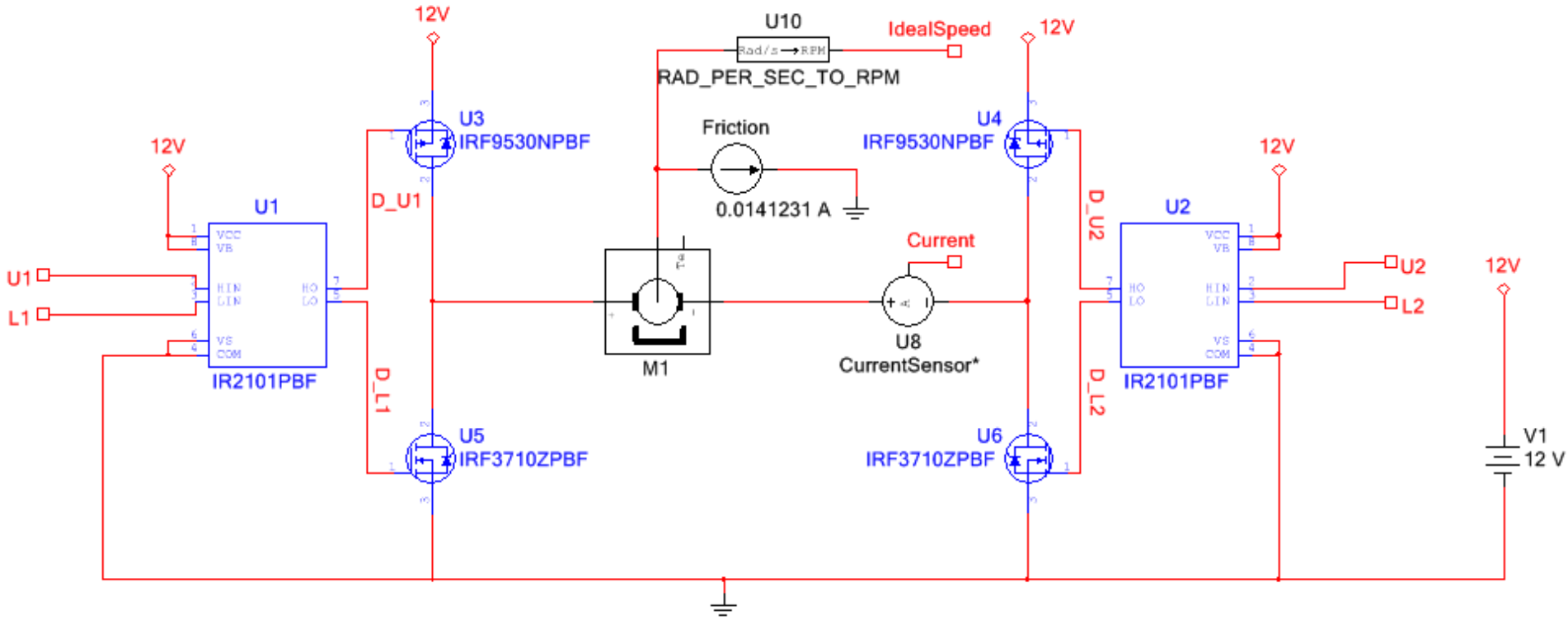






Brushed DC Motor: Simulation vs. Physical Measurements



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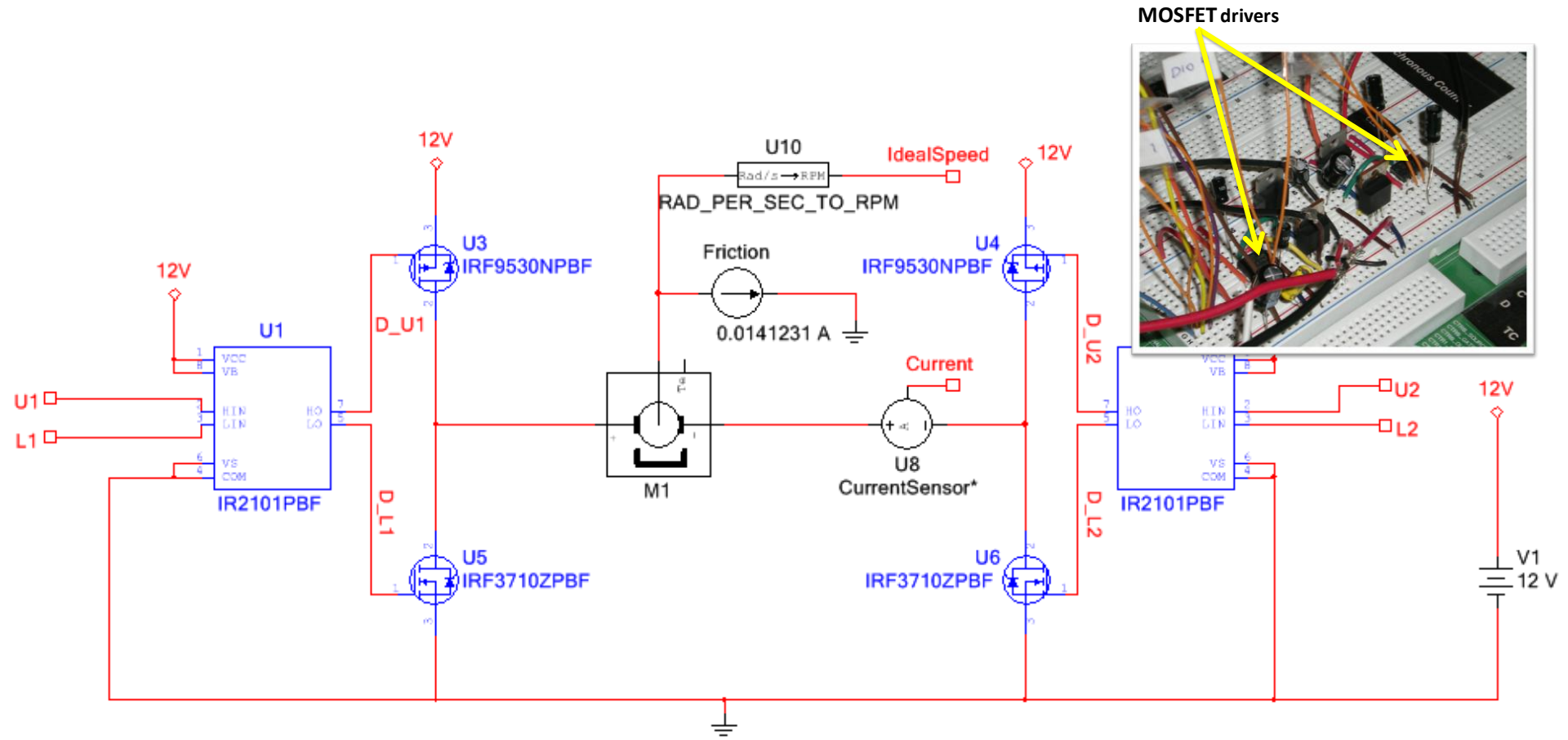

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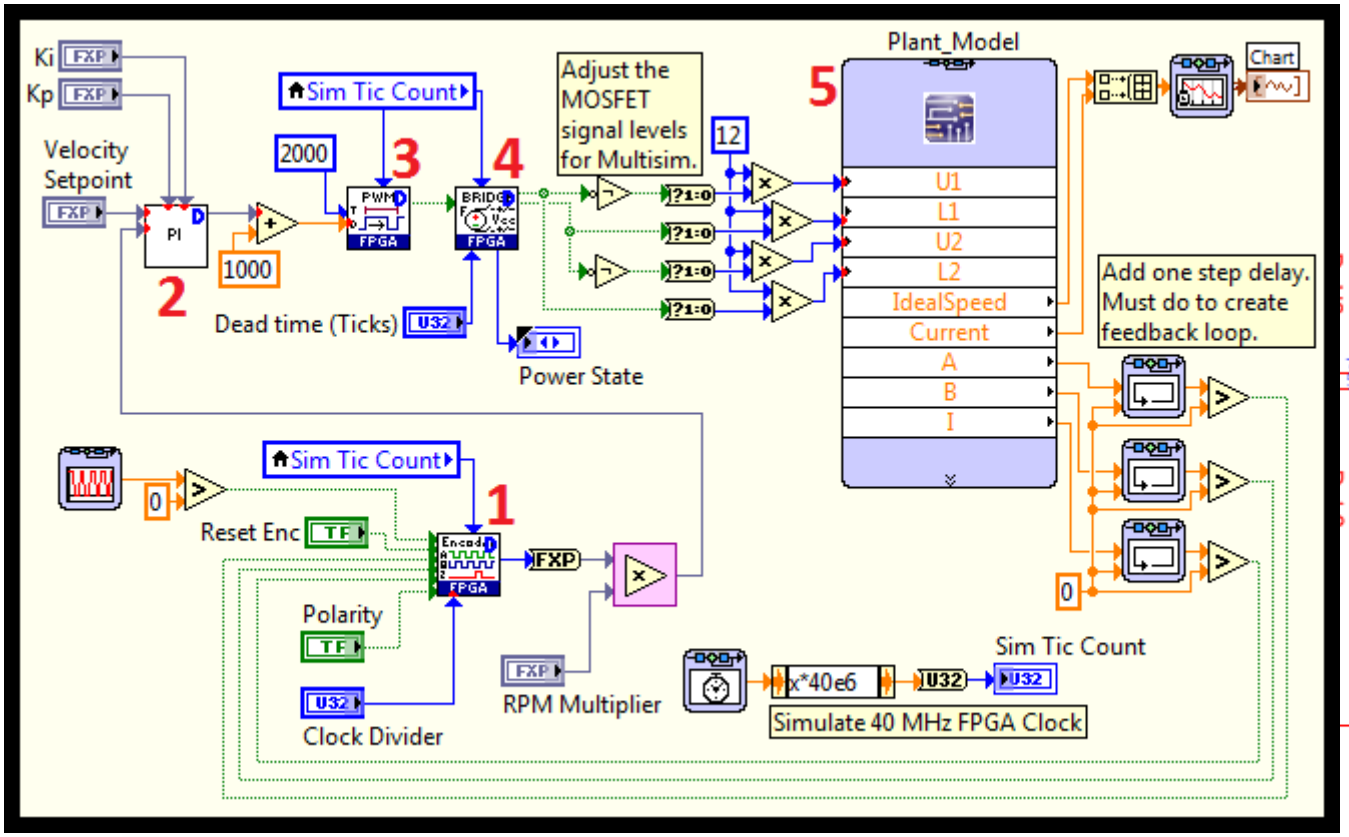

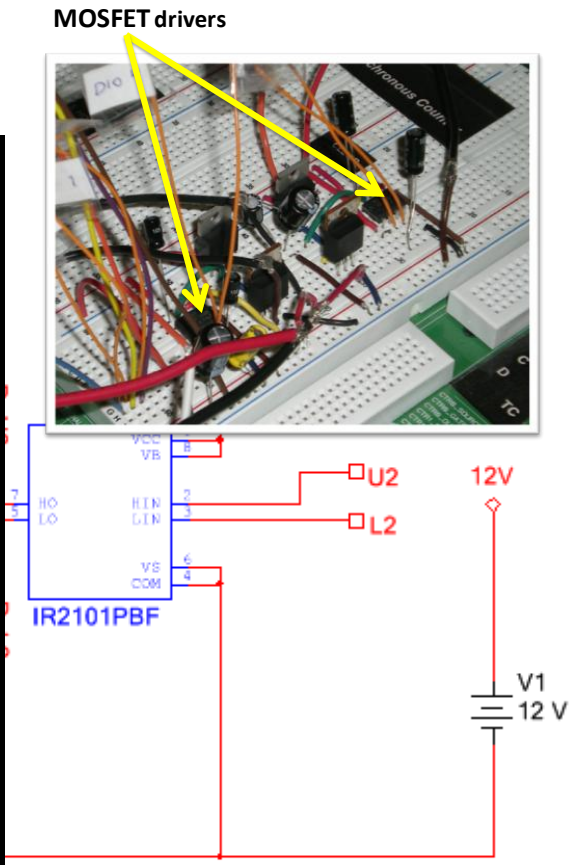

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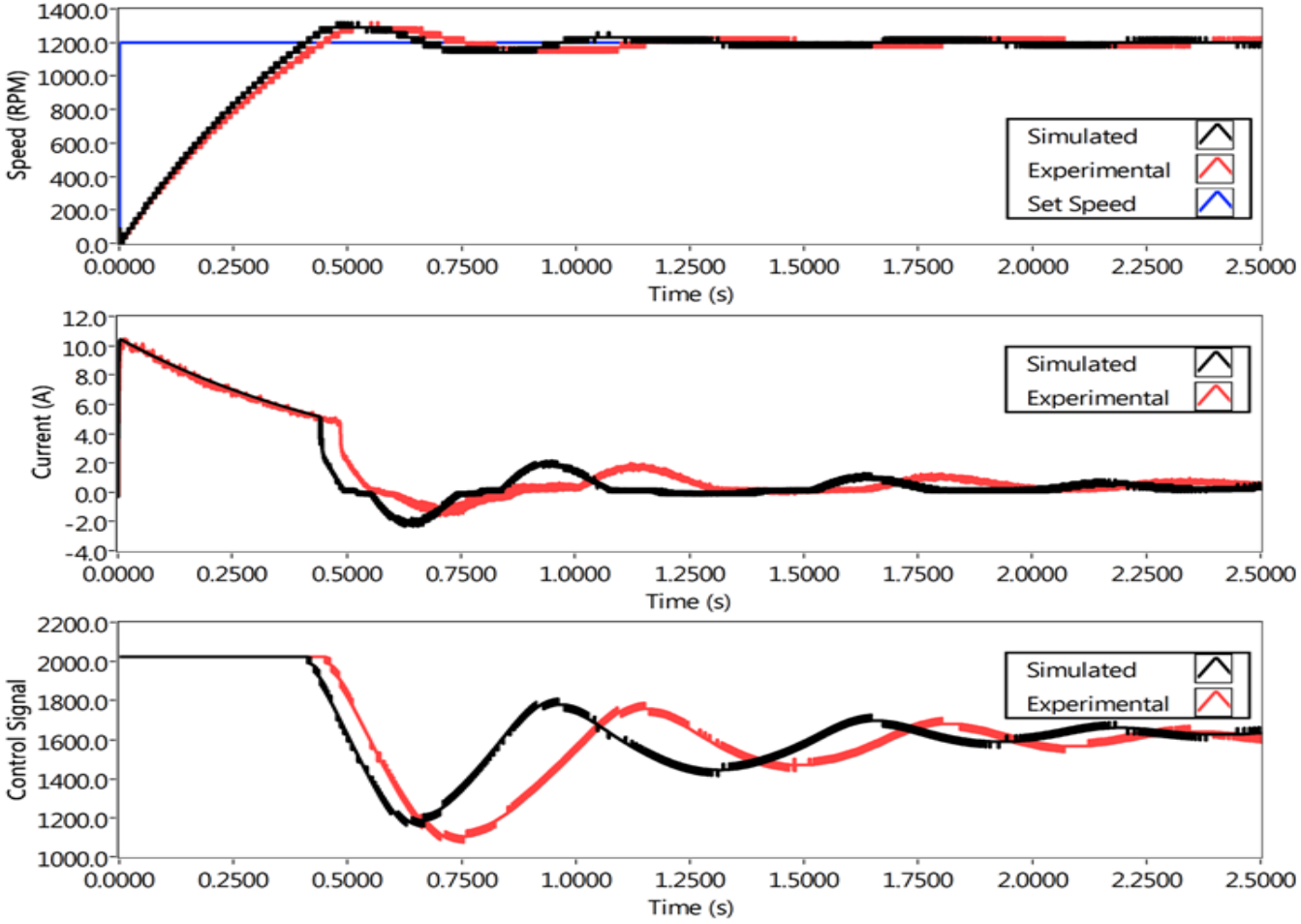
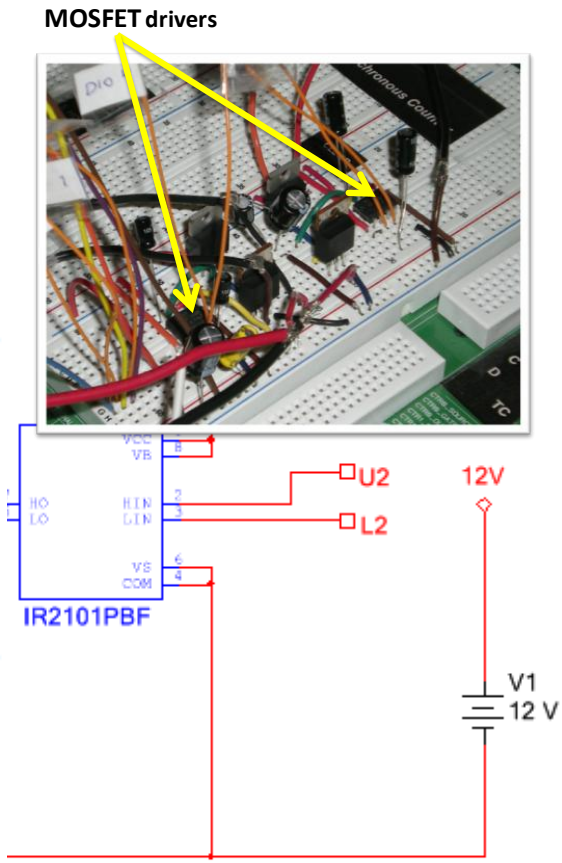
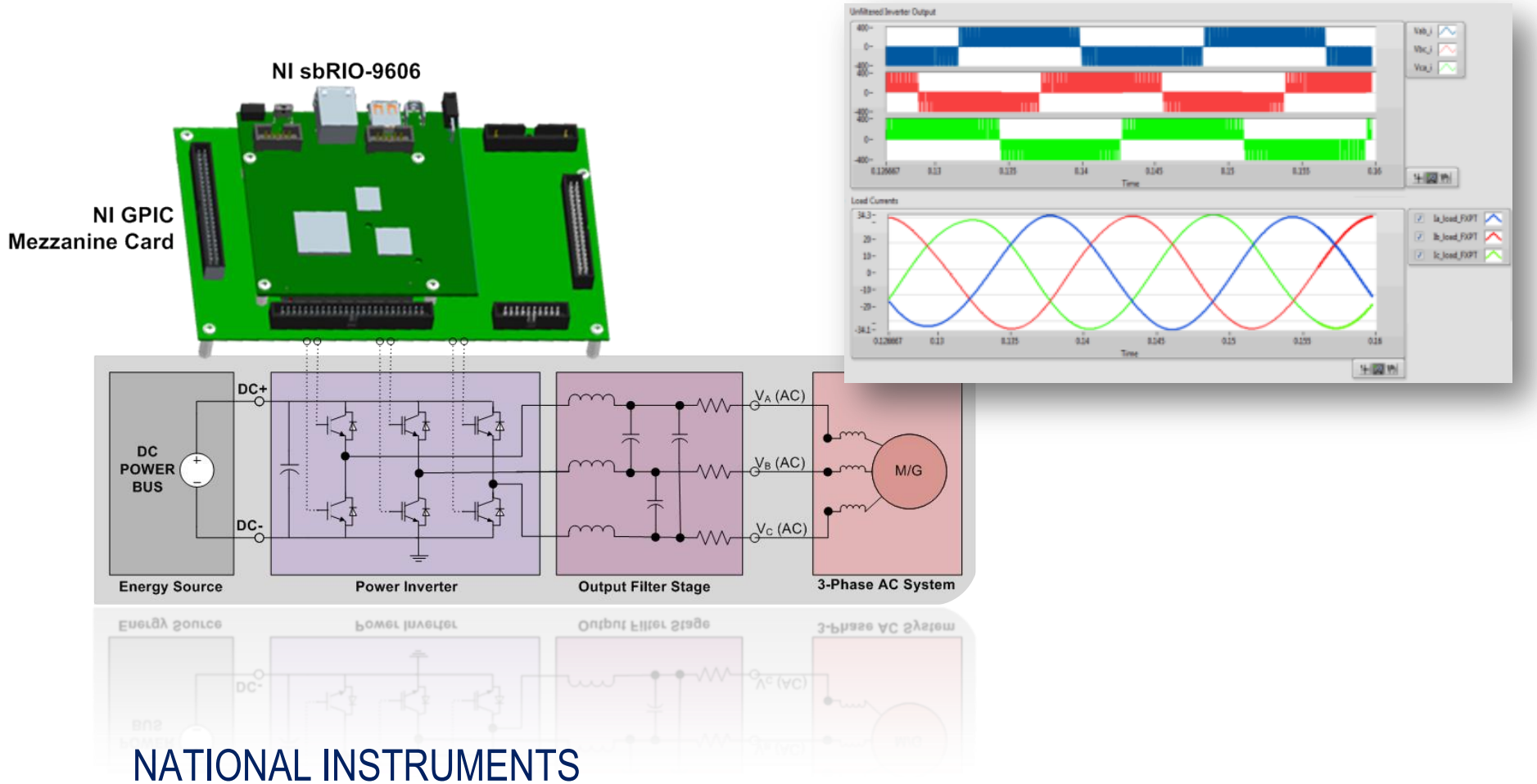
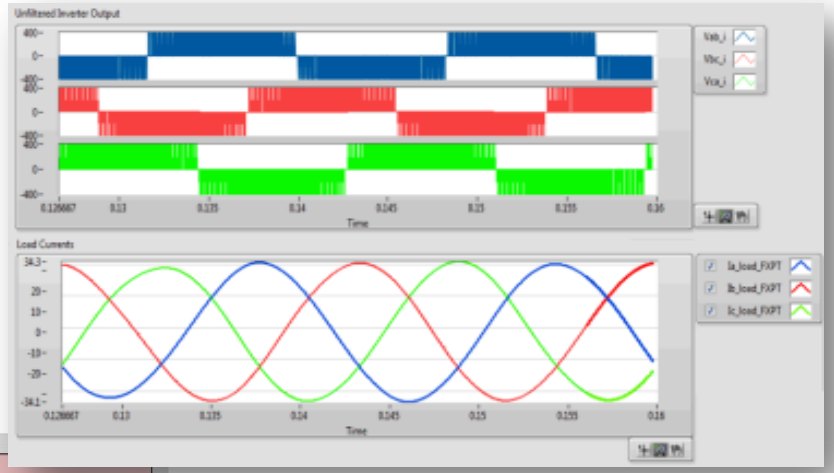


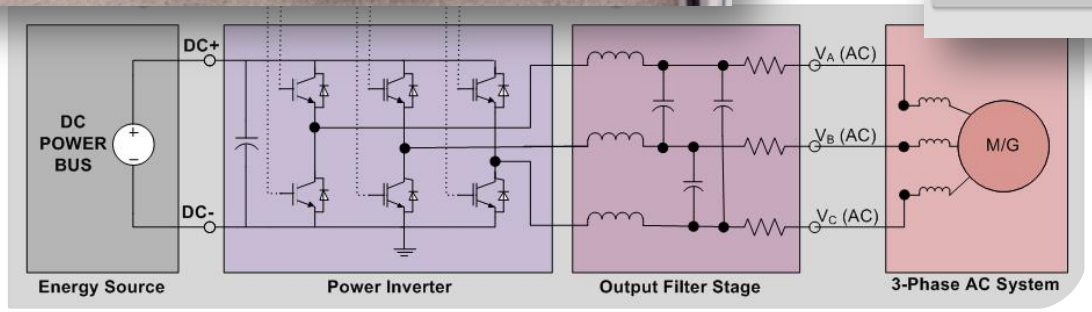




NATIONAL INSTRUMENTS

HIGH VOLUME COMMERCIAL DEPLOYMENT (NI GPIC)

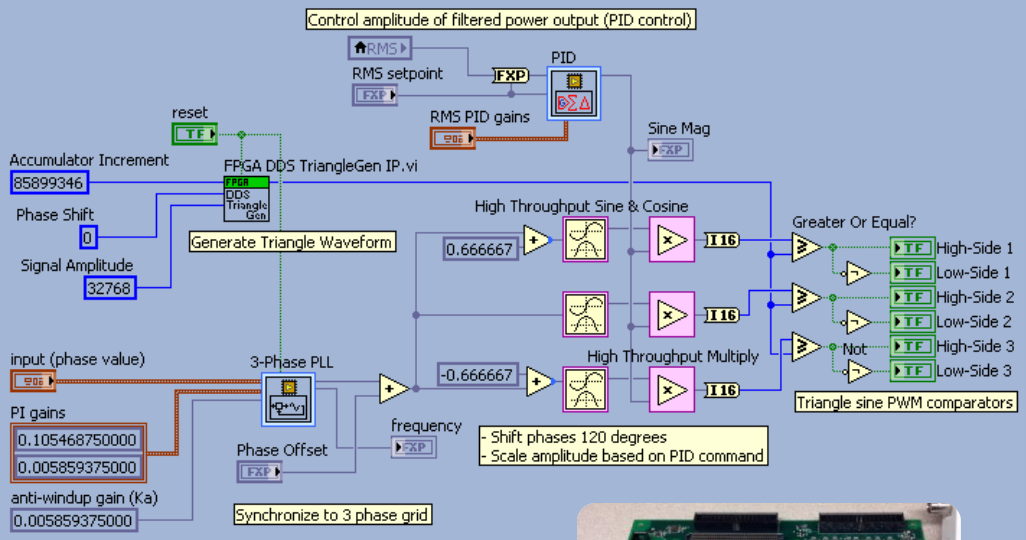


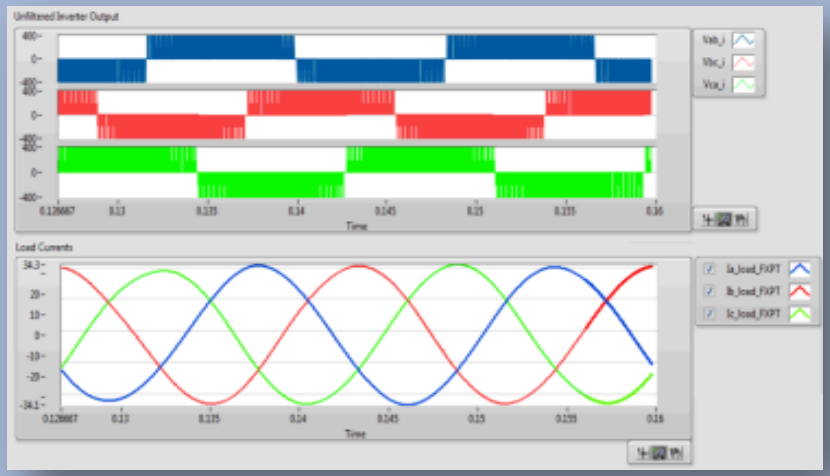


NATIONAL INSTRUMENTS

HIGH VOLUME COMMERCIAL DEPLOYMENT (NI GPIC)

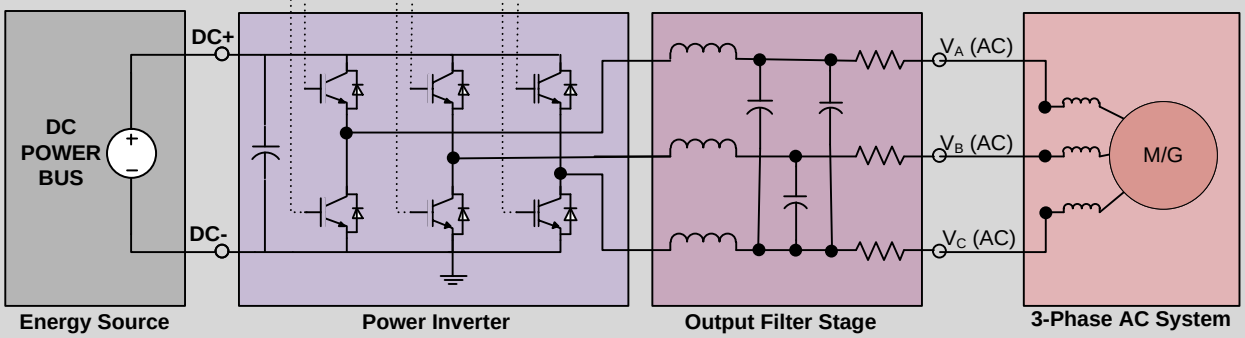
NI Single-Board RIO General Purpose Inverter Controller (GPIC)





CONTROL SYSTEM

NREL
NATIONAL RENEWABLE ENERGY LABORATORY



NI General Purpose Inverter Control (GPIC) System

NI Single-Board RIO General Purpose Inverter Controller *IN DEVELOPMENT*

- Deployment-ready commercial embedded system for high-volume grid-tied inverter, DC/DC converter and motor/generator drives
- High level graphical system design tools and reconfigurable FPGA enable rapid development of highly differentiated control algorithms
- Complete, industry proven LabVIEW tool chain with I/O drivers, IP libraries and tightly integrated simulation tools
- FPGA-based control logic for ultra fast pin-to-pin response time, lifetime upgradeability and IP protection
- Xilinx Spartan-6 LX45 FPGA with 58 DSP cores yielding 4,600 MMAC computing performance and hardware parallel execution
- 400 MHz PowerPC processor with VxWorks RTOS for hard real-time floating point processing, networking, and event capture data logging
- Smart grid utility network protocol support (DNP3, IEC 60870, IEC 61850, Modbus, CAN, …) and onboard real-time 3-phase power and IEC 61000-4-7:2002 harmonic spectra analysis
- 10/100BASE-TX Ethernet port with FTP, HTTP, HTTPS and SSL support and SNTP or IEEE1588 time synchronization
- DMA data scope capabilities for high speed waveform capture and automatically triggered event recording
- Options for depopulation, LEM-style 20-100 mA current sense AI, 16-bit calibrated AI, real-time clock battery, conformal coating, top/bottom/side connectors
- I/O signal compatibility with most standard IGBT intelligent power modules— FUJI, Infineon, Hitachi, Mitsubishi, Powerex, SEMIKRON (SKiiP 3 and 4), Toshiba, …

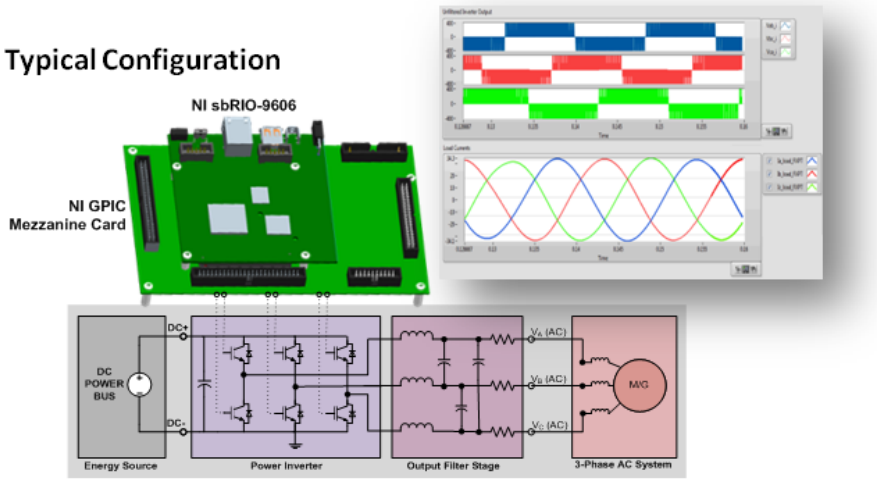
LabVIEW Development Software

- LabVIEW Real-Time (VxWorks) 2011 SP01 or higher
- LabVIEW FPGA 2011 SP01 or higher

Recommended Software

- NI MultiSim Co-Simulation Interface for LabVIEW FPGA (design guide)
- NI Power Electronics IP Library (included with NI SoftMotion 2011 f1)
- NI Electrical Power Measurement Suite
- NI Veristand (for automated real-time virtual/physical testing)
- NI Simulation Interface Toolkit (interface to 3rd party simulator)

Typical Configuration



Download the preliminary datasheet

Worst Case Specifications

PRELIMINARY—SUBJECT TO CHANGE

400 MHz Real-Time Processor

- 256 MB RAM
- 512 MB Non-volatile Storage

Xilinx Reconfigurable FPGA

- Spartan-6 LX 45
- 43,661 logic cells
- 2,088 Kb FPGA RAM
- 22.6 GMACs DSP performance
- 58 DSP48A1 slices (multipliers)

Communication Ports

- 10/100BASE-T Ethernet
- 1 Mbps max CAN
- 115,200 bps max RS-232 Serial
- USB 2.0 Host

Physical Characteristics

- 4.7”x7.08”x1.75” (prelim.)
- 11.9x17.9x4.4 cm (prelim.)
- -40 to 70°C operating temp. range
- -40 to 50°C in still-air enclosure

High Speed Digital Output (to Gate Driver or IPM)

- 12 channels
- Source/sink (push-pull)
- 5-24 VDC, external power
- 10 mA/ch continuous
- 100 Ω output impedance
- ≤100 ns propagation delay
- 25 ns ON/OFF resolution
- 100 kHz max PWM freq. (5V)
- 20 kHz max PWM freq. (24V)
- 10 ns rise/fall time (no load)
- 500 ns min pulse width
- Non-isolated
- Power up state: OFF

General Purpose and Contactor Digital Output

- 28 channels, total
- Sinking driver
- 24 VDC max
- 20 mA/ch continuous
- 1 A total (GP channels)
- ≤1 ms propagation delay
- Non-isolated
- Power up state: OFF

Contactor Relay DO:

- 4 of the 28 channels
- 8 A/ch inrush, 200 mA continuous
- Individual return pin per channel

FPGA Expansion I/O

- 16 channels (min)
- 3.3 V DIO, non-buffered
- Unprotected, very high speed
- Non-isolated

General Purpose Digital Input

- 28 channels
- Sourcing digital input
- 5-24 VDC, external power
- Two banks, 14-ch per bank
- 1-5 kΩ pull-up resistor
- 7 µs min pulse-width
- 200 us propagation delay
- Non-isolated
- ±30 V protection
- Impedance matched for SKiiP 3,4

High Speed Simultaneous Analog Input

- 16 pseudo diff. channels
- Simultaneous sampling
- 100 kSPS/ch, single rate
- 12-bit, ±10 V range
- 0.24% typ. acc.: 25°C±10°C
- 0.81% acc. over temp.
- ≥100 kΩ input impedance
- 100 kHz -3 dB bandwidth
- ±100 mV common mode range
- 2512 shunt resistor pads for LEM
- 60 VDC CAT I bank isolation
- ±30 V protection

General Purpose Analog Input

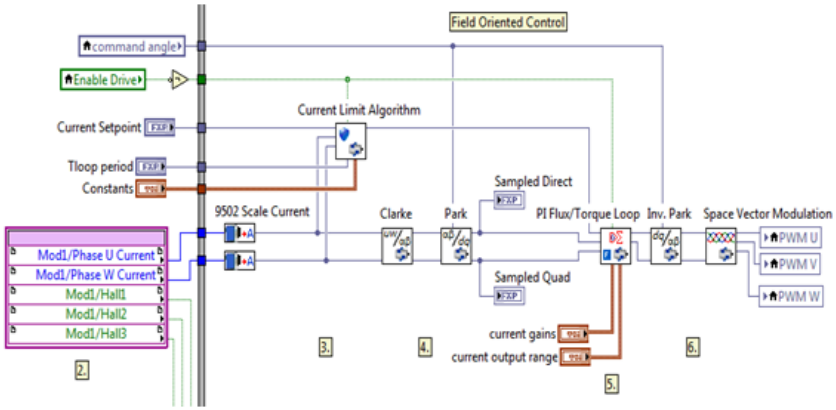
- 8 single-ended channels
- 12-bit, 0-5 V range
- Multiplexed sampling
- 1 kSPS scan rate, all chan.
- 1% accuracy over temp.
- 100 kΩ input impedance
- 100 kHz -3 dB bandwidth
- 60 V CAT I isolation
- ±30 V protection

General Purpose Analog Output

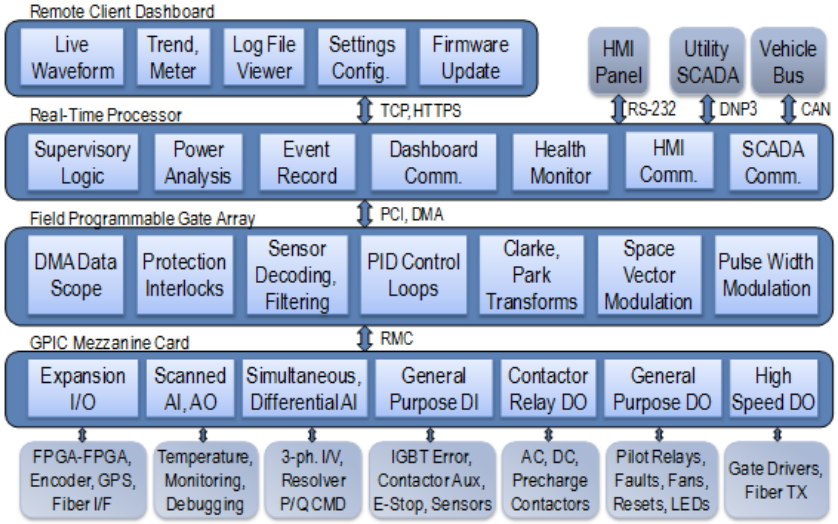
- 8 single-ended channels
- 12-bit, 0-5 V range
- Simultaneous update
- 1 kSPS update rate
- 1% accuracy over temp.
- 4 mA/ch output current
- 60 VDC CAT I isolation
- Power on state: 0 V

NI Power Electronics IP Library

- Completely editable reference design examples for space vector field oriented control and trapezoidal commutation
- Included with NI LabVIEW NI SoftMotion Module 2011 f1 or higher
- Full desktop validation of FPGA control algorithms using NI Multisim co-simulation tools (video)

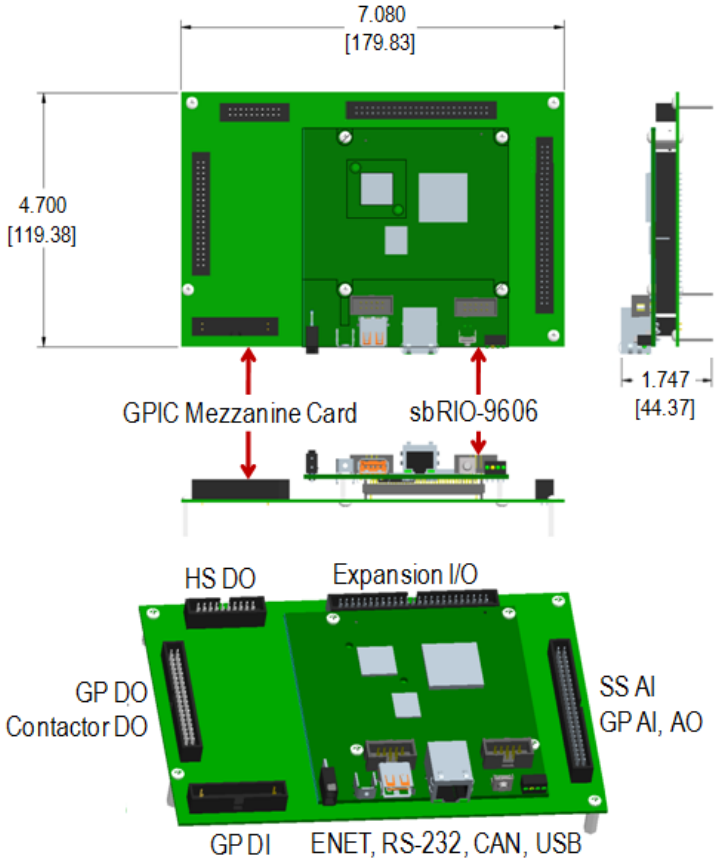


Typical Software Elements



Mechanical Design

- Standard 0.1" header connectors with high retention force (non-latching)
- Mating board options:
  - Ribbon cable to gate drive board
  - Connector interface and signal conditioning PCB with custom cable harness
  - Fiber optic interface or GPS time synch PCB
  - Directly mate to gate drive board

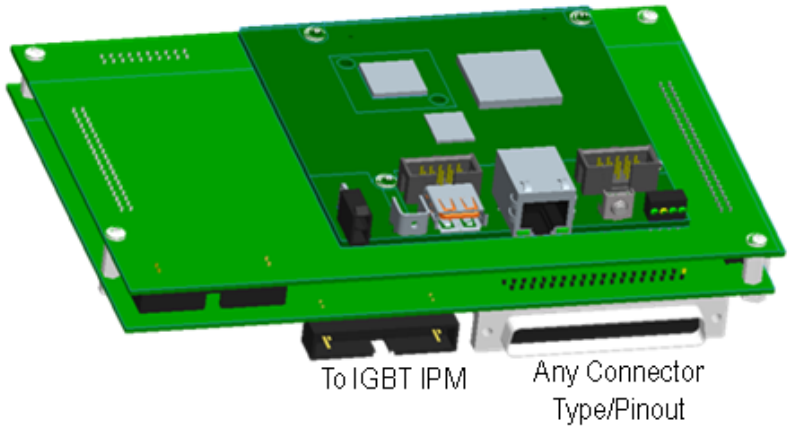


I/O Connectors

High Speed Digital Output (Gate Drive) *(20-pin 100 mil header)*	• 12-ch HS DO (18-pins, 6 GND) • 1 V_{PWR_IN} (1-pin) • 1-pin reserved
General Purpose and Contactor Digital Output *(40-pin 100 mil header)*	• 24-ch GP DO (28-pins, 4 GND) • 4-ch Contactor DO (8-pins, 4 GND) • 4-pins reserved
FPGA and Processor Expansion I/O *(50-pin 100 mil header)*	• 16-ch +3.3 V FPGA IO (24-pins, 8 GND) • +3.3 V $FPGA_{PWR\_IN}$ (1-pin) • +5 V SYS_{PWR_OUT} (1-pin) • 24-pins reserved
General Purpose Digital Input *(26-pin 100 mil header)*	• 24-ch GP DI (26-pins, 2 V_{PWR_IN})
High Speed Simultaneous Analog Input, General Purpose Scanned AI, General Purpose AO *(60-pin 100 mil header)*	• 16-ch Differential SS AI (32 pins) • 8-ch Scanned GP AI (9-pins,1 COM) • 8-ch GP AO (9-pins, 1 COM) • 10-pins reserved

Typical Stack

1. NI Single-Board RIO Control & Monitoring System (sbRIO-9606)
2. NI GPIC RIO Mezzanine Card (bottom orientation connectors)
3. User defined cable interface, gate drive or signal conditioning PCB (not provided by NI)

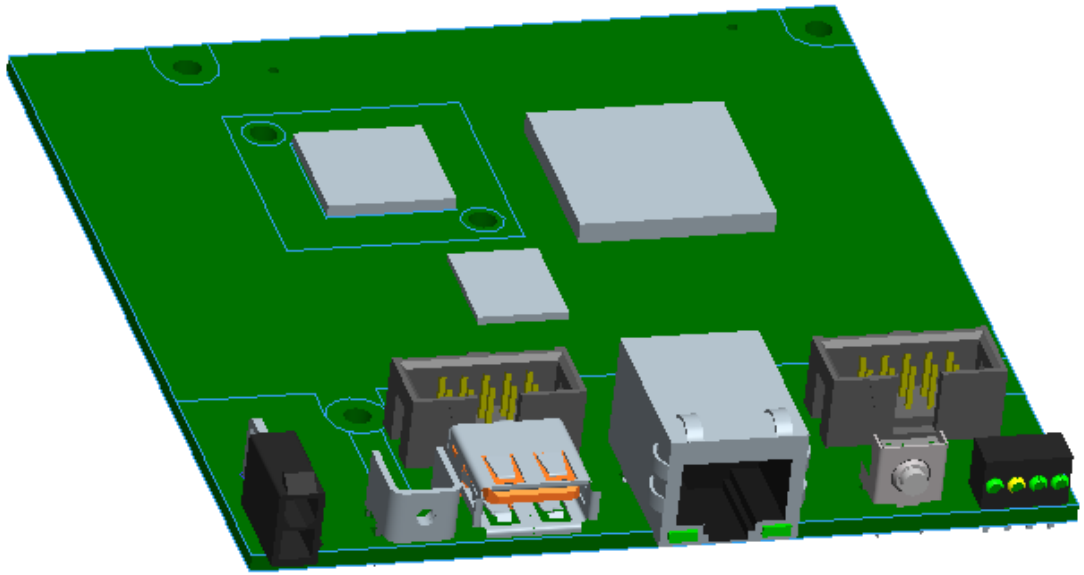


NATIONAL INSTRUMENTS™

ni.com/powerdev

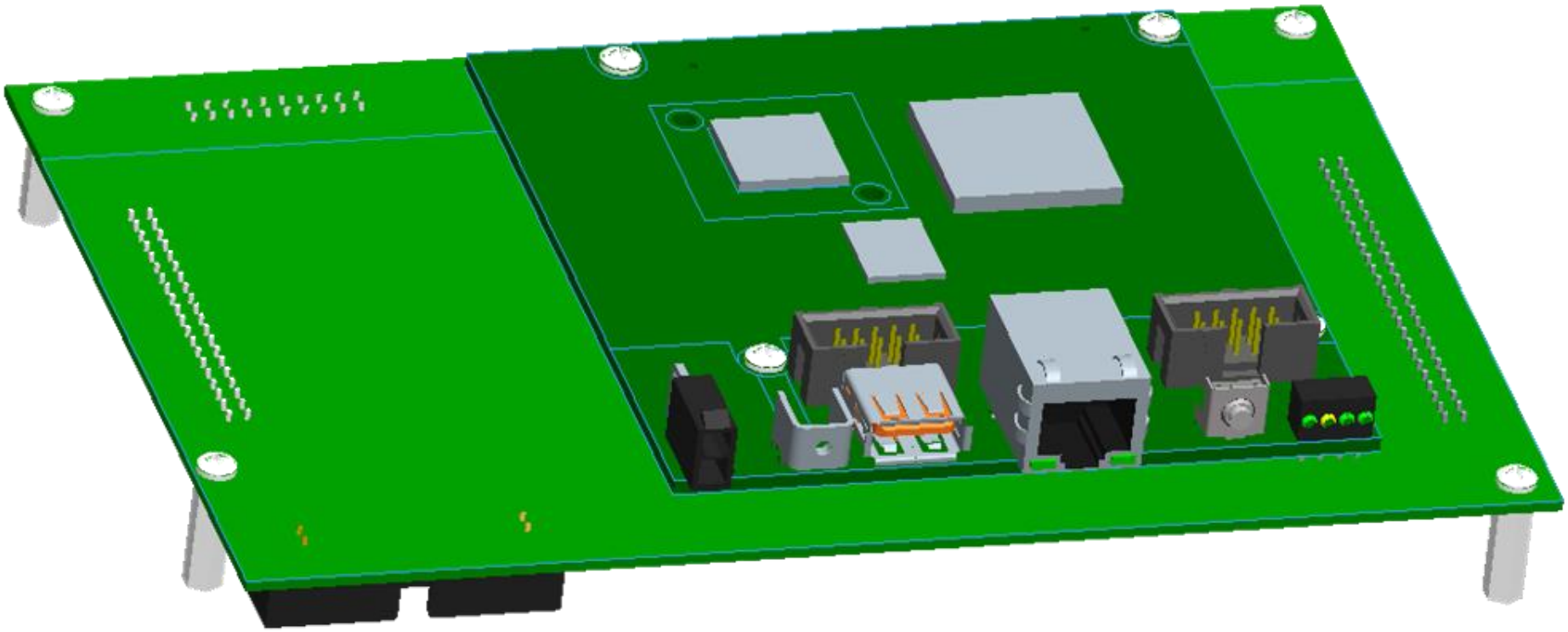
Typical Stack

1. NI Single-Board RIO sbRIO-9606



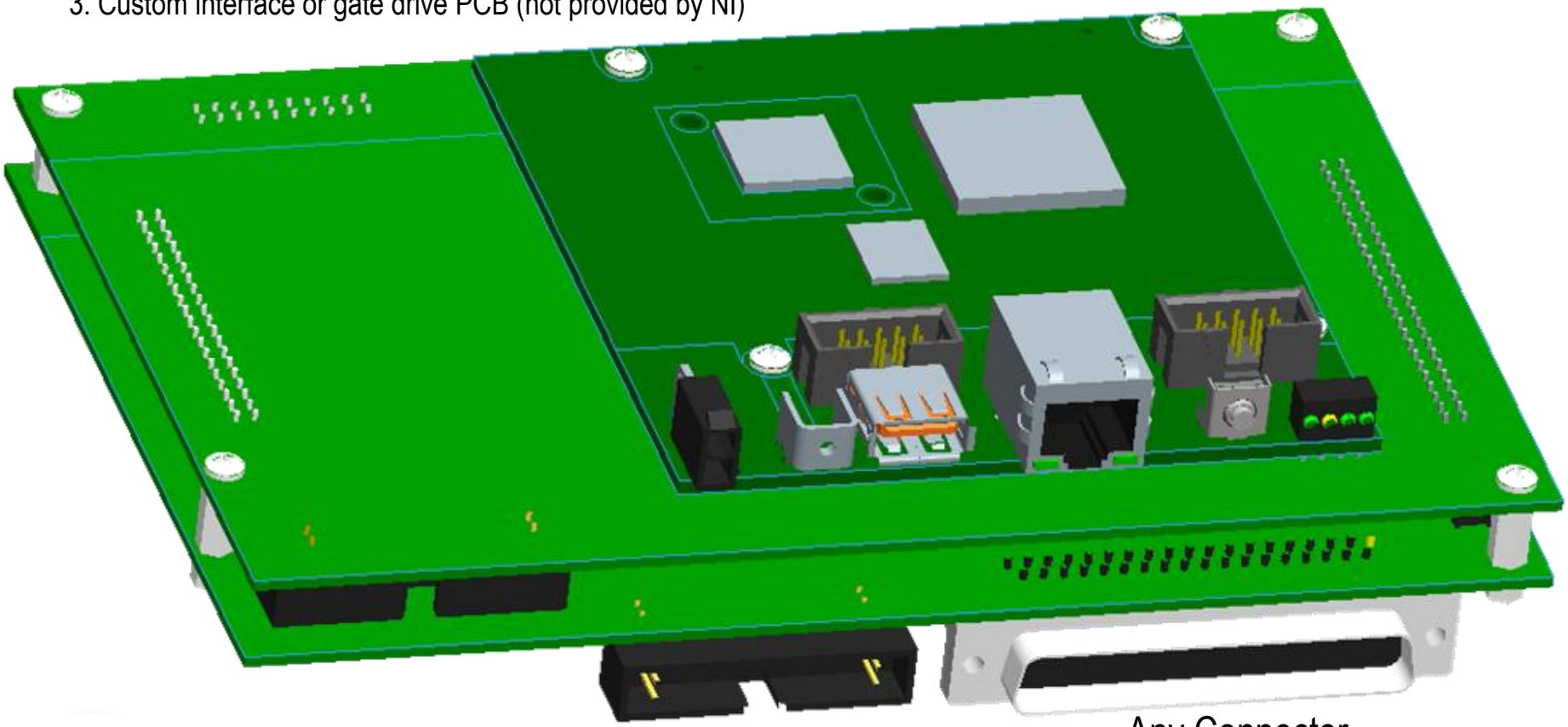
Typical Stack

1. NI Single-Board RIO sbRIO-9606
2. NI GPIC RIO Mezzanine Card (bottom orientation connectors)



Typical Stack

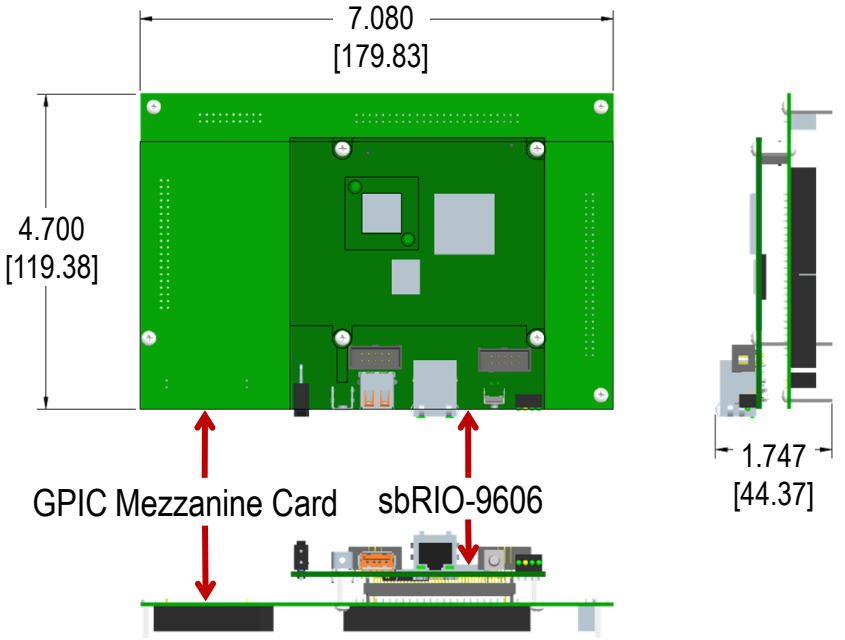
1. NI Single-Board RIO sbRIO-9606
2. NI GPIC RIO Mezzanine Card (bottom orientation connectors)
3. Custom interface or gate drive PCB (not provided by NI)

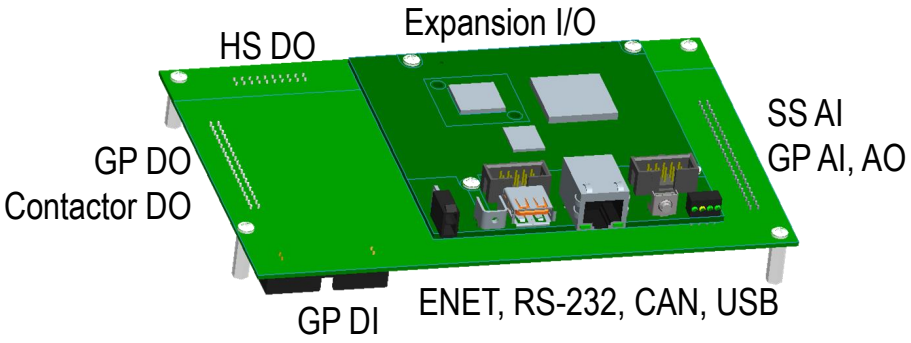


Mechanical Design

High Speed Digital Output (Gate Drive) *(20-pin 100 mil header)*	• 12-ch HS DO (18-pins, 6 GND) • 1 V_{PWR_IN} (1-pin) • 1-pin reserved
General Purpose and Contactor Digital Output *(40-pin 100 mil header)*	• 24-ch GP DO (28-pins, 4 GND) • 4-ch Contactor DO (8-pins, 4 GND) • 4-pins reserved
FPGA and Processor Expansion I/O *(50-pin 100 mil header)*	• 16-ch +3.3 V FPGA IO (24-pins, 8 GND) • +3.3 V $FPGA_{PWR\_IN}$ (1-pin) • +5 V SYS_{PWR_OUT} (1-pin) • 24-pins reserved
General Purpose Digital Input *(26-pin 100 mil header)*	• 24-ch GP DI (26-pins, 2 V_{PWR_IN})
High Speed Simultaneous AI, General Purpose Scanned AI , General Purpose AO *(60-pin 100 mil header)*	• 16-ch Differential SS AI (32 pins) • 8-ch Scanned GP AI (9-pins,1 COM) • 8-ch GP AO (9-pins, 1 COM) • 10-pins reserved

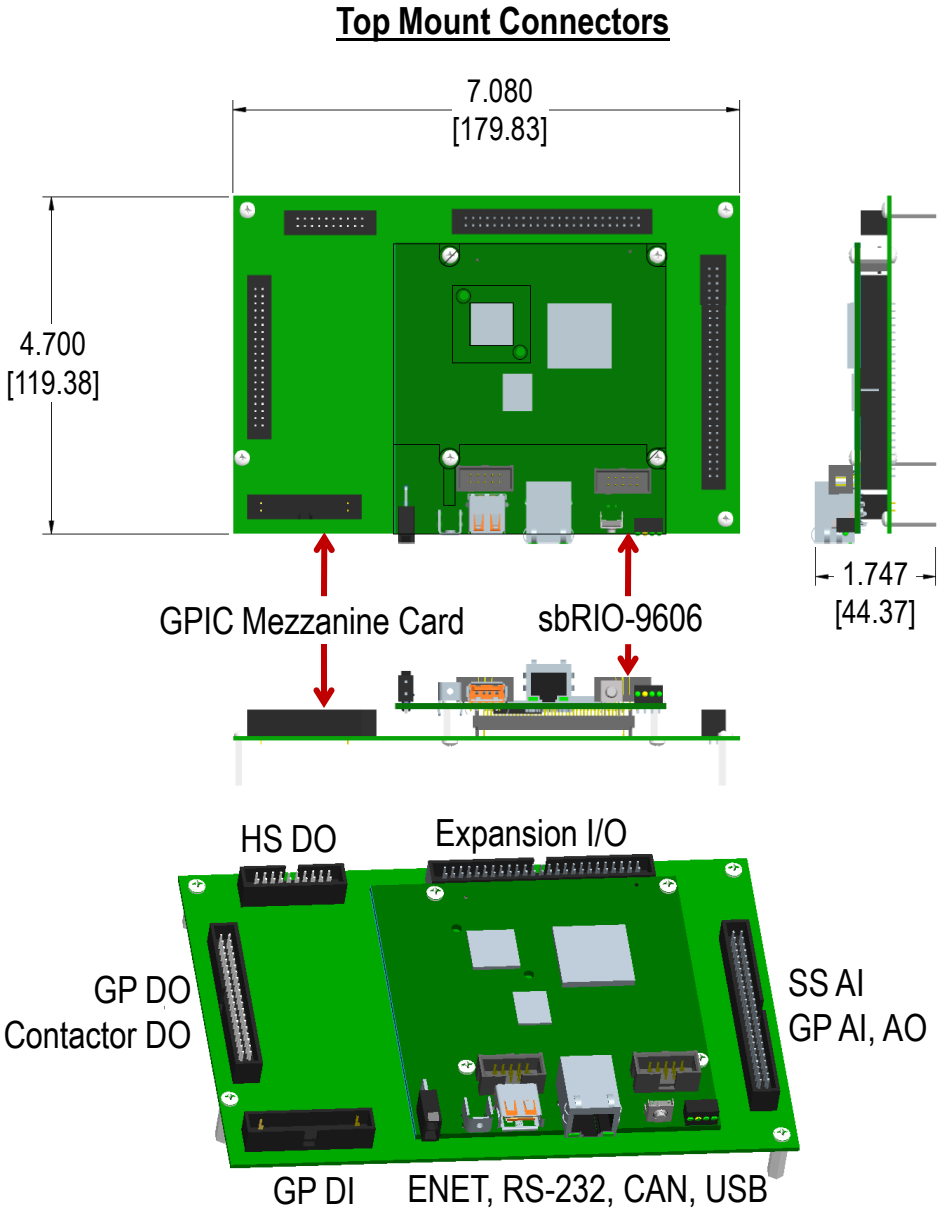
Bottom Mount Connectors





Mechanical Design

- Sturdy 100-mil header connectors with high retention force (non-latching)
- Support for bottom, top and right-angle connector orientations
- Mating board options:
  - Ribbon cable to gate drive board
  - Connector interface PCB with custom cable harness
  - Signal conditioning PCB with custom cable harness
  - Fiber optic interface PCB
  - Directly mate to gate drive board



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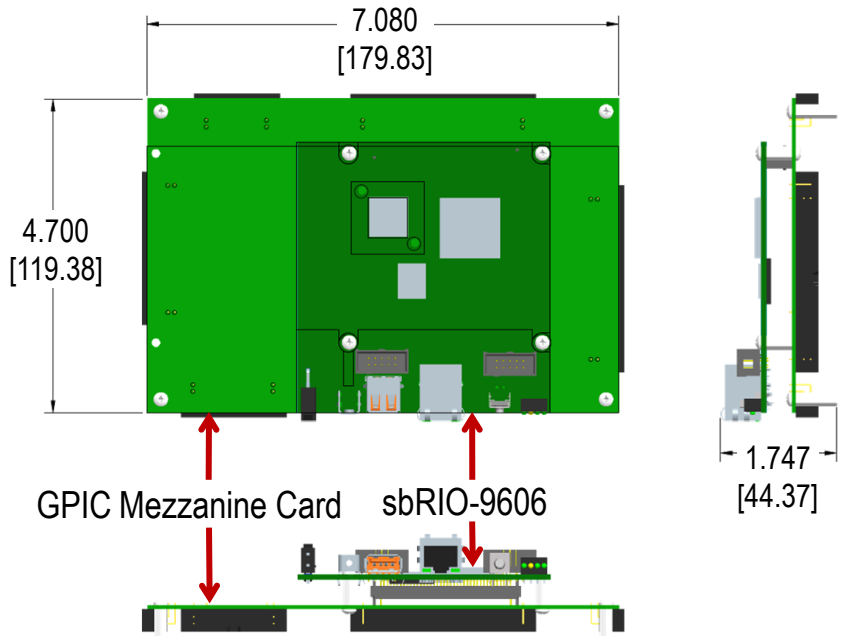
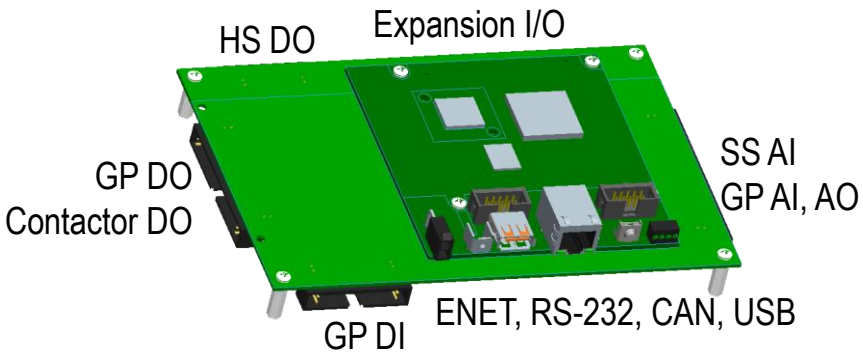
Right-Angle Connectors

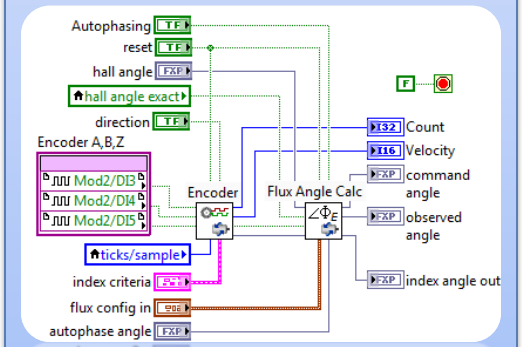




NI Single-Board RIO 960x

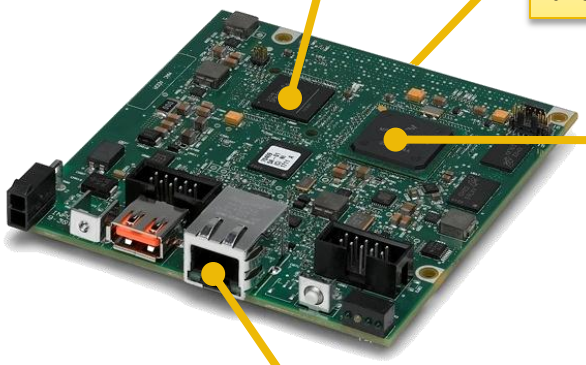
LabVIEW Tool Chain

- Rapid commercialization of differentiated, high performance products
- Complete, industry proven graphical system design tools
- Available IP block libraries and reference design examples
- Fully integrated support for processor, FPGA , I/O and networking in single language
- Integrate existing C, VHDL, simulation or text-based math code



Reconfigurable FPGA
Silicon level reconfigurability, lifetime upgradability, true parallel execution in dedicated hardware

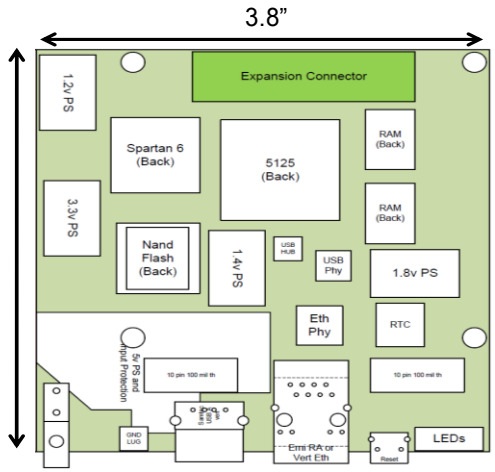
RIO Mezzanine Connector (RMC)
High density, high bandwidth connector gives direct access to FPGA and processor I/O

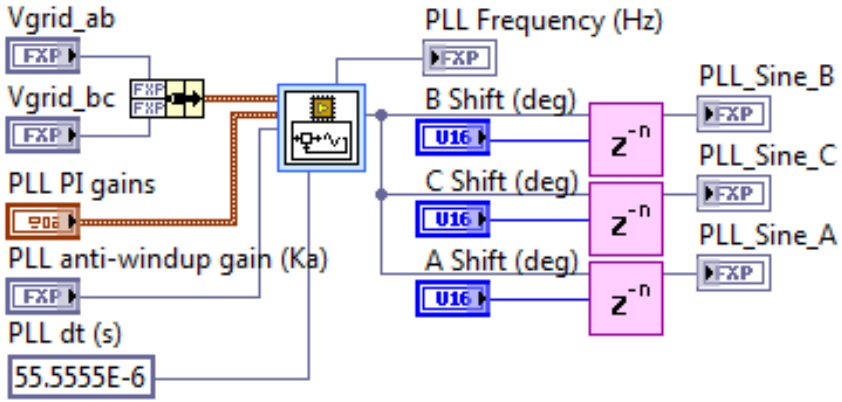


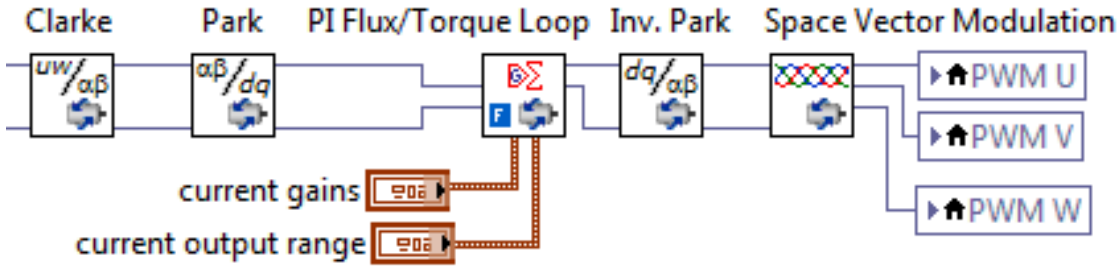
Real-Time Processor
400 MHz PowerPC for floating-point control, analysis, logging and network communication

Networking Peripherals
Ethernet, RS-232, CAN, USB
Modbus, DNP3, HTTPS and SSL support

Small Size, Low Power
10.3 x 9.6 cm (4 x 3.8 in.)
9-30 VDC power



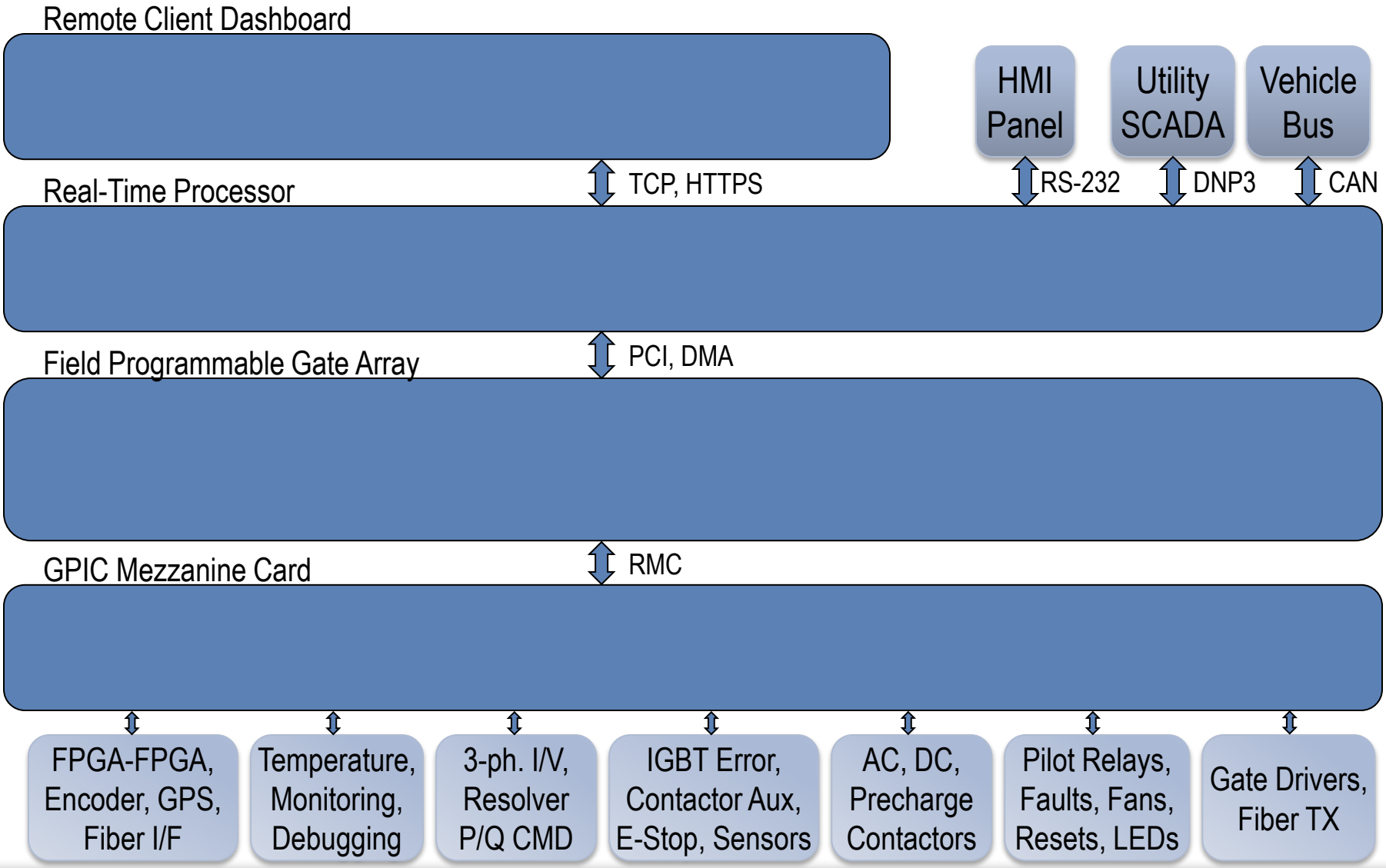




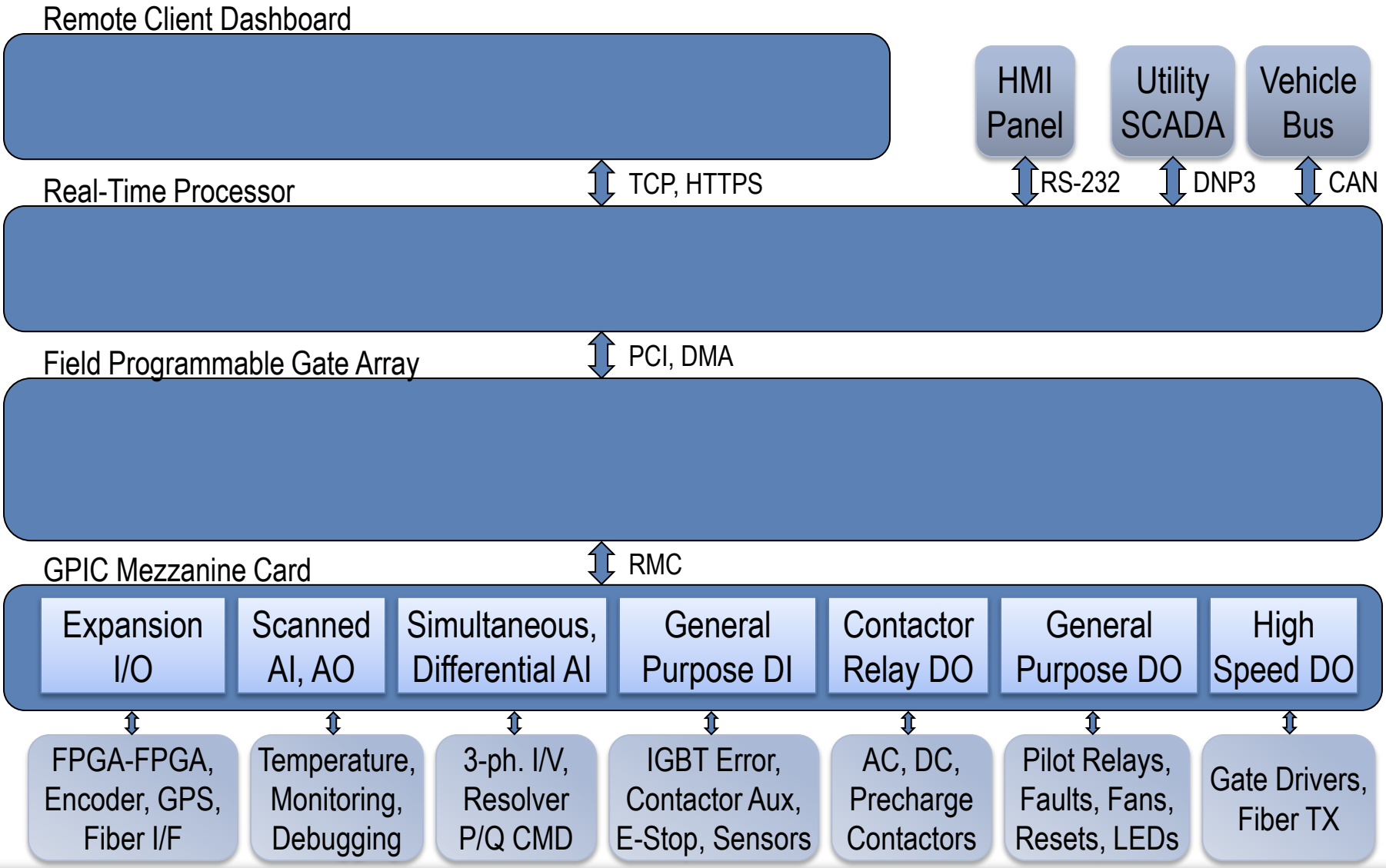
NATIONAL INSTRUMENTS

POWER ELECTRONICS IP

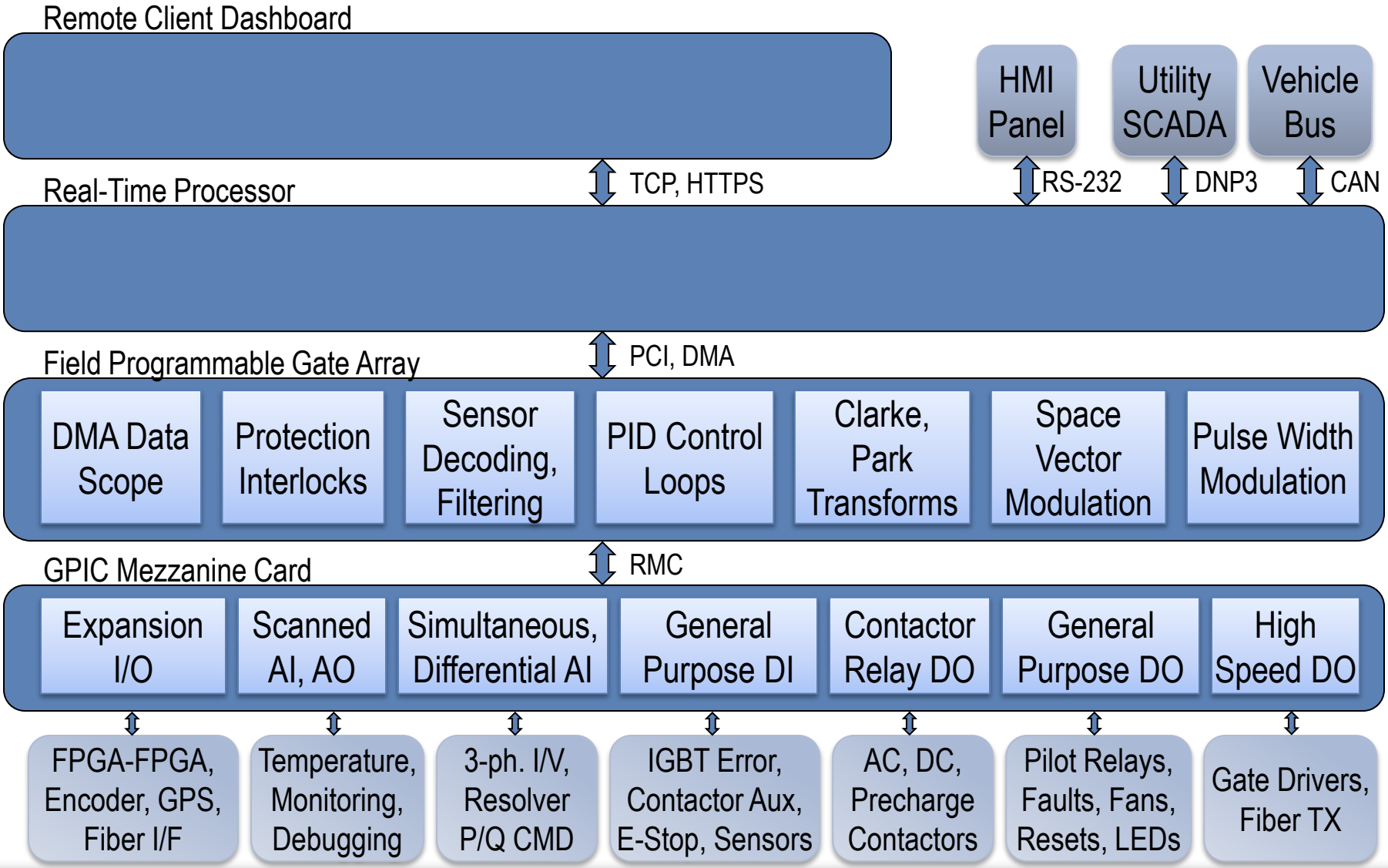
Typical Software Hierarchy Elements



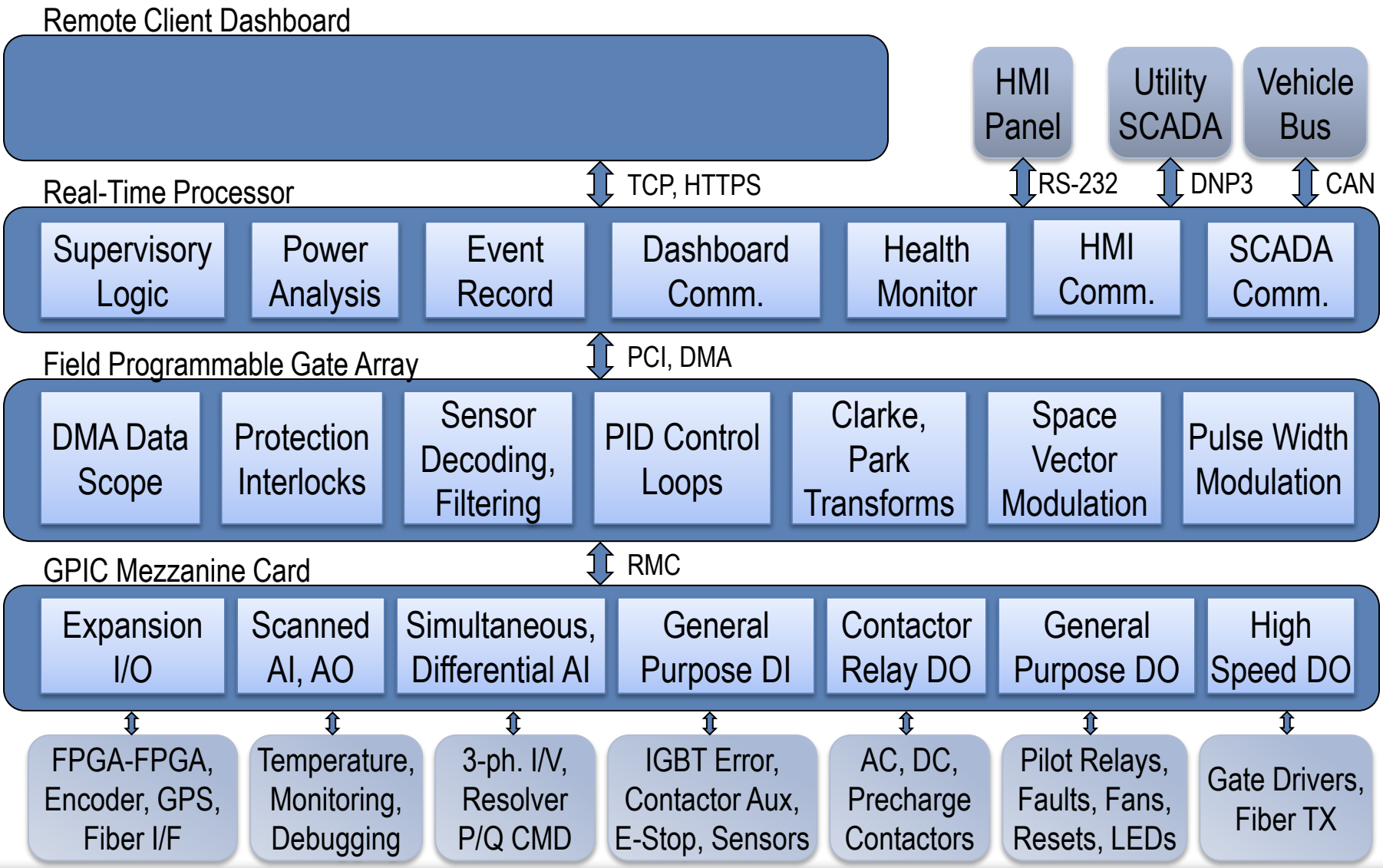
Typical Software Hierarchy Elements



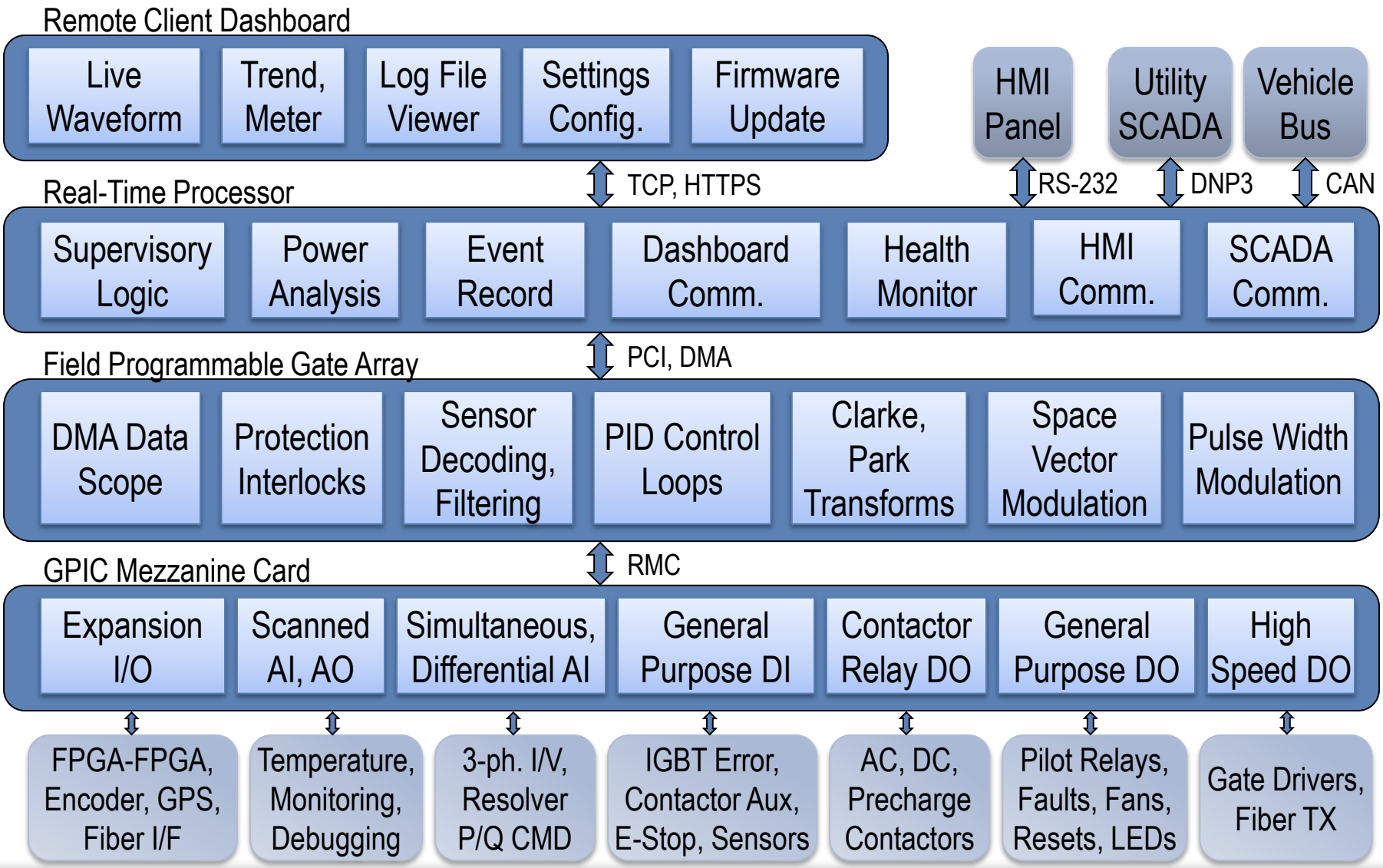
Typical Software Hierarchy Elements



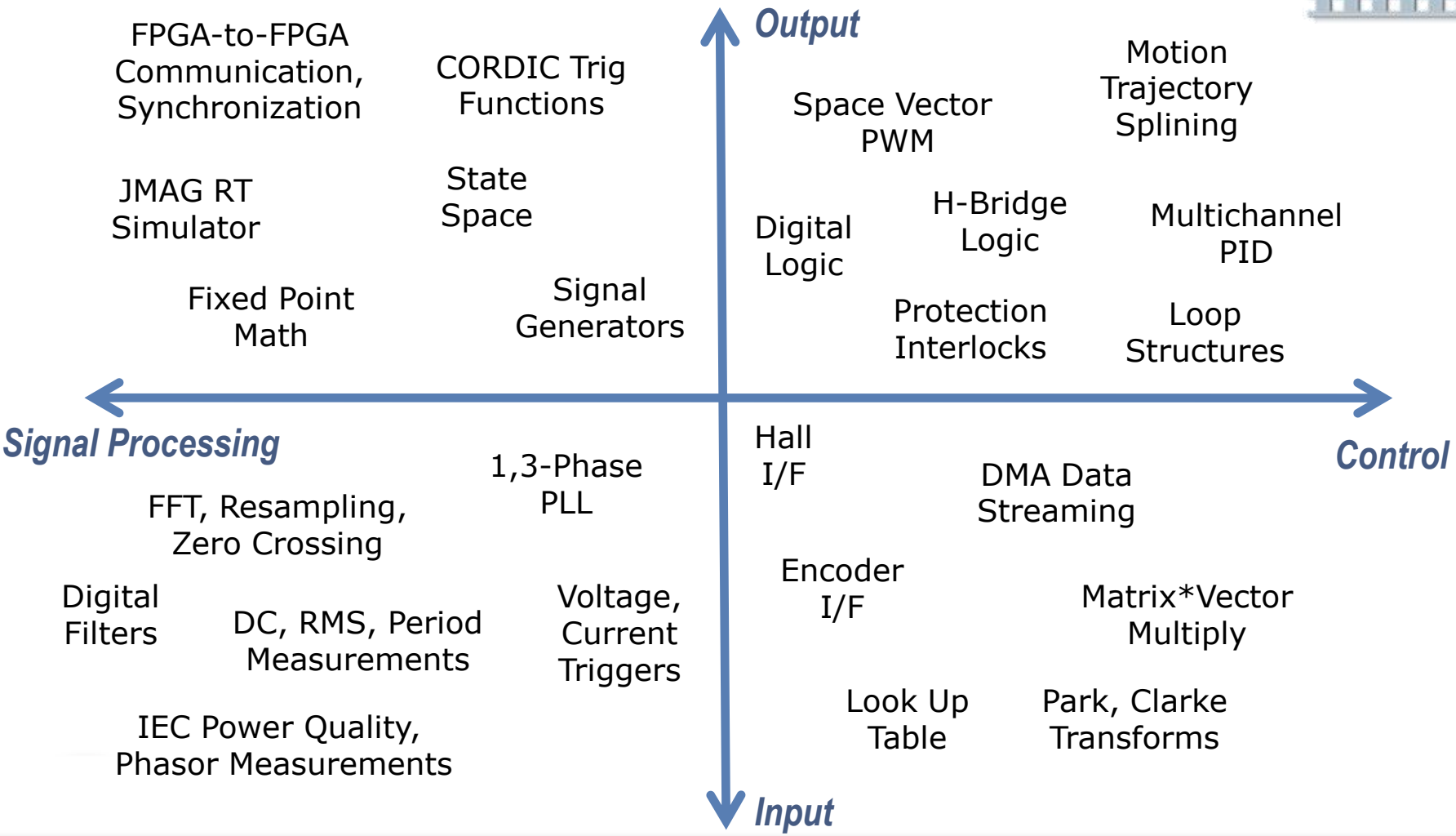
Typical Software Hierarchy Elements



Typical Software Hierarchy Elements

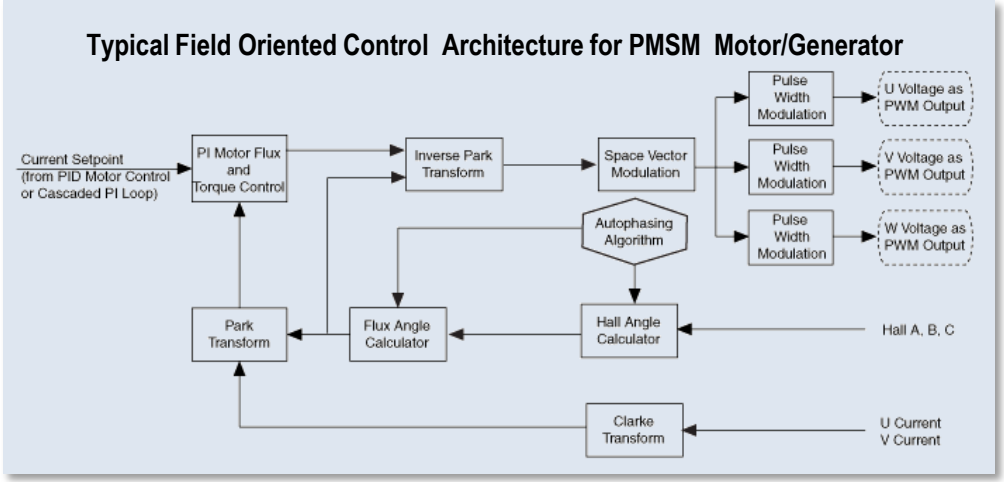


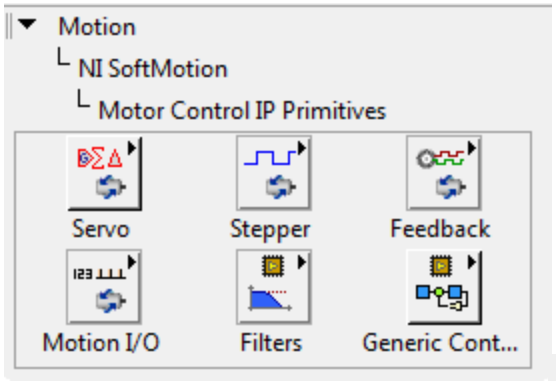
LabVIEW FPGA Power Electronics IP

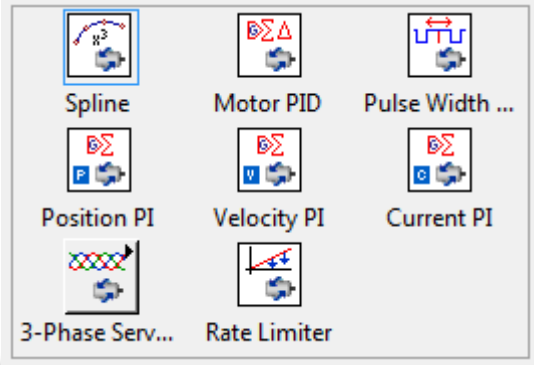


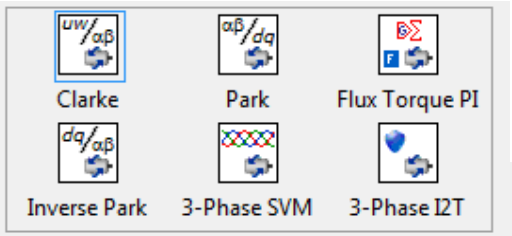
NI Power Electronics IP Library*

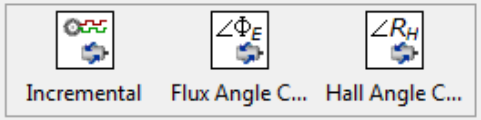
- New officially supported IP blocks for power electronics control, including Trapezoidal and Space Vector commutation for three phase inverters and PMSM/BLDC motor/generators!

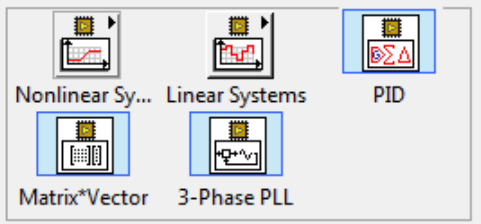






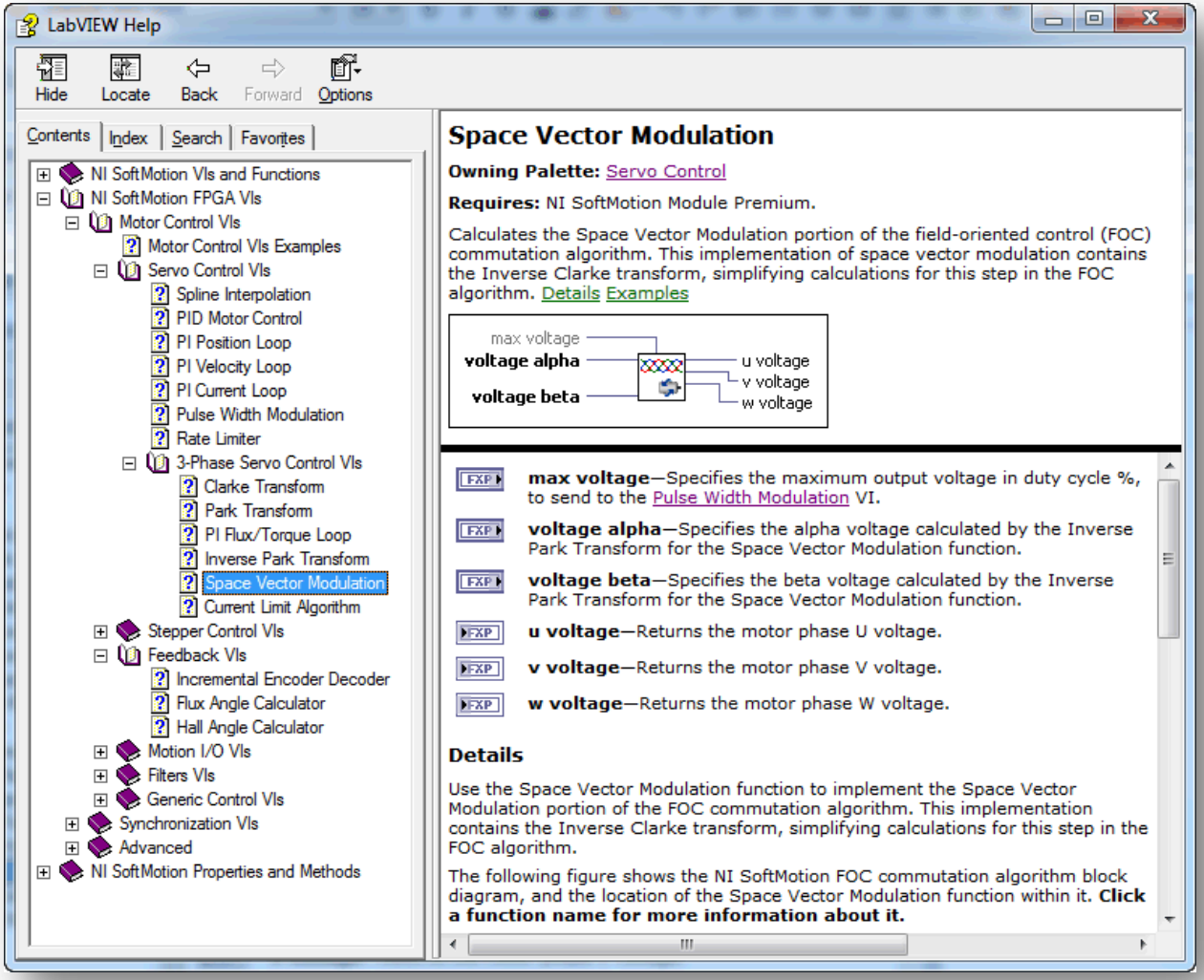




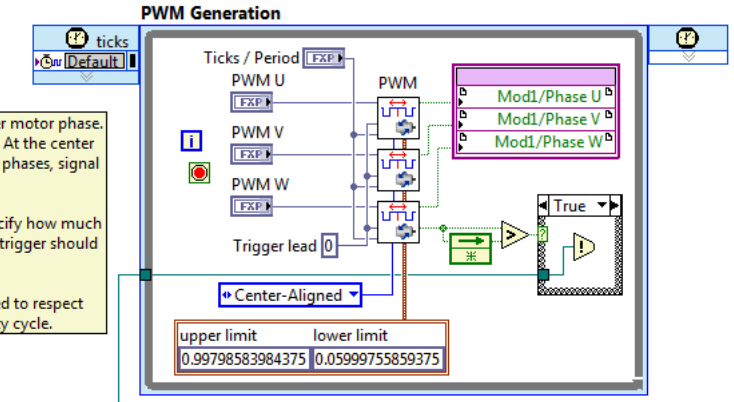


* Included with NI SoftMotion Module 2011 f1 or higher

NI Power Electronics IP Library



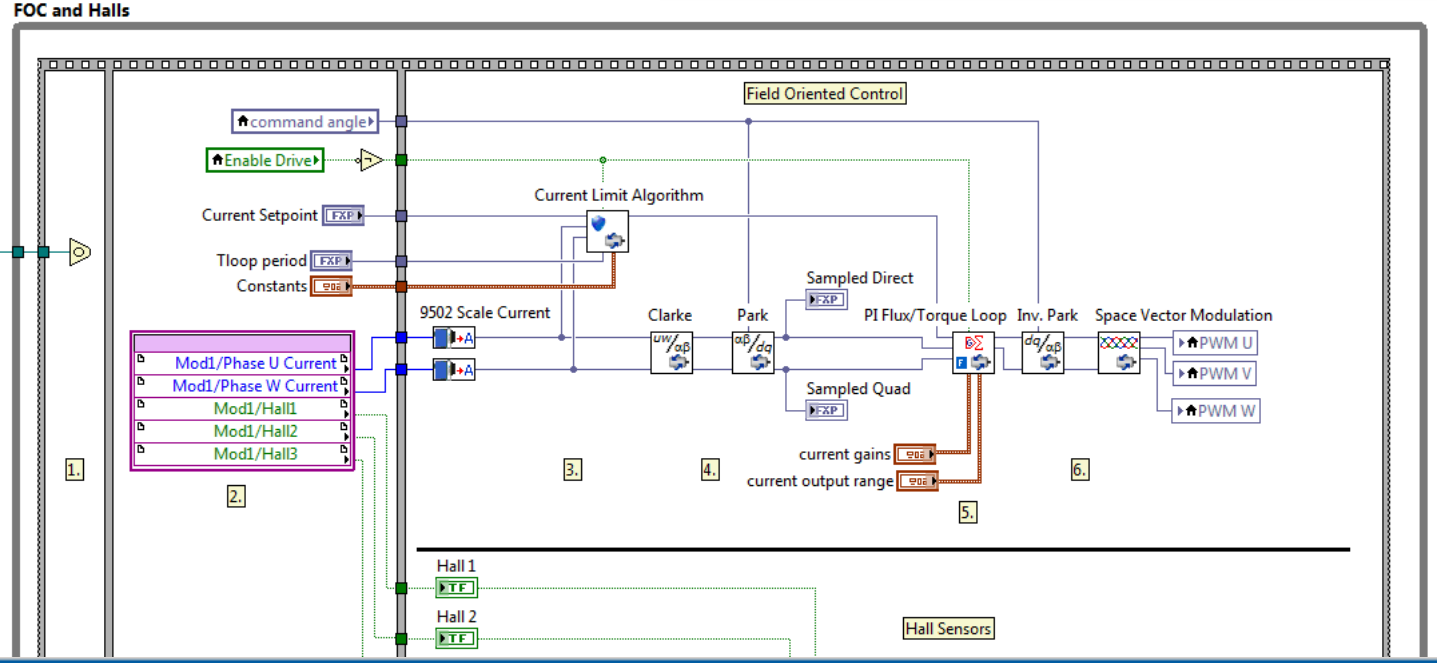
NI Power Electronics IP Library



Generate three PWM signals, one per motor phase. The three signals are center aligned. At the center point, which is common to all three phases, signal the current loop to take a sample.

The Trigger lead can be used to specify how much earlier than the center point the the trigger should fire.

The output range of the PWM is used to respect hardware-imposed limits on the duty cycle.



The FOC algorithm

1. Wait for the midpoint of the PWM to sample current.
2. Inputs from the 9502 should all be read in the same node to avoid any timing problems.
3. Calculate the current through phase V.
4. Using Clarke and Park algorithms convert the three AC phase currents in the static frame of reference to two DC vectors, a parallel and perpendicular, in a frame of reference that rotates with the rotor.
5. Control the two DC currents.
6. Using Inverse Parke and a modified Clarke and Space Vector Modulation algorithm, convert the controlled voltages to PWMs on the three phases.

The NI 9502 can output a maximum 94% duty cycle.

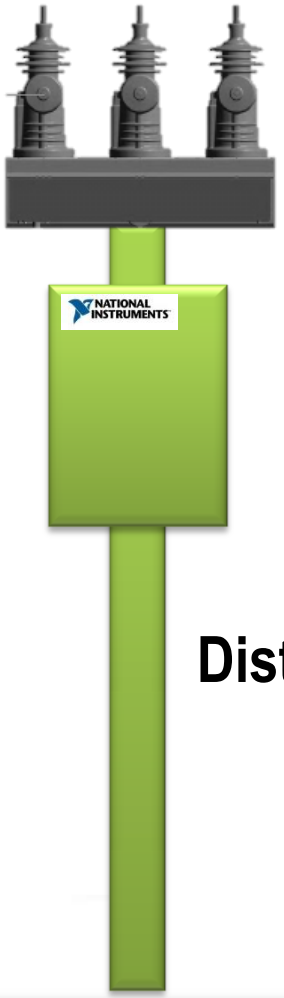
Current Sample Sync

- Complete reference design examples for Field Oriented (Space Vector) and Trapezoidal Commutation
- Plug and play support for the NI 9502 BLDC/PMSM drive module and AKM brushless servo motors.

New! LabVIEW Electrical Power Measurement Suite

Voltage and Current	Power and Energy	Power Quality
Three Phase RMS (V and I)	Power per Phase	Voltage Sag (dip)
THD	Three Phase or Total	Voltage Swell
Harmonic (up to 64th)	Power Factor	Impulsive Transient (V + I)
Interharmonics (0.5 to 63.5th)	Active Power Total	Oscillatory Transient (V + I)
Voltage Unbalance	Active Power Harmonic	Overvoltage and undervoltage
Frequency Oscillation	Apparent Power Total	Overcurrent
Flicker	Apparent Power Harmonic	Phasor Imbalance
DC Portion	Reactive Power	Three Phase Voltage Harmonic
	Reactive Power Harmonic	Four Current Harmonic
	Energy Active Total	Harmonic per sec and per cycle
	Energy Apparent Total and +/-	Synchrophasor IEEE-C37.118
	Energy Reactive Total and L/C	

Advanced Smart Distribution Switch



- Advanced analytics for distribution automation
- Development and introduction of advanced switching features
- Embedded electrical power measurements and monitoring
- Wireless communication for configuration and file transfer
- Remote updates, configuration and firmware upgrades

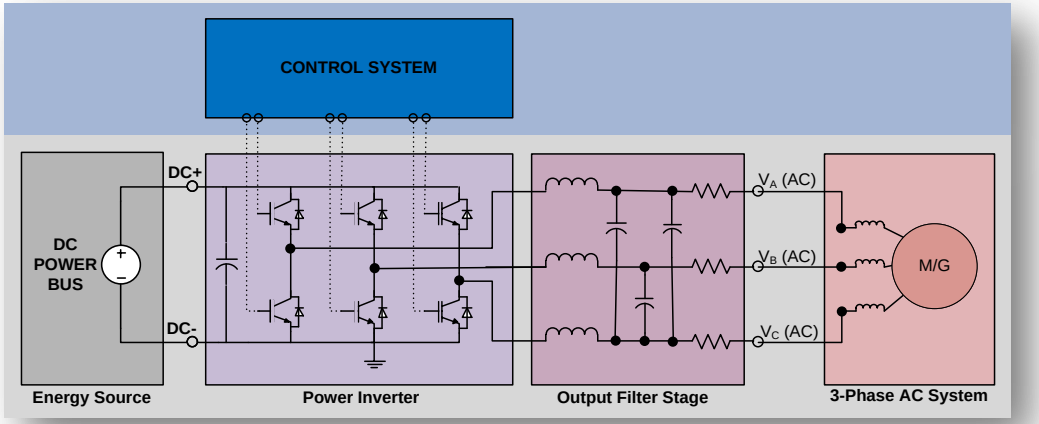
NATIONAL INSTRUMENTS

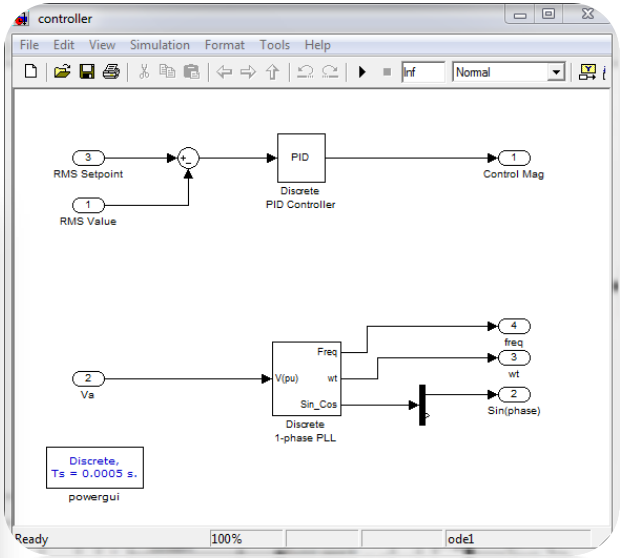
Distribution Switch

- *Rated Through 38kV*
- *Vacuum Interruption Technology*
- *Integrated CTs & Voltage Sensors*
- *Optional future upgrades*
  - *ANSI / IEEE C37.60*
  - *3-phase protection*

Analytics (NI Smart Grid Analyzer)

- *833 Samples/Cycle, 24-bit Resolution*
- *Advanced Embedded Analytics*
- *Data Storage, 1000+ event captures*
- *Remote upgrade*
- *Multi Protocol Communications*





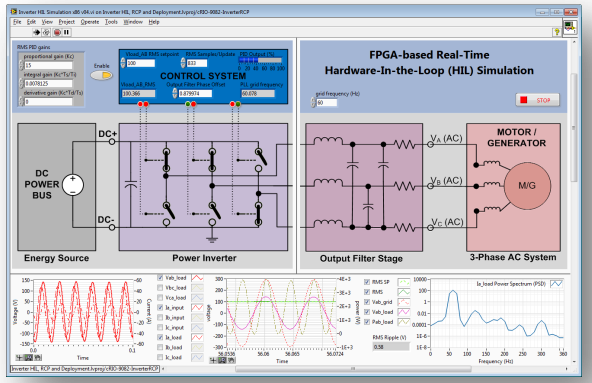
NATIONAL INSTRUMENTS

RAPID CONTROL PROTOTYPING

Rapid Control Prototyping (RCP)

- **Recommended Software**
  - NI LabVIEW Real-Time
  - NI LabVIEW FPGA
  - NI MultiSim 12 or higher
  - NI Control Design & Simulation Module
  - NI Power Electronics IP Library (included with NI SoftMotion 2011 f1)
  - NI Electrical Power Measurement Suite
  - NI Veristand (for control prototyping and real-time HIL simulation)
  - NI Simulation Interface Toolkit
  - NI Teststand (for automated testing)
  - NI Unit Test Framework

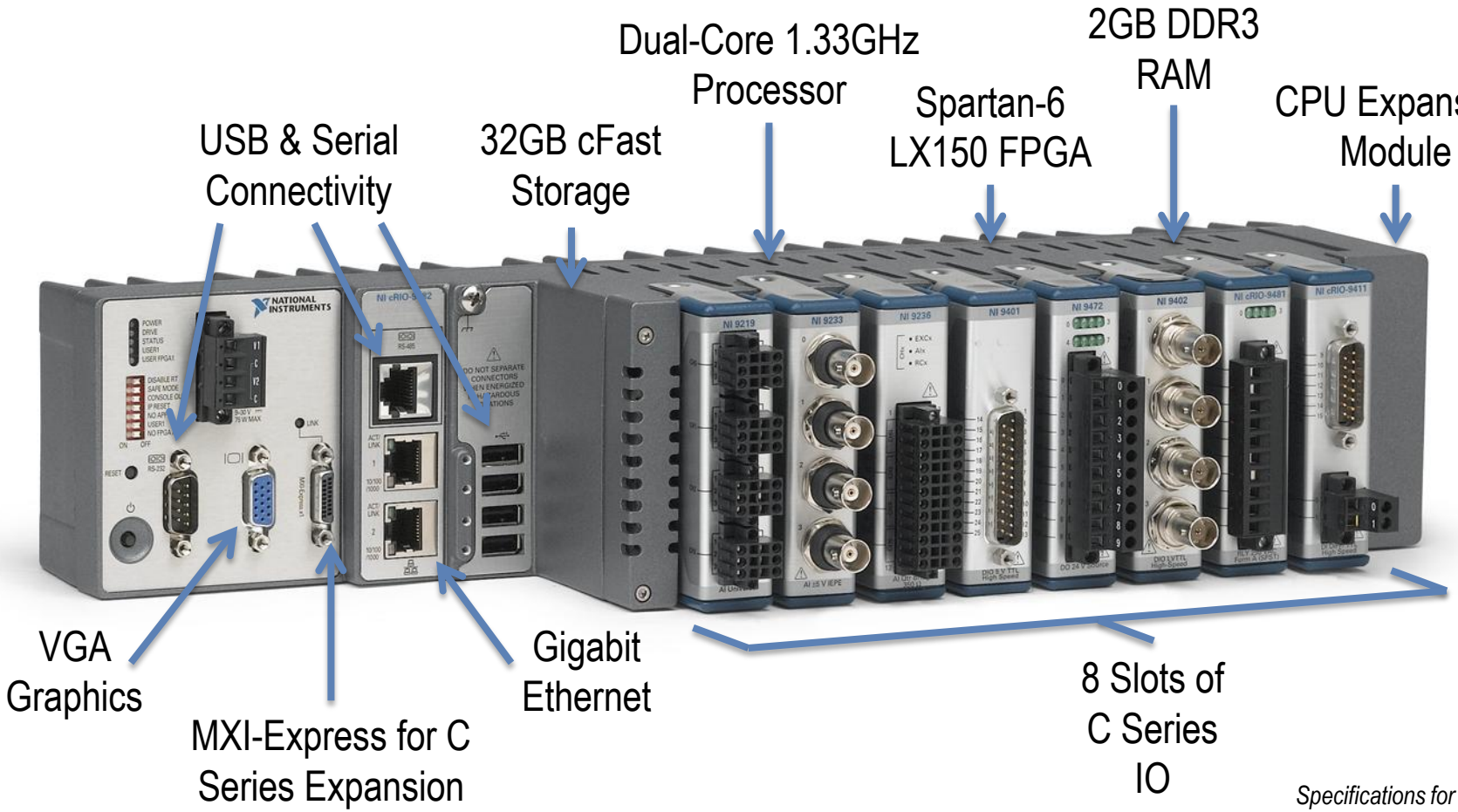
High-Performance Multicore CompactRIO



Power Electronics Design Guide Code

Download the design guide at ni.com/powerdev

High-Performance Multicore CompactRIO

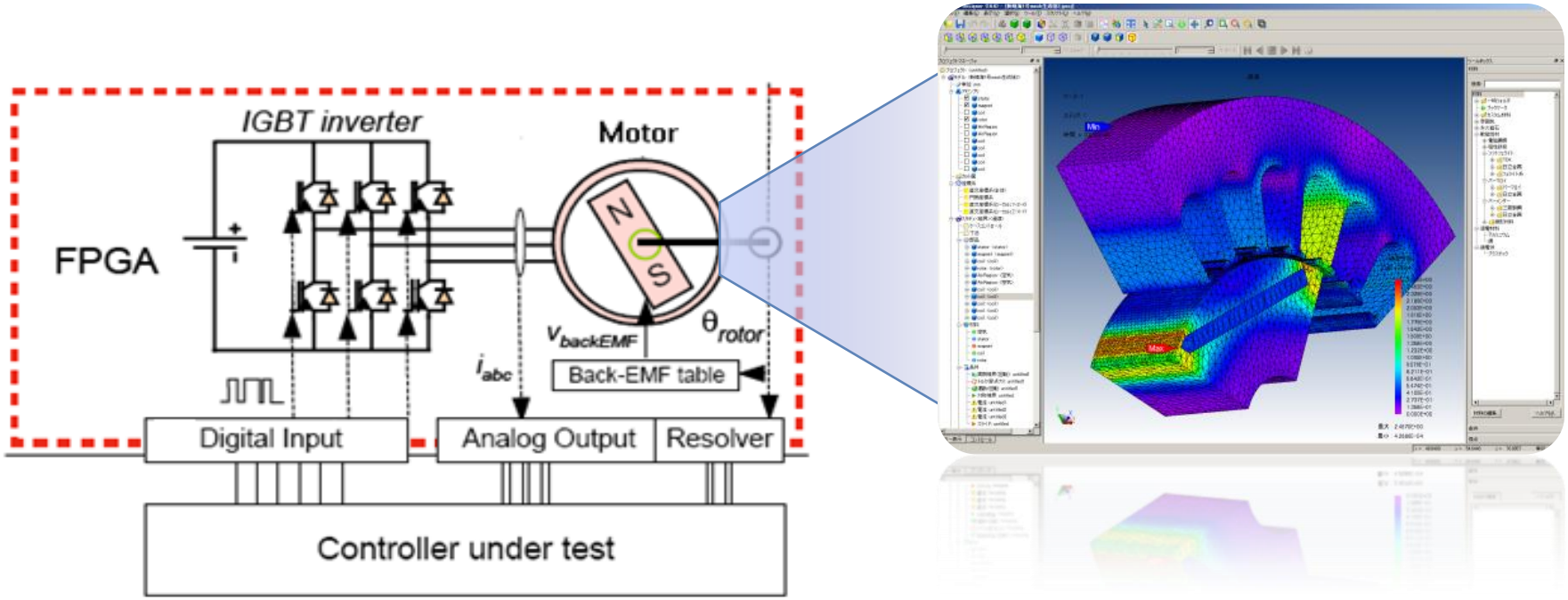


Specifications for cRIO-9082

NI RIO Hardware Platform

	CompactRIO & Single-Board RIO			PXI/PC RIO
	 Value	 Ultra Rugged	 Performance	 High Performance
Processor Performance	Up to 400MHz	Up to 800 MHz	Up to 1.33 GHz Dual-Core	Up to 2.26 GHz Quad-Core
FPGA Performance	Up to 43,661 logic cells, up to 58 DSP cores	Up to 110,592 logic cells, up to 64 DSP cores	Up to 147,443 logic cells, up to 180 DSP cores	Up to 94,208 logic cells, up to 640 DSP cores
Analog I/O Speed	Up to 1 MS/s	Up to 1 MS/s	Up to 1 MS/s	Up to 250 MS/s
Operating System	Real-Time OS	Real-Time OS	Window/Real-Time OS	Windows/Real-Time OS
Ruggedness	-20 to 55° C*, passively cooled	-40 to 70° C, passively cooled	0 to 55° C, passively cooled	0 to 55° C, actively cooled
Size	Starts at 17.8x9.3x8.7 cm.^{3}*	Starts at 18x9.3x8.7cm.^{3}	Starts at 40.4x13.4x8.7 cm.^{3}	Starts at 25.7x21.4x18.4 cm.^{3}
Target Application Examples	• Smart grid analyzer • Environmental Monitoring • Mobile robotics • Medical diagnostics & device control • Special Purpose Machines (SPM) • Chemical Process Control • Motion control	• In-vehicle logging • Machine Condition Monitoring • Industrial Machine Control • Oil & Gas Monitoring • Power Monitoring • Structural Monitoring • Automated Welding Control	• Machine Vision • Power Distribution/Control • ECU Prototyping • Analytical Instruments • Turbine Control • Industrial Robotics • Rapid Control Prototyping • Big physics & research	• Hardware-in-the-Loop (HIL) Test • Medical Imaging • High-end Simulation • Protocol Aware Test • Wireless Test • Software Defined Radio • Signal Intelligence

*Single-Board RIO versions are available that operate from -40 to 85° C and start at 10.3x9.7x2.4 cm^3



NATIONAL INSTRUMENTS

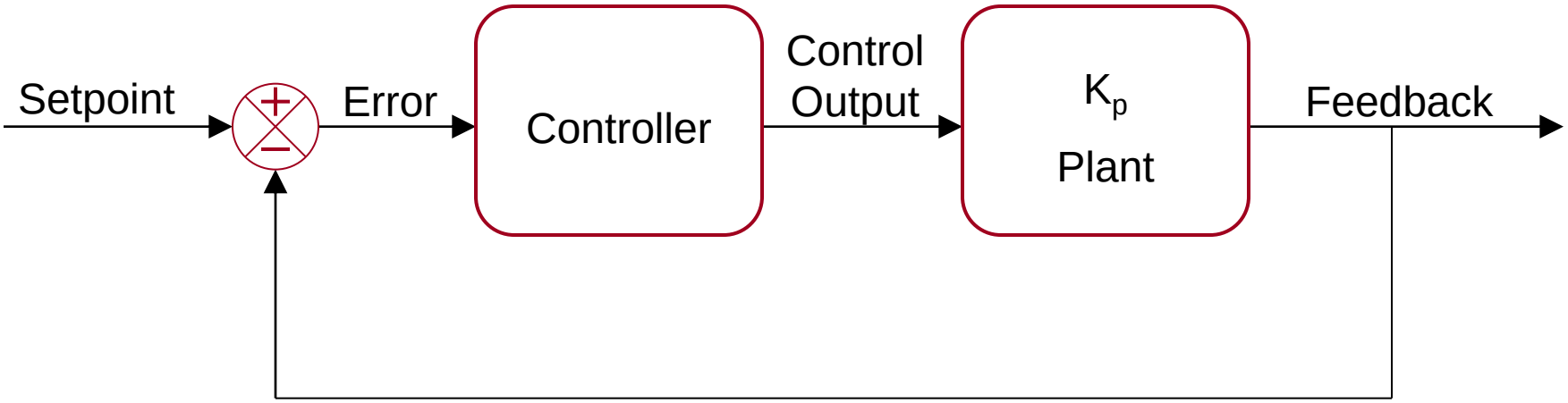
POWER ELECTRONICS REAL-TIME HIL SIMULATION

BACKGROUND

NATIONAL INSTRUMENTS

REAL-TIME HIL SIMULATION OF POWER ELECTRONICS

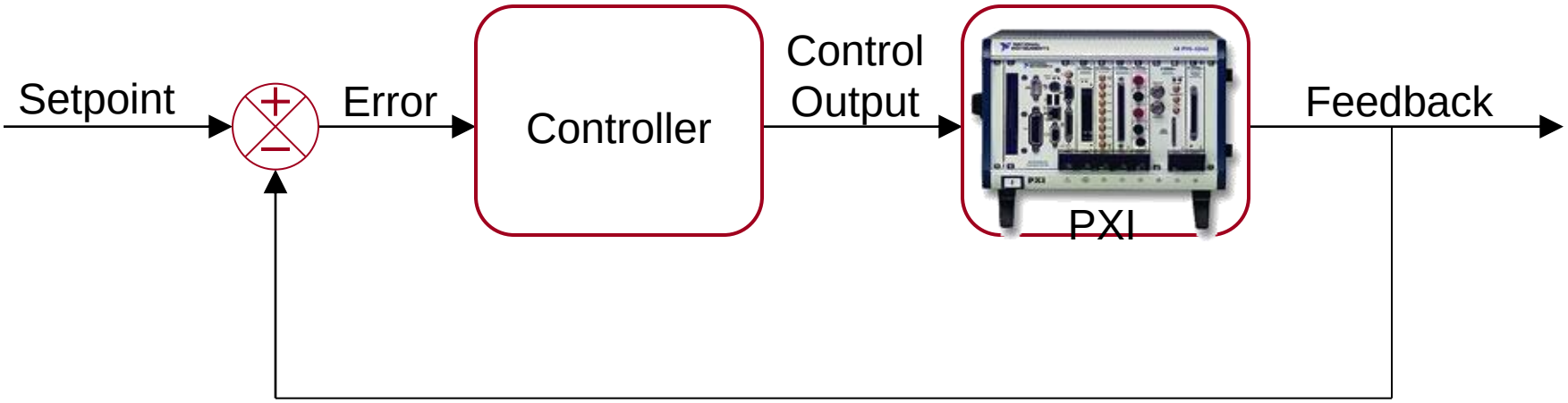
Hardware-In-the-Loop (HIL) Simulation of Power Electronics



Keys to success for power electronics simulations:

- High fidelity models
  - Non-linear
  - Time varying
- Sub 1us timing
- High speed I/O (1-10x the loop rate)

Hardware-In-the-Loop (HIL) Simulation of Power Electronics



Keys to success for power electronics simulations:

- High fidelity models
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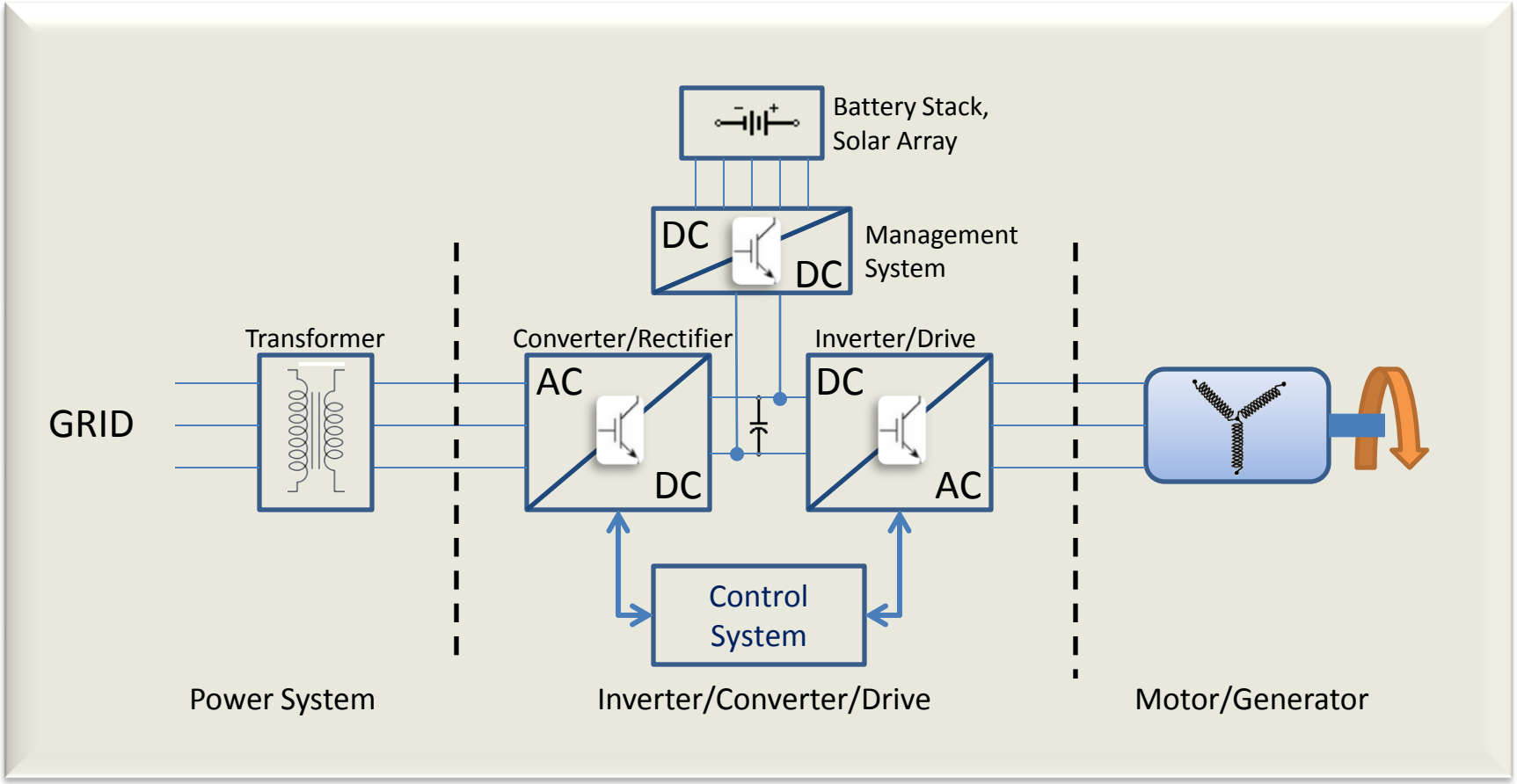
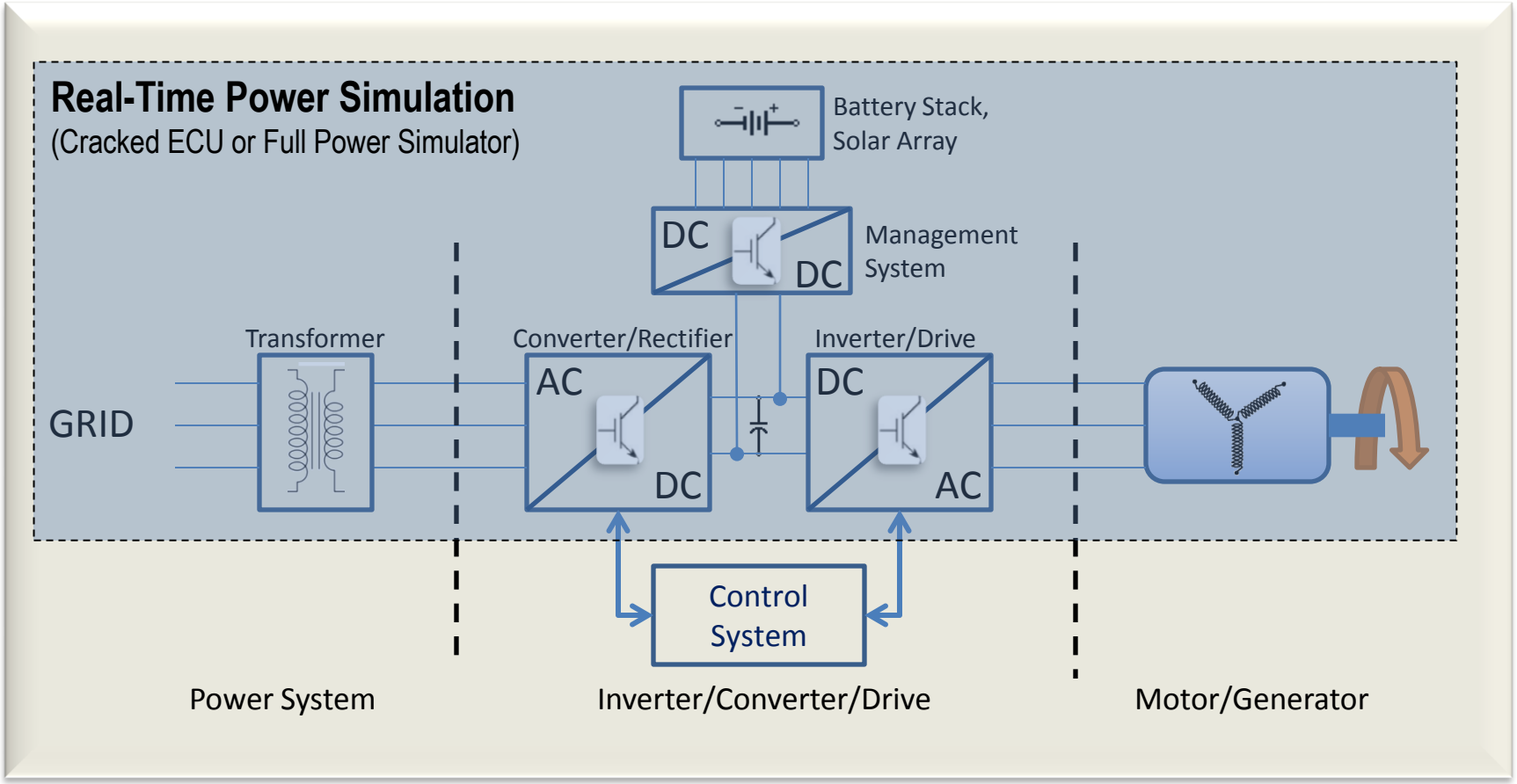
- Sub 1us timing
- High speed I/O (1-10x the loop rate)

What is a power electronics HIL test system?



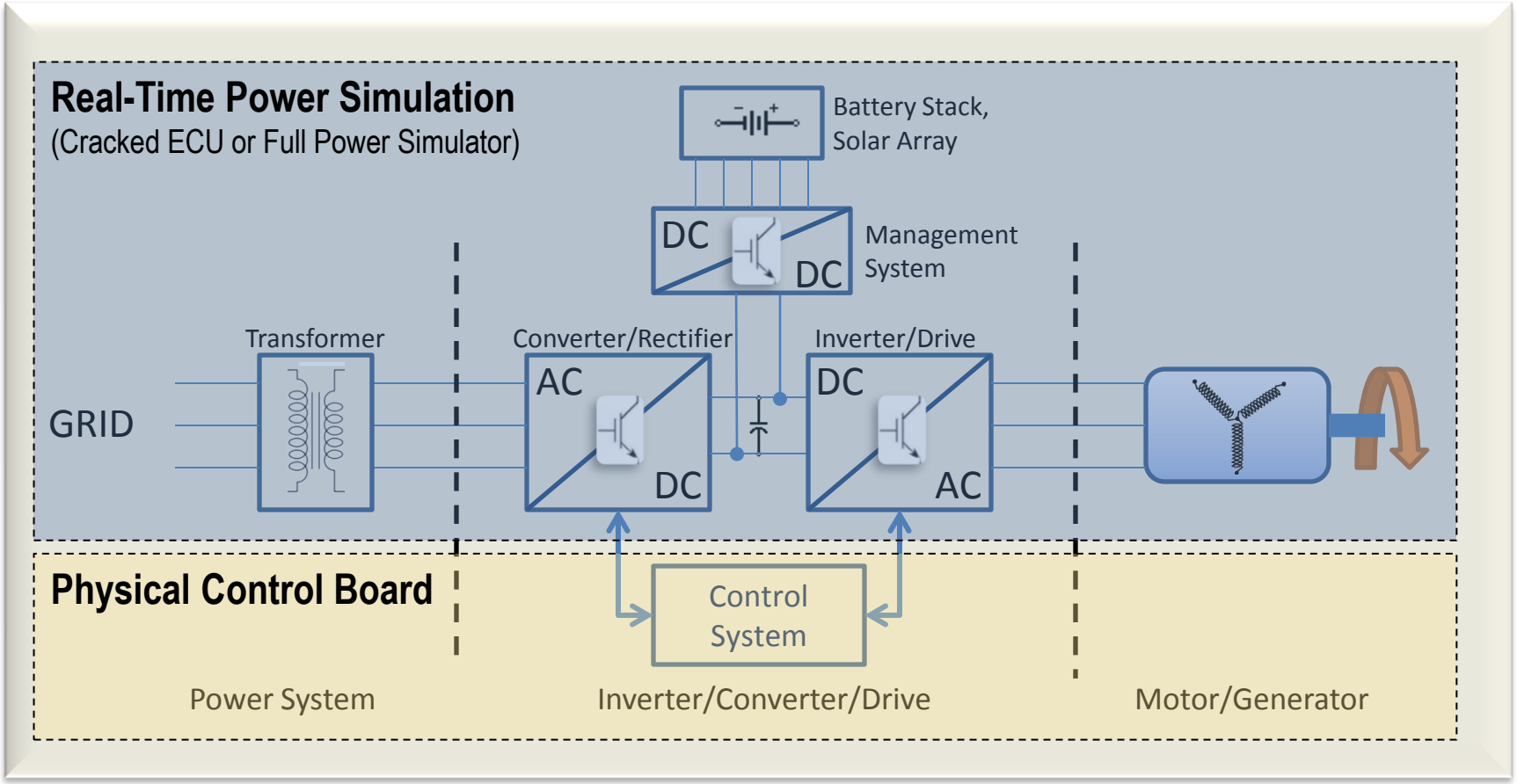
HIL = Hardware-In-the-Loop

What is a power electronics HIL test system?



HIL = Hardware-In-the-Loop

What is a power electronics HIL test system?



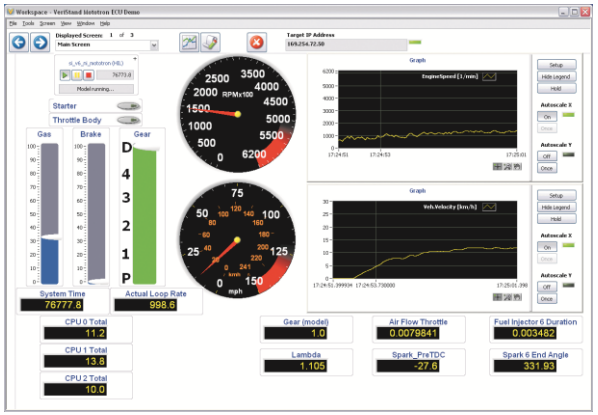
HIL = Hardware-In-the-Loop

Why is HIL necessary?

- **Comprehensive validation of system reliability**
  - HIL enables comprehensive test coverage
  - Find the “needle in haystack” problems
- **Formal evaluation of design tradeoffs**
  - Evaluate design tradeoffs to reduce cost while increase energy efficiency
  - Evaluate control system performance across a wide range of test profile scenarios
- **Risk free performance of “impossible” tests**
  - Evaluate scenarios that would be physically destructive or impossible to due bandwidth limitations of physical test systems

NI Real-Time Testing Platform

Real-Time Processor



NI VeriStand

Fault Insertion

FPGA Based I/O

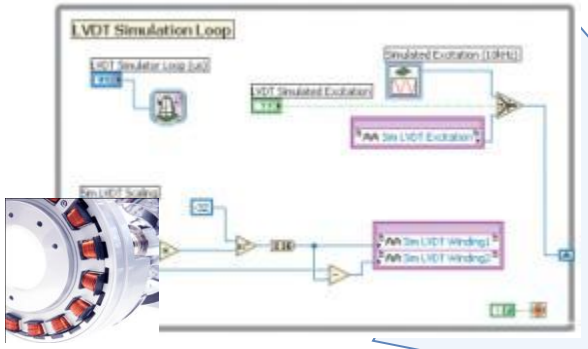
Bus Interfaces

NI PXI Platform

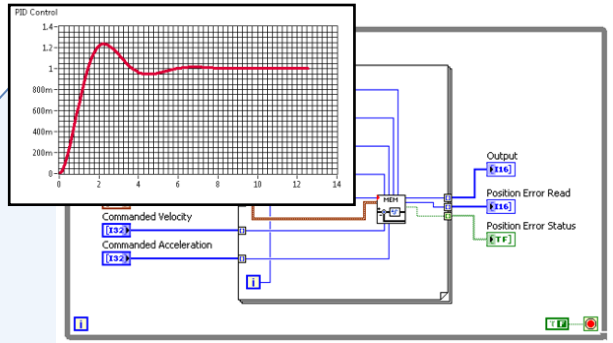
Analog/ Digital I/O

Instrument Grade and RF I/O

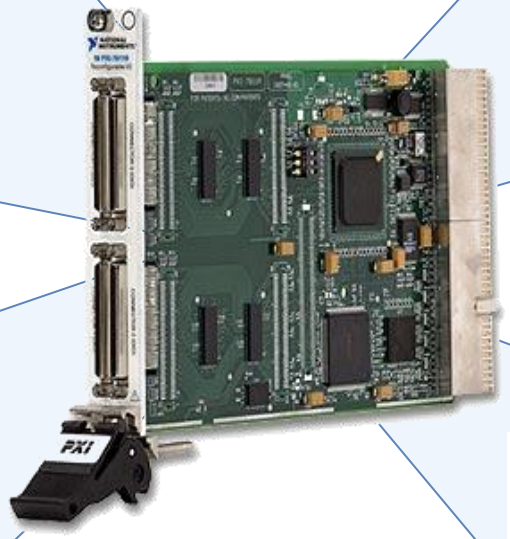
FPGA-Based I/O Interfaces

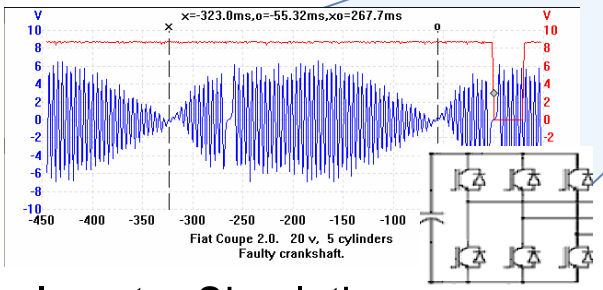


Motor Simulation

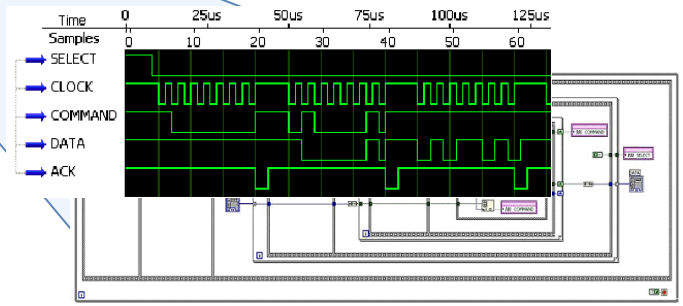


High-Speed Control



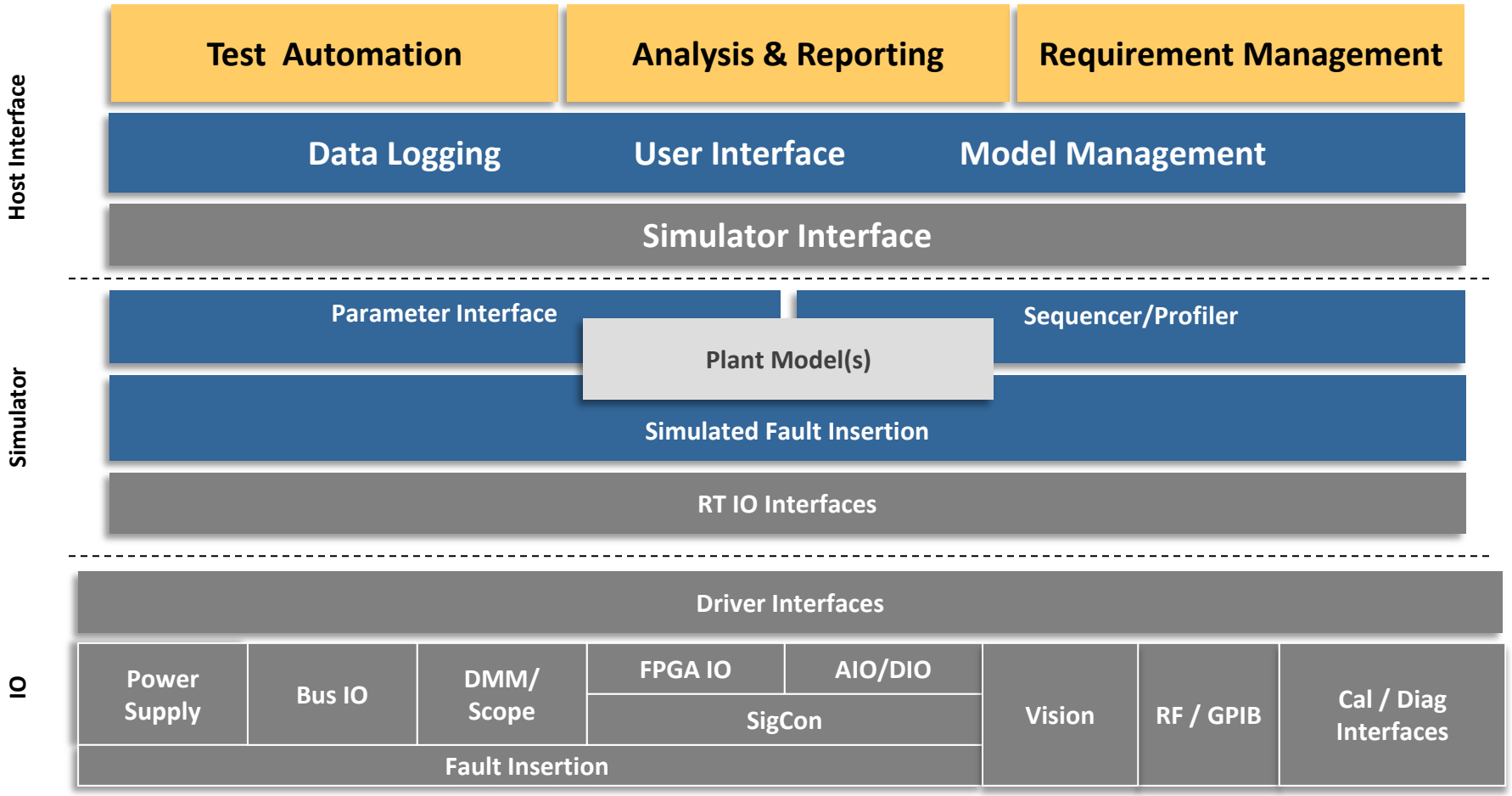


Inverter Simulation



Custom Protocols

HIL Test System Elements



NI VeriStand™

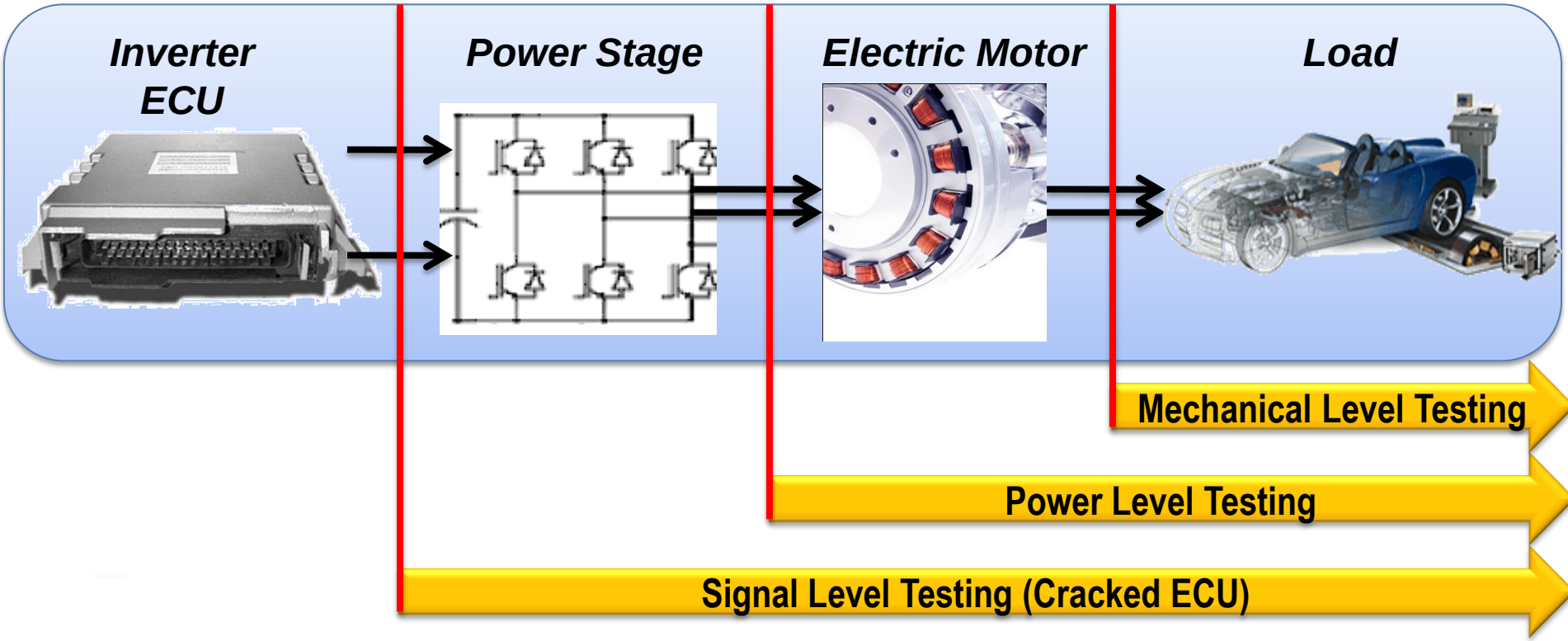
Real-Time Testing and Simulation Software

- Stimulus Generation
- Data Logging
- Single-Point I/O
- Alarming
- Calculated Channels
- Run-time Editable User Interface
- User Management
- Multi-Chassis Synchronization
- Closed-Loop Control
- Deterministic Model Execution

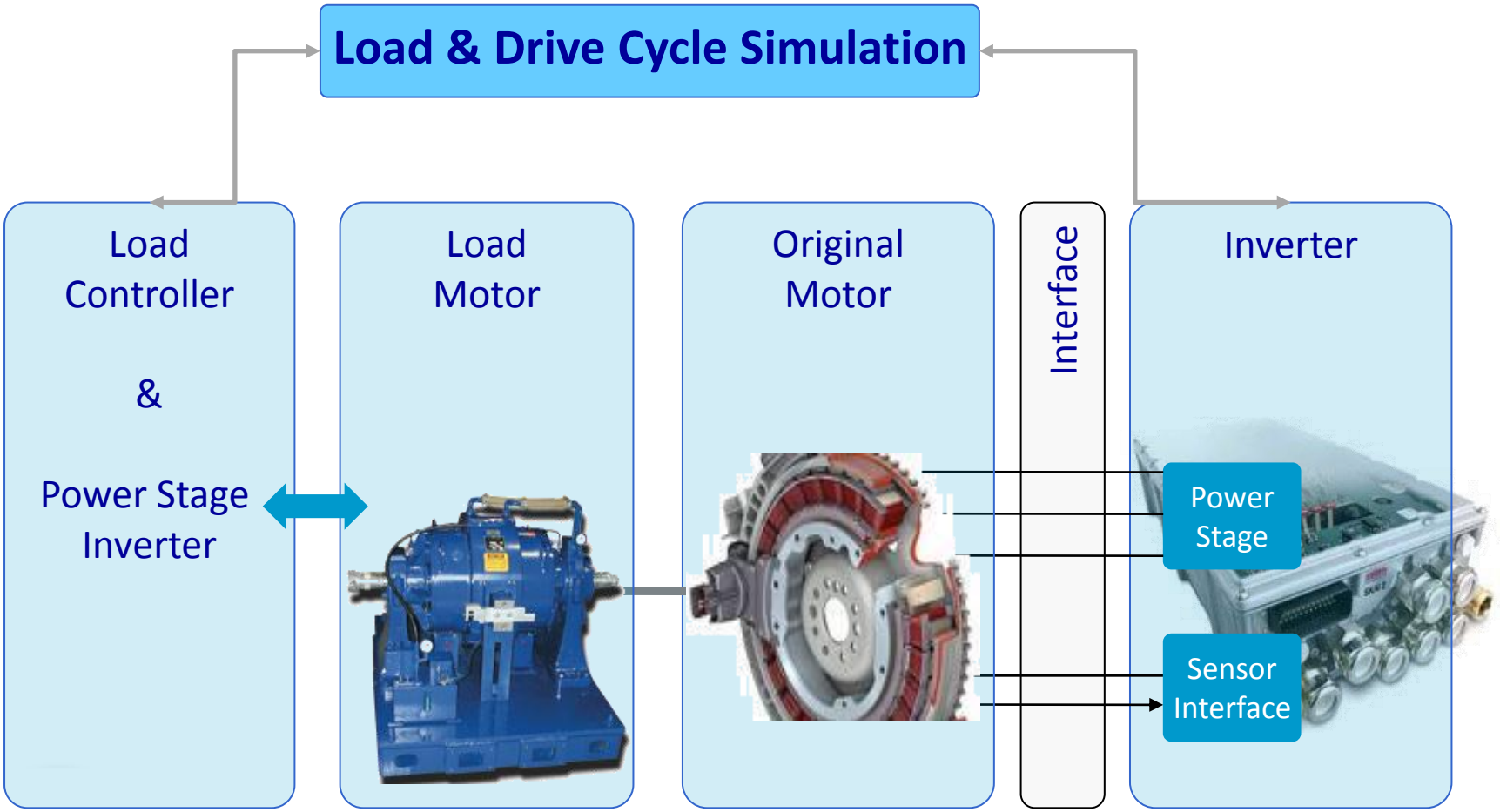
The revolutionary platform for supporting Model Based Design by easily deploying models throughout your development process.

Case Study: Full Power Electric Motor Emulation with SET and JMAG

TRADITIONAL APPROACH (DYNOMOMETER):



SET Electric Motor Emulator (EME)



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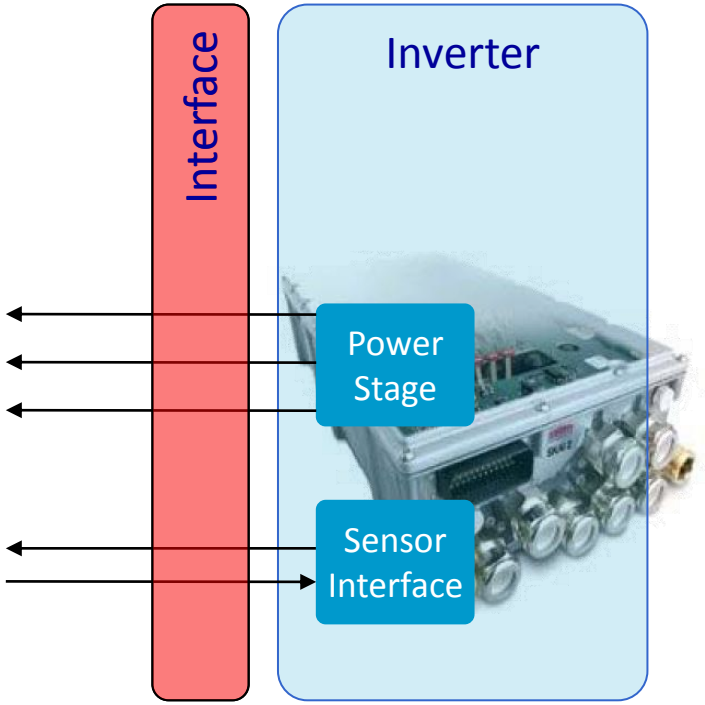

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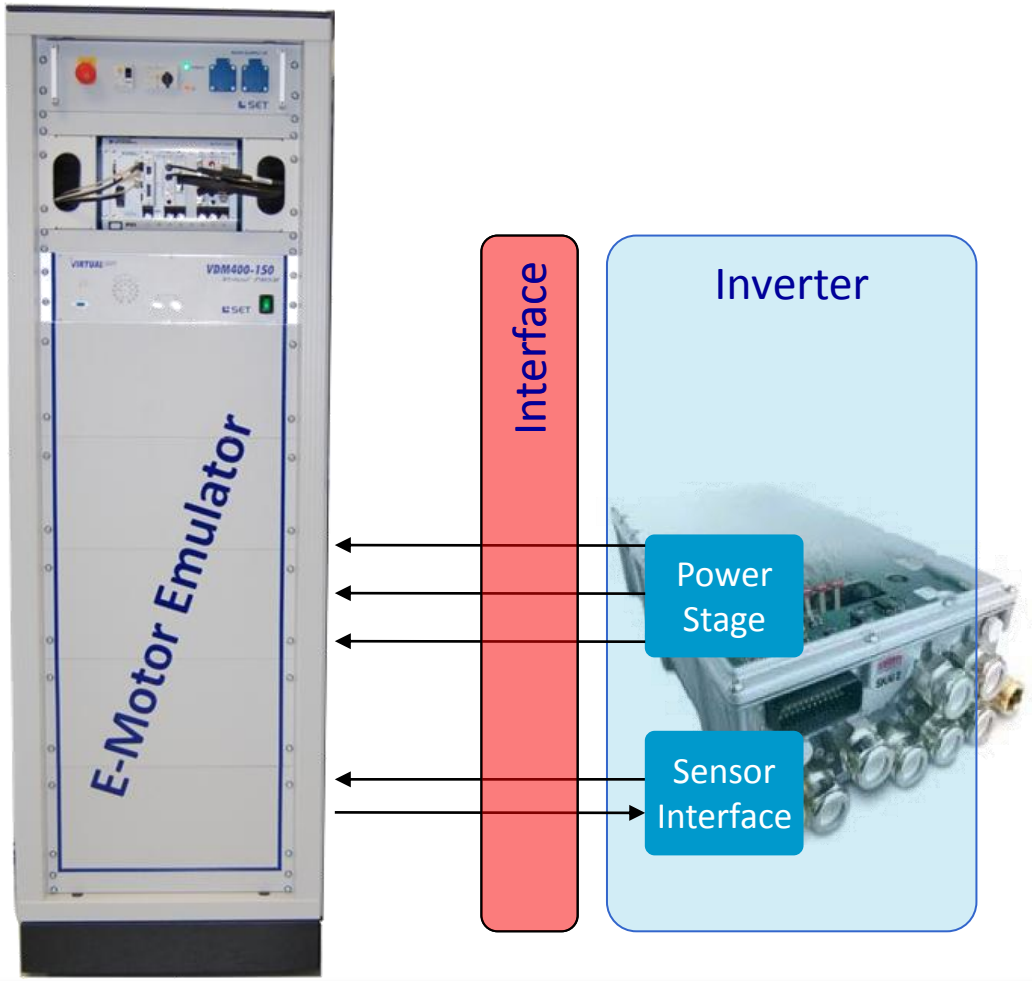
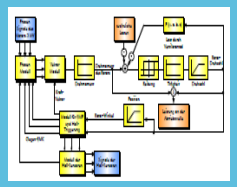


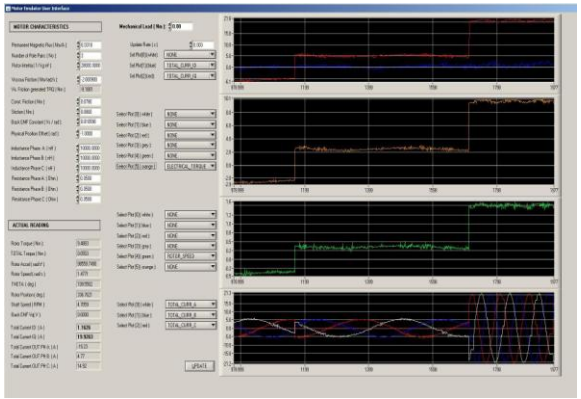
SET Electric Motor Emulator (EME)

Phase Emulation

Sensor Emulation

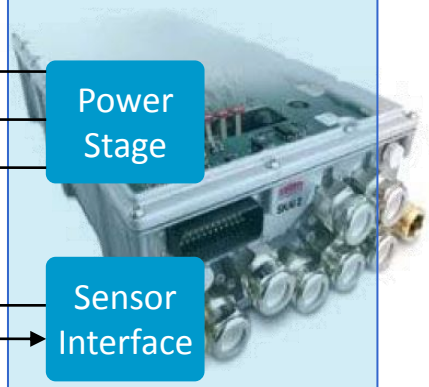
Motor Model





Interface

Inverter



Power Stage

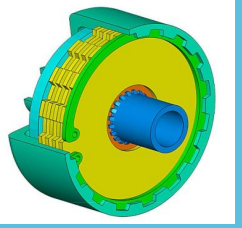
Sensor Interface

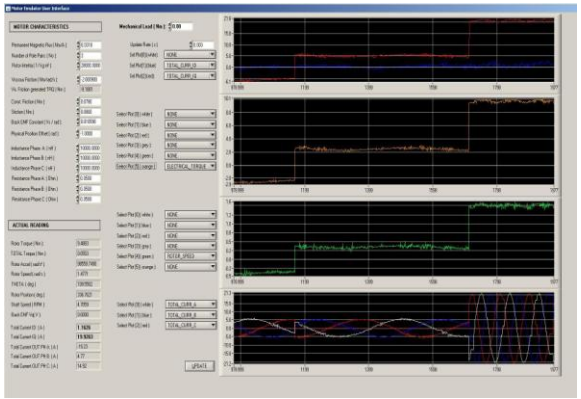
SET Electric Motor Emulator (EME)

Phase Emulation

Sensor Emulation

Motor Model



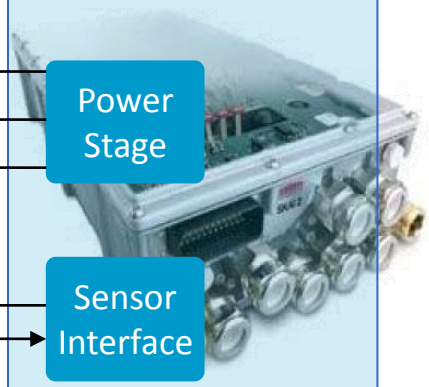


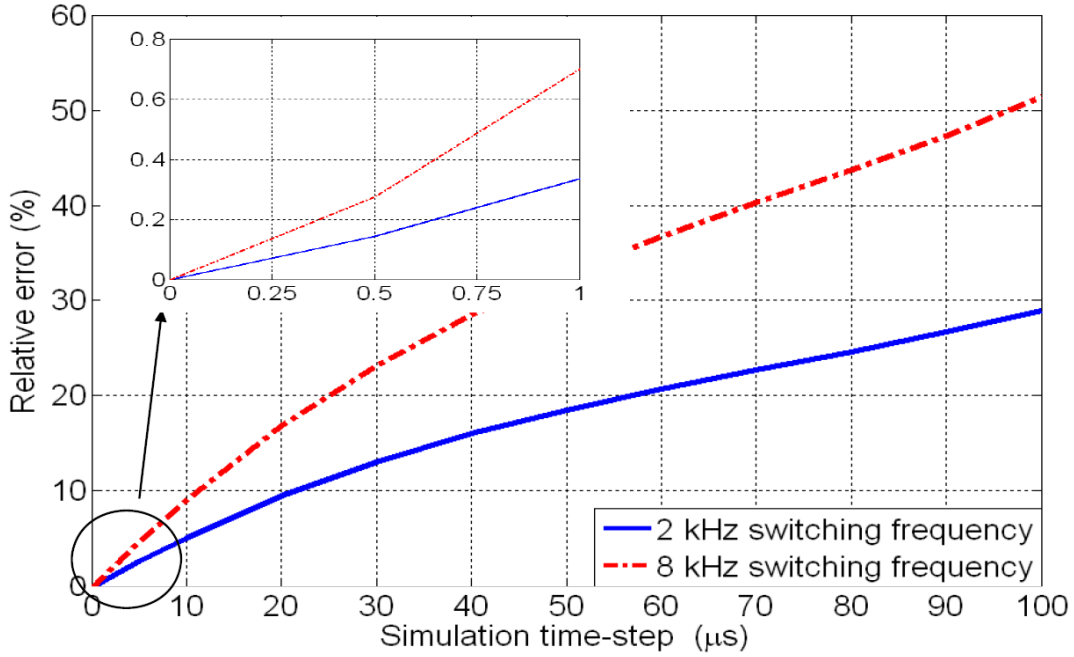
Interface

Inverter

Power Stage

Sensor Interface





NATIONAL INSTRUMENTS

PROCESSOR BASED SIMULATION CHALLENGES

Image courtesy Prof. Reza Iravani, University of Toronto

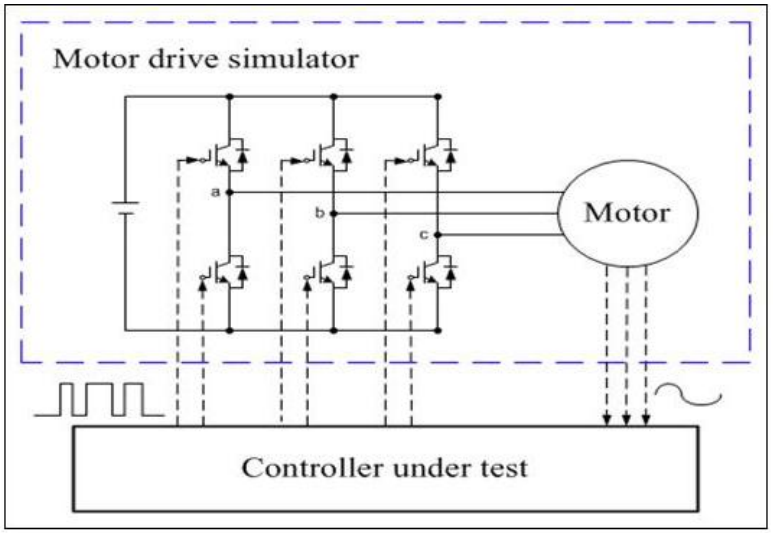
Processor vs. FPGA based PE Simulation

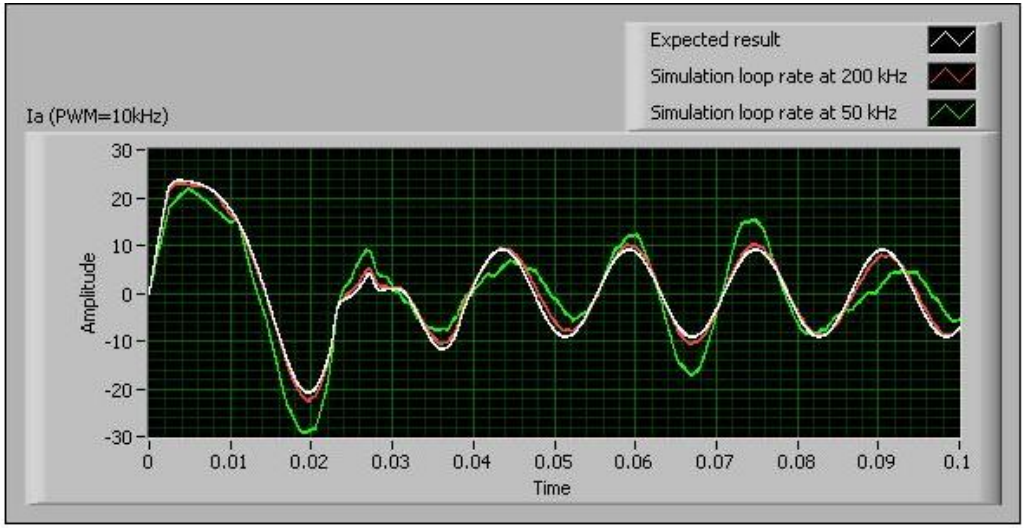
Processor	FPGA
Floating point models > greatly simplified porting to real time	Fixed point models > word length choices must be validated for the floating point model
Large simulation time steps (typical Δt=50 µs)	Small simulation time steps (typical Δt=0.5 µs)
Switching events occur in between simulation time steps	Switching events are orders of magnitudes slower than simulation speed
Limited model accuracy due to simplifications	Limited model accuracy due to effort in porting to discrete-time, fixed point format
Reasonably good scalability and flexibility to adapt to larger/different system models	Changing the simulation model may require significant rework/re-architecture
Non-linear system response often must be linearized	Non-linear system response typically can be accurately captured

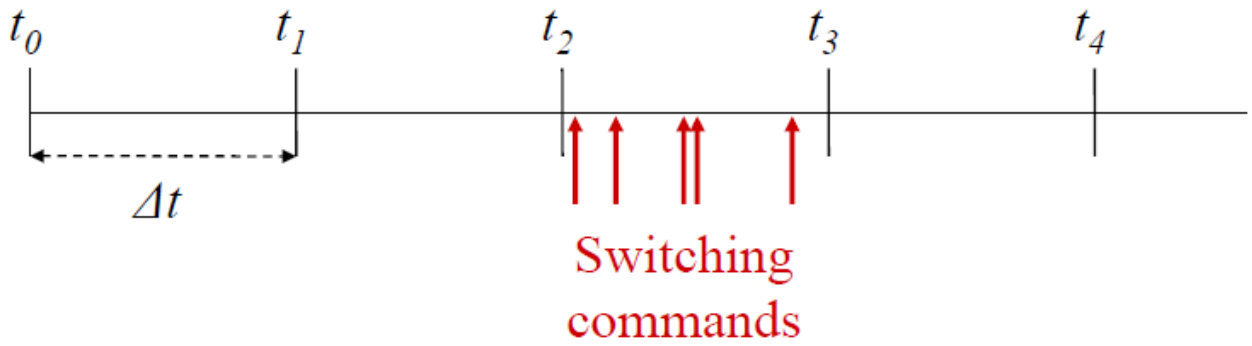
Processor-based power simulation issues

- Very fast pin-to-pin times are required
  - Bus latency causes prohibitive delays even if the processing core is very fast. Δt typically hits the limit at 10 µs to 80 µs.
- The simulation timestep (Δt) is asynchronous with respect to the control system under test
  - If multiple switching events occur within one timestep, inaccurate results occur.
  - For negligible error, the simulation timestep should be 100 times faster than the PWM switching frequency.
  - (Special solvers that use timestamp information can help.)
- The computational horsepower of the simulator is limited
  - Advanced component models are inherently demanding, therefore models often need to be simplified for real-time simulation
- The simulator can only produce a controlled frequency response up to ½ of the simulation timestep (Nyquist limit)
  - i.e. The frequency bandwidth of a 50 us simulation is 10 kHz

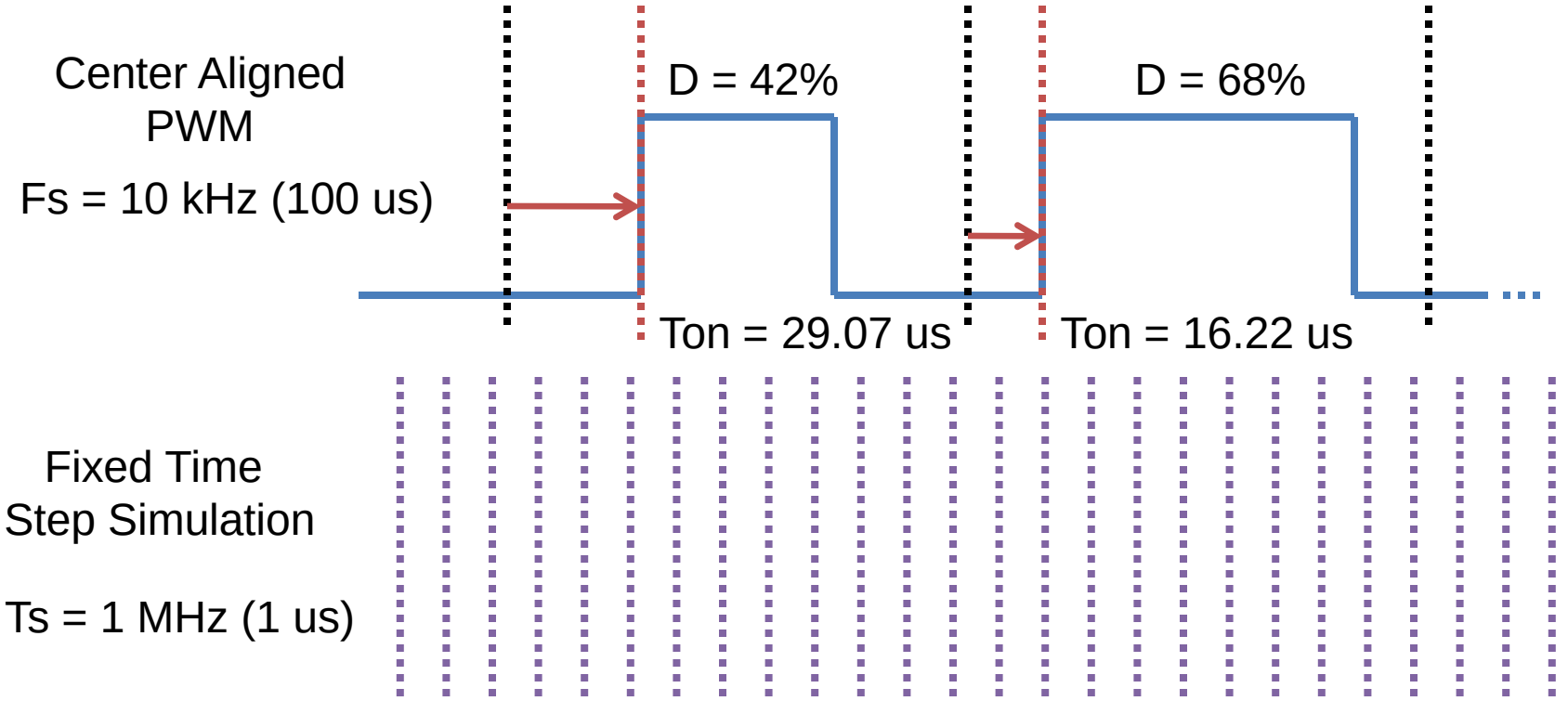
When simulating switch-mode power systems, speed matters!







Switch mode power meets fixed step solver



Result

Worst Case Duty Cycle Sampling Error = 2%

Assuming 480 V, 3 phase power = 480 Vrms*sqrt(2)*2% = 13.6 Volts

For negligible error, the simulation timestep should be 100 times faster than the PWM switching frequency

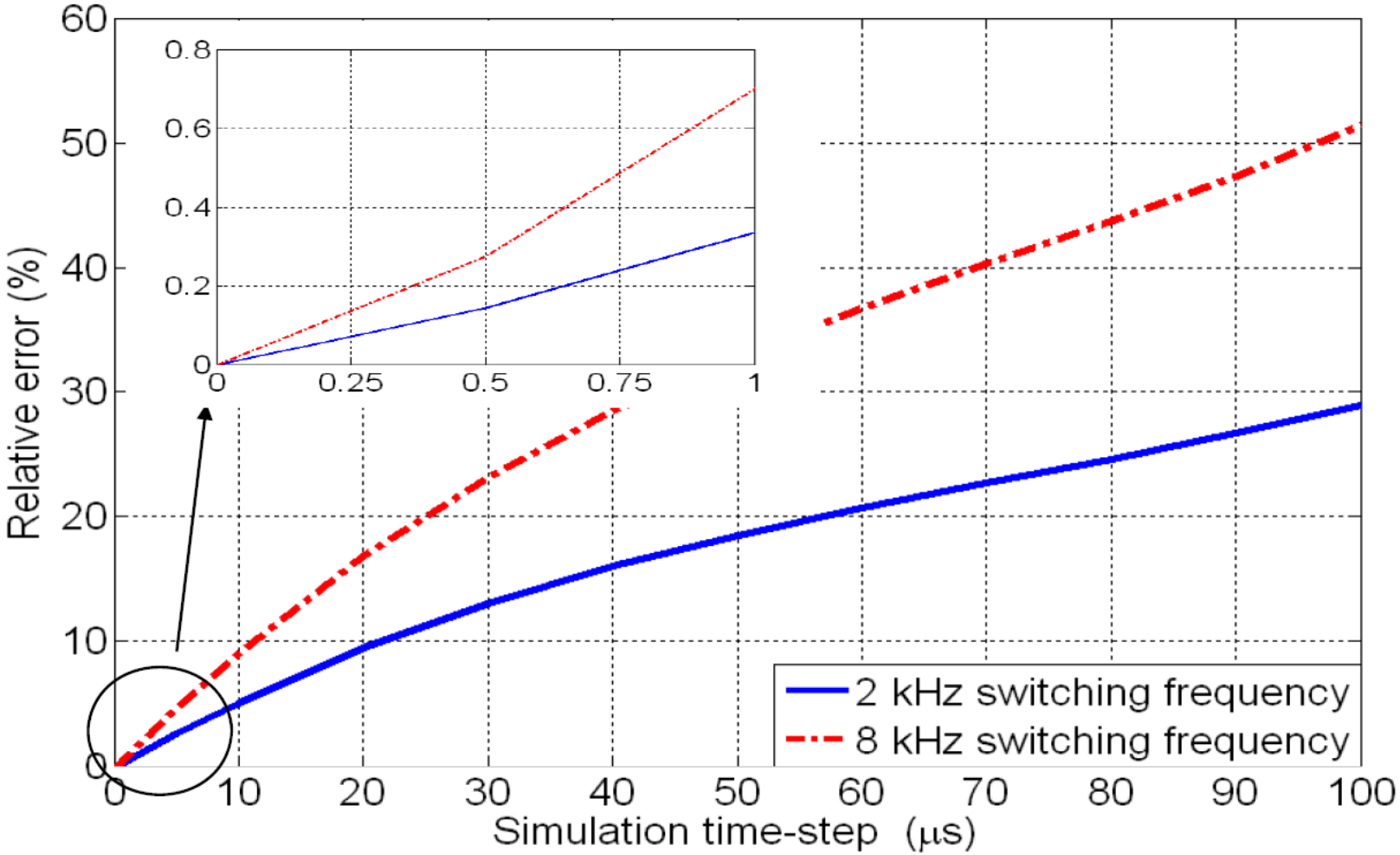
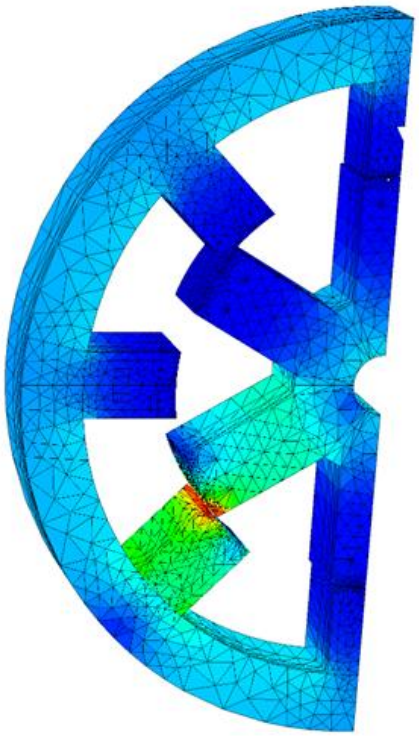


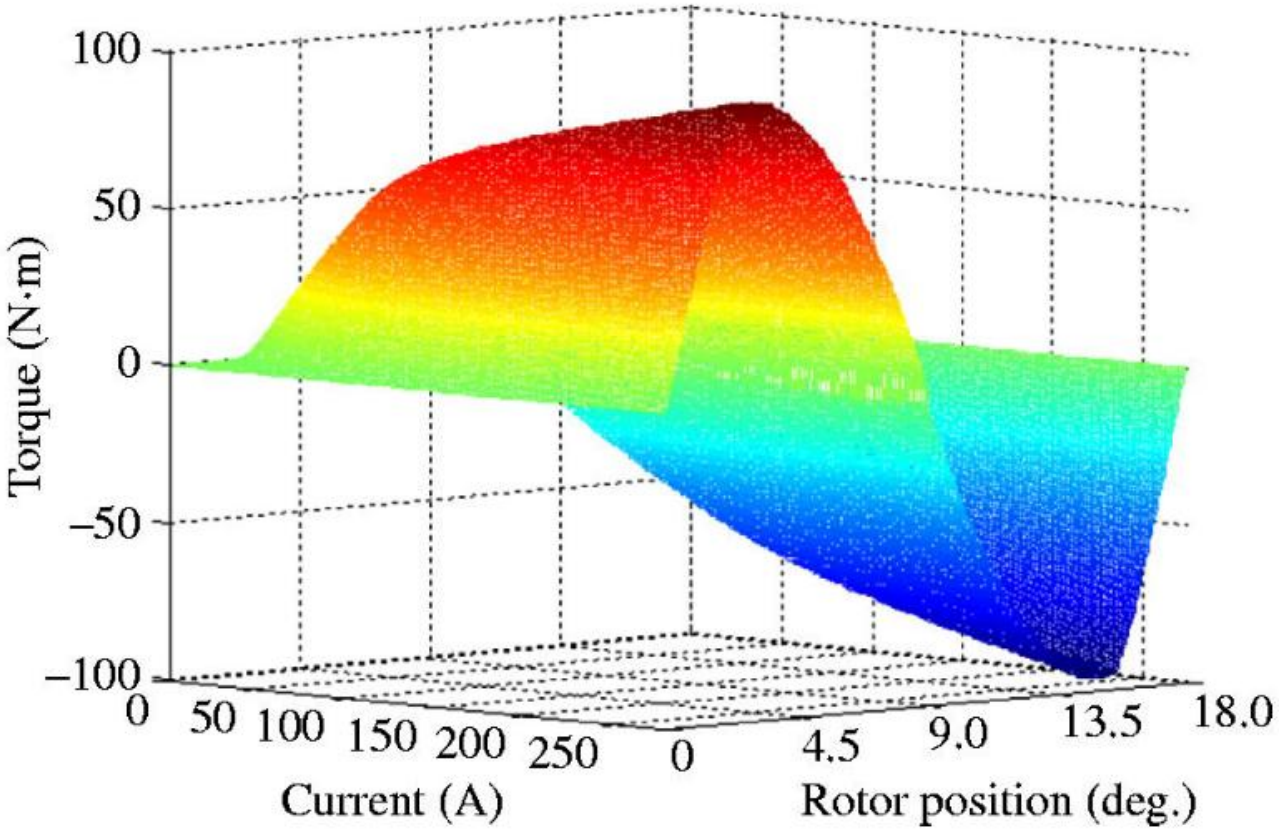
Image courtesy Prof. Reza Iravani, University of Toronto

Non-linear physics

Switched Reluctance Motor (SRM)



Finite Element Analysis (FEA)

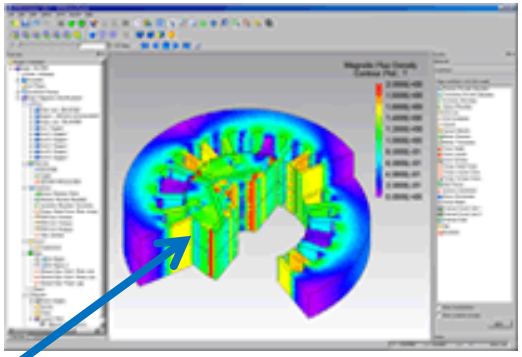


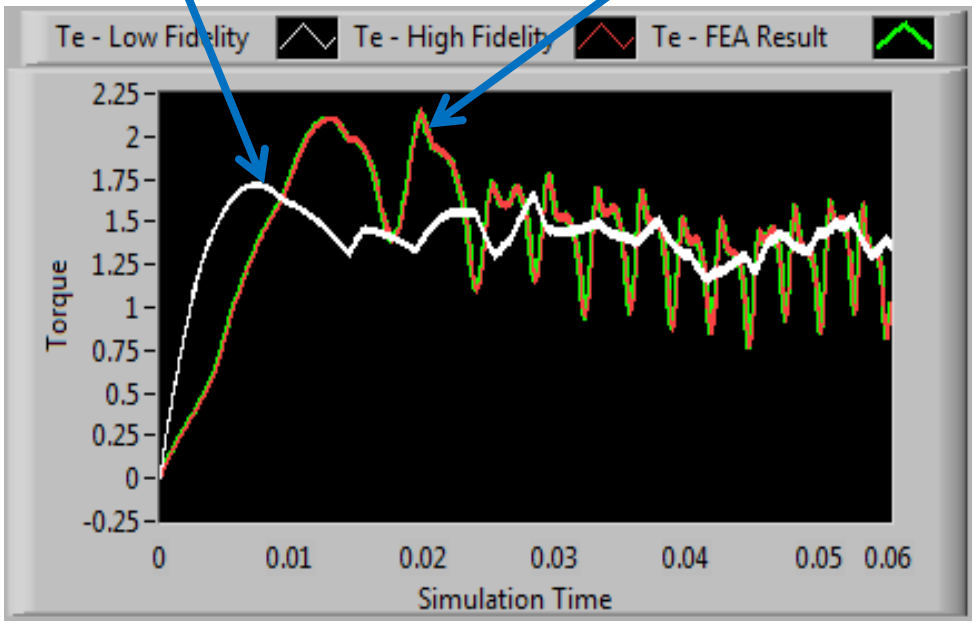
When simulating electromagnetic systems, model accuracy matters!

PMSM Sinusoidal Flux Model*
(DQ Reference Frame)

$$Vsvd = P * \omega_m * Lq * Iq$$
$$Vsvq = P * \omega_m * (Ld * Id * \lambda)$$
$$Te = \frac{3}{2} * P * (Iq * (Id * Ld + \lambda) - Id * (Iq * Lq))$$

JMAG FEA Model





<u>Low Fidelity Model Assumptions:</u>

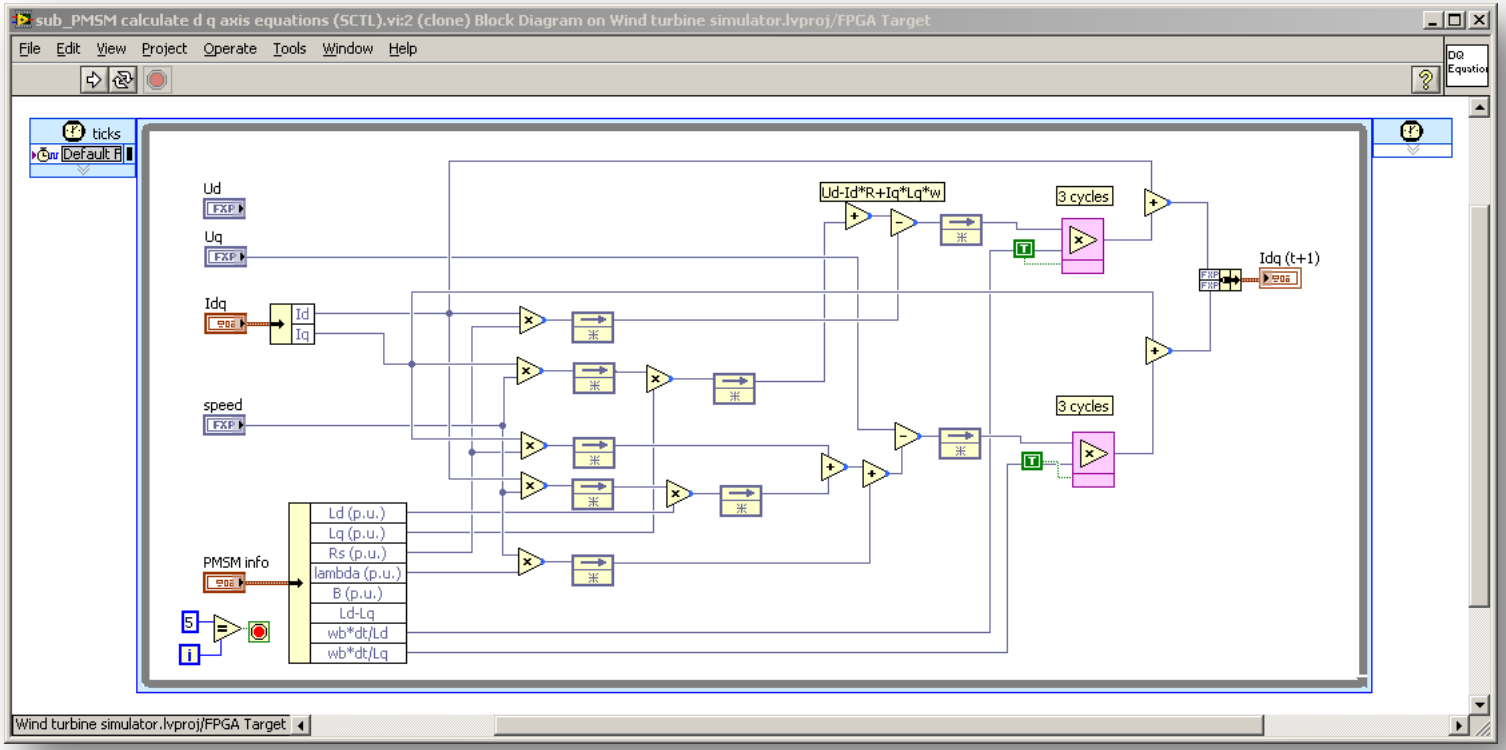
- Uniform air-gap
- No slot harmonics
- No stator saturation
- Sinusoidally distributed windings
- No zero phase sequence (system is balanced)

<u>High Fidelity Model Assumptions:</u>

- Complex geometry
- Magnetic materials
- Permanent magnets
- Nonlinear inductance
- Saturation effects
- Coil winding
- Copper and iron losses
- Efficiency (post processing)

Summary

- Processor based power electronics simulations have the following challenges:
  - Limited accuracy due to model simplifications
  - Limited accuracy due to large simulation time steps relative to the PWM switching frequency
  - No control of frequency response above Nyquist limit; ~10 kHz typ.



NATIONAL INSTRUMENTS

OVERCOMING FPGA SIMULATION CHALLENGES

FPGA-based power simulation challenges > solutions

- Simulation of discontinuous switch mode power systems with active and passive switching components
  - Use piecewise state-space models with coefficients stored in FPGA RAM
- Very high speed discrete real-time simulations
  - Use first order state-space format for numerical stability
- Fixed point math
  - Use parallel connections when possible- avoid higher order blocks connected in series
  - Create a test bench simulation to validate fixed point math before compiling to FPGA
- Nonlinear models
  - Use non-linear differential equations or look-up tables based on FEA
- Stiff system (combined high and low bandwidth components)
  - Use parallel loops, filter the lower speed signals when passing to the faster loops

Simulation of discontinuous switch mode power systems

- The model changes depending on whether each switch is open or closed– therefore, the simulation equations are discontinuous in time.

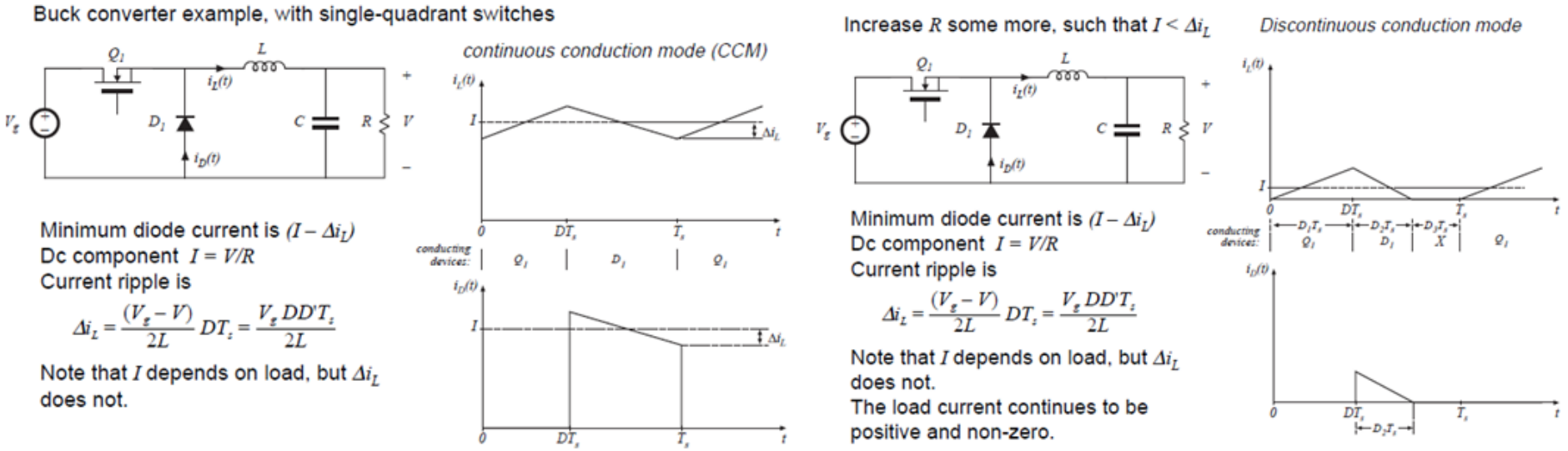
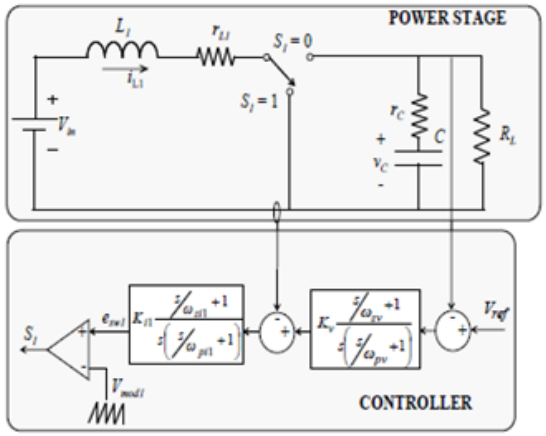


Figure 6. In this buck converter, the discontinuous conduction mode (DCM) occurs when the current ripple causes the diode to reverse polarity

Images courtesy Prof. Sudip K. Mazumder, University of Illinois

Piecewise state-space models

- The result is a piecewise model to represent the switch states in continuous conduction and discontinuous conduction modes of operation.



- Additional switching state corresponds to $S_1 = 0$ and $i_{L1} = 0$.

OFF Time and Discontinuous ($S_1 = 0_D$, i = 3)

$$\frac{d}{dt}\begin{bmatrix} i_{L1} \\ v_C \\ \xi_1 \\ \xi_2 \\ \xi_3 \\ \xi_4 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C}\frac{1}{R+r_C} & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & K_v & K_v\omega_{zv} & -\omega_{pil} & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & \varepsilon \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_C \\ \xi_1 \\ \xi_2 \\ \xi_3 \\ \xi_4 \end{bmatrix} + \begin{bmatrix} \frac{V_{in}}{L_1} \\ 0 \\ V_{ref} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$\dot{\Psi} = A_{03}\Psi + B_3$$

ON Time ($S_1 = 1$, i = 2)

$$\frac{d}{dt}\begin{bmatrix} i_{L1} \\ v_C \\ \xi_1 \\ \xi_2 \\ \xi_3 \\ \xi_4 \end{bmatrix} = \begin{bmatrix} -\frac{r_{L1}}{L_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C}\frac{1}{R+r_C} & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & K_v & K_v\omega_{zv} & -\omega_{pil} & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & \varepsilon \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_C \\ \xi_1 \\ \xi_2 \\ \xi_3 \\ \xi_4 \end{bmatrix} + \begin{bmatrix} \frac{V_{in}}{L_1} \\ 0 \\ V_{ref} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$\dot{\Psi} = A_{02}\Psi + B_2$$

OFF Time ($S_1 = 0$, i = 1)

$$\frac{d}{dt}\begin{bmatrix} i_{L1} \\ v_C \\ \xi_1 \\ \xi_2 \\ \xi_3 \\ \xi_4 \end{bmatrix} = \begin{bmatrix} -\frac{1}{L_1}\left(r_{L1}+\frac{R}{R+r_C}\right) & -\frac{1}{L_1}\frac{R}{R+r_C} & 0 & 0 & 0 & 0 \\ \frac{1}{C}\frac{R}{R+r_C} & -\frac{1}{C}\frac{1}{R+r_C} & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & K_v & K_v\omega_{zv} & -\omega_{pil} & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & \varepsilon \end{bmatrix} \begin{bmatrix} i_{L1} \\ v_C \\ \xi_1 \\ \xi_2 \\ \xi_3 \\ \xi_4 \end{bmatrix} + \begin{bmatrix} \frac{V_{in}}{L_1} \\ 0 \\ V_{ref} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$\dot{\Psi} = A_{01}\Psi + B_1$$

Images courtesy Prof. Sudip K. Mazumder, University of Illinois

Simulation of switch mode power systems

- Solutions:
  - Use piecewise state-space models with matrix coefficients stored in FPGA RAM.
  - Use logic executing in LabVIEW FPGA to determine which piecewise model is active.
- Notes:
  - Time varying, non-linear and look up table based matrix coefficients can also be calculated in separate FPGA loops and updated via FPGA RAM.

Very high speed discrete real-time simulations

- Problem: Discrete time simulations become numerically unstable as two or more poles approach the edge of the unit circle and overlap.

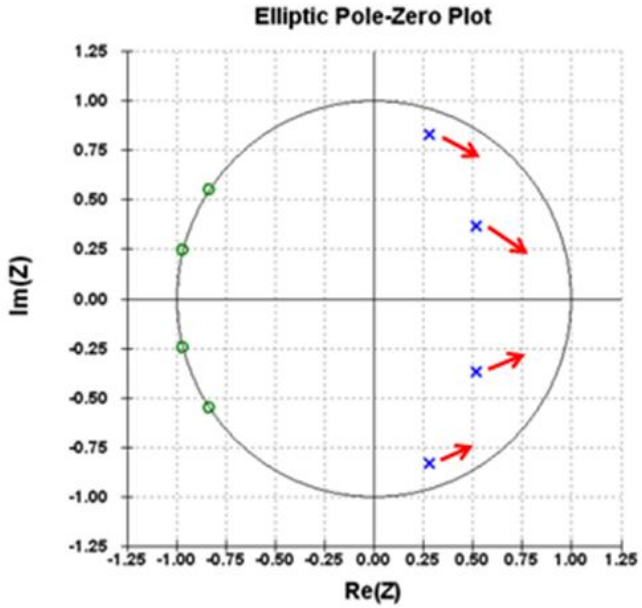


Figure 11. Increasing the sampling rate pushes the poles closer to the stability boundary.

Very high speed discrete real-time simulations

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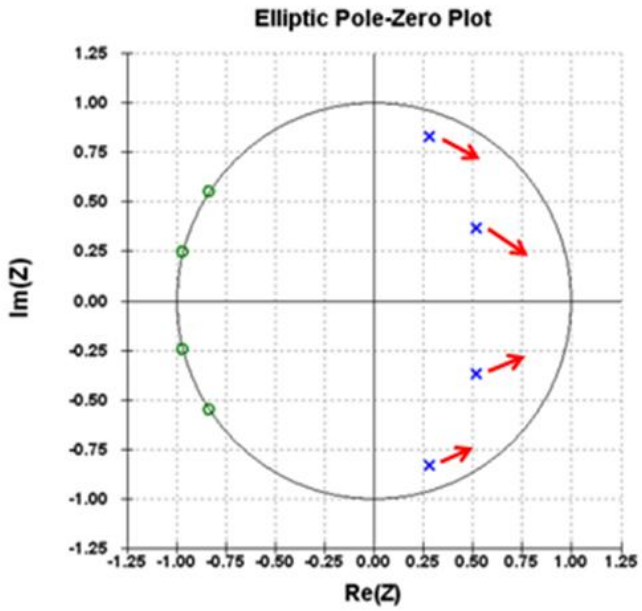
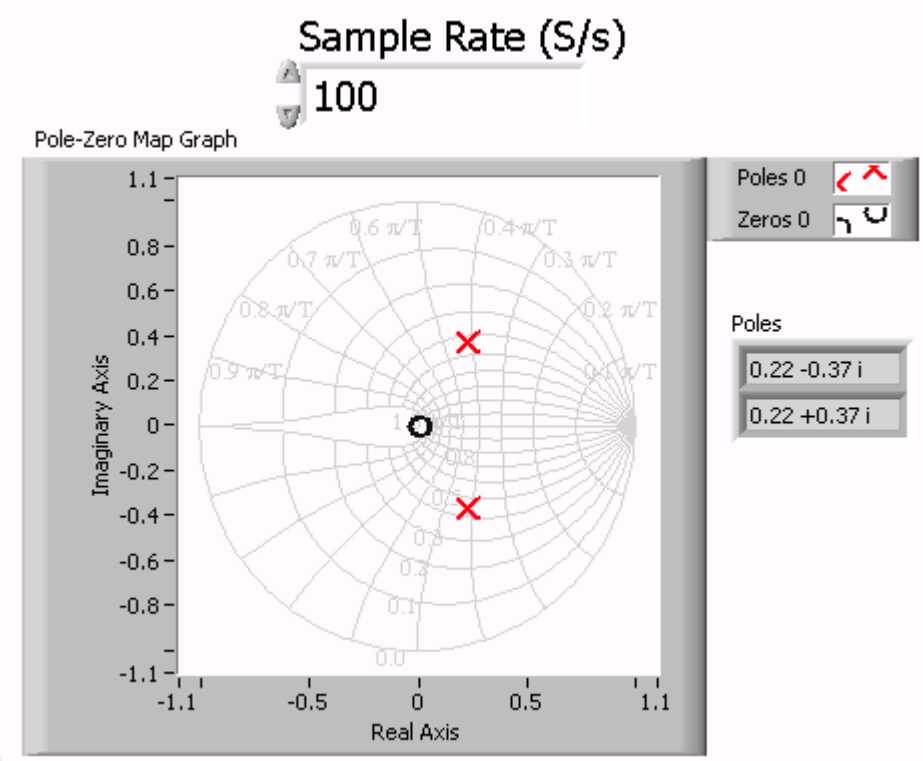


Figure 11. Increasing the sampling rate pushes the poles closer to the stability boundary.

RLC Circuit Example (2nd order):



NATIONAL INSTRUMENTS

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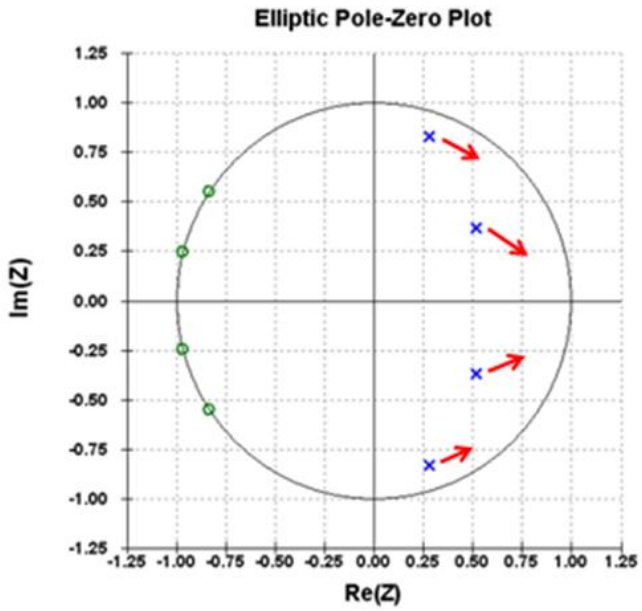

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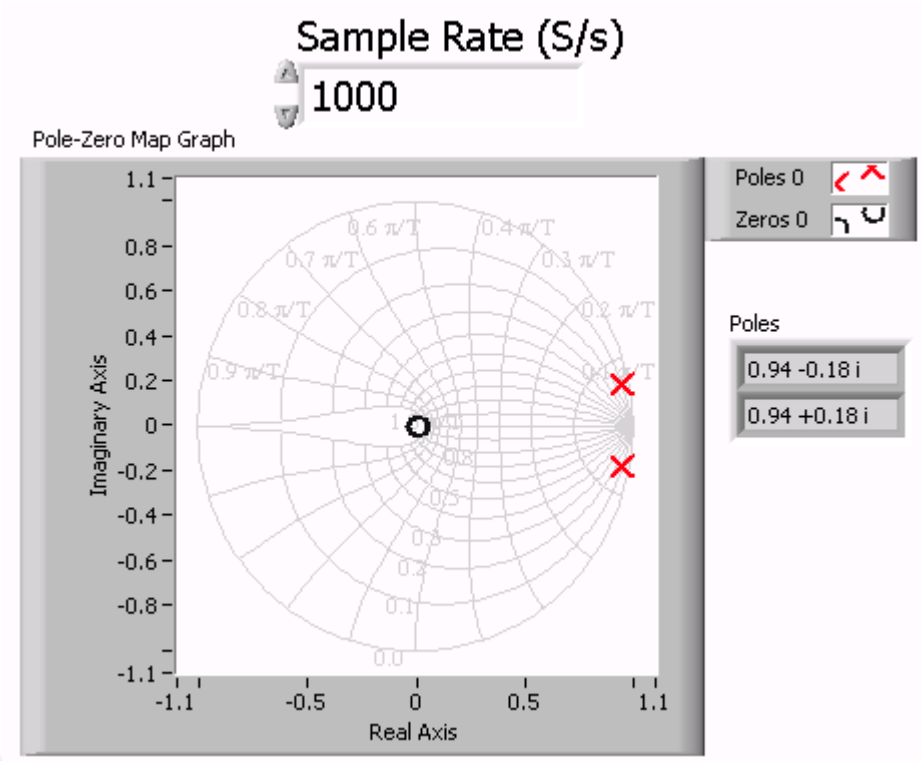

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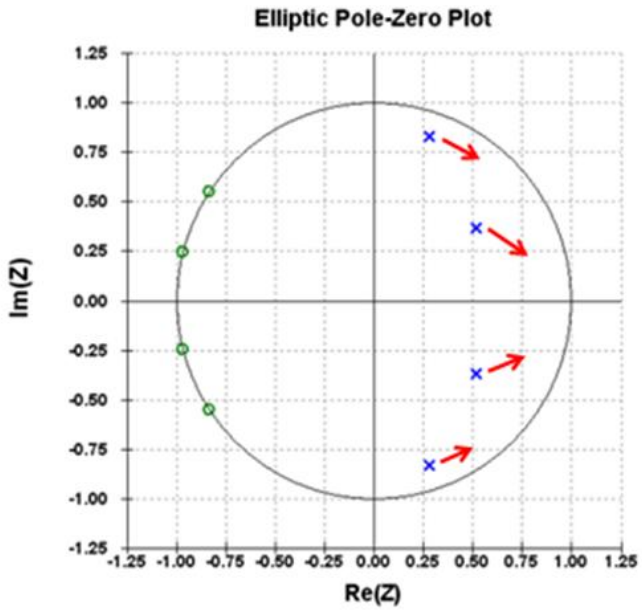

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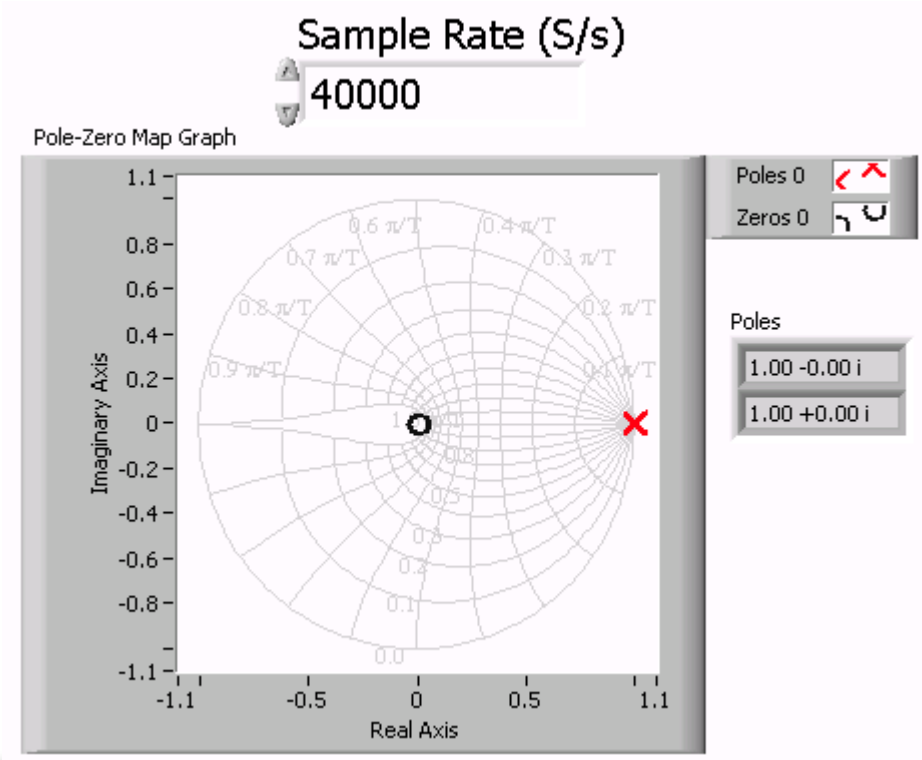


NATIONAL INSTRUMENTS

Very high speed discrete real-time simulations

- Solutions:
  - Use first order formulations like state space format.

$$\begin{bmatrix} x'_G \\ x'_F \end{bmatrix} = \begin{bmatrix} A_G & B_G C_F \\ 0 & A_F \end{bmatrix} \begin{bmatrix} x_G \\ x_F \end{bmatrix} + \begin{bmatrix} B_G D_F \\ B_F \end{bmatrix} u$$

$$\begin{bmatrix} y_G \\ y_F \end{bmatrix} = \begin{bmatrix} C_G & D_G C_F \\ 0 & C_F \end{bmatrix} \begin{bmatrix} x_G \\ x_F \end{bmatrix} + \begin{bmatrix} D_G D_F \\ D_F \end{bmatrix} u$$

  - Avoid high order transfer functions. Convert to a reduced order equivalent and change series connections to parallel.

Fixed-point math advice

- Problem: Conversion from floating point to a mathematically accurate fixed-point version cannot be fully automated at this time.
  - Specifics:
    - Quantization error- numeric performance is typically measured in terms of the Signal-to-Quantization Noise Ratio (SQNR)
    - Dynamic range of signals (ability to represent large signals with fine resolution)- overflow occurs if calculated signal exceeds range
    - Accumulation of error in accumulators (like the integrators of the simulation solver)
    - Accumulation of error when blocks are connected in series

Fixed-point math advice

- Start development in windows with a simple test bench application to check basic word lengths, functionality.
- Then create a simulation benchmark to compare the variable-step floating point simulation block to the fixed-point equivalent. The floating point model is the gold standard against which you evaluate the performance of your fixed-point FPGA model.
- Avoid building individual simulation blocks containing their own solvers. You can run into a problem where you have validated each block individually, but then you run into numerical issues when they are strung together in series. As a rule, try to use a single solver rather than multiple distributed solver.
- The state-space architecture is preferred because it uses a single solver and parallel first order difference equations. State space:
  - Reduces series connected accumulation of errors.
  - Minimizes number of solver integrator/accumulators “distributed” throughout the simulation.

Fixed-point math advice

- If you must have multiple solvers, try to run them all at the same rate and at a fast rate. The connections between solvers are discrete delays (zero order holds) that can be problematic unless your timestep is small for **both** solvers. If your solvers are running at different rates, you need to account for the different ΔT values in the solver, which adds complexity.
  - The main problems that occurs when using multiple solvers comes from coupled dynamics that span between the solvers:
  - Take a simple brushed DC motor as an example: You may want to put the mechanical/transmission equations (torque/load equations) in one solver that runs at a relatively slow rate, say in an RT processor, and the electrical equations (voltage/current/back EMF) in another solver that runs at a fast rate, say in an FPGA. The problem is that the equations are coupled (Torque = current*motor torque constant). A large ΔT for the communication path between the solvers will cause completely inaccurate results- especially during the times when the current (and therefore the torque and motor speed) changes quickly at the startup inrush conditions and spinning direction reversals.

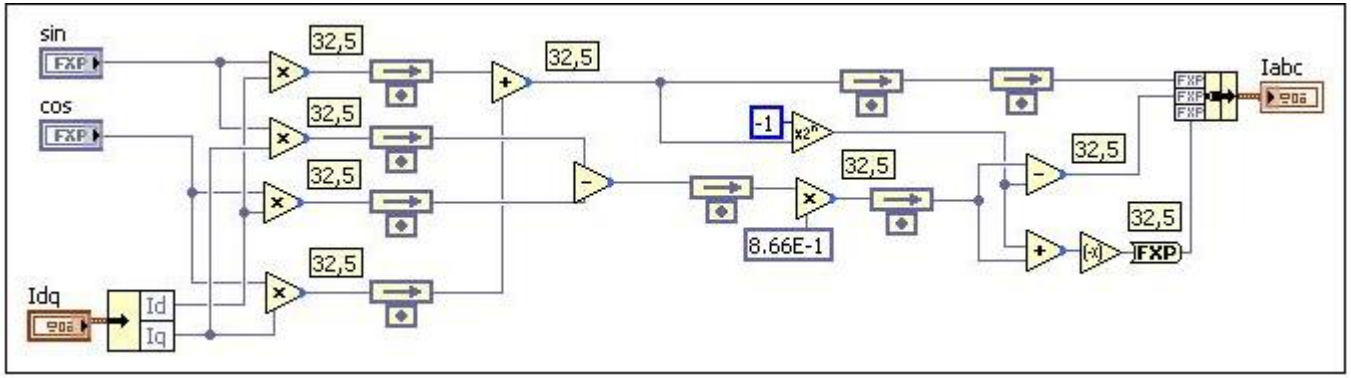
Modeling the power system connected to the device

- You can model the aggregate behavior of the DC bus or AC transmission line network connected to your inverter by using a power simulation tool to obtain the frequency response of the overall grid network, then model that in the FPGA by creating a state-space model that has the equivalent frequency response (Bode amplitude and phase). This enables you to efficiently model the aggregate response of the network efficiently, while boiling it down to frequency response. Then you focusing your detailed modeling effort on the power blocks (inverters/converters/motors/generators) that you are designing/testing.

Converting arbitrary models from floating to fixed point

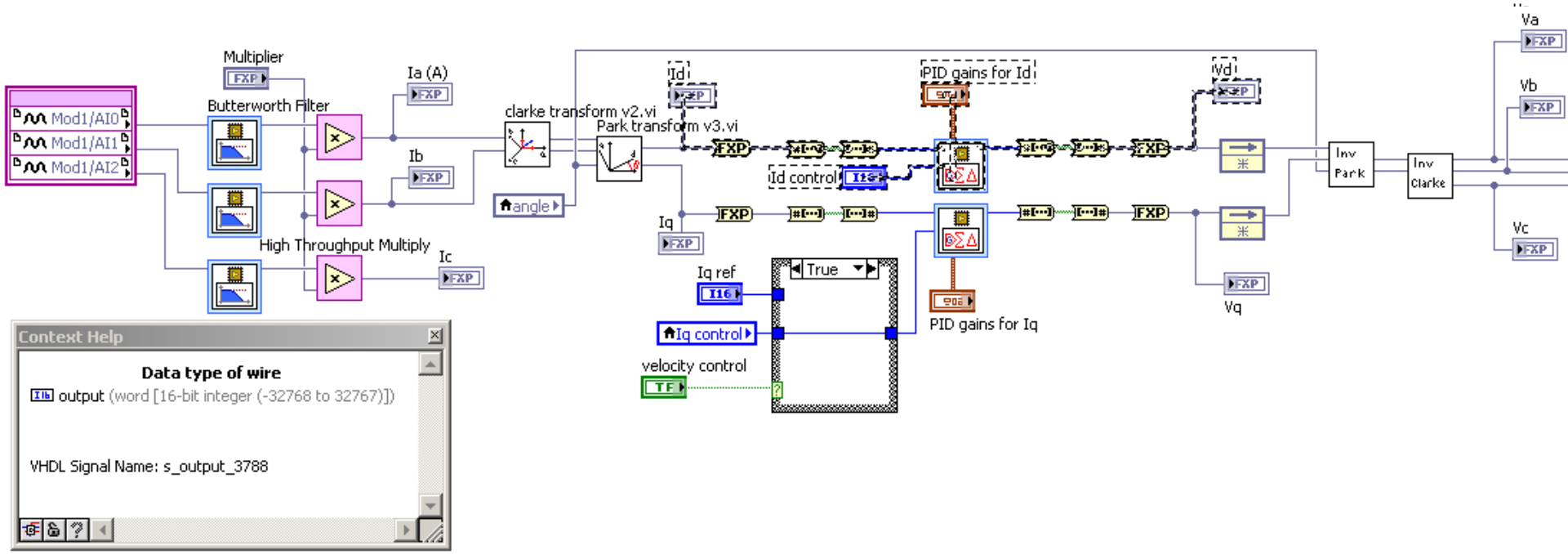
1. Floating point continuous time > Floating point discrete time
   - Simulation for verification
2. Floating point discrete time to > Fixed point discrete time
   - Simulation for verification
3. Compile to FPGA

Inverse Park Transform Example:



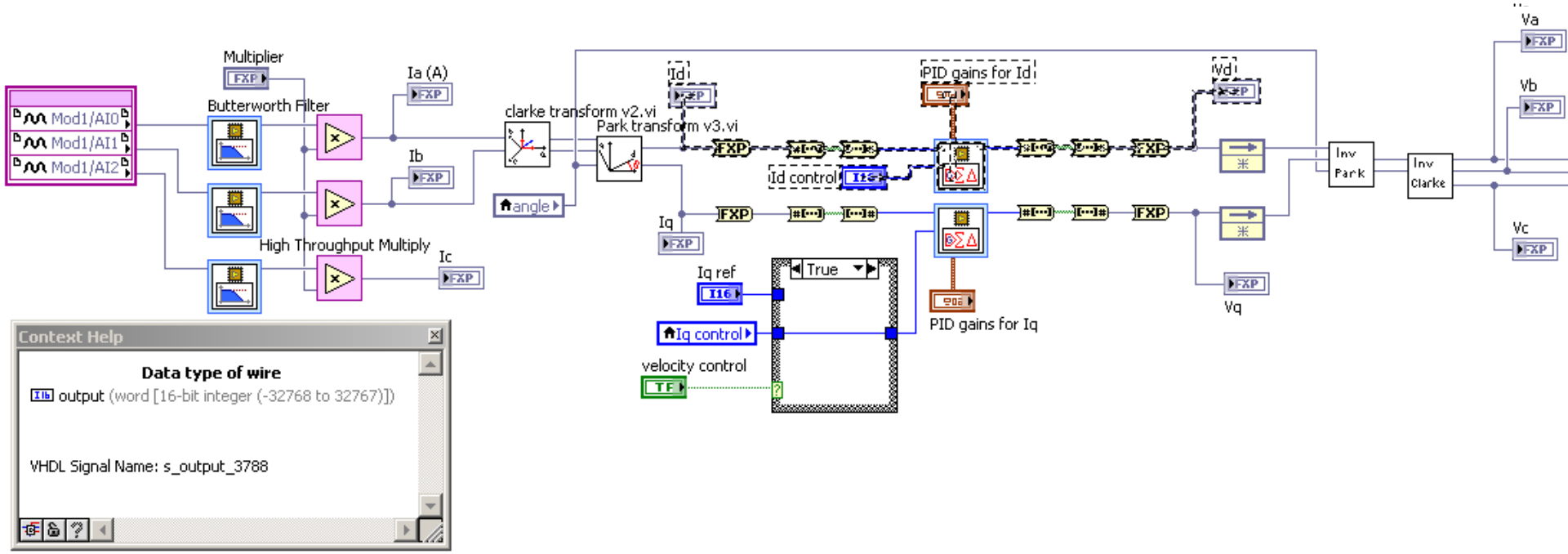
Start with a simple windows “test bench” to check your math

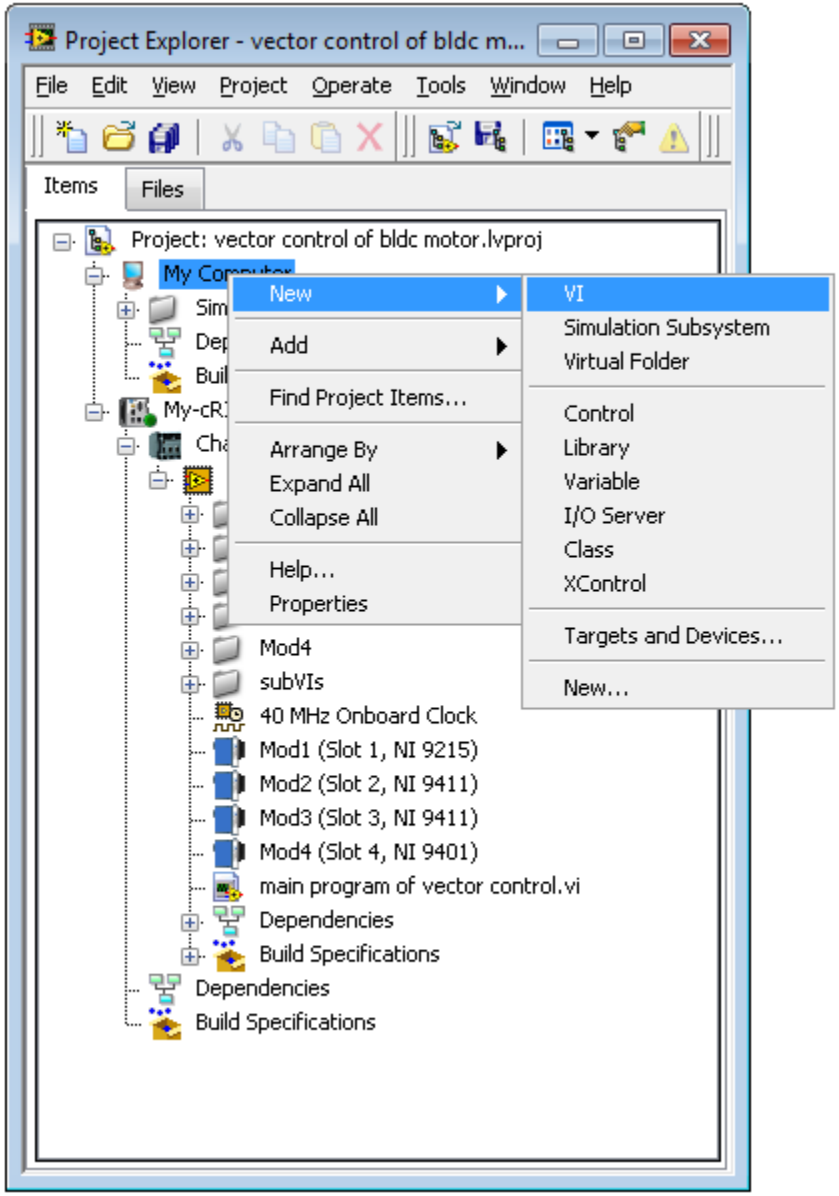
- Example: Space Vector PMSM Motor Control
  - The word length for **Id** is 24,9. Is that the optimal choice?

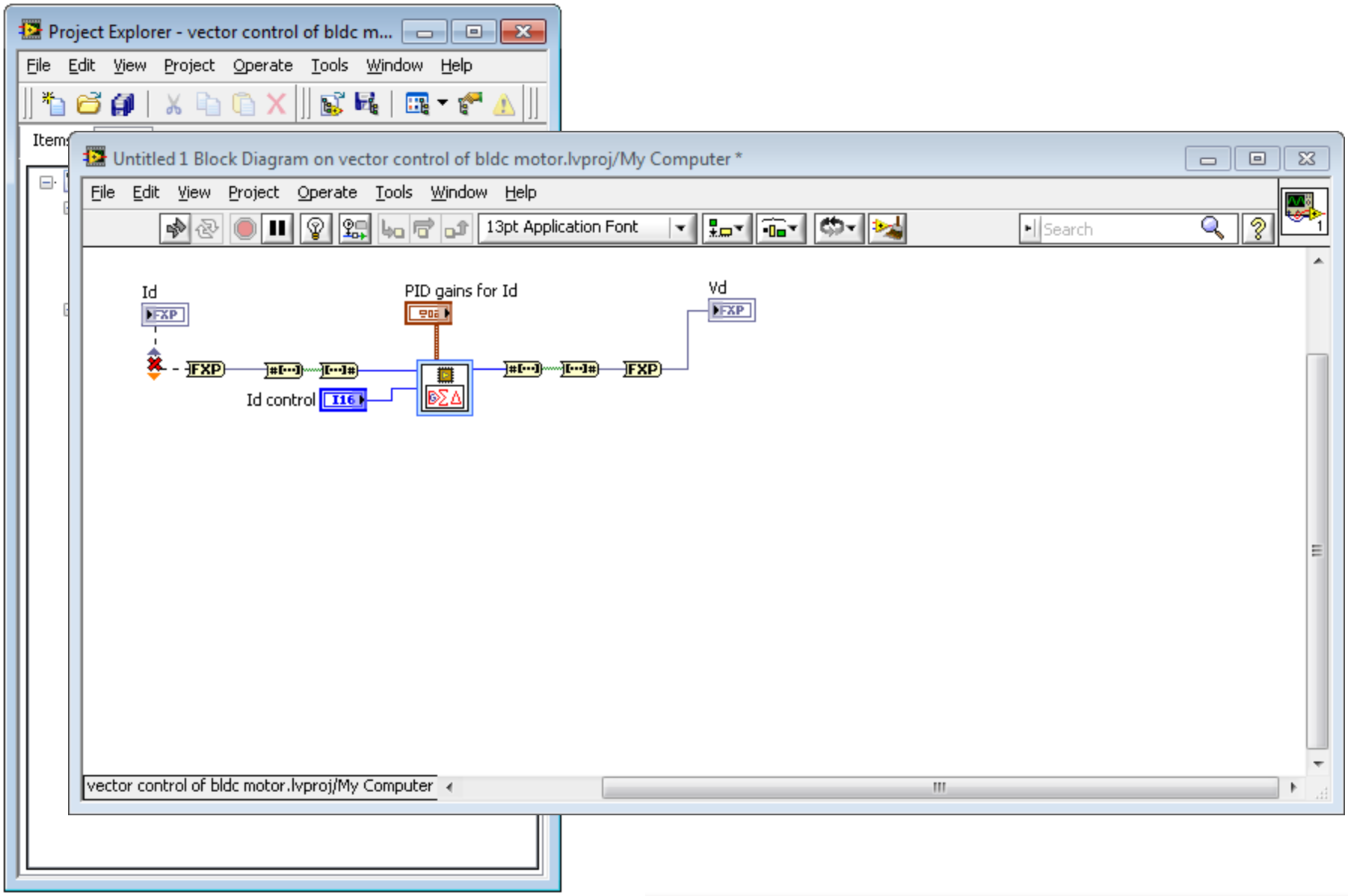


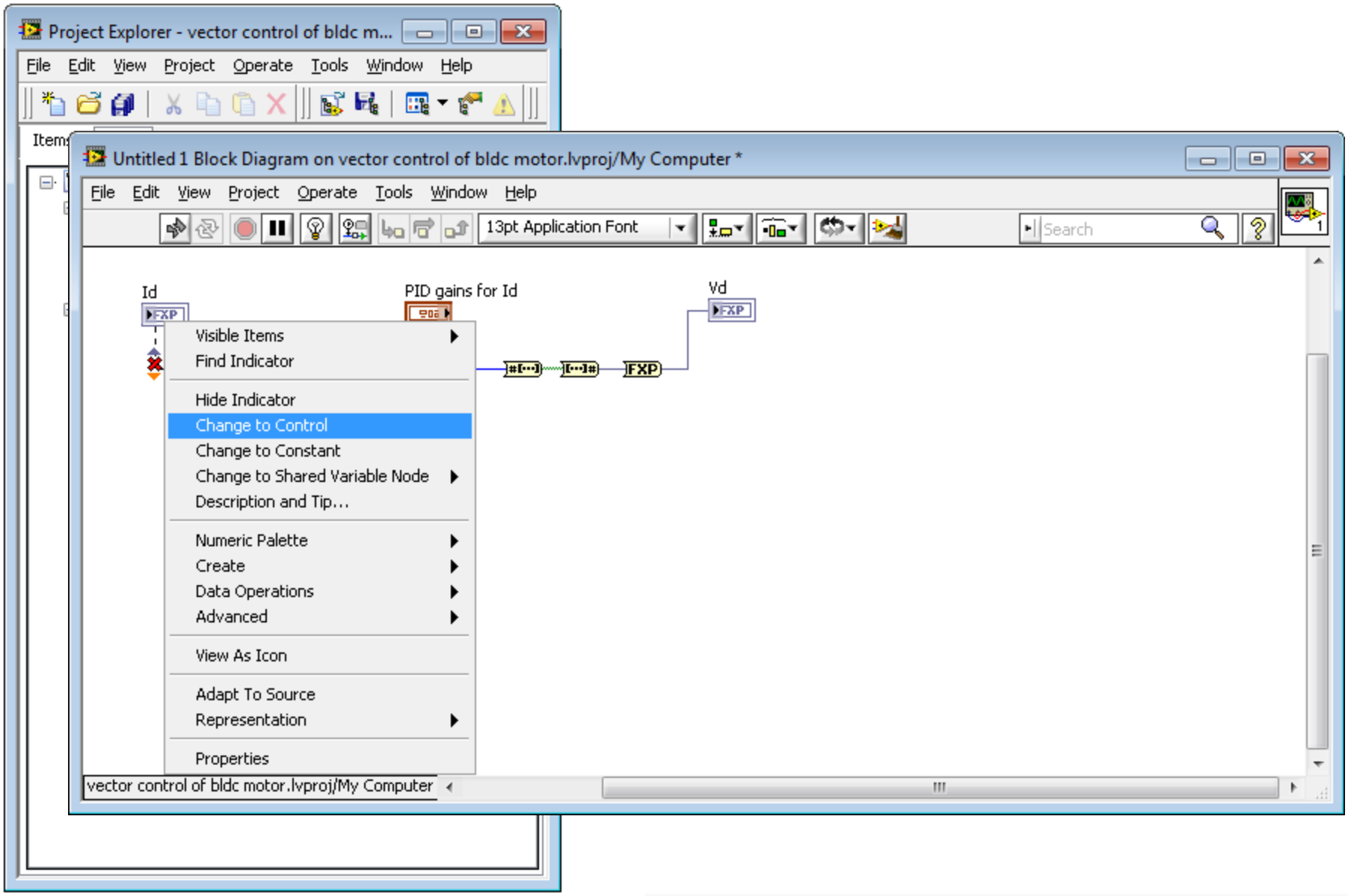
Start with a simple windows “test bench” to check your math

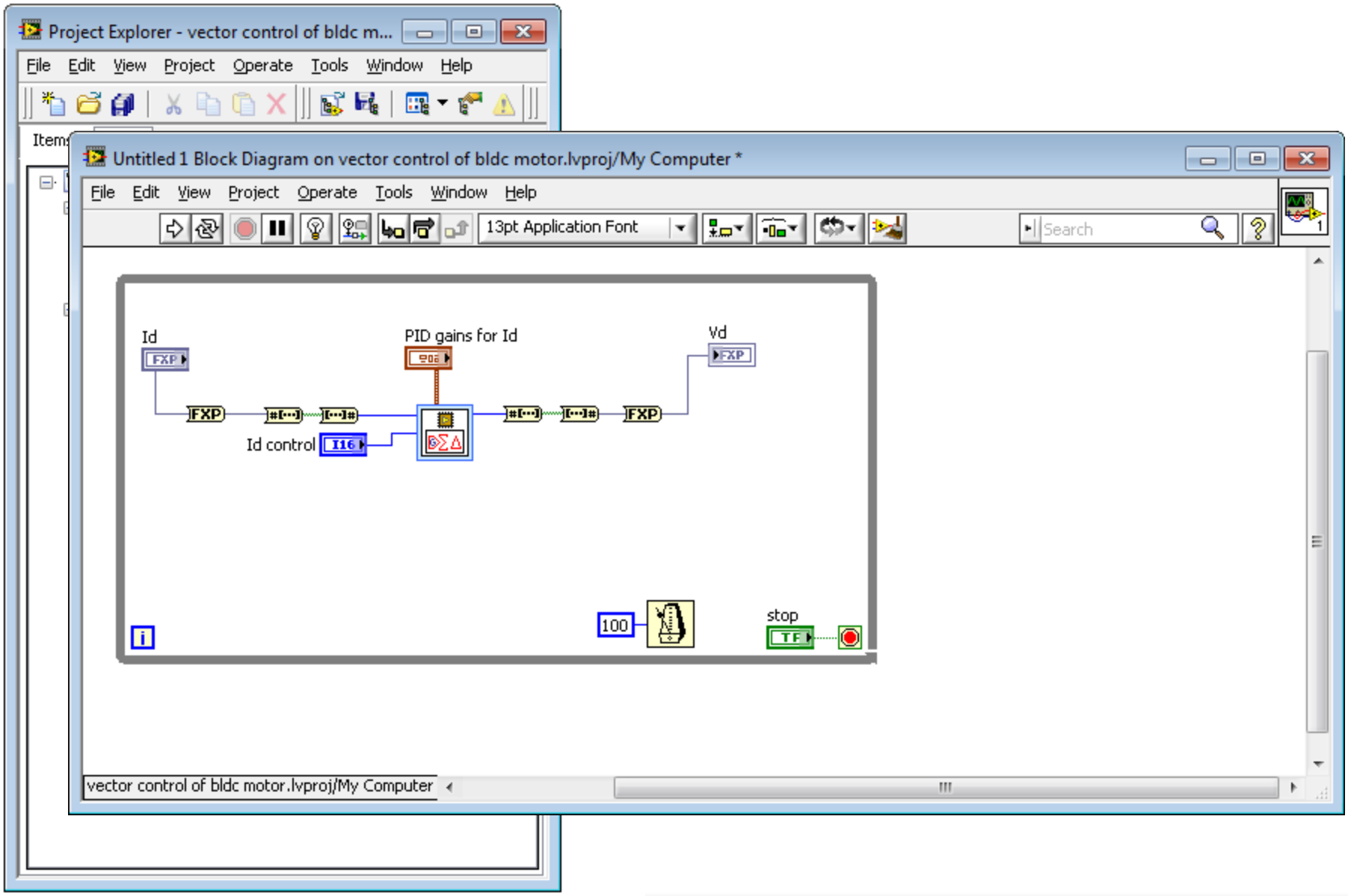
- Example: Space Vector PMSM Motor Control
  - The word length for **Id** is 24,9. Is that the optimal choice?
  - Let’s copy that section to Windows and find out…

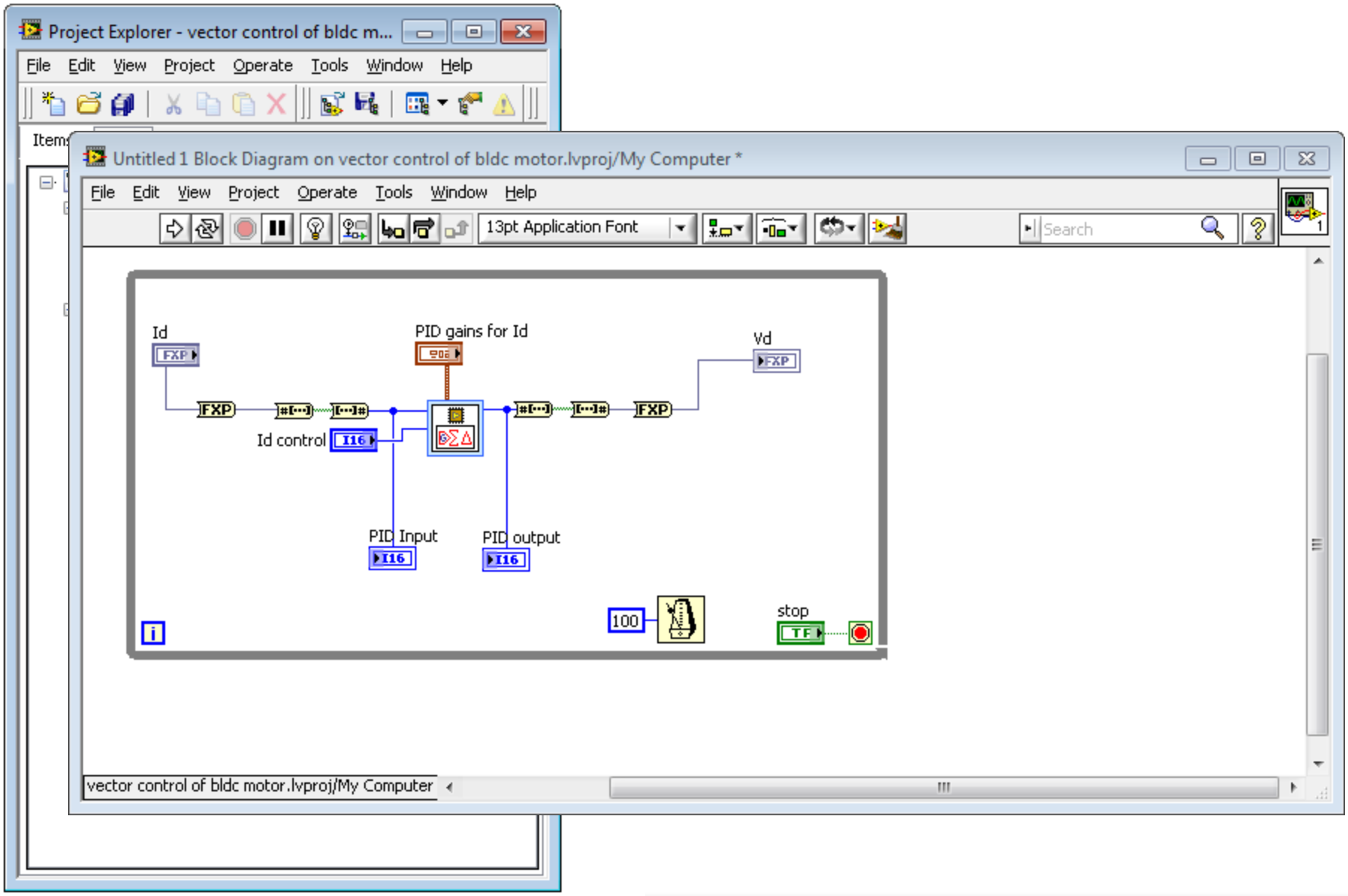




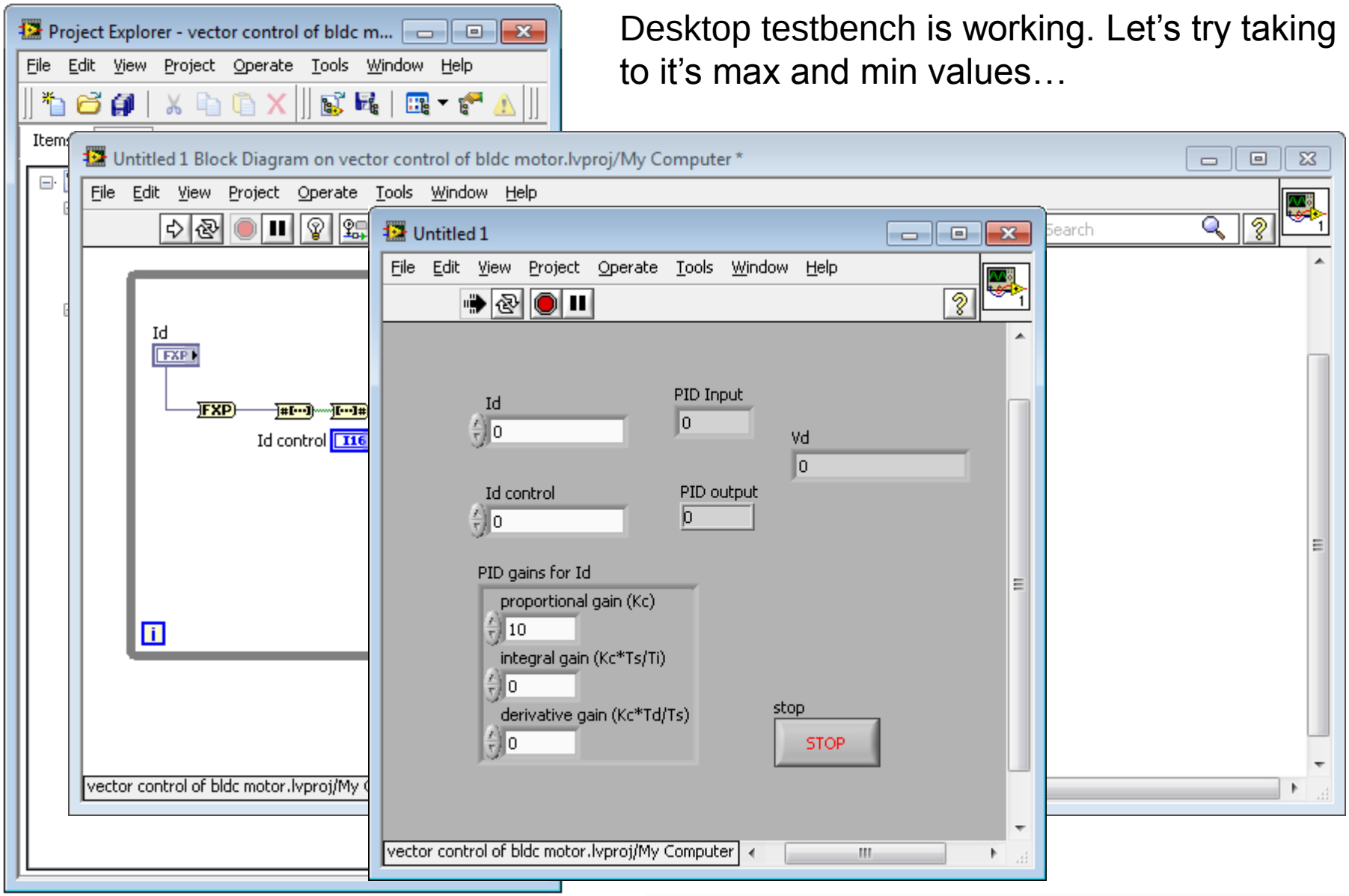




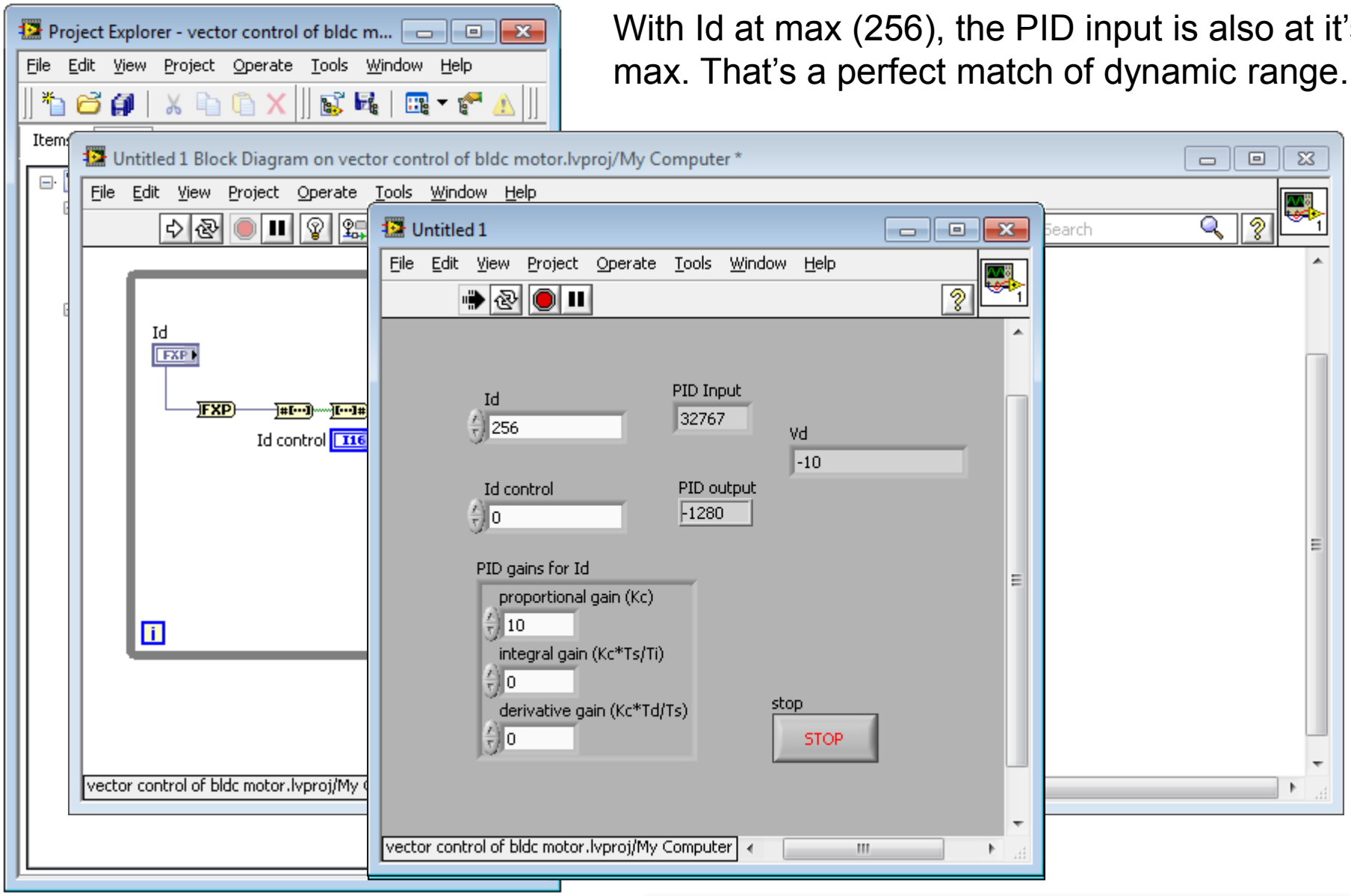




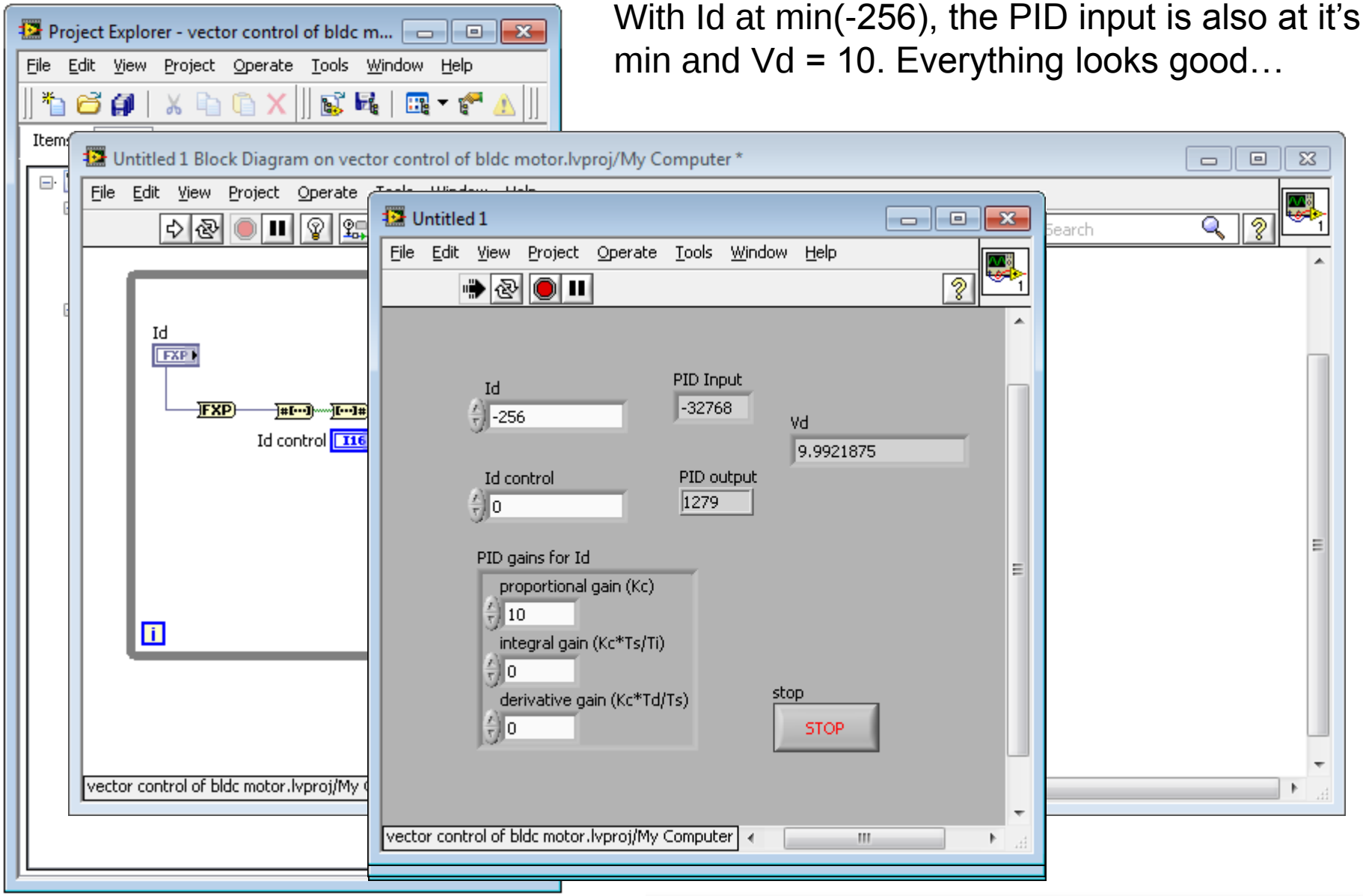
Desktop testbench is working. Let's try taking Id to it's max and min values…



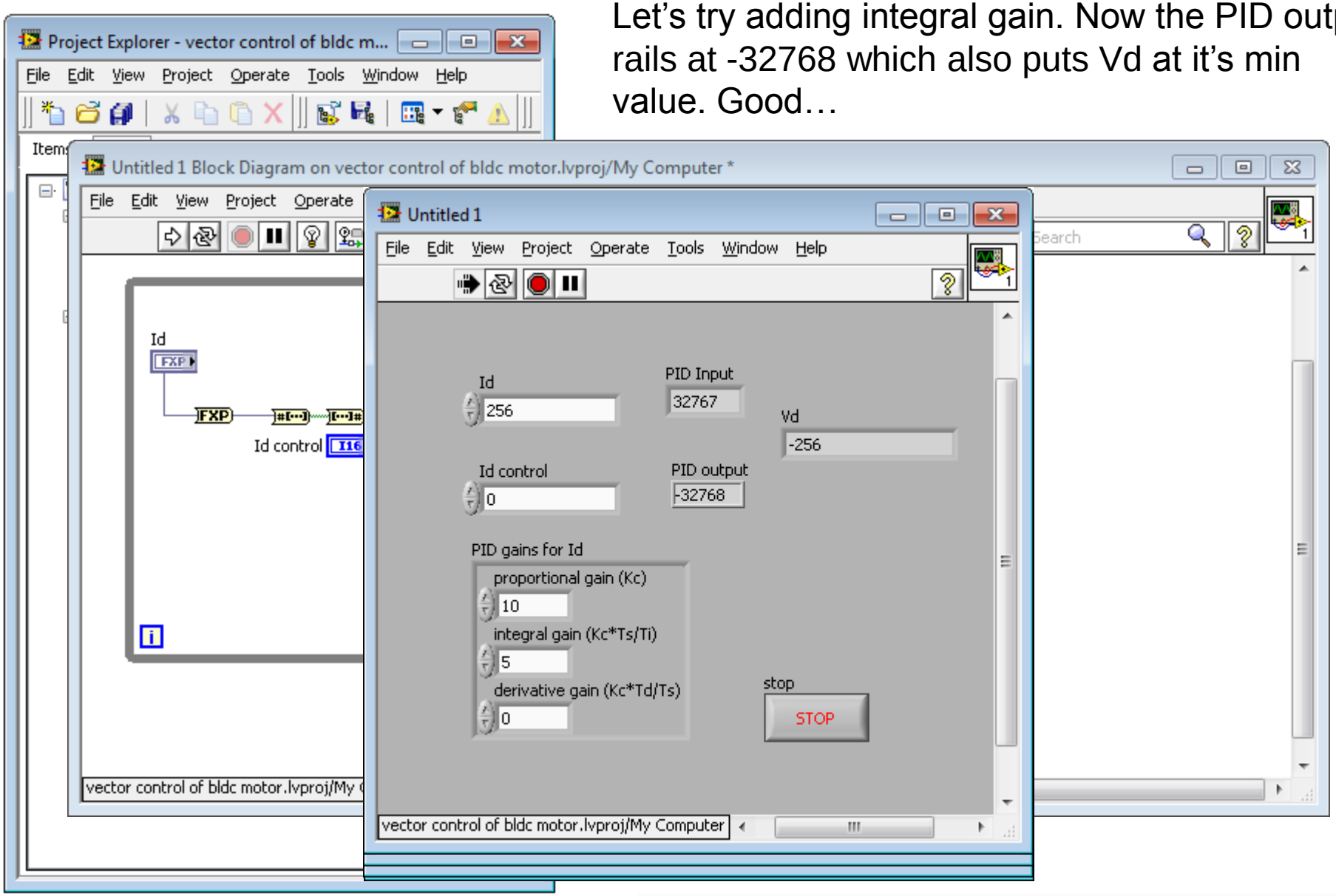
With Id at max (256), the PID input is also at it's max. That's a perfect match of dynamic range…



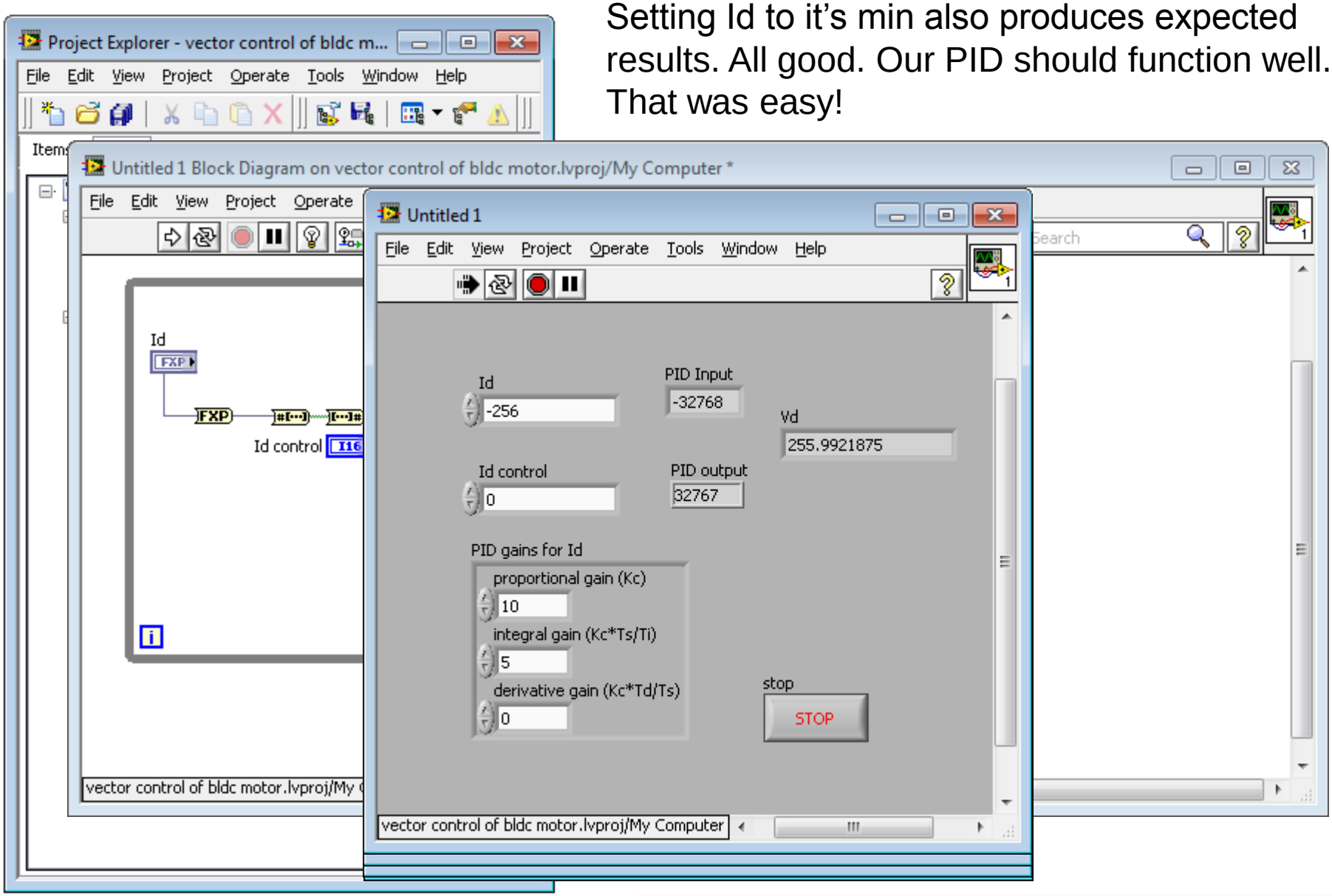
With Id at min(-256), the PID input is also at it's min and Vd = 10. Everything looks good…



Let's try adding integral gain. Now the PID output rails at -32768 which also puts Vd at it's min value. Good…

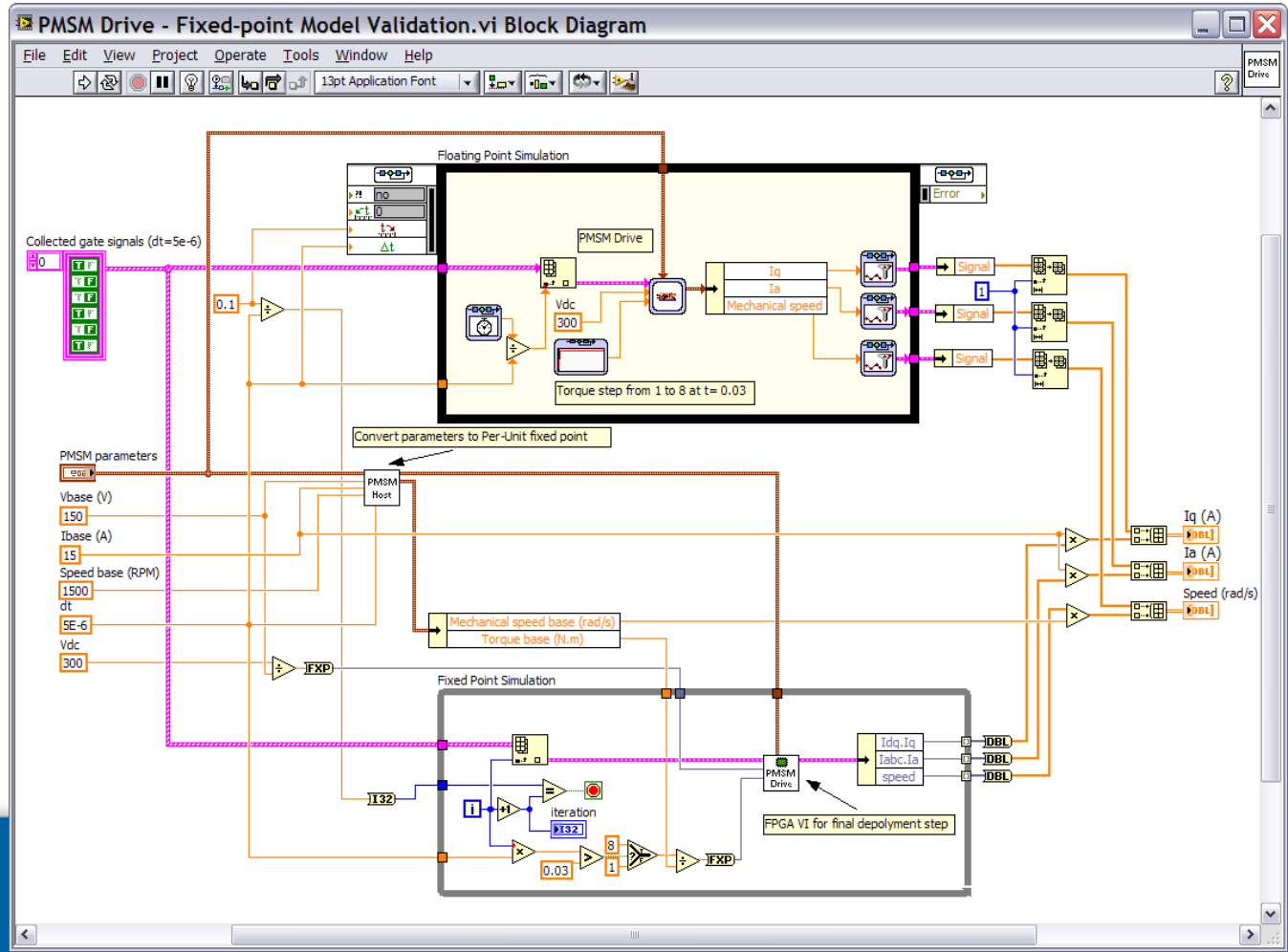


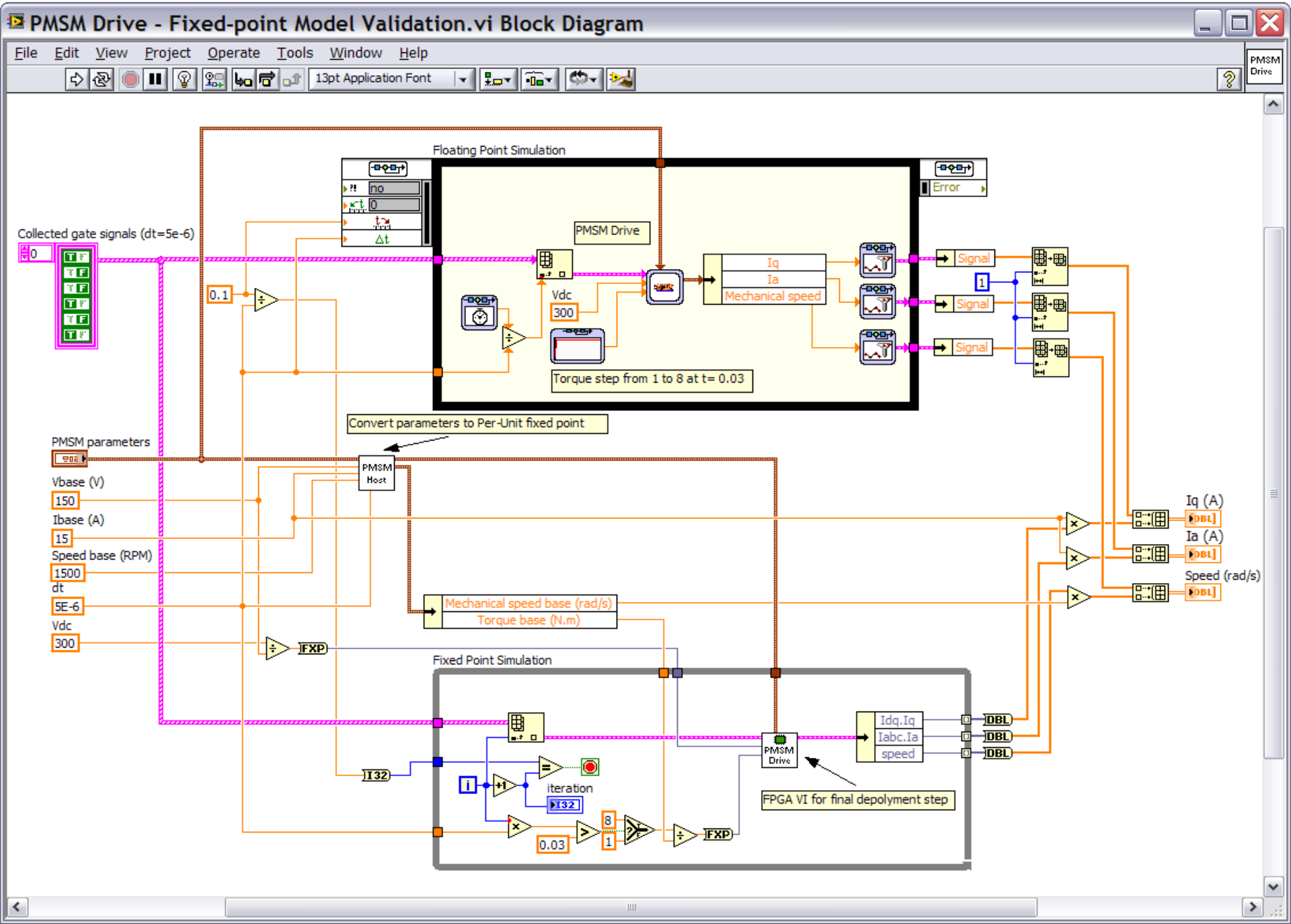
Setting Id to it's min also produces expected results. All good. Our PID should function well. That was easy!



Create a benchmark simulation to compare floating, continuous time models to your fixed point version

- Desktop testbench application used to validate fixed point LabVIEW FPGA code by comparing results to a floating point simulation




PMSM Drive - Fixed-point Model Validation.vi Block Diagram
File Edit View Project Operate Tools Window Help
13pt Application Font
PMSM Drive
Floating Point Simulation
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Δt
Error
Collected gate signals (dt=5e-6)
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0.1
PMSM Drive
Vdc
300
Iq
Ia
Mechanical speed
Signal
Signal
Signal
1
Torque step from 1 to 8 at t= 0.03
Convert parameters to Per-Unit fixed point
PMSM parameters
PMSM Host
Vbase (V)
150
Ibase (A)
15
Speed base (RPM)
1500
dt
5E-6
Vdc
300
FXP
Mechanical speed base (rad/s)
Torque base (N.m)
Iq (A)
Ia (A)
Speed (rad/s)
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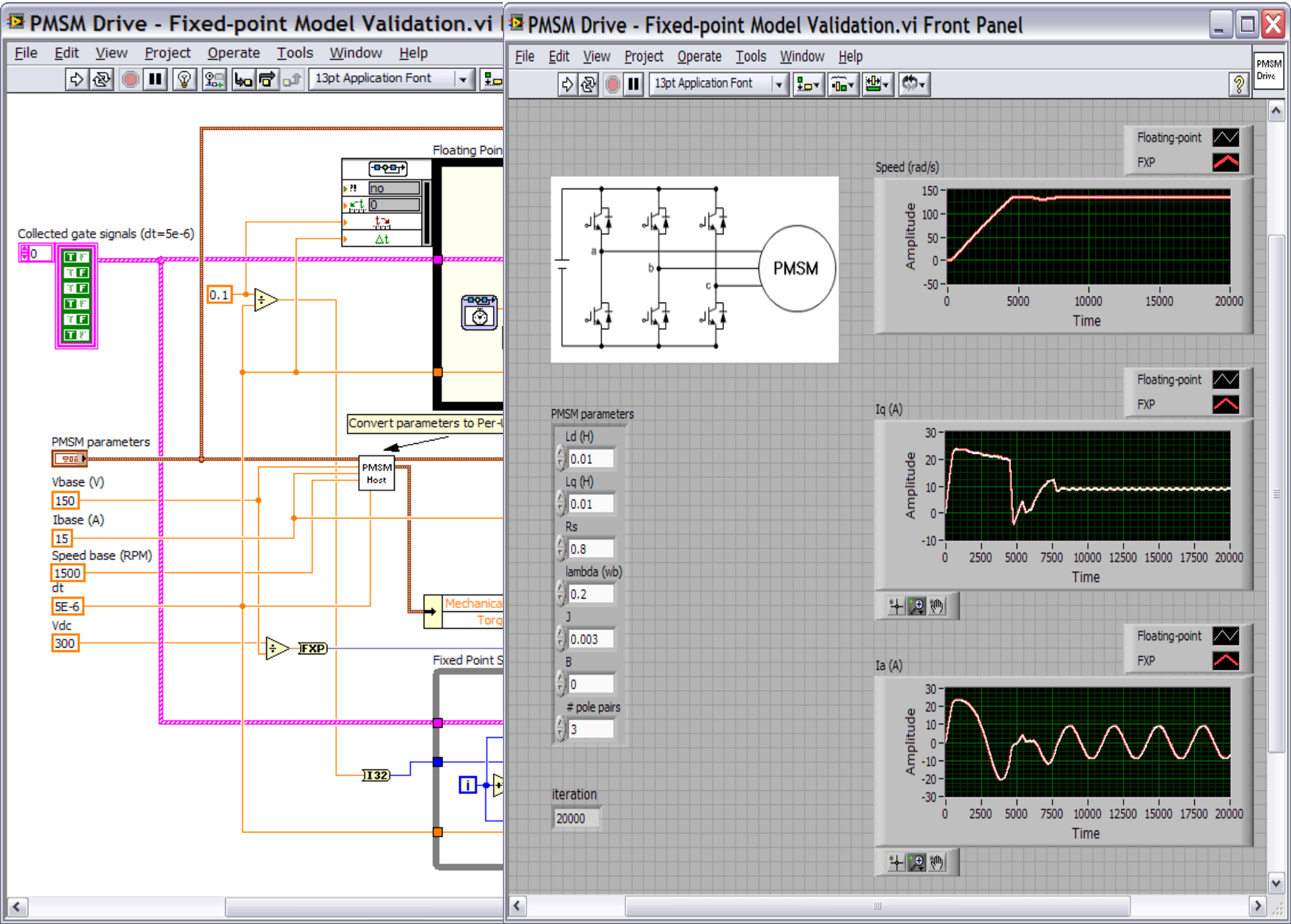
DBL
DBL
FPGA VI for final depolyment step


PMSM Drive - Fixed-point Model Validation.vi
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20000

Hard DSP processing cores integrated into FPGA fabric!

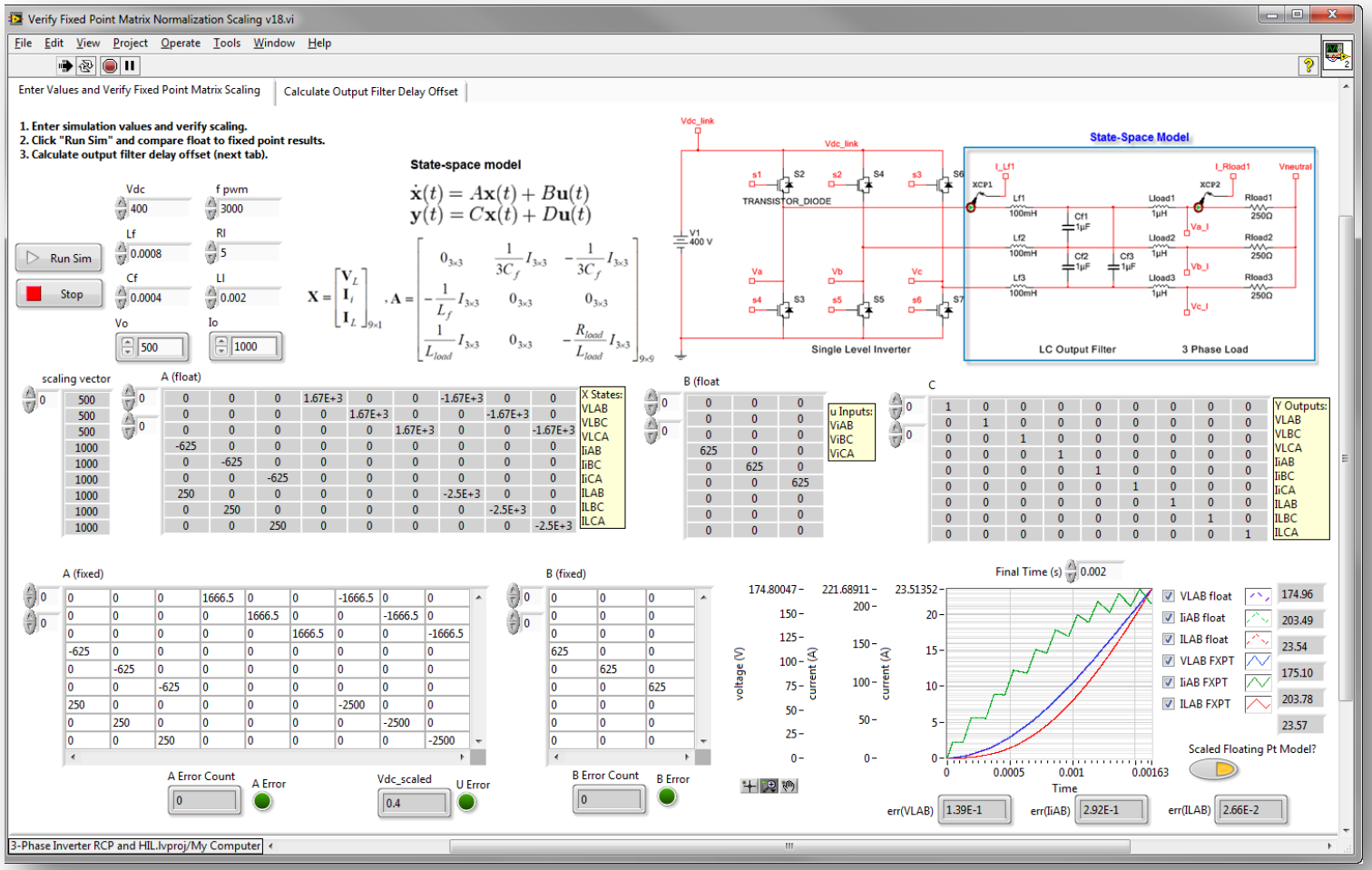
Model	Bus/ Form Factor	FPGA	FPGA Slices	FPGA DSP Slices	FPGA Memory (Block RAM)	Onboard Memory (DRAM)
NI PXIe-7965R	PXI Express	Virtex-5 SX95T	14,720	640	8,784 kbits	512 MB

DSP Performance: 352,000 MMACs!

(352 billion multiply accumulate operations per second)

Figure 2. *NI FlexRIO FPGA modules offer peer-to-peer data streaming technology.*

	Spartan-3 1000	Spartan-3 2000	Virtex-II 1000	Virtex-II 3000	Virtex-5 LX30	Virtex-5 LX50	Virtex-5 LX85	Virtex-5 LX110	Virtex-5 SX50T	Virtex-5 SX95T
									PXIe-FlexRIO	PXIe-FlexRIO
Gates	1 million	2 million	1 million	3 million	-----	-----	-----	-----	-----	-----
LUTs/FFs	15,360	40,960	10,240	28,672	19,200	28,800	51,840	69,210		
Multipliers (DSP48E on V5/V6)	24	40	40	**96**	32	48	48	64	288	**640**
Block RAM (kb)	432	720	720	1,728	1,152	1,728	3,456	4,608	4,752	8,784



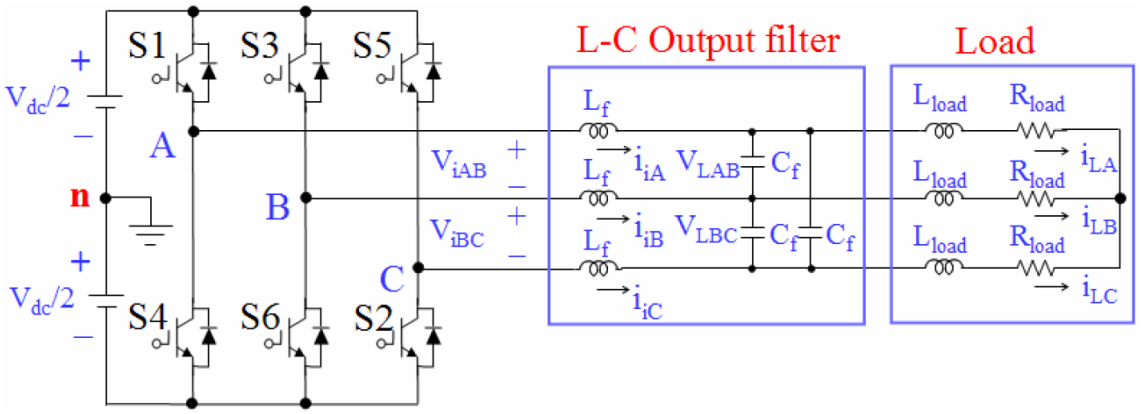
NATIONAL INSTRUMENTS

STATE SPACE BASED FPGA SIMULATION

State-Space Based Simulation in FPGA: Pros & Cons

- Pros
  - System arranged into first order differential equations
    - Avoids instability caused by multiple poles at boundary of unit circle
- Cons
  - If components are added or removed, the state-space equations must be re-derived
    - Symbolic math tools can help automate the process (i.e. Maple, Mathematica)

A New Era: Inverter Real-Time Virtual Prototype



System Parameters

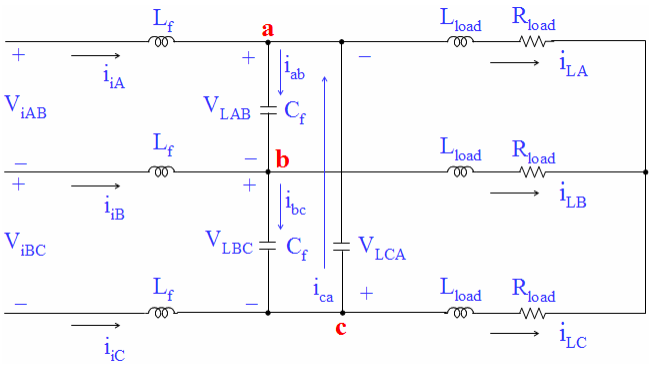
IGBTs: SEMIKRON SKM 50 GB 123D, 600 V, 80 A
DC – link voltage: Vdc = 400 V
Fundamental Freq = 60 Hz
PWM (carrier) Freq = 3 KHz
Output Filter: Lf = 800 μH Cf = 500 μF
Load: Lload = 2 mH Rload = 5 Ω

Simulation loop rate of **3.57 MHz (0.28 μs)**

> 3000X Acceleration vs. Processor

Reference: MCBRYDE, JAMES. Inverter Efficiency Simulation and Measurement for Various Modern Switching Devices.

Development of State-Space Model



Apply Kirchoff's current and voltage laws

Final equation set scaled for more accurate FXP handling

$$I = il_0$$

$$V = vV_0$$

$$\dot{\mathbf{X}}(t) = \mathbf{A}\mathbf{X}(t) + \mathbf{B}\mathbf{u}(t),$$

$$\text{where, } \mathbf{X} = \begin{bmatrix} \mathbf{V}_L \\ \mathbf{I}_i \\ \mathbf{I}_L \end{bmatrix}_{9\times 1}, \mathbf{A} = \begin{bmatrix} 0_{3\times 3} & \frac{1}{3C_f} I_{3\times 3} & -\frac{1}{3C_f} I_{3\times 3} \\ -\frac{1}{L_f} I_{3\times 3} & 0_{3\times 3} & 0_{3\times 3} \\ \frac{1}{L_{load}} I_{3\times 3} & 0_{3\times 3} & -\frac{R_{load}}{L_{load}} I_{3\times 3} \end{bmatrix}_{9\times 9}, \mathbf{B} = \begin{bmatrix} 0_{3\times 3} \\ \frac{1}{L_f} I_{3\times 3} \\ 0_{3\times 3} \end{bmatrix}_{9\times 3}, \mathbf{u} = \left[\mathbf{V}_i\right]_{3\times 1}.$$

Reference: MCBRYDE, JAMES. Inverter Efficiency Simulation and Measurement for Various Modern Switching Devices.

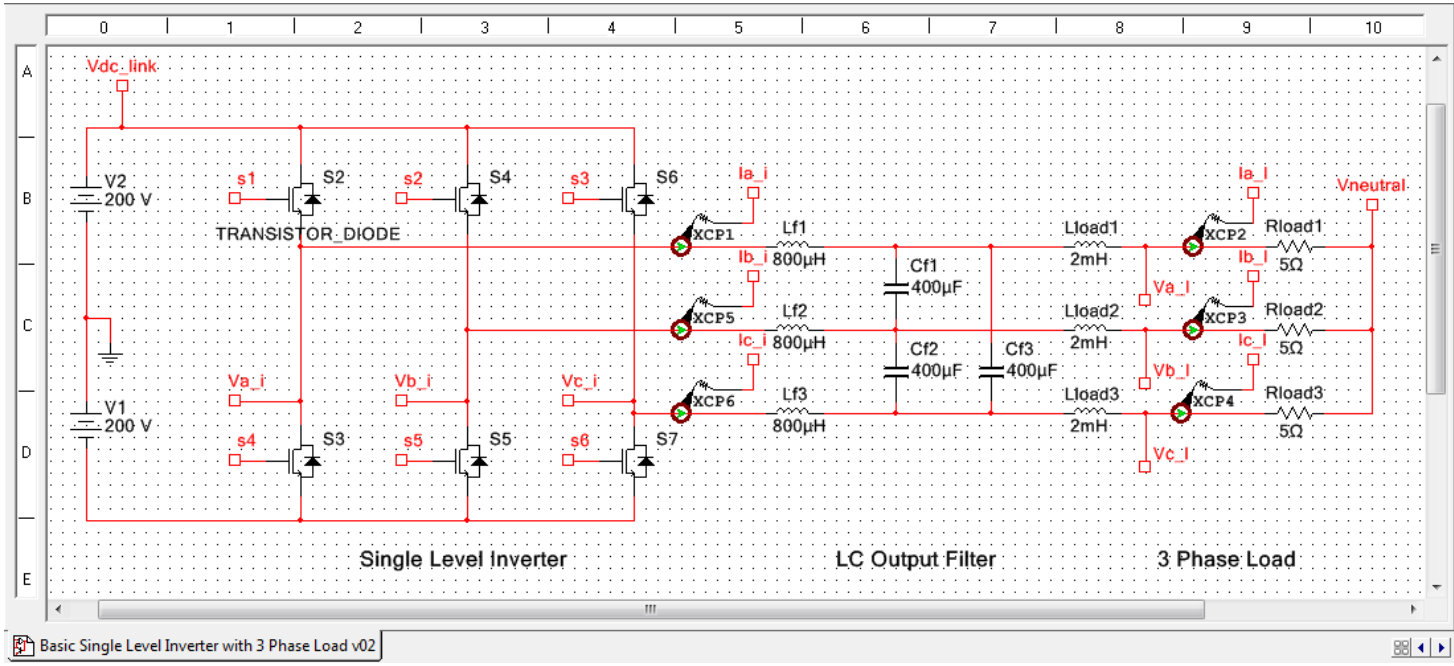
Resource Usage and Timing of Current Implementation (7965R)

- Total Slices: 37.9% (5585 out of 14720)
- Slice Registers: 25.6% (15070 out of 58880)
- Slice LUTs: 27.3% (16057 out of 58880)
- DSP48s: 6.2% (40 out of 640)

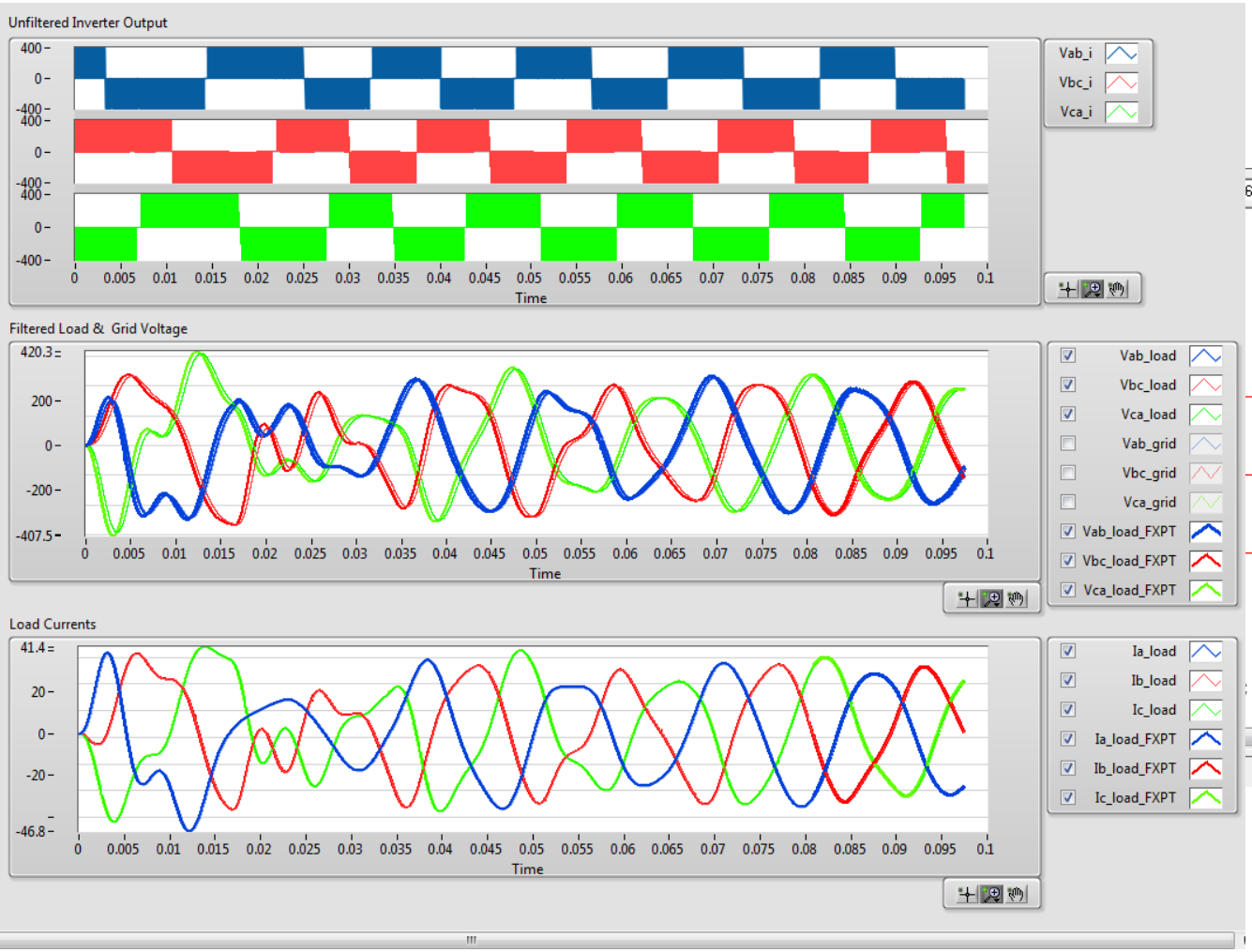
Inverter Calculation time: 28 ticks of 100 MHz clock (280 ns)

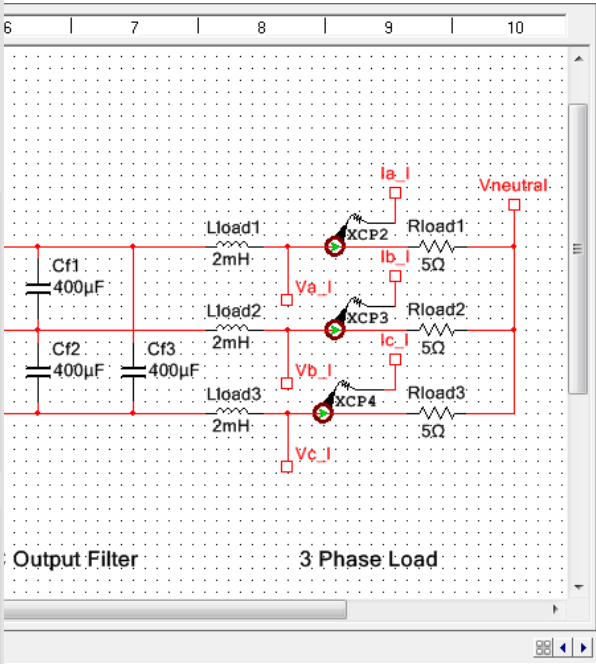
(178 times faster than 20 kHz PWM switching frequency)

Comparison of Multisim vs. LabVIEW FPGA Results



Comparison of Multisim vs. LabVIEW FPGA Results





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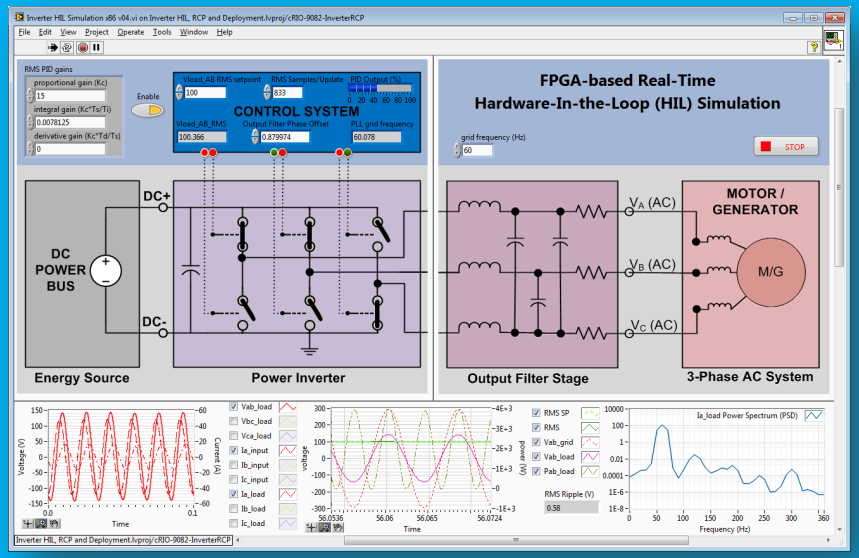


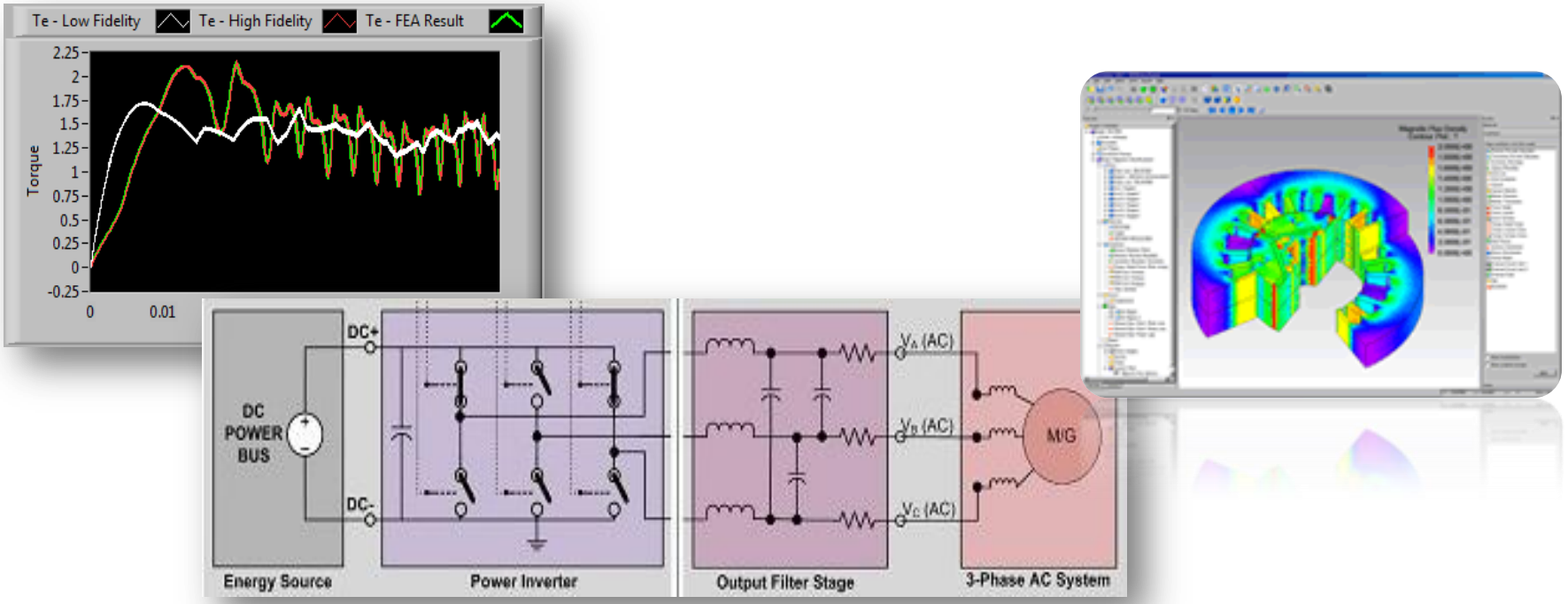
Device Utilization on Multicore CompactRIO (Spartan-6 LX150 with 180 DSP48A1 cores)

3-ph Inverter HIL + sine-triangle PWM control

Total Slices: 35.8% (8238 out of 23038)
Slice Registers: 13.7% (25197 out of 184304)
Slice LUTs: 24.9% (22945 out of 92152)
DSP48s: 51.7% (93 out of 180)
Block RAMs: 9.3% (25 out of 268)

Complete Reference Design: 3-Phase Inverter RCP and HIL with LabVIEW Project

VIDEOS AND CODE



NATIONAL INSTRUMENTS

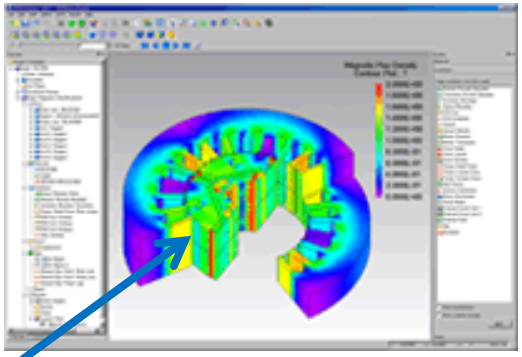
JMAG FEA-BASED MOTOR-INVERTER HIL SIMULATION

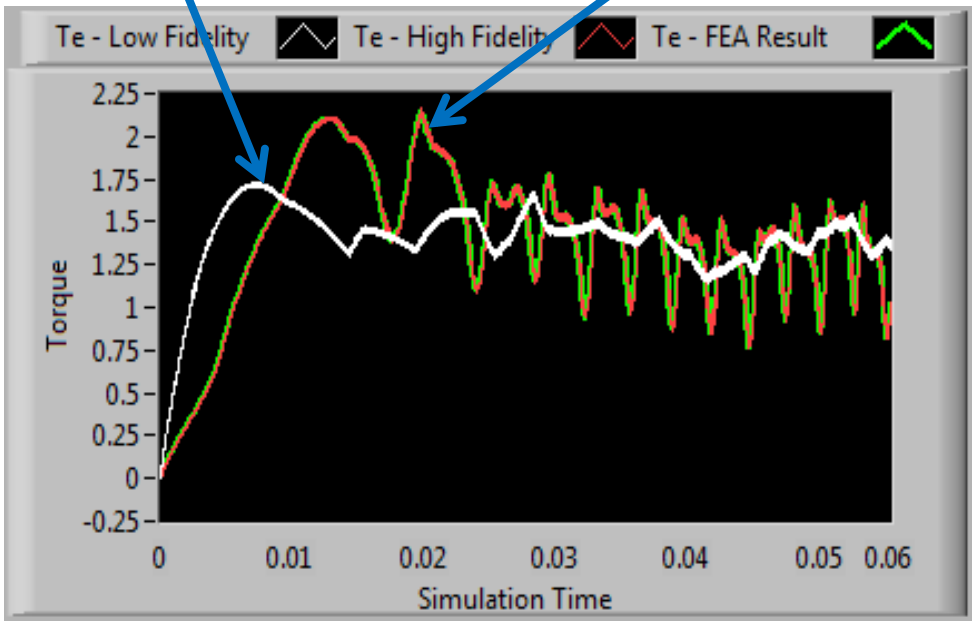
When simulating electromagnetic systems, model accuracy matters!

PMSM Sinusoidal Flux Model*
(DQ Reference Frame)

$$Vsvd = P * \omega_m * Lq * Iq$$
$$Vsvq = P * \omega_m * (Ld * Id * \lambda)$$
$$Te = \frac{3}{2} * P * (Iq * (Id * Ld + \lambda) - Id * (Iq * Lq))$$

JMAG FEA Model





<u>Low Fidelity Model Assumptions:</u>

- Uniform air-gap
- No slot harmonics
- No stator saturation
- Sinusoidally distributed windings
- No zero phase sequence (system is balanced)

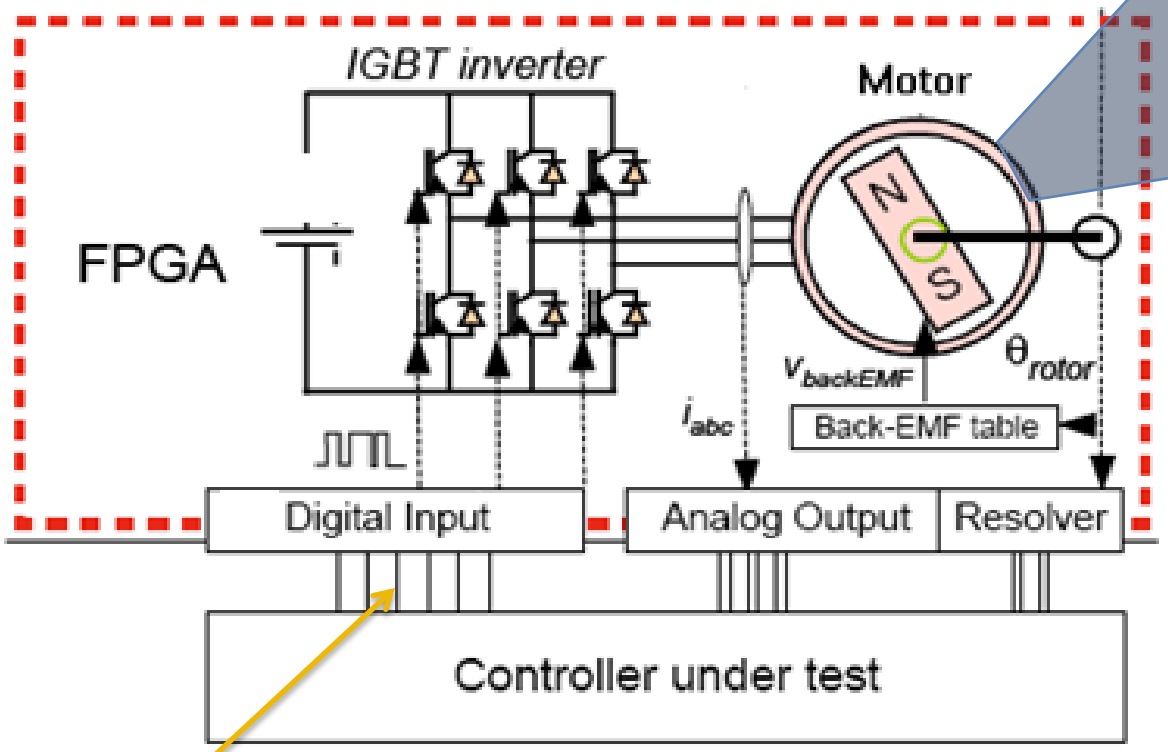
<u>High Fidelity Model Assumptions:</u>

- Complex geometry
- Magnetic materials
- Permanent magnets
- Nonlinear inductance
- Saturation effects
- Coil winding
- Copper and iron losses
- Efficiency (post processing)

Used Today for the Future of Tomorrow

JMAG®

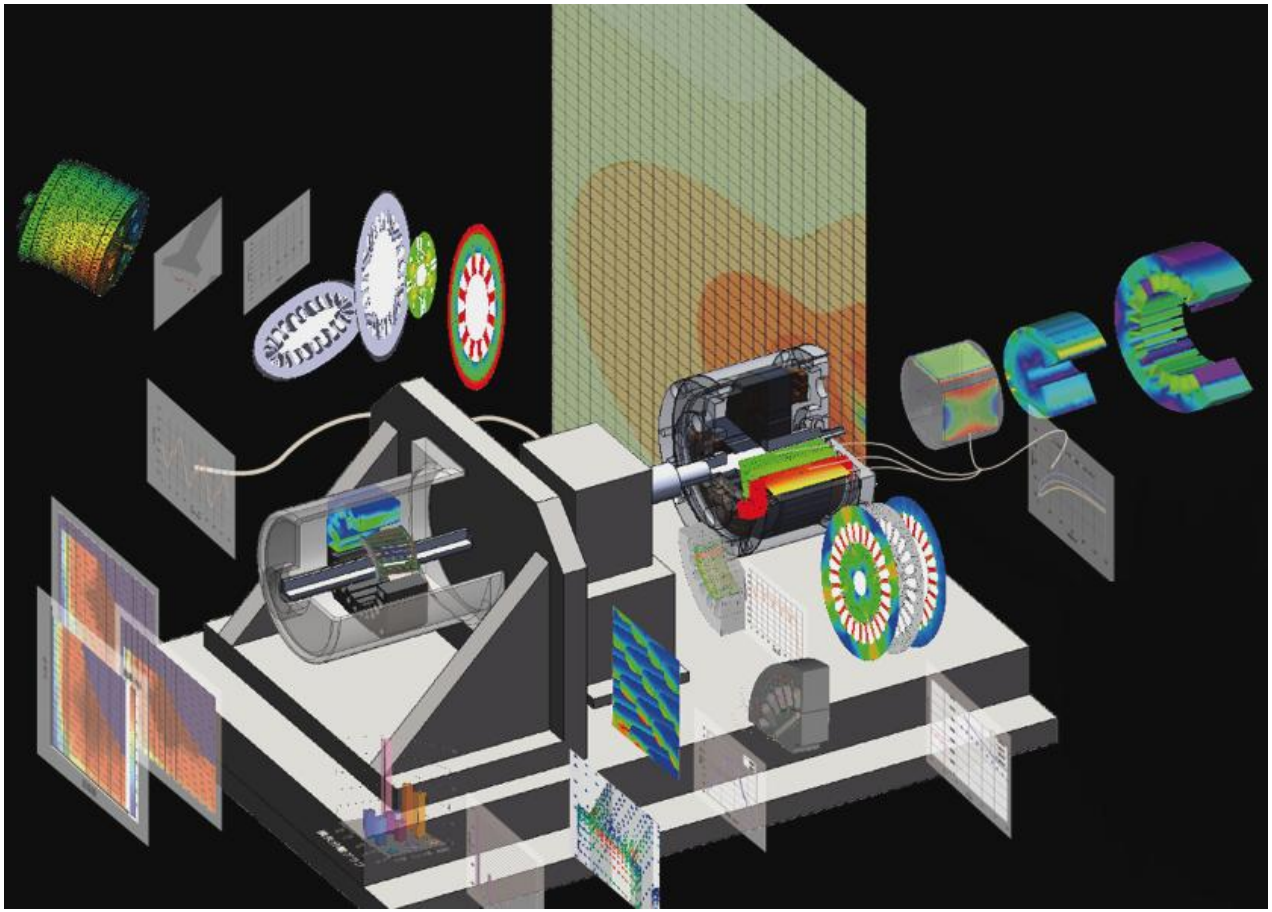
Electric Motor Systems



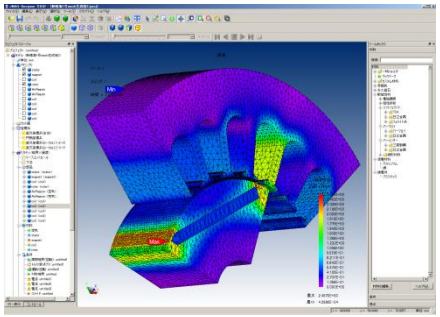
25kHz PWM → Loop rate of simulator > 250k

FPGA-Based Power Electronics HIL

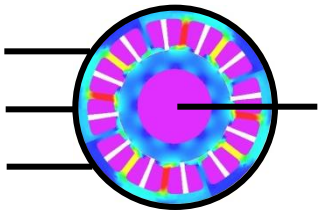
JMAG RT Add-Ons for LabVIEW and NI VeriStand



JMAG High Fidelity Simulation



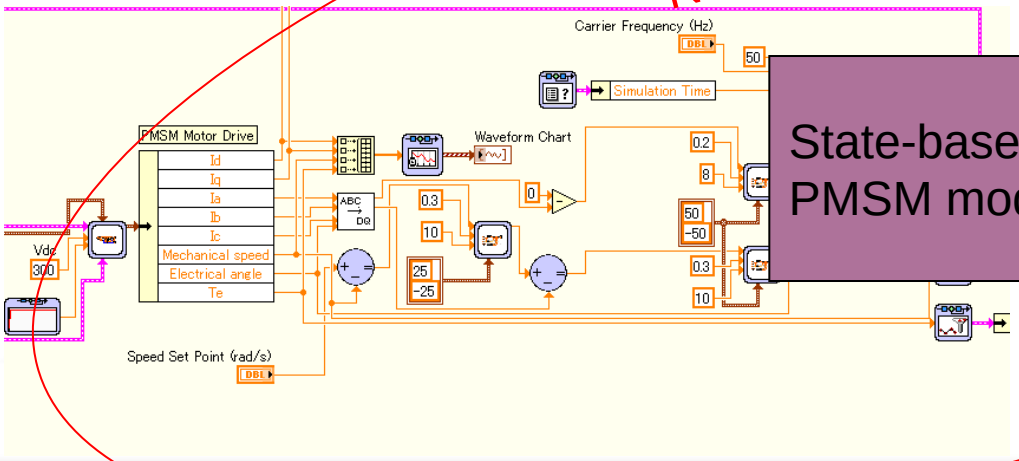
JMAG FEA



JMAG-RT model
·RTT file; look-up table
·Binary

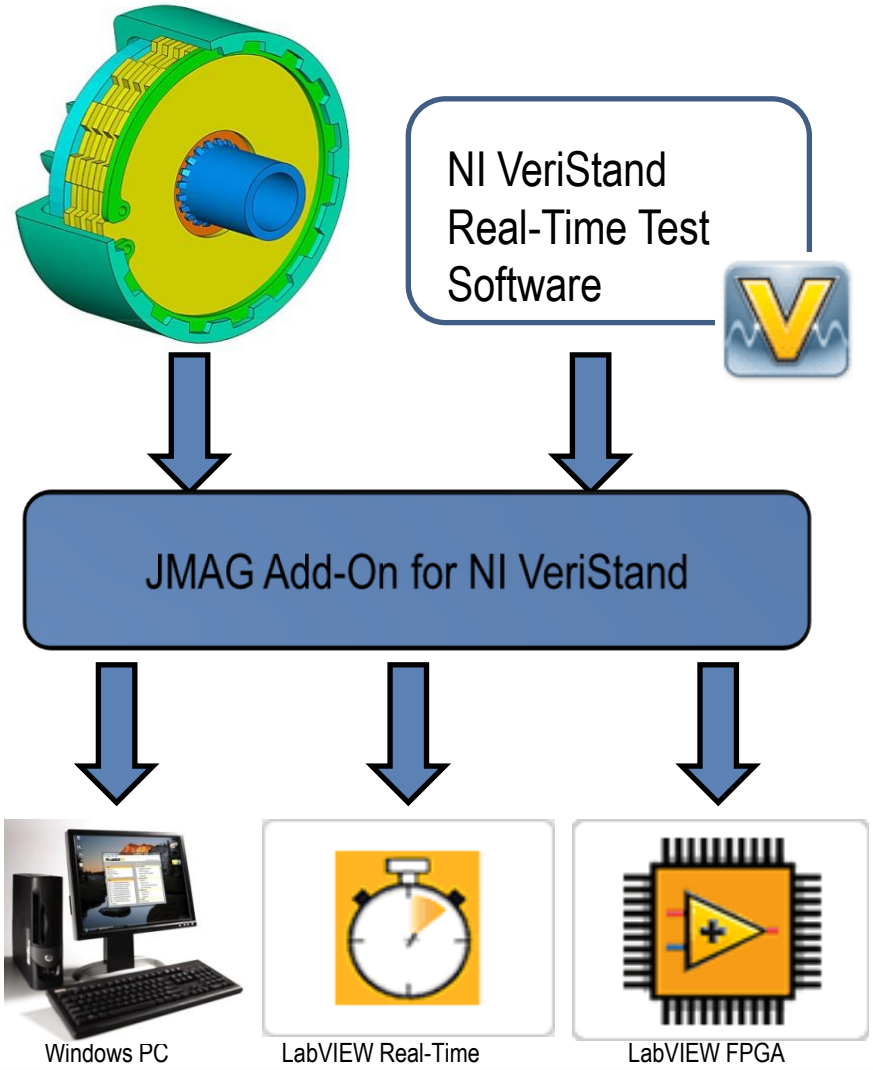
NI Real-Time Hardware

Converter
•Reads RTT file
•Generates LUTs



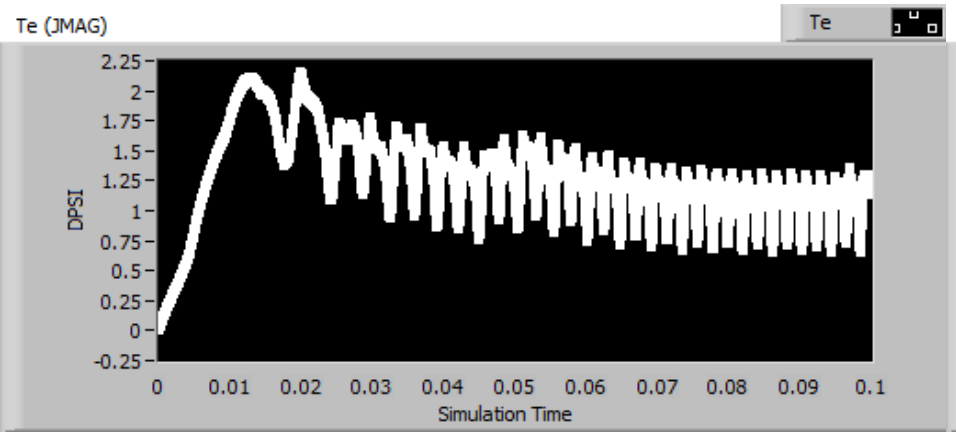
State-based parameters for PMSM models

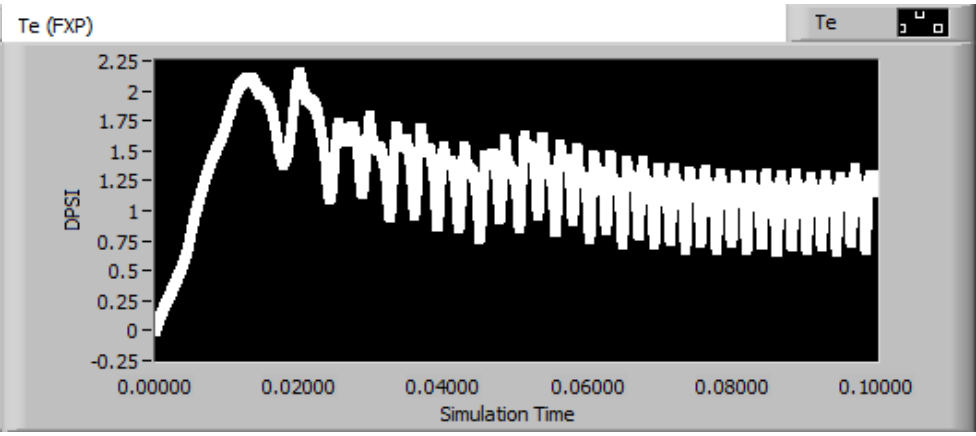
Creating High Fidelity Models

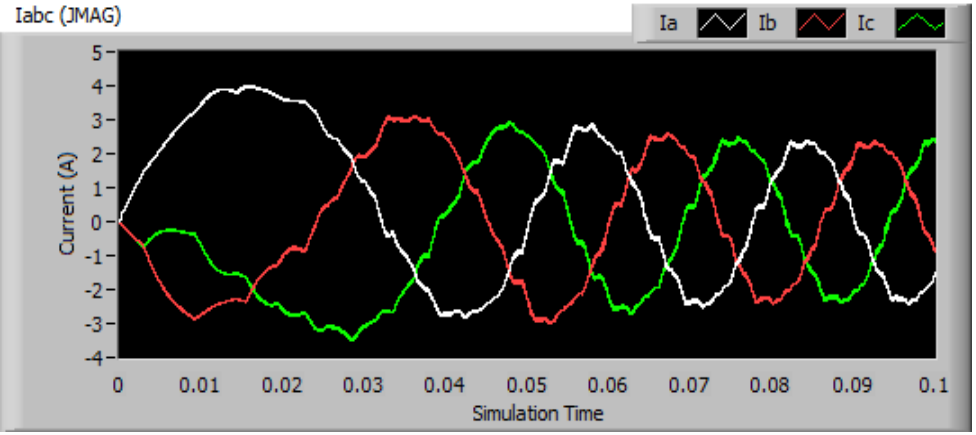


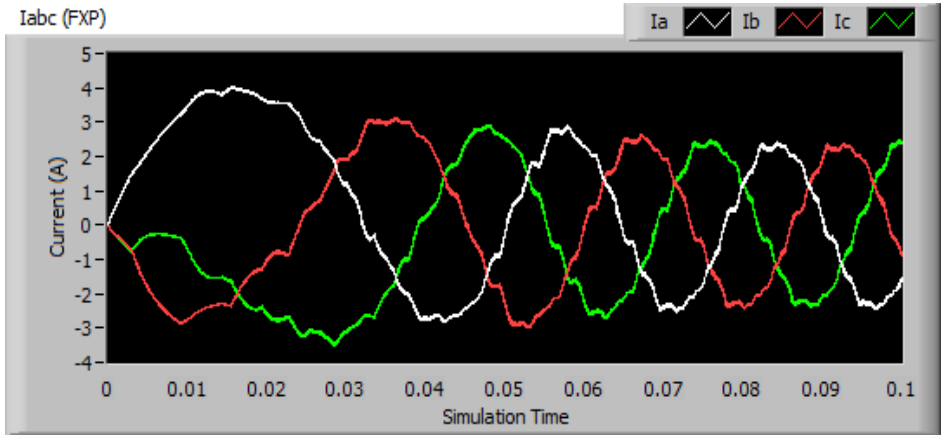
Model	Execution Target	Simulation Fidelity	Real-Time Simulation Speed
FEA with JMAG	Windows	High	Non-RT: Minutes to hours
DQ Model with Constant Parameters	Real-Time	Low	20-30 us
	NI FPGA	Medium	1-2 us
DQ Model with JMAG-RT	Windows Real-Time	Medium	20-30 us
	NI FPGA	Medium	2-3 us
JMAG Spatial Harmonic Model	Windows Real-Time	Medium	20-30 us
	NI FPGA Hardware	High	~1 us

JMAG-RT Versus FPGA

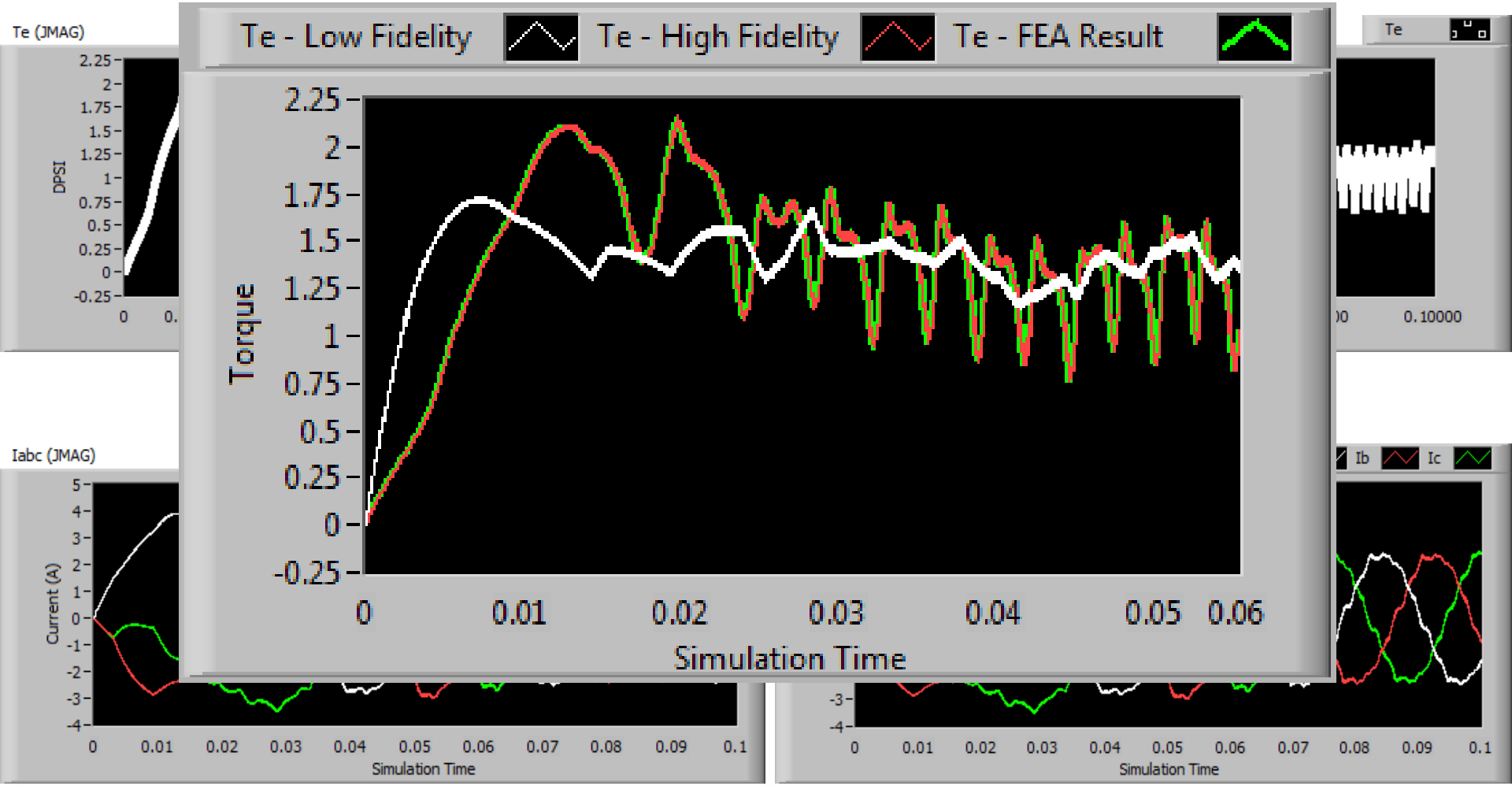


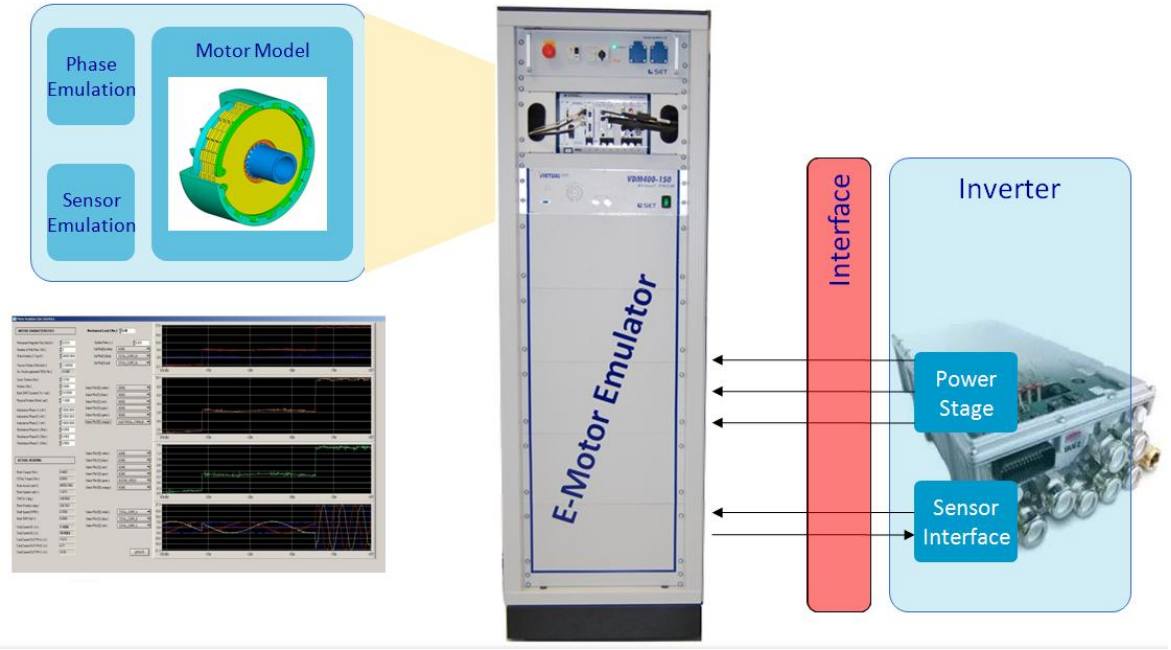






JMAG-RT Versus FPGA

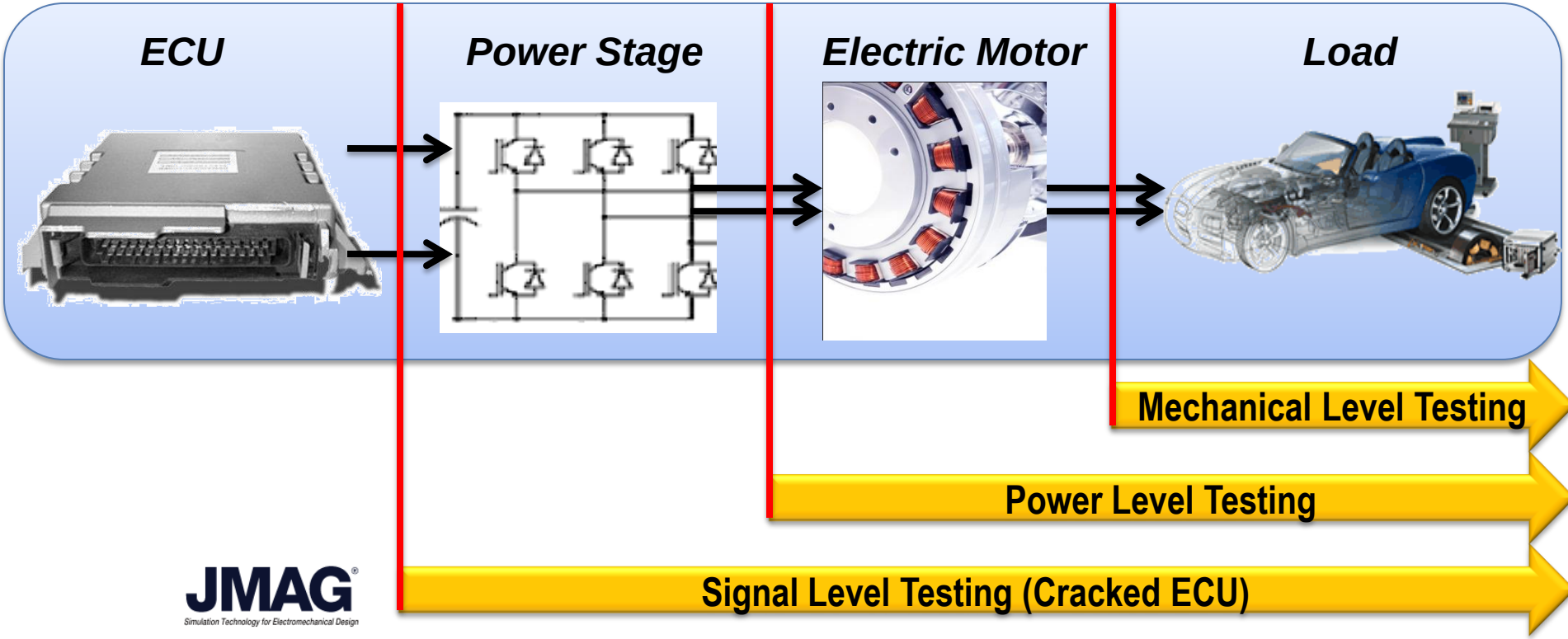




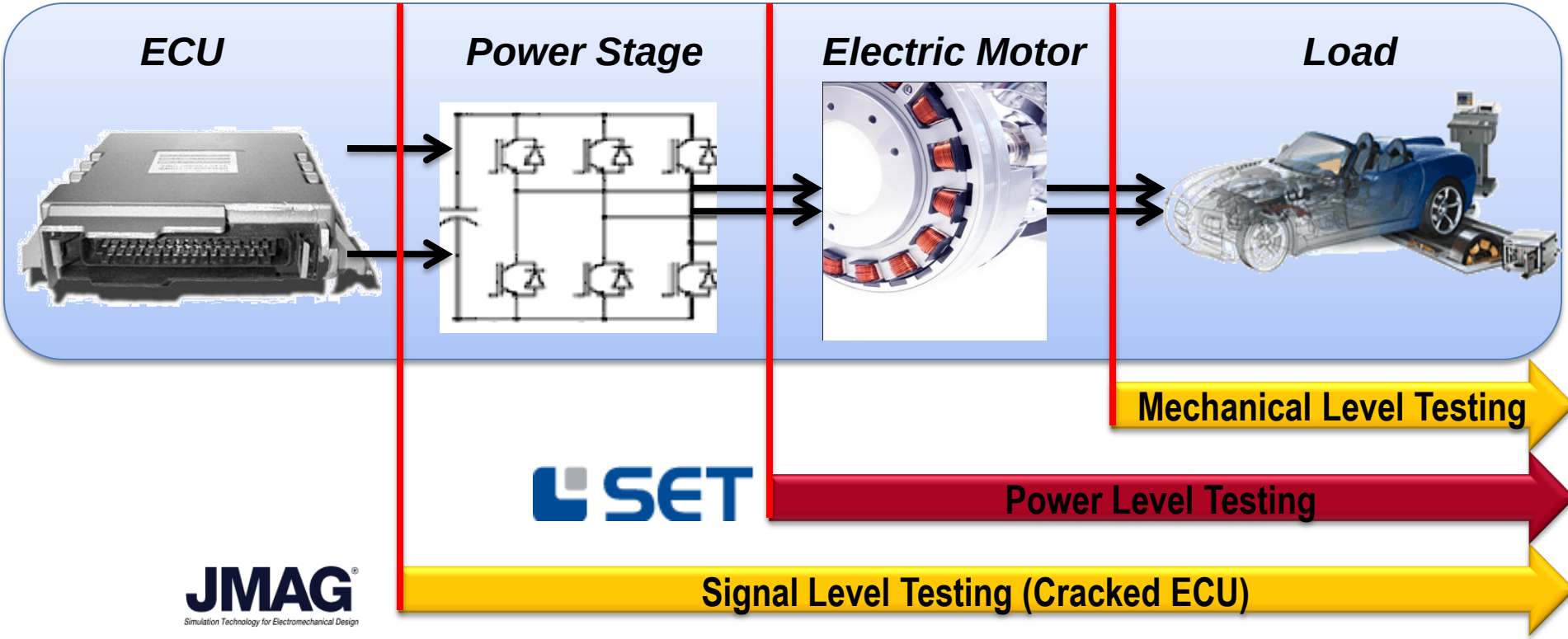
NATIONAL INSTRUMENTS

FULL POWER HIL TESTING OF INVERTERS

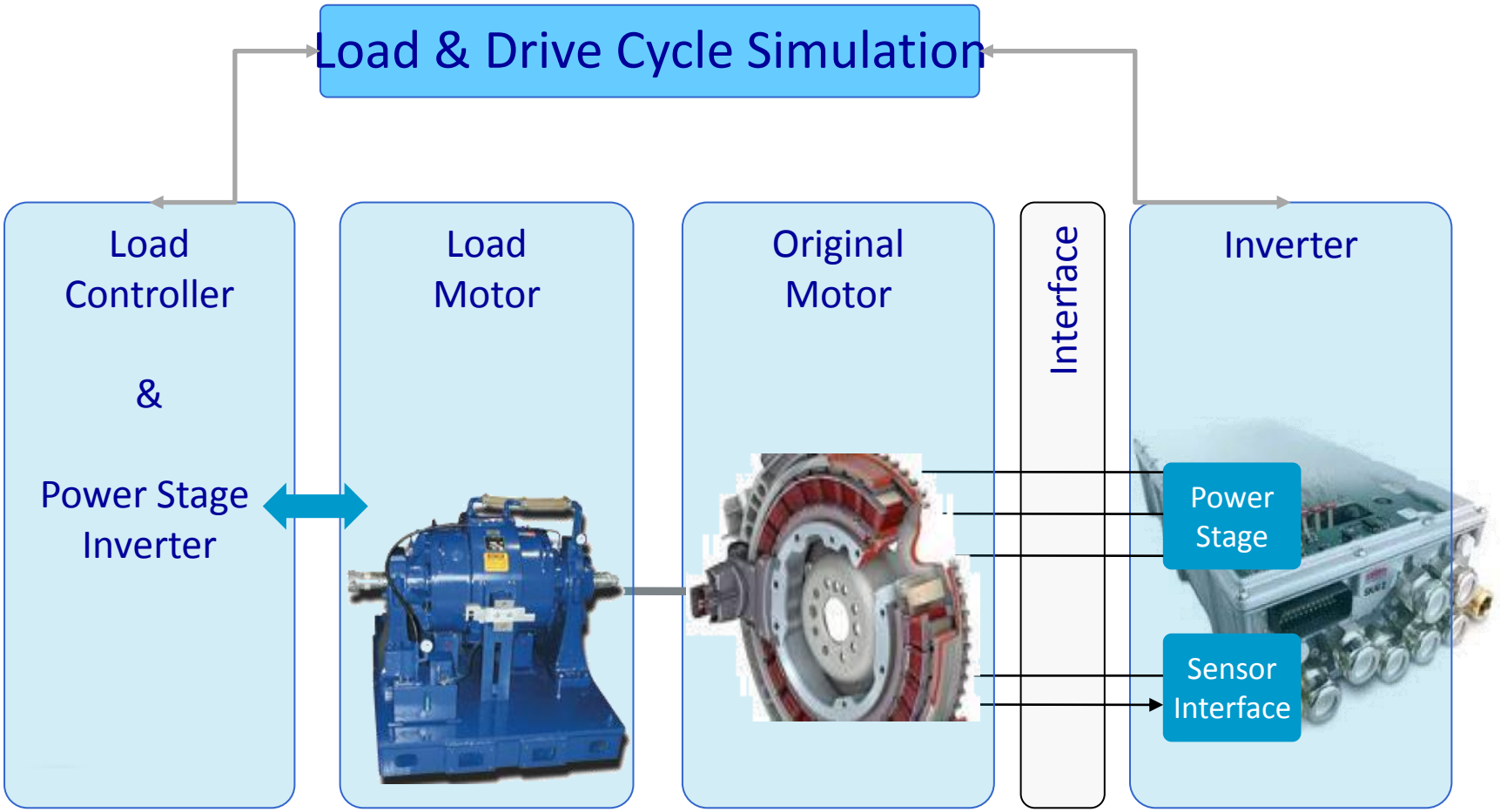
Electric Motor Emulation



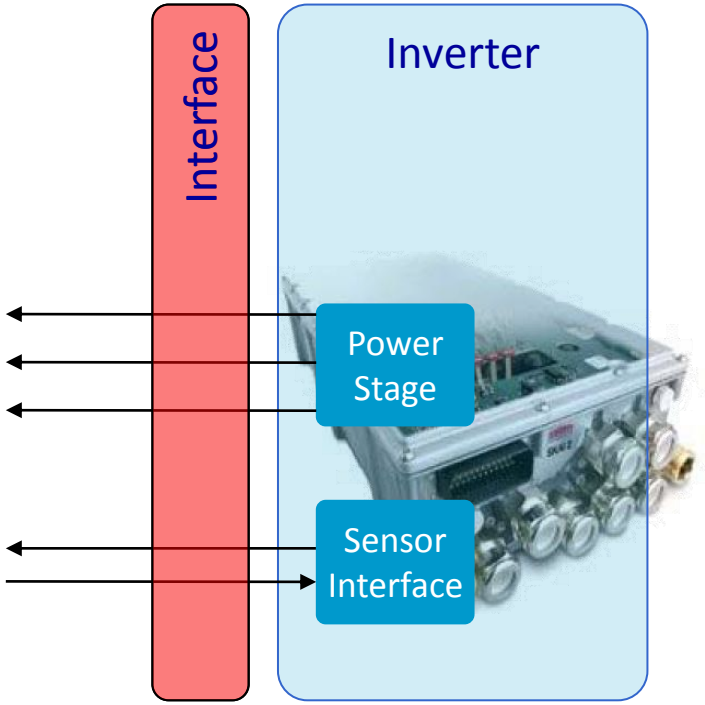
Electric Motor Emulation



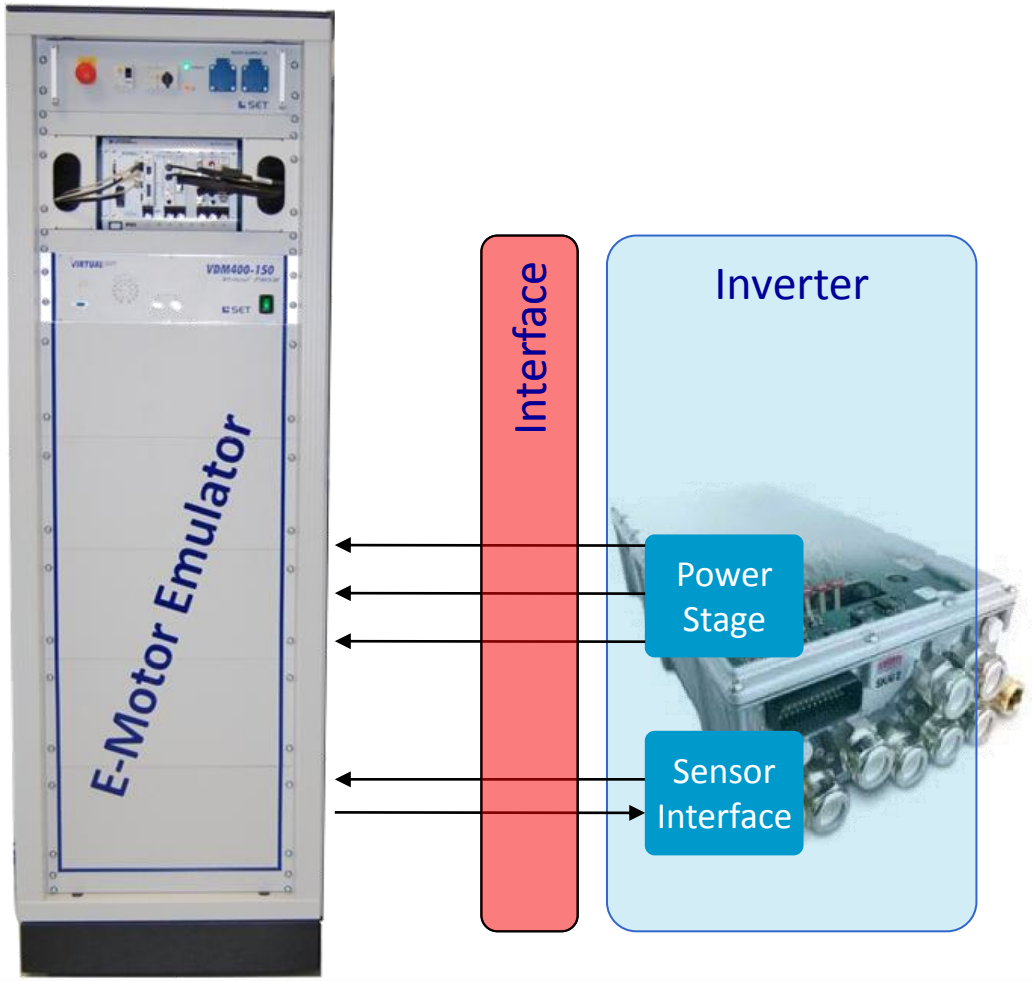
EME


Load & Drive Cycle Simulation
Load Controller
&
Power Stage Inverter
Load Motor
Original Motor
Interface
Inverter
Power Stage
Sensor Interface

EME



EME

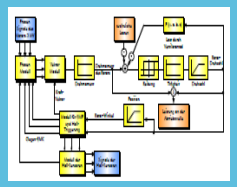

E-Motor Emulator
Interface
Inverter
Power Stage
Sensor Interface

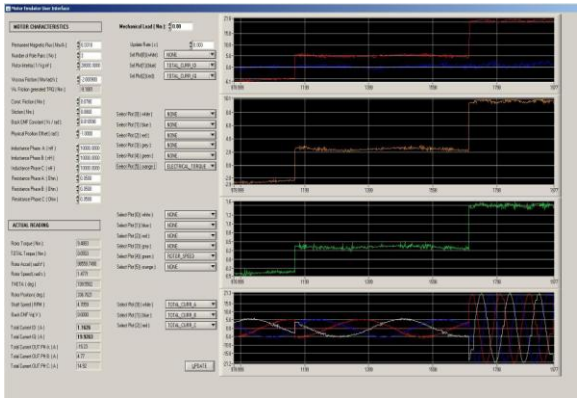
EME

Phase Emulation

Sensor Emulation

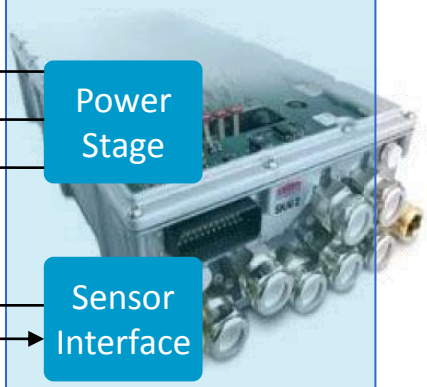
Motor Model





Interface

Inverter



Power Stage

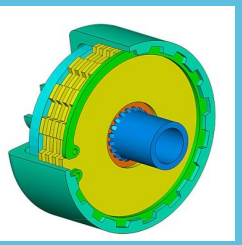
Sensor Interface

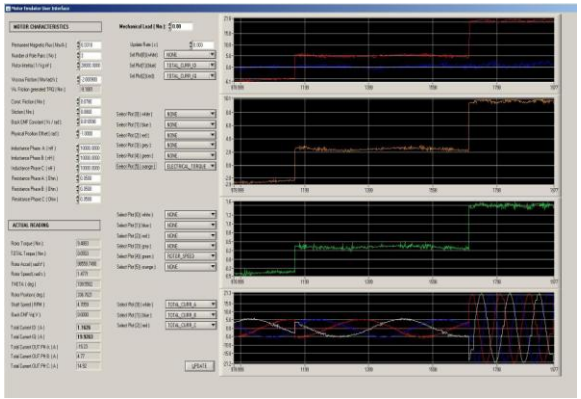
EME

Phase Emulation

Sensor Emulation

Motor Model



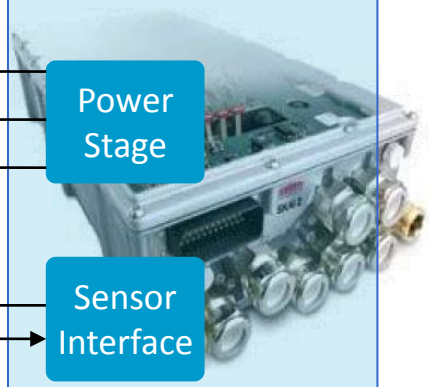


Interface

Inverter

Power Stage

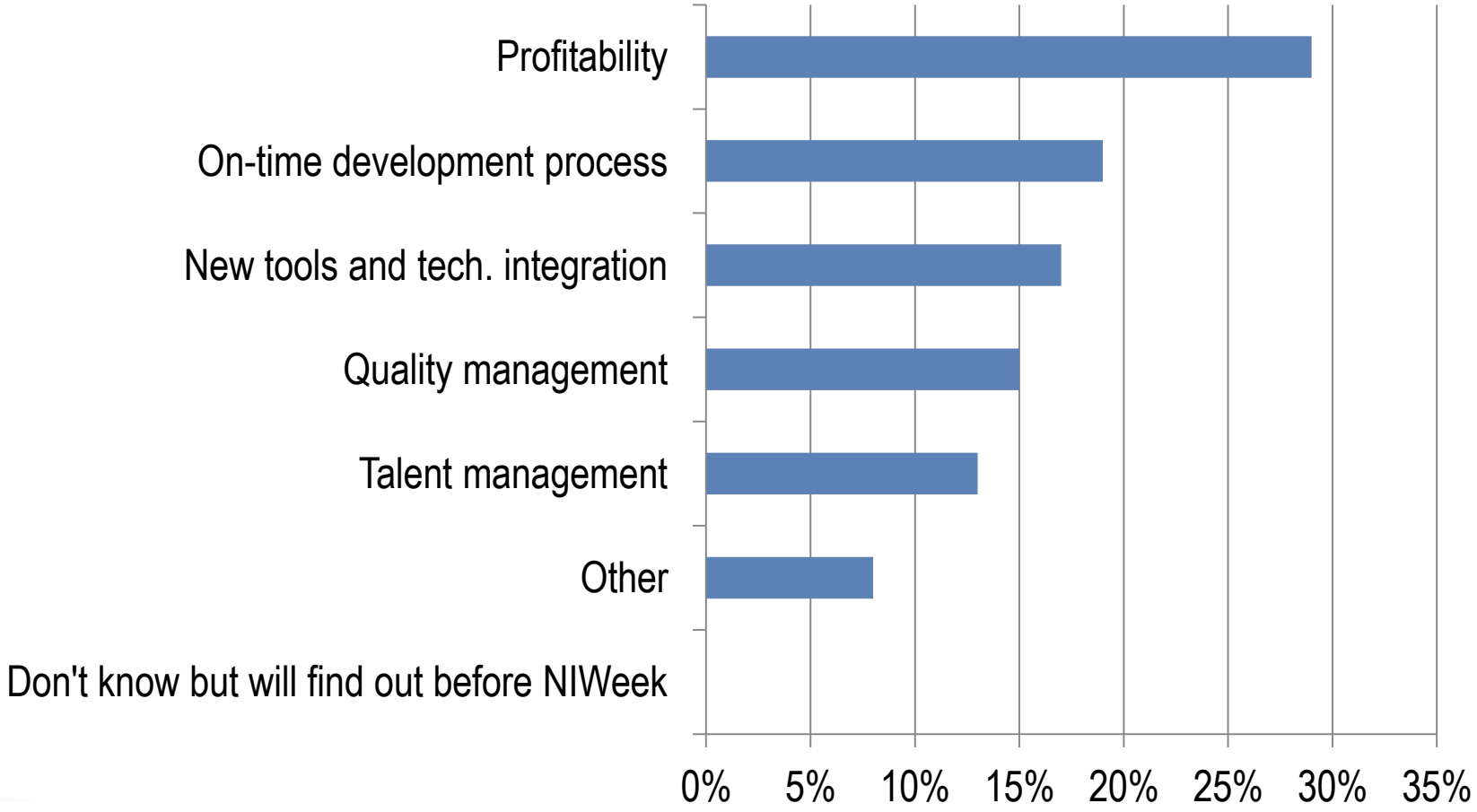
Sensor Interface



NATIONAL INSTRUMENTS

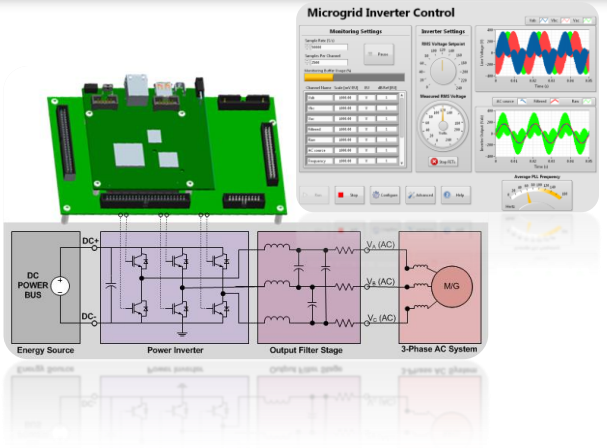
BUSINESS IMPACT

Manager's Top Business Challenges*



* From a recent survey of engineering managers and executives at 35 key NI accounts who have chosen to adopt the NI-RIO platform.

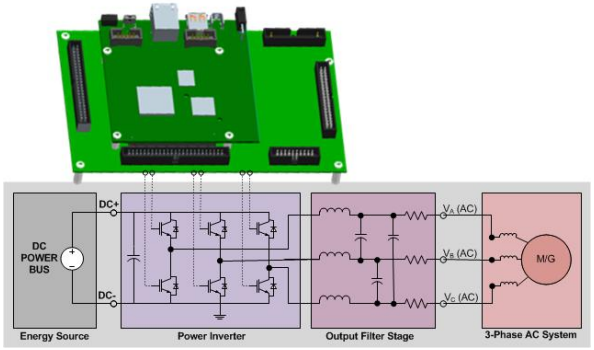
Business Impact

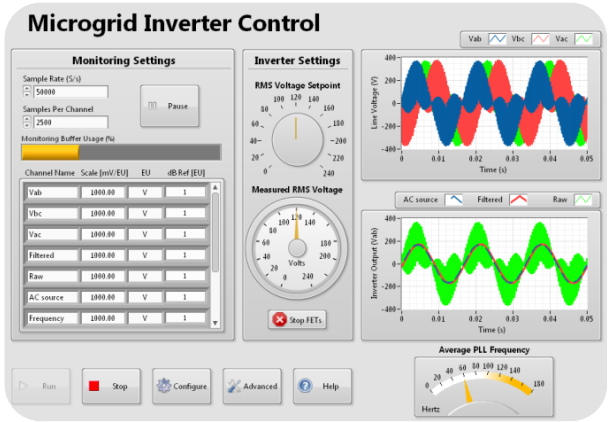


Reduce your engineering cost, risk and development time	→ Profitability
Focus on your core competency and value (not DSP board design)	→ Product differentiation
Incorporate the latest technologies while reusing software investments	→ On-time delivery
Ship fully tested, supported commercial embedded systems	→ Product quality
Empower your control experts to do embedded development	→ Development efficiency

Strengths of NI RIO inverter control platform

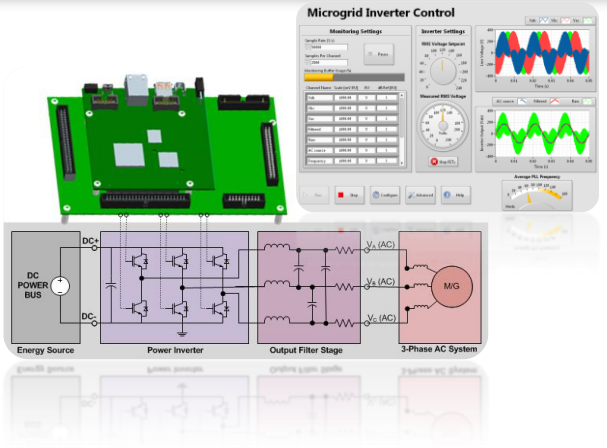
- Development tools
  - Complete, system level, high productivity, industry proven tool chain
  - Integration with 3rd party simulation tools and NI real-time power electronics HIL simulator technology
- Control quality
  - High performance control loops with true parallel processing in dedicated FPGA circuitry
  - Advanced processing, filtering of sensor I/O signals
- Measurement capabilities
  - DMA data scope capability for high speed waveform capture
  - Real-time power analysis and transient event recording
- Flexibility
  - Expandable for synchronized control of large, multilevel inverters
  - Software-defined device– install once, upgrade remotely

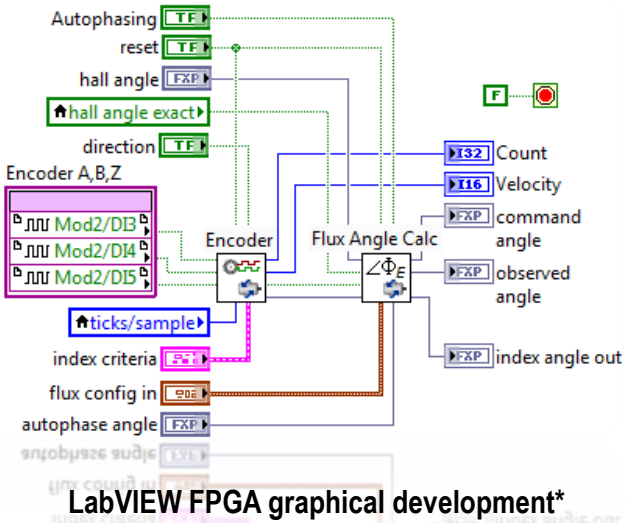




Key Features

- **LabVIEW development tool chain**
  - Deployment-ready commercial embedded system for high-volume grid-tied inverter and motor/generator drive applications
  - High level graphical system design platform enables rapid development of differentiated, high performance products
  - Complete, industry proven LabVIEW tool chain and drivers for real-time OS, reconfigurable FPGA, and inverter control I/O board
  - Available IP block libraries, reference design examples and integration with common simulation environments
- **FPGA-based control system**
  - FPGA-based system for silicon level reconfigurability, lifetime field upgradability, IP protection and true parallel execution in dedicated hardware with 25 nanosecond timing resolution
  - Xilinx Spartan-6 LX45 FPGA with 22.6 GMACs DSP performance for advanced control, custom PWM, protection interlocks, inter-board communication protocols, GPS timestamping, …



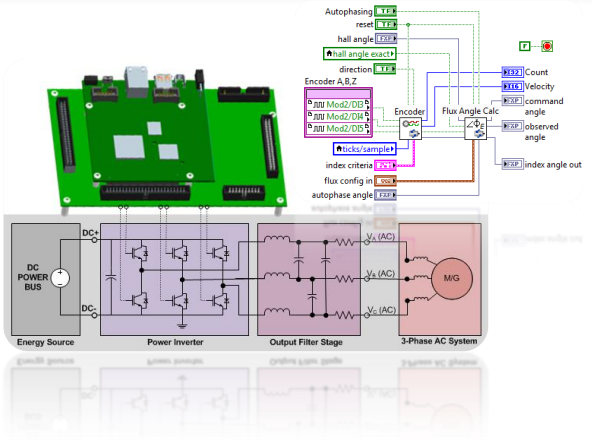


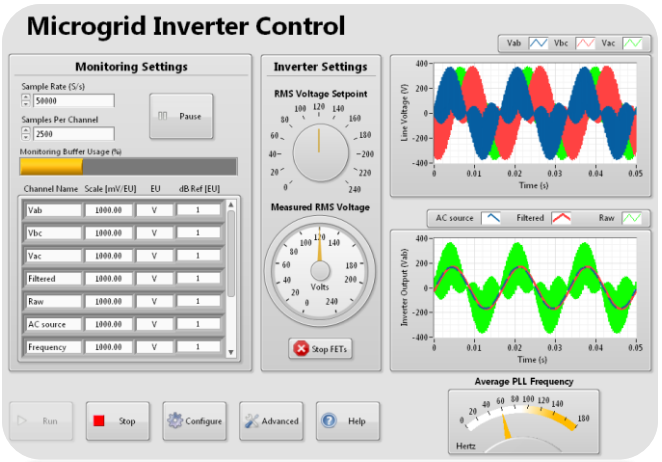
LabVIEW FPGA graphical development*

* NI Power Electronics Library included with NI SoftMotion Module 2011 f1 or higher

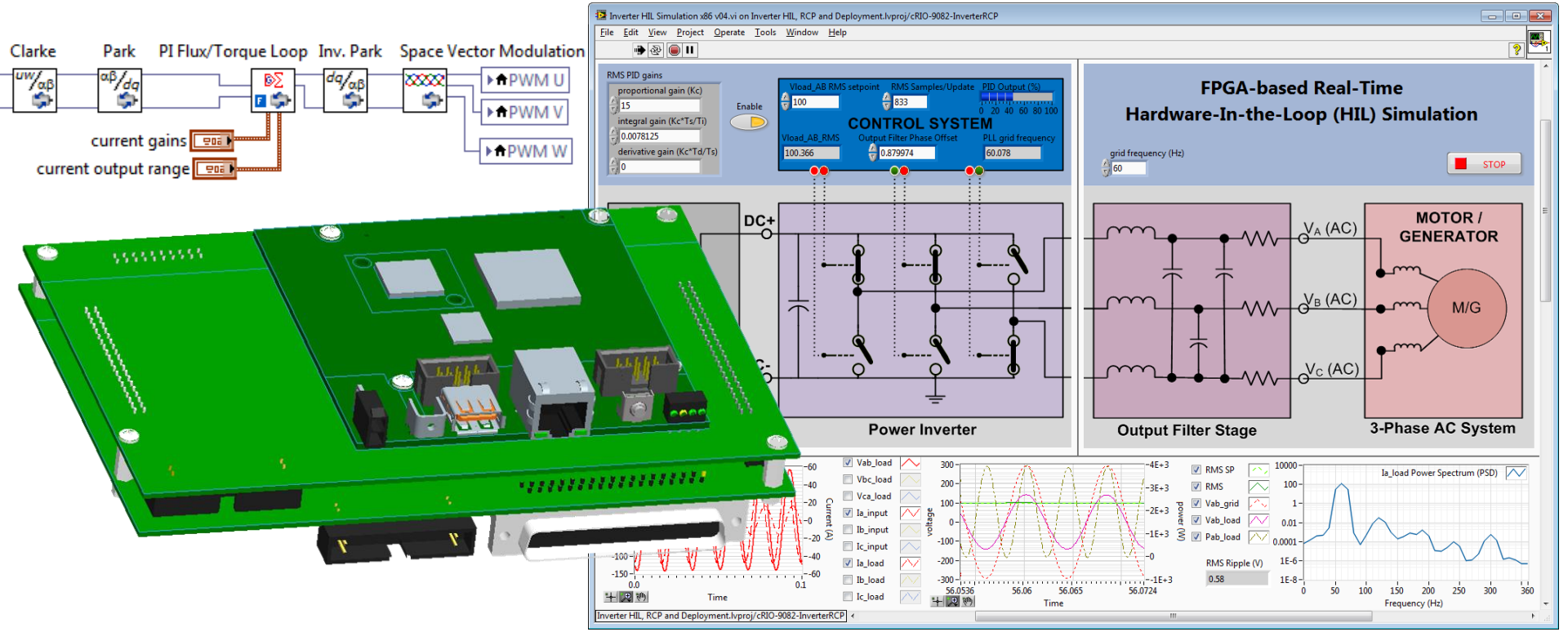
Key Features

- **Measurement and signal processing capabilities**
  - DMA data scope capabilities for high speed waveform capture and transient event recording of physical I/O and internal register signals
  - Real-time power analysis and transient event recording
  - 400 MHz PowerPC processor with VxWorks OS for hard real-time multi-threaded floating point signal processing, networking, data logging, …
- **Flexibility**
  - Expandable for synchronized control of large, multilevel inverters
  - Software-defined device– install once, upgrade remotely
  - Smart grid utility communication protocol support (DNP3, IEC 60870, IEC 61850, Modbus, …), remote client dashboards, SCADA systems and remote firmware upgrade tools
  - Options for depopulation, current AI, 16-bit calibrated AI, real-time clock battery, conformal coating, top/bottom/right-angle connectors





LabVIEW Real-Time graphical user interface



NEXT STEP

JOIN THE DEVELOPER COMMUNITY AT

NI.COM/POWERDEV