
NATIONAL
INSTRUMENTS™

Technology Exchange

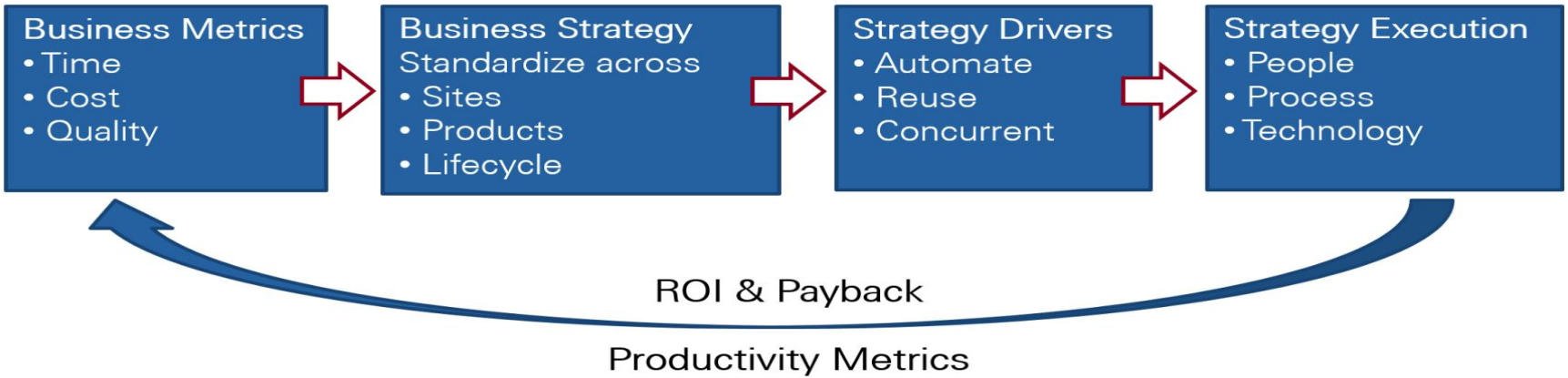
Speakers from

imec, Soliton and National Instruments

Why National Instruments?

NI has been collecting insight from test organizations for the last 30 years through our Test Leadership Forum and customer engagements to understand how a best in class test organization functions. We now use this insight with our closest customers to enable them to create a competitive advantage for their business through leveraging change in their test organization across People, Process and Technology

Test Business Impact Creation Process



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How do we do this?

National Instruments is uniquely positioned to help in optimizing test process and decrease project lead times through a combination of insight and a highly industry proven disruptive platform that can scale across the whole design cycle from R&D to Production

Approaches to Test and Measurement

CLOSED

- “Vendor knows best”
- Fixed functionality
- Closed ecosystem
- Customer pays

PLATFORM

- “Customer knows best”
- Customizable solution
- Open, vibrant ecosystem
- Customer designs

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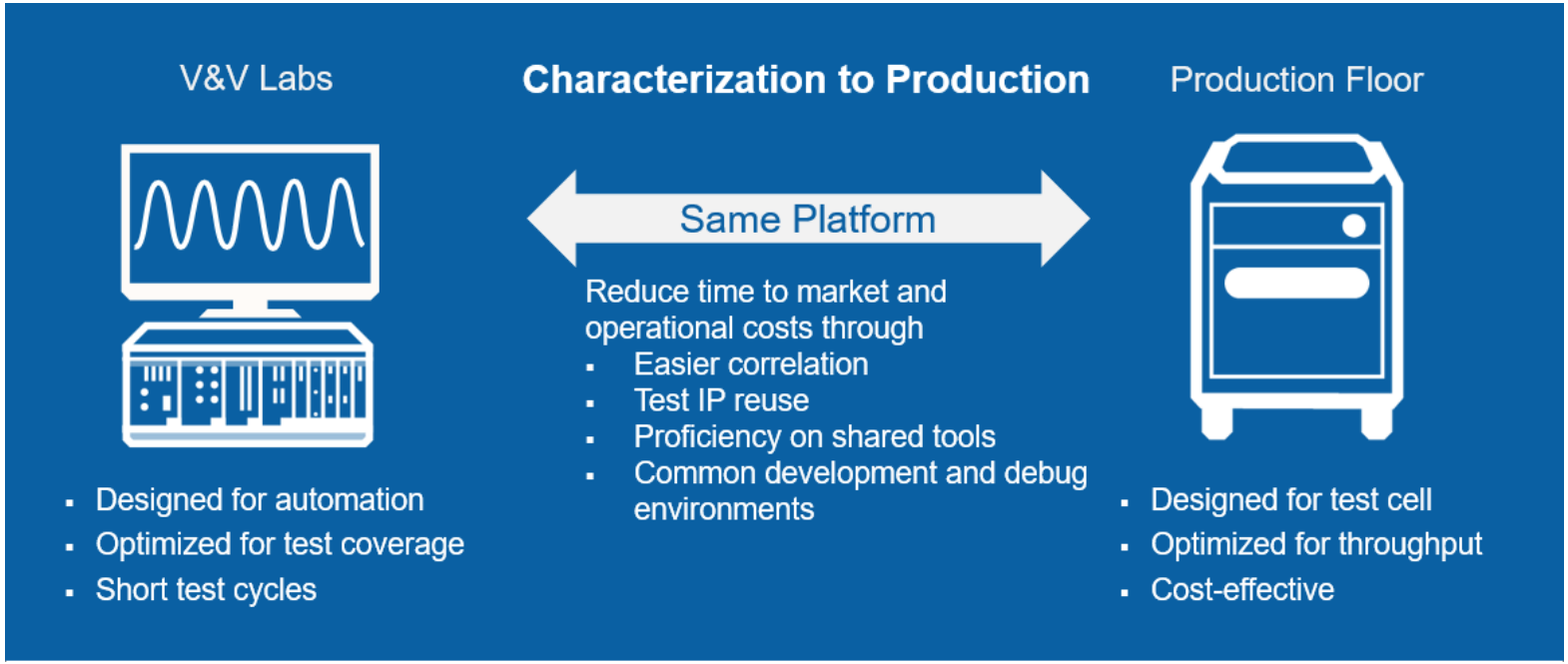
What do we provide?



A flexible COTS based modular platform to serve the needs of semiconductor customers across lab and production environments with a common software and hardware platform

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WorldClass Examples

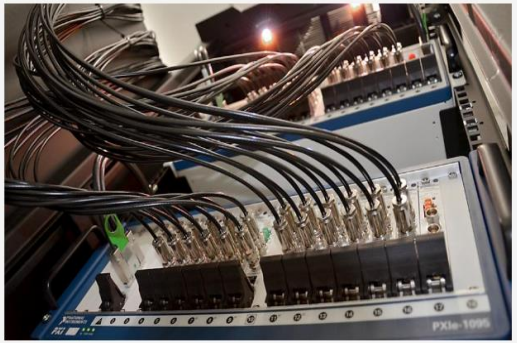
Soliton

APPLICATION OF THE YEAR

Highly Parallel Parametric Test System for In-Fab Wafer Characterization

Bart De Wachter and Kristof Croes, imec

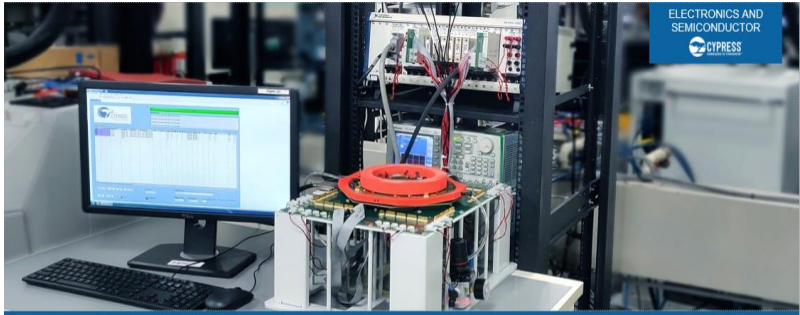
imec built a wafer-level parametric measurement system using femtoampere-class NI SMUs. Controlled and synchronized with LabVIEW, in-fab ATE has helped imec reduce project cycle time from one month to three days, decreased wafer loss from four to one, and cut the overall wafer process cost by 75 percent.



	Feature Group 1 – Custom Test Automation GUI	Feature Group 2 – Automated Report Generation & APIs	Feature Group 3 – Database Connectivity & Automation
Cumulative Investment (Hours)	2,500	200	675
Cost of Investment – Avg. Development Cost of 50 USD / Hr	USD 125,000	USD 10,000	USD 33,750
Time Saving per instance of usage (Hours)	6	2	1
Cumulative Savings for 2500 instances of usage across multiple projects, users, teams in a 4-year window	15,000 Hours or 7.5 Man Years	5,000 Hours or 2.5 Man Years	2,500 Hours or 1.25 Man Years
Cumulative Cost Savings – Avg. Cost Saving to customer calculated at 75 USD / Hour	USD 1,125,000	USD 375,000	USD 187,500
ROI	800 %	365 %	455 %

ADI Uses NI PXI and STS to Lower Operational Costs

- Lower Cost and Smaller Footprint
- Flexibility and Range of Configurations
- Improved Correlation from R&D to Production Test



"The 4X parallelism has decreased characterization times, which has allowed us to identify and fix bugs more rapidly. The newer characterization setup has directly reduced our characterization time by over 60 percent."

—Vinodh J Rakesh, Cypress Semiconductor Technology India Pvt. Ltd.

Who are we?

- Alex Floor: Account Manager for imec
- Joris Donders: EMEIA Semiconductor Go-to-Market Lead
- Jake Harnack: Senior Product Manager, Platform & Precision I/O
- George Tsalavoutis: Senior Applications Engineer, Automated Test
- Tarek Safwan: Senior Field Marketing Engineer, Semiconductor Test
- Christian Hartshorne: Regional Sales Manager
- Ganesh Devaraj: CEO & Founder Soliton Technologies
- Bart Dewachter: Researcher imec-REMO
- Lorenzo Ricotti: Software engineer imec-AMSIMEC

Who are you?

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Agenda

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08:30	Welcome and Introductions		
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16:30	**Finish**		

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FULL FORCE AHEAD

NIDays Europe | Munich, Germany

November 20-21 2019

Join us at NIDays Europe 2019, the industry leading conference for automated test and automated measurement professionals. Take advantage of learning from industry trailblazers, network with like-minded peers, and increase your proficiency to develop cutting-edge applications.

NIDays Europe offers

- 100+ technical sessions over two days
- 100+ demos from 50+ exhibitors on the exposition floor
- Networking with industry peers
- Access to NI leadership, sales, and R&D
- Inspiring keynote speakers

Register Now

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Overview of NI's Strategy and Commitment for Semiconductor Test

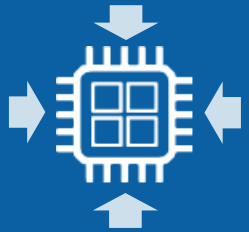
Smarter Test From Characterization to Production

Joris Donders

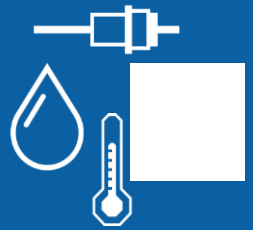
EMEIA Semiconductor Go-to-Market Lead

National Instruments

Realities of the Semiconductor Industry



Smaller Footprint & Higher Complexity

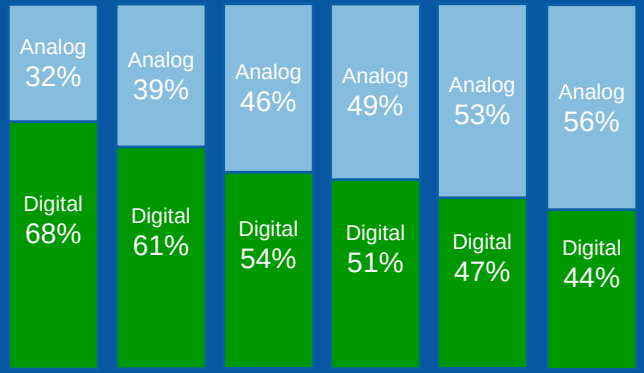


Innovations in Wireless & Sensing

Faster Design Cycles

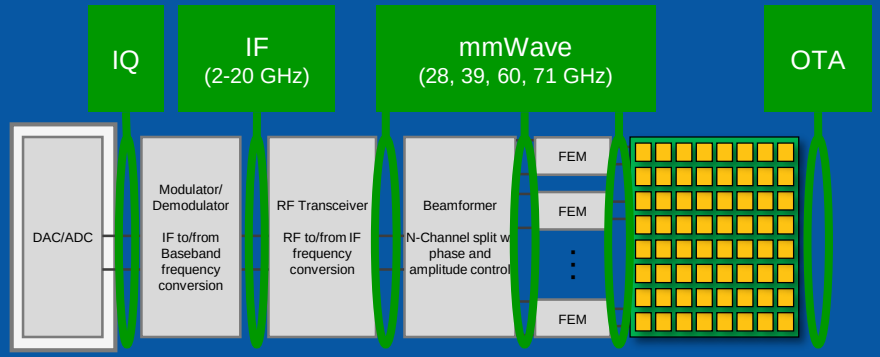
Higher Analog Content & New Test Methodologies

Analog vs Digital IC Volumes

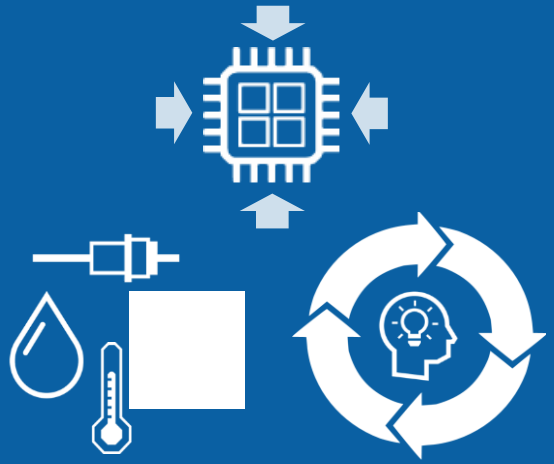


Source: IC Insights

5G Requires New Measurement Methodologies



Semiconductor Realities Driving Test & Measurement



Integration, Innovation,
& Faster Design Cycles

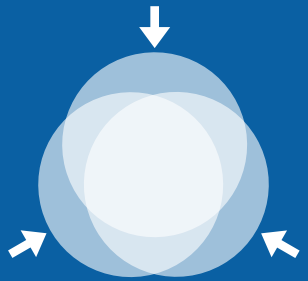
Higher Integrated
Analog Content

Requires New Test
Methodologies

Demand for
Increased Reliability

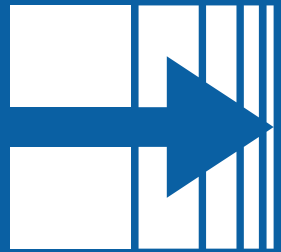
Semiconductor Challenges Driving Common Test Needs

CONVERGENCE



LOWER PRICE

RAPID CHANGE



- More functionality
- Ensure high reliability
- Lowest cost
- Fast time to market

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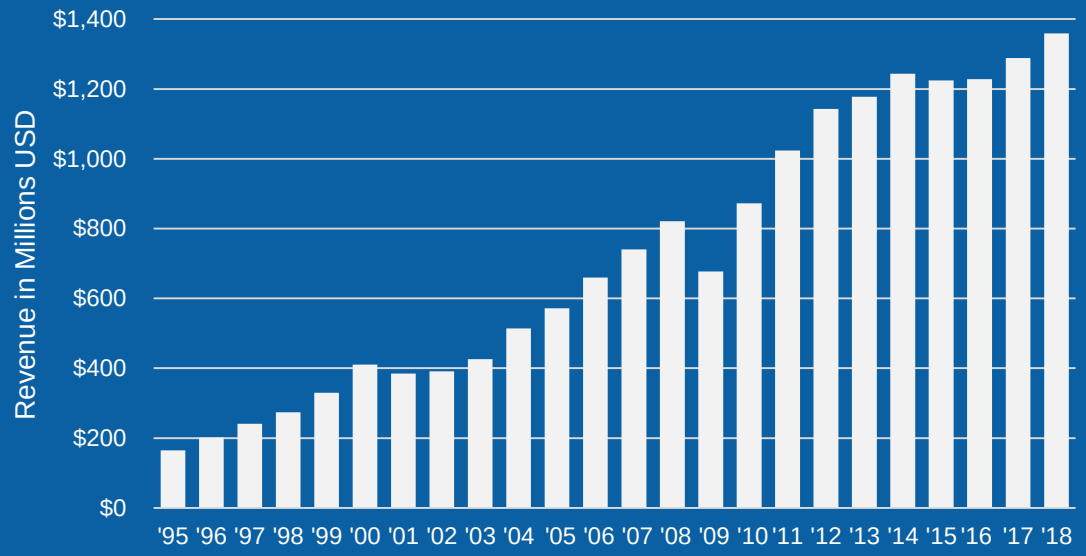
OPERATIONS IN
50+ COUNTRIES

$1.36
BILLION
IN 2018

35,000+
CUSTOMERS WORLDWIDE

18%
INVESTMENT IN R&D

Long-Term Track Record of Growth



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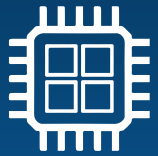

SEMICONDUCTOR

TRANSPORTATION

AEROSPACE/DEFENSE/
GOVERNMENT

PORTFOLIO

NI PLATFORM

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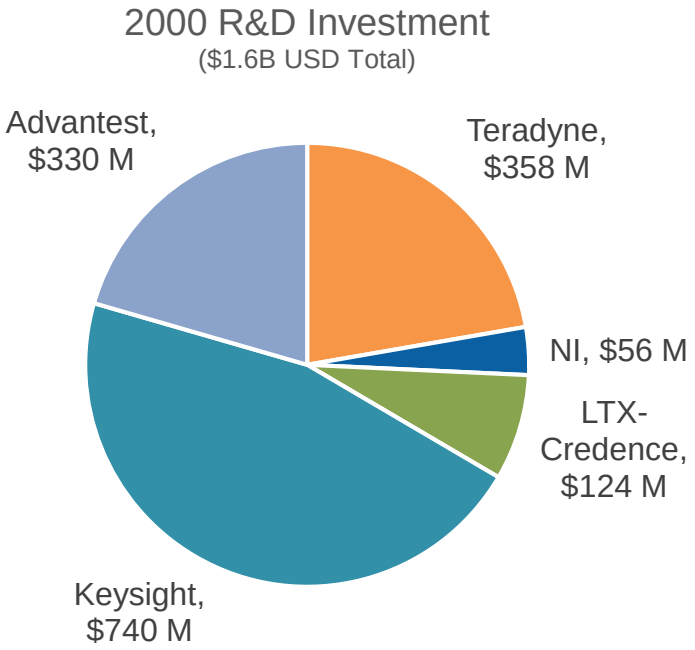
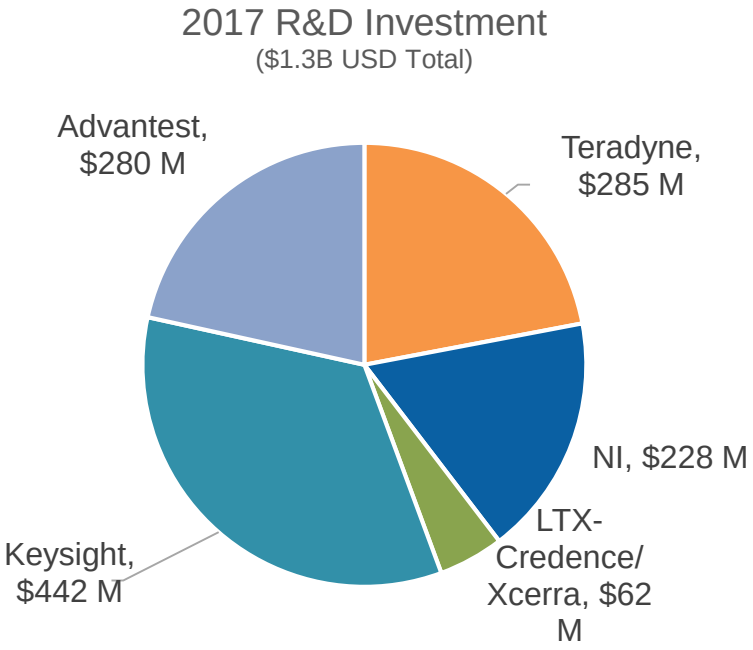
Consistent Investment in Innovation





*Keysight data does not include Ixia (acquisition from 2017)
Source: Publicly Available IR Content

Accelerate Time to Market with Reuse Across Lab and Production Environments

Characterization & Validation

Benefits of a Common Platform
Eases Correlation Efforts, Facilitates IP Reuse, and Improves Proficiency on Common Tools for Development and Debugging

Production Test

Platform Scalability

PXI

ATE Core Configurations

STS T1

STS T2

STS T4

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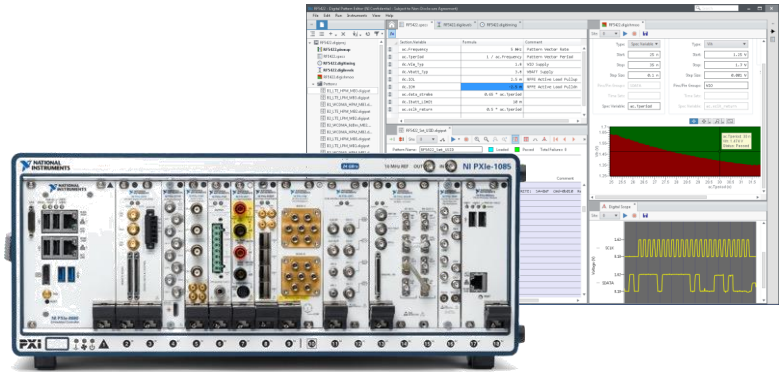
Leadership in Standardized Lab V&V

Core Needs: Test coverage, test speed, and time to market

Approach: Automate for speed & coverage, standardize for reuse

Why Choose NI? Faster development and optimization of test sequences with the most productive, integrated hardware and software toolchain

- Over 500 high-accuracy PXI Modules from DC to mmWave
- 300K+ members in NI's software community utilizing support and training
- Highly extensible to 3rd party hardware and programming languages



500+ Each Year

NI PXI SYSTEMS SOLD TO SEMICONDUCTOR CHARACTERIZATION

intel	Intel Mobile Communications division speeds measurements by 5X with LabVIEW and PXI
ST ERICSSON	ST-Ericsson Reduces Semiconductor Test Time by 10X With LabVIEW and NI PXI RF
qorvo	Qorvo Reduces Characterization Time of RF Power Amplifiers by 10X with PXI & LabVIEW
ANALOG DEVICES	Analog Devices Reduces MEMS Test Costs by 11X with PXI and LabVIEW
CIRRUS LOGIC	Improving Validation With a LabVIEW-Based Interactive Framework
Texas Instruments	TI's Standardized Infrastructure Built On NI TestStand, LabVIEW, and PXI
ON Semiconductor	NI PXI for Semiconductor Validation Achieves Performance Improvements, 3X Cost Savings
Melexis	Worldwide Standardization of Semiconductor Characterization Test at Melexis
amu	Automated Characterization of Analog-to-Digital Converters Using PXI and LabVIEW
MICROCHIP	Designing Highly Scalable Semiconductor Validation Systems With PXI and LabVIEW

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5,000 PXI **600+** STS

SOLD TO
SEMICONDUCTOR PRODUCTION TEST

BROADCOM
ANALOG DEVICES
NXP
CIRRUS LOGIC
TDK InvenSense
ON Semiconductor
IDT A Renesas Company
Qualcomm

And more

Smarter Alternative for Production Test

Core Needs

- Accelerated throughput
- Shortened time to market
- Reduced test cost

Approach

Deliver savings through faster test times and lower cost

Why NI? Faster development and optimization of test sequences with the most productive, integrated hardware and software toolchain

- High-performance instrumentation options ranging from DC to mmWave
- Prebuilt test code for common semiconductor test operations
- Unified software for developing, debugging, and deploying test programs
- Potential for IP reuse, reduced correlation efforts, and improved proficiency

NI Semiconductor Test System (STS)

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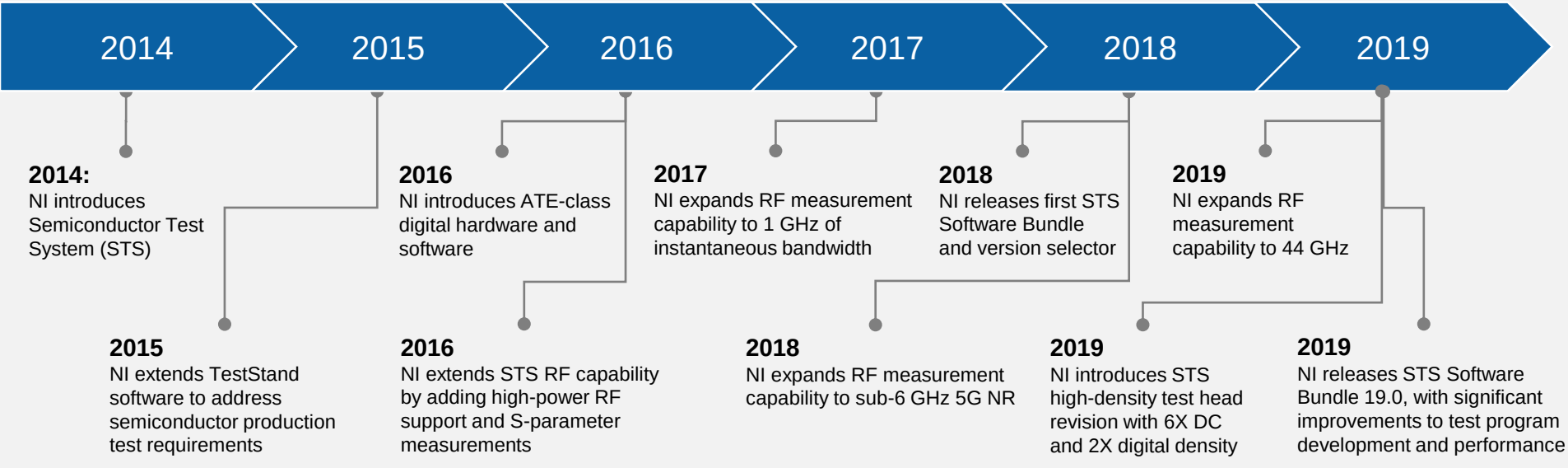
Evolution of NI's Semiconductor Production Test Offering

200,000+
PXI Systems Shipped Globally

15,000+
PXI Systems in Semiconductor R&D Labs

5,000+
PXI Systems in Semiconductor Production

600+
Deployed STS Systems



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NI as a Global System Supplier

200,000	PXI chassis shipped since 1997
50,000	PXI systems deployed globally into high-volume manufacturing
15,000	PXI systems deployed in semiconductor labs (design, V&V, and char.)
5,000	PXI systems deployed in semiconductor production
600	STS semiconductor production systems deployed since 2014

Diverse Applications

MEMS Devices	RF Front Ends	Mixed-Signal ICs
Optoelectronics	Package and Wafer Test	

Comprehensive Services & Support

Onsite Apps Support	Parts Replacement	Calibration Solutions
Development Services	DUT Migration	Training

Why Are Customers Adopting STS?

LOWER TOTAL COST OF TEST

SIZES DOWN BASED ON NEEDS

REUSE BETWEEN CHARACTERIZATION AND PRODUCTION

Analog Devices Honors NI with Two Global Supplier Awards

2018 Overall Supplier of the Year

2018 Top Performer for Equipment and Services

Links: NI Press Release | ADI Press Release


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Soliton Technologies

Importance of a Post-Silicon Validation Automation Framework

Sept 19 2019, IMEC Tower, Leuven

About Us

Dr. Ganesh Devaraj

Founder & CEO

Education

- Bachelors in Electronics and Communications Engineering, PSG College of Technology, Coimbatore, India - 1989
- Masters in Electrical Engineering (Solid State and Optics), University of Michigan, Ann Arbor, USA - 1991
- Ph.D. in Theoretical Particle Physics, University of Michigan, Ann Arbor, USA (student of 1999 Noble Laureate Prof. Veltman) - 1996

Experience

- Project Scientist – V I Engineering, Michigan, USA
  - Test & Measurement Automation Solutions in LabVIEW (1997)
- CEO – Soliton Technologies, Coimbatore & Bangalore
  - Technology and Management (since 1998)

About Us

Soliton

Founded in 1998

200+ employees

Offices in US & India

Semiconductor focus since 2006

Working with many of the leading Semiconductor companies

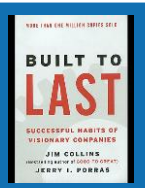
Our Core Values

- Innovation
- Integrity
- Excellence

ISO 9001 : 2008 Certified

A Soliton is a special wave that travels forever without dispersion

Our name represents our goal of building a Build to Last Company



Key Customers

Team Strength & Recognition

NATIONAL INSTRUMENTS LabVIEW™ Certified Architect

Largest semiconductor focused LabVIEW team

among NI Partners (80 Engineers)

Technology	# of Engineers
LabVIEW & TestStand	80
Web Technologies	33
Embedded (FPGA, MCU)	17
Python	15
Machine Learning & Data Science	5

NATIONAL INSTRUMENTS Alliance Partner — STS/Semiconductor Specialty

NATIONAL INSTRUMENTS Alliance Partner — SystemLink™ Specialty

National Instruments Alliance Partner for **20+ years**

First NI Alliance Member in India

FROST & SULLIVAN

2016 Frost & Sullivan Post-Silicon Validation Solutions -

Customer Value Leadership Award Winner

Soliton has won **24 awards** from National Instruments so far

Record **3-time Overall Winner** of the NIWeek Best Application Contest

Outstanding Technical Resources Award (Alliance) – 2014. 2015, 2016, 2017, 2018

Texas Instruments Supplier Excellence Award 2014

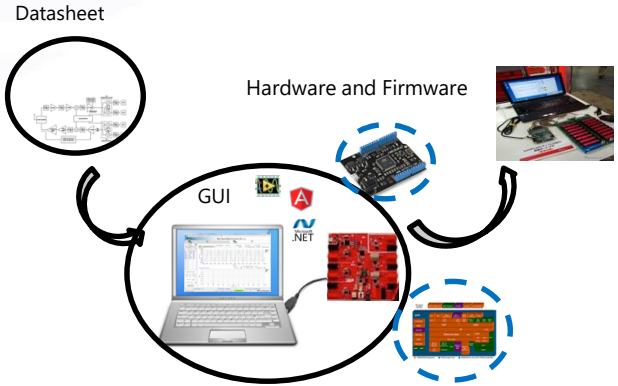
Services Across Industries

	Semiconductor	Medical Equipment	Electronics	Manufacturing	Industrial
Test & Measurement Automation	Soliton's strong point & differentiation in the customer's eyes. Engineers trained to service customer needs using a multitude of software technologies of the customers' choice – LabVIEW, Python, C# .NET, VB, Web Technologies, etc.				
Web Technologies	Engineers with experience developing aesthetic solutions using new age technology on the web. Technologies include HTML, CSS, JavaScript along with Angular Framework & Node JS Environment. The expertise is used to primarily deliver customer eval GUIs & development frameworks / tools.				
Embedded System & FPGA Design	Engineers with experience in providing system-level solutions using FPGA , ARM, Microcontrollers technologies. Our experience extends to high speed data capture applications using JESD204b/c interfaces & Xilinx / Altera / Lattice platforms.				
Machine Learning & Data Analytics	5 member ML team, experienced in working with Machine Learning and Deep Learning projects. Soliton is a certified solution partner on the Rapid Miner Data Science Software Platform				
OEM Hardware Development	Soliton is India's first manufacturer of an indigenous Smart Camera. Bundled along with a powerful vision library, the camera is used to address OEM applications like print registration, food sorting & end-of-line inspection.				

Soliton Services for Semiconductor Customers

Design Validation
Software and Tools

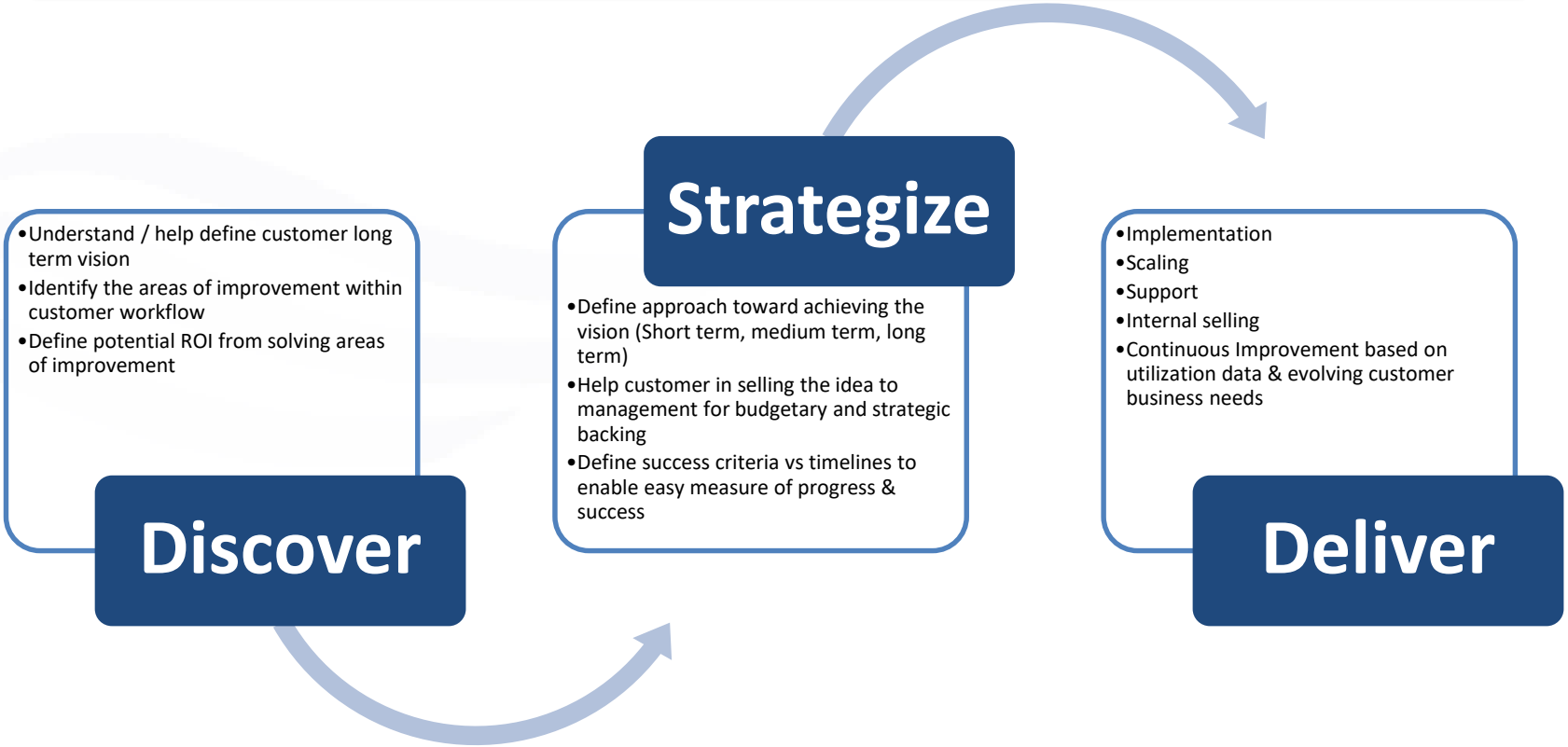
Design Evaluation
Firmware and GUI



Production Test Automation
NI STS

Enterprise Software

How Does Soliton Engage with Semiconductor Customers?



Common Customer Challenges

Chip Complexity

Test coverage requirement

Global Development teams

Product Development Timelines

Engineering Bandwidth

All customers have responded with an increased focused on automation across Silicon Validation Lifecycle

What ails the Automation?

Soliton

Over 30% Loss in Efficiency in Post Silicon Design Validation

Fragmented Software Development	• Minimal Software reuse
Lack of hardware standardization	• Multiple Code for Same Purpose
No Effective expertise transfer mechanism	• Debugging software instead of the device
Lack of Effective Data Infrastructure	• Manual Data Preparation • Manual Data Analysis & Reporting
Minimal integration across workflows	• Manual Requirements Tracking

Developing Software vs Architecting Software

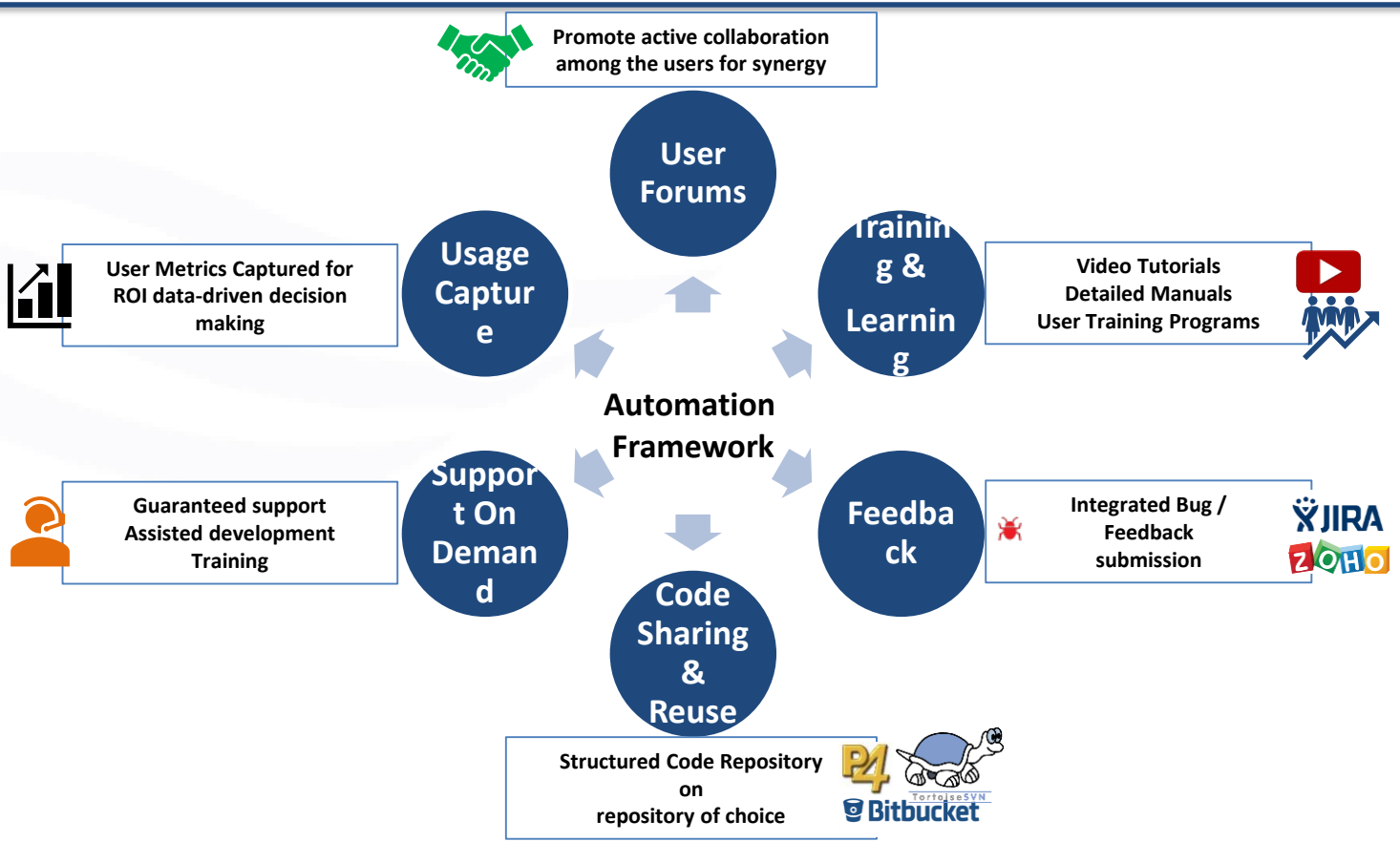
Minimize the time spent by Electrical Engineers architecting automation software

Maximize the time spent by a Product Eval Engineer on Characterizing / Debugging the DUT

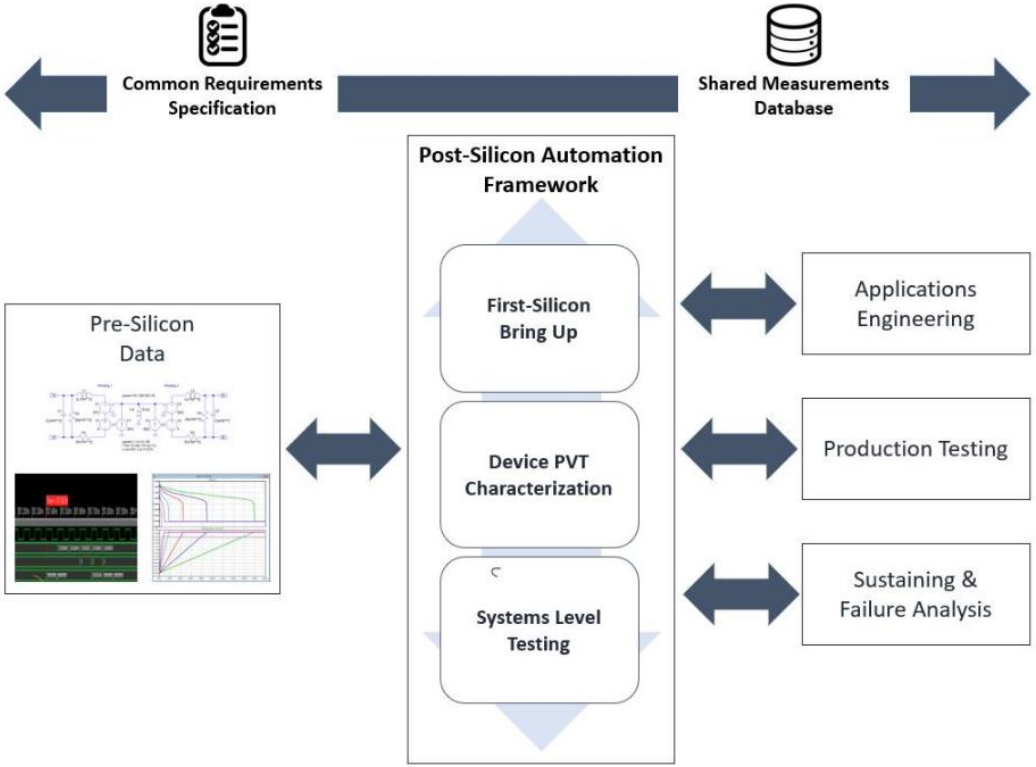
MEASUREMENT AUTOMATION
Device / IP Specific Measurement, Custom Instrumentation, etc.
Developed by Device / Measurement Experts (Product Engineer)

ALL NON-MEASUREMENT RELATED SOFTWARE	WORKFLOW AUTOMATION
Instrument Drivers, Register Map & DUT communication, Macros / Scripts, Sequencers, Data logging, etc.	Systems Testing (PSS / EMC) , Requirements Linkage, Sharing & reuse, Training, Report Generation etc.
Developed by Software Experts (Central Framework team)	

Sustaining The User Base

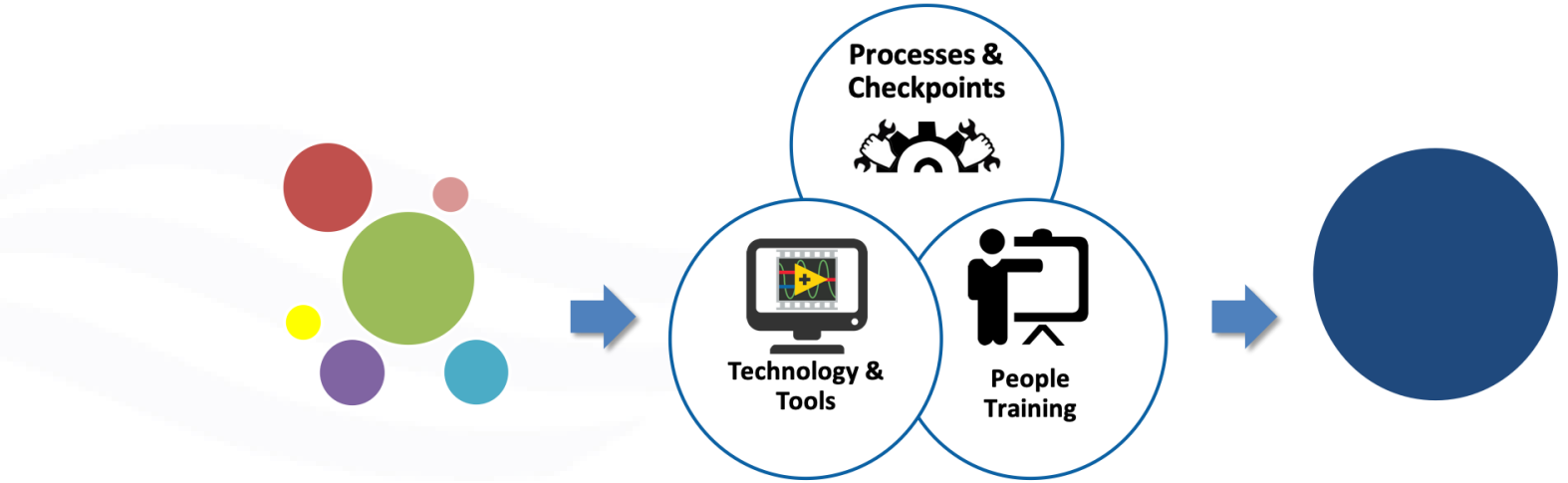


Integration Across Workflows



- Helps enhance the debug experience across the workflows
- Improved Data Correlation
- Improved Efficiency through breaking silos, allowing collaboration across global sites

Soliton Case Study
Establishing a Standardized Automation Framework



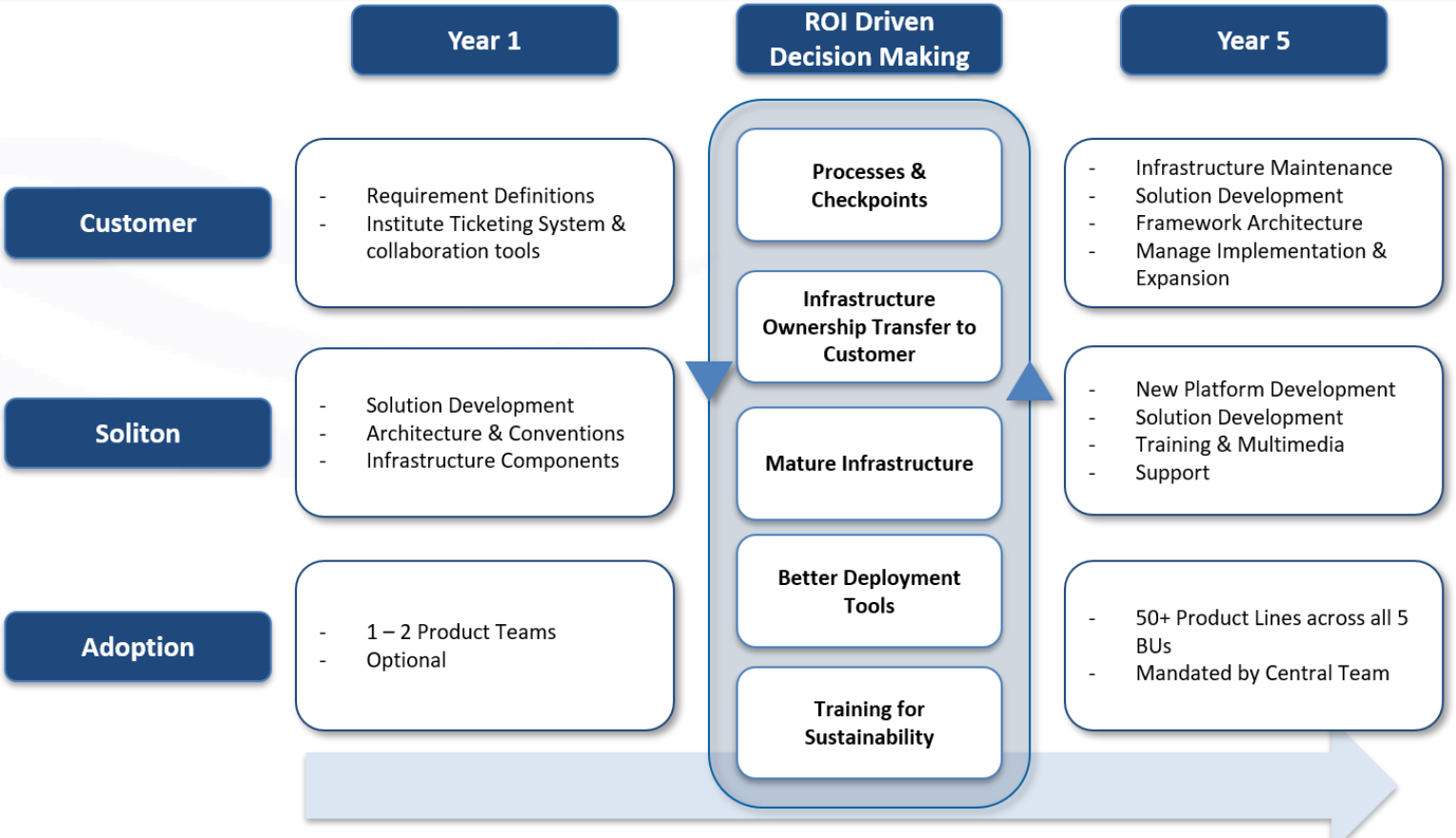
Minimum / No Automation or Fragmentation

Soliton Expert Services across the Customer Organization

Fully Automated on a Standardized Framework

Soliton provided a Fortune 500 Semiconductor company with a comprehensive set of services to develop, deploy, and sustain standardized platform(s) that helped eval engineers across product lines and geographies move away from a fragmented automation development approach in their labs to a standardized, centrally supported infrastructure over a 5 year period

Soliton Case Study
How we got there?



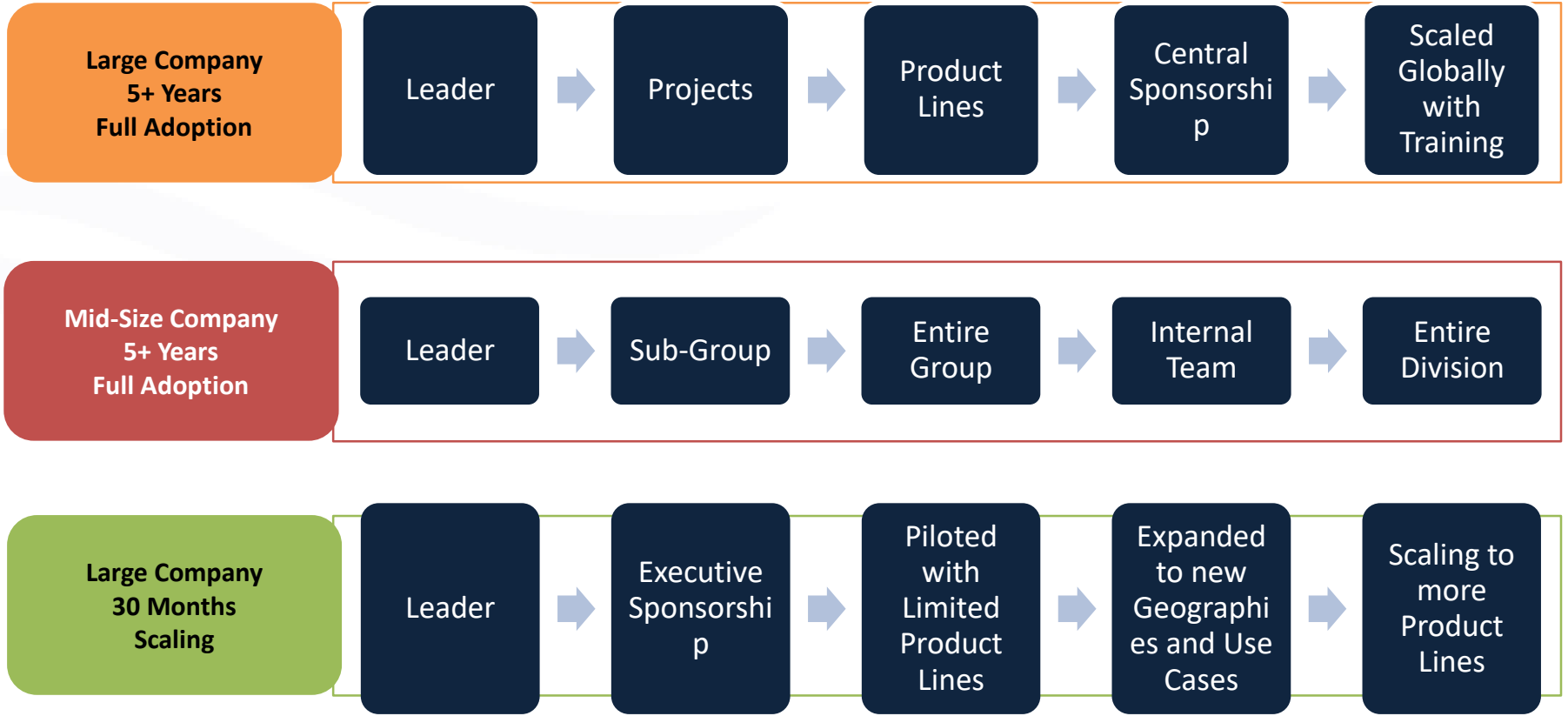
Soliton Case Study

Per Re-usable ROI over a 4 year period

	Reusable 1	Reusable 2	Reusable 3	Reusable 4	Reusable 5
Cost of Investment for Reusable Development Average Soliton Development Cost USD 50 / Man Hour	USD 125,000	USD 2,000	USD 5,000	USD 10,000	USD 33,750
Time Saving Demonstrated Per Instance of Usage (Man Hours)	6	0.5	0.5	2	1
Total Time Savings for 2500 usage instances over 4 years globally across multiple users & projects	15,000 Hrs (or) 7.5 Man Years	1,250 Hrs (or) .625 Man Years	1,250 Hrs (or) .625 Man Years	5,000 Hrs (or) 2.5 Man Years	5,000 Hrs (or) 2.5 Man Years
Total Cost Savings (USD) Average Cost Savings to Customer calculated at USD 75/hr	USD 1,125,000	USD 93,750	USD 93,750	USD 375,000	USD 187,500
ROI	800%	4600%	1800%	365%	455%

The data in the above case study is **only a subset of a large number of reusable components & platforms Soliton delivered to the customer**. For this subset of data, we are able to demonstrate **savings of 12.5 Man Years & USD 1.875 million** for an **investment of USD 176,000**, with **10x Returns over a 4 year period**

Soliton Case Studies
Path to Standardization



Achieving Standardization

The Common Denominator

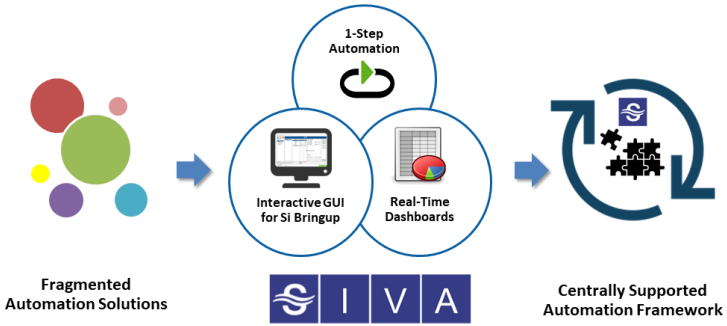
Soliton Integrated Validation Architecture

A Ready-to-Deploy Post-Silicon Validation Framework

Soliton

An automation tool focused on increasing efficiency within post-silicon validation

- ✓ GUI-centric tool for better debug & automation with minimal / no software coding
- ✓ Developed on NI's LabVIEW & TestStand
- ✓ Facilitates higher re-use of software assets and code across teams, projects and programs
- ✓ Enables easy onboarding of new engineers onto the validation activity
- ✓ Measurable Metrics to continuously validate the return on investment & benefits



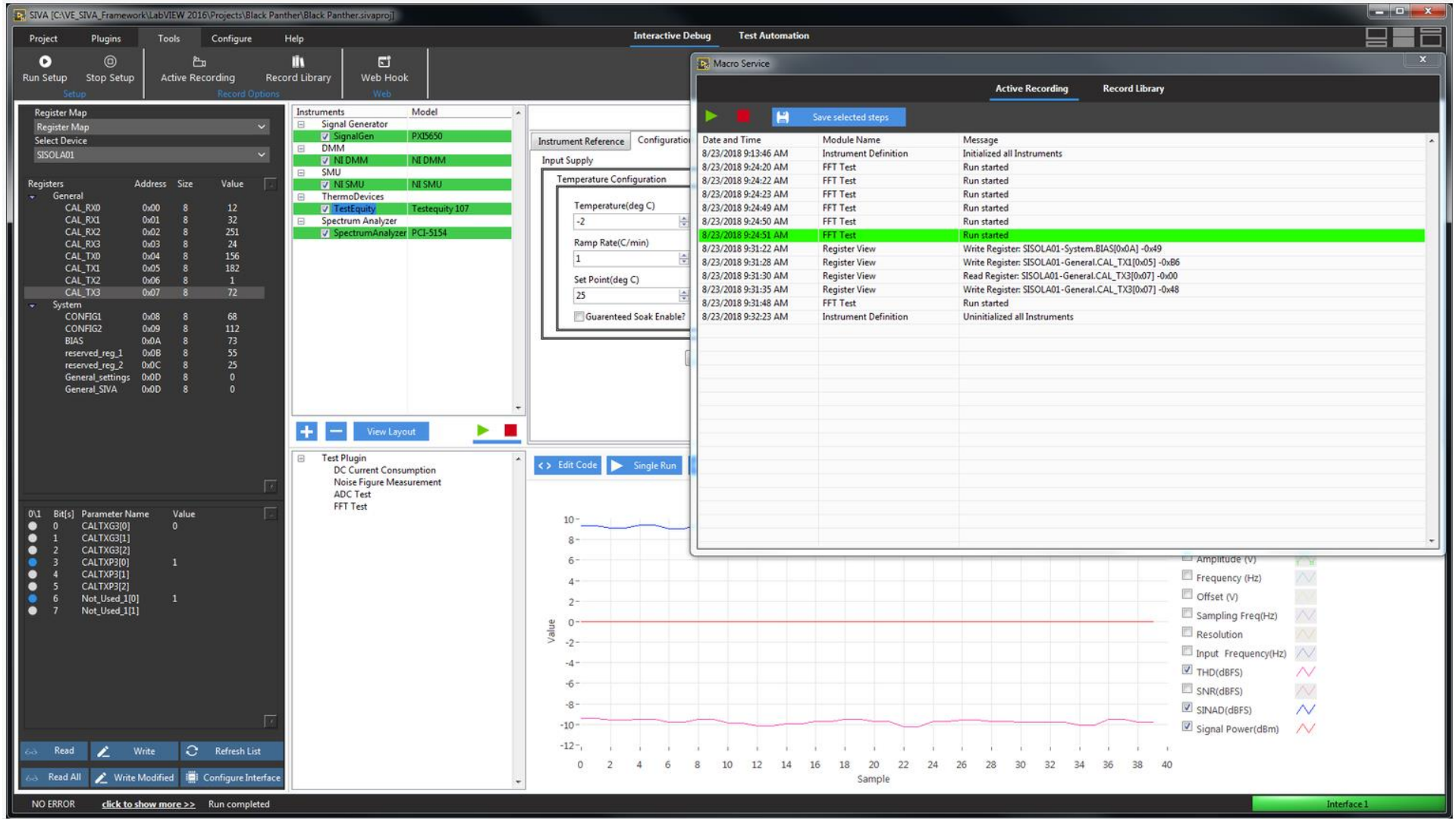
"SIVA allows its users to focus on their validation tasks instead of having to do any heavy-lifting in developing automation software. First-hand customer feedback that adoption of SIVA has helped in realizing quantifiable productivity gains of at-least 30% within 6 months of deployment. "

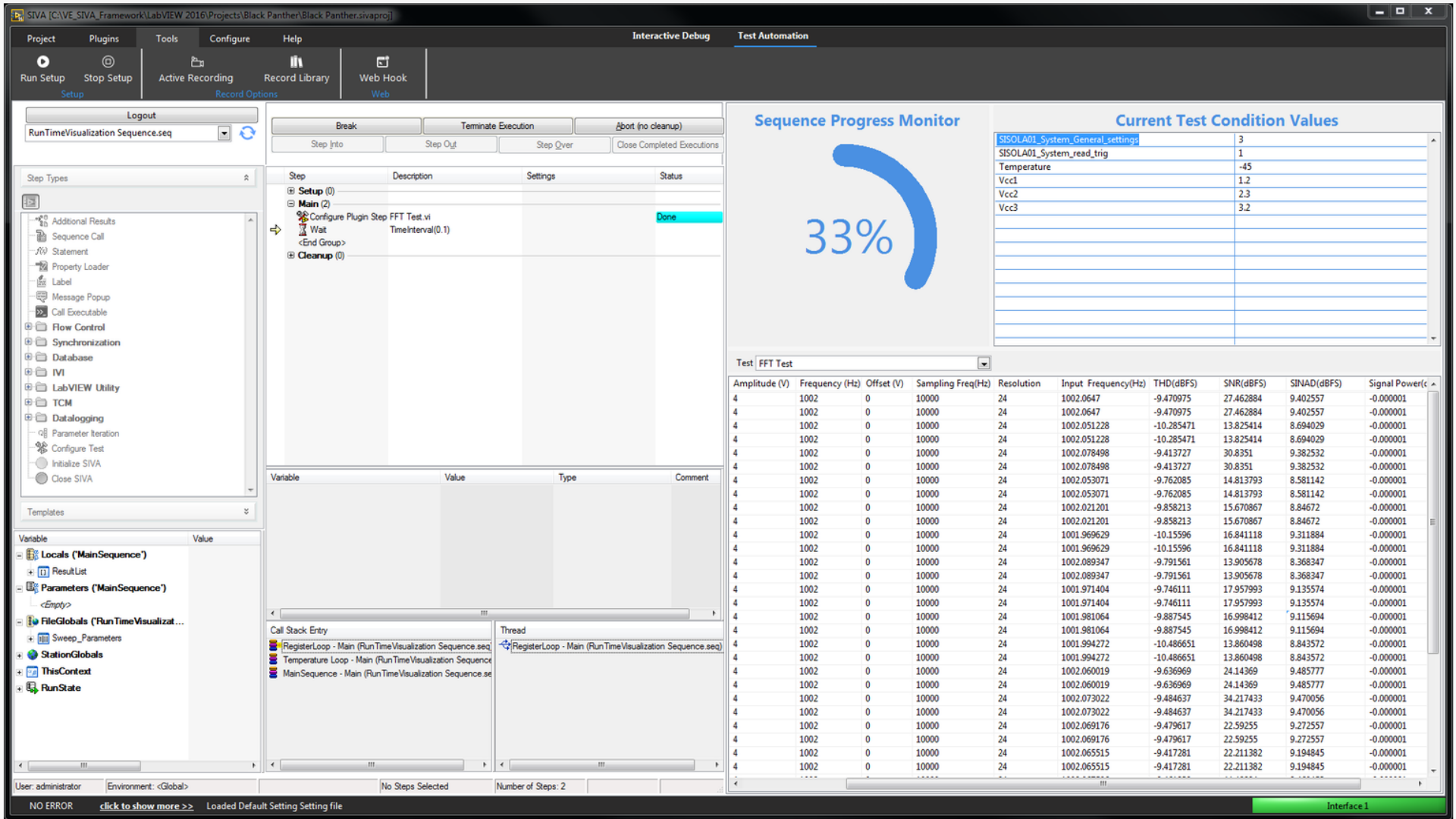
Improved Out of the Box Experience

Abstract the need for Software Architecting in Semiconductor Validation Automation Frameworks
Continuous Feature Addition in terms of productivity enhancement & measurement capability
Simple Integration with code repository, source code control tools to promote global reuse
Standardization & Minimal Training / Onboarding
Instrument Abstraction - Support Multiple Vendors & Models
High Performance with minimum overheads
Minimum maintenance from Customer End
Interactive DUT Bring Up Experience with Smooth Transition into Sequencing & Looping
Simplified Data Management for correlation, visualization & long-term retrieval

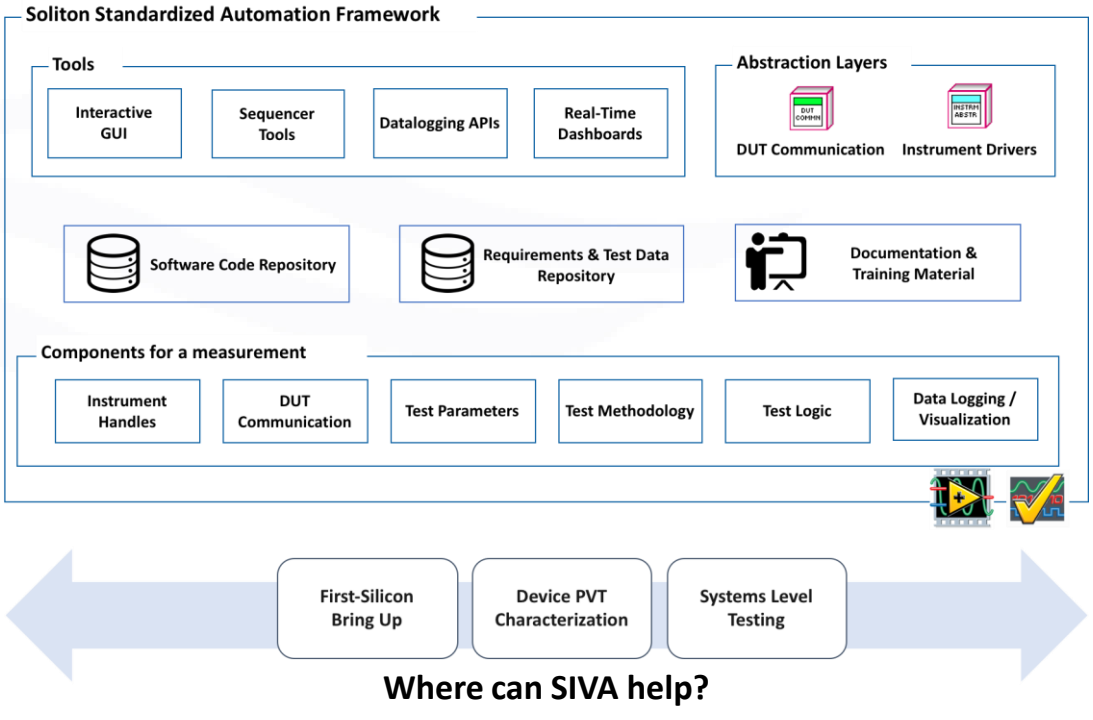
Common Customer Software Framework Needs provided out of the box

1. **Time to Impact <6 Months = High ROI**
2. **Invest only on highly custom components – Minimal long-term maintenance needs**
3. **Leverage improvements from across the Soliton customer-base for NON-CONFIDENTIAL PORTIONS ONLY**


SIVA [C:\VE_SIVA_Framework\LabVIEW 2016\Projects\Black Panther\Black Panther.sivaproj]
Project
Plugins
Tools
Configure
Help
Interactive Debug
Test Automation
Run Setup
Stop Setup
Active Recording
Record Library
Web Hook
Setup
Record Options
Web
Register Map
Register Map
Select Device
SISOLA01
Registers
Address
Size
Value
General
CAL_RX0 0x00 8 12
CAL_RX1 0x01 8 32
CAL_RX2 0x02 8 251
CAL_RX3 0x03 8 24
CAL_TX0 0x04 8 156
CAL_TX1 0x05 8 182
CAL_TX2 0x06 8 1
CAL_TX3 0x07 8 72
System
CONFIG1 0x08 8 68
CONFIG2 0x09 8 112
BIAS 0x0A 8 73
reserved_reg_1 0x0B 8 55
reserved_reg_2 0x0C 8 25
General_settings 0x0D 8 0
General_SIVA 0x0D 8 0
0\1
Bit[s]
Parameter Name
Value
0 CALTXG3[0] 0
1 CALTXG3[1]
2 CALTXG3[2]
3 CALTXP3[0] 1
4 CALTXP3[1]
5 CALTXP3[2]
6 Not_Used_1[0] 1
7 Not_Used_1[1]
Read
Write
Refresh List
Read All
Write Modified
Configure Interface
Instruments
Model
Signal Generator
SignalGen PXIS650
DMM
NI DMM NI DMM
SMU
NI SMU NI SMU
ThermoDevices
TestEquity Testequity 107
Spectrum Analyzer
SpectrumAnalyzer PCI-5154
View Layout
Test Plugin
DC Current Consumption
Noise Figure Measurement
ADC Test
FFT Test
Instrument Reference
Configuratio
Input Supply
Temperature Configuration
Temperature(deg C)
-2
Ramp Rate(C/min)
1
Set Point(deg C)
25
Guarenteed Soak Enable?
Edit Code
Single Run
Value
Sample
Amplitude (V)
Frequency (Hz)
Offset (V)
Sampling Freq(Hz)
Resolution
Input Frequency(Hz)
THD(dBFS)
SNR(dBFS)
SINAD(dBFS)
Signal Power(dBm)
Macro Service
Active Recording
Record Library
Save selected steps
Date and Time
Module Name
Message
8/23/2018 9:13:46 AM Instrument Definition Initialized all Instruments
8/23/2018 9:24:20 AM FFT Test Run started
8/23/2018 9:24:22 AM FFT Test Run started
8/23/2018 9:24:23 AM FFT Test Run started
8/23/2018 9:24:49 AM FFT Test Run started
8/23/2018 9:24:50 AM FFT Test Run started
8/23/2018 9:24:51 AM FFT Test Run started
8/23/2018 9:31:22 AM Register View Write Register: SISOLA01-System.BIAS[0x0A] -0x49
8/23/2018 9:31:28 AM Register View Write Register: SISOLA01-General.CAL_TX1[0x05] -0xB6
8/23/2018 9:31:30 AM Register View Read Register: SISOLA01-General.CAL_TX3[0x07] -0x00
8/23/2018 9:31:35 AM Register View Write Register: SISOLA01-General.CAL_TX3[0x07] -0x48
8/23/2018 9:31:48 AM FFT Test Run started
8/23/2018 9:32:23 AM Instrument Definition Uninitialized all Instruments
NO ERROR
click to show more >>
Run completed
Interface 1


SIVA [C:\VE_SIVA_Framework\LabVIEW 2016\Projects\Black Panther\Black Panther.sivaproj]
Project
Plugins
Tools
Configure
Help
Interactive Debug
Test Automation
Run Setup
Stop Setup
Active Recording
Record Library
Web Hook
Setup
Record Options
Web
Logout
RunTimeVisualization Sequence.seq
Break
Terminate Execution
Abort (no cleanup)
Step Into
Step Out
Step Over
Close Completed Executions
Step Types
Additional Results
Sequence Call
Statement
Property Loader
Label
Message Popup
Call Executable
Flow Control
Synchronization
Database
IVI
LabVIEW Utility
TCM
Datalogging
Parameter Iteration
Configure Test
Initialize SIVA
Close SIVA
Templates
Step
Description
Settings
Status
Setup (0)
Main (2)
Configure Plugin Step
FFT Test.vi
Done
Wait
TimeInterval(0.1)
<End Group>
Cleanup (0)
Variable
Value
Type
Comment
Call Stack Entry
RegisterLoop - Main (RunTimeVisualization Sequence.seq)
Temperature Loop - Main (RunTimeVisualization Sequence
MainSequence - Main (RunTimeVisualization Sequence.se
Thread
RegisterLoop - Main (RunTimeVisualization Sequence.seq)
Locals ('MainSequence')
ResultList
Parameters ('MainSequence')
<Empty>
FileGlobals ('RunTimeVisualizat...
Sweep_Parameters
StationGlobals
ThisContext
RunState
Sequence Progress Monitor
33%
Current Test Condition Values
SISOLA01_System_General_settings 3
SISOLA01_System_read_trig 1
Temperature -45
Vcc1 1.2
Vcc2 2.3
Vcc3 3.2
Test FFT Test
Amplitude (V)
Frequency (Hz)
Offset (V)
Sampling Freq(Hz)
Resolution
Input Frequency(Hz)
THD(dBFS)
SNR(dBFS)
SINAD(dBFS)
Signal Power(
4 1002 0 10000 24 1002.0647 -9.470975 27.462884 9.402557 -0.000001
4 1002 0 10000 24 1002.0647 -9.470975 27.462884 9.402557 -0.000001
4 1002 0 10000 24 1002.051228 -10.285471 13.825414 8.694029 -0.000001
4 1002 0 10000 24 1002.051228 -10.285471 13.825414 8.694029 -0.000001
4 1002 0 10000 24 1002.078498 -9.413727 30.8351 9.382532 -0.000001
4 1002 0 10000 24 1002.078498 -9.413727 30.8351 9.382532 -0.000001
4 1002 0 10000 24 1002.053071 -9.762085 14.813793 8.581142 -0.000001
4 1002 0 10000 24 1002.053071 -9.762085 14.813793 8.581142 -0.000001
4 1002 0 10000 24 1002.021201 -9.858213 15.670867 8.84672 -0.000001
4 1002 0 10000 24 1002.021201 -9.858213 15.670867 8.84672 -0.000001
4 1002 0 10000 24 1001.969629 -10.15596 16.841118 9.311884 -0.000001
4 1002 0 10000 24 1001.969629 -10.15596 16.841118 9.311884 -0.000001
4 1002 0 10000 24 1002.089347 -9.791561 13.905678 8.368347 -0.000001
4 1002 0 10000 24 1002.089347 -9.791561 13.905678 8.368347 -0.000001
4 1002 0 10000 24 1001.971404 -9.746111 17.957993 9.135574 -0.000001
4 1002 0 10000 24 1001.971404 -9.746111 17.957993 9.135574 -0.000001
4 1002 0 10000 24 1001.981064 -9.887545 16.998412 9.115694 -0.000001
4 1002 0 10000 24 1001.981064 -9.887545 16.998412 9.115694 -0.000001
4 1002 0 10000 24 1001.994272 -10.486651 13.860498 8.843572 -0.000001
4 1002 0 10000 24 1001.994272 -10.486651 13.860498 8.843572 -0.000001
4 1002 0 10000 24 1002.060019 -9.636969 24.14369 9.485777 -0.000001
4 1002 0 10000 24 1002.060019 -9.636969 24.14369 9.485777 -0.000001
4 1002 0 10000 24 1002.073022 -9.484637 34.217433 9.470056 -0.000001
4 1002 0 10000 24 1002.073022 -9.484637 34.217433 9.470056 -0.000001
4 1002 0 10000 24 1002.069176 -9.479617 22.59255 9.272557 -0.000001
4 1002 0 10000 24 1002.069176 -9.479617 22.59255 9.272557 -0.000001
4 1002 0 10000 24 1002.065515 -9.417281 22.211382 9.194845 -0.000001
4 1002 0 10000 24 1002.065515 -9.417281 22.211382 9.194845 -0.000001
User: administrator
Environment: <Global>
No Steps Selected
Number of Steps: 2
NO ERROR
click to show more >>
Loaded Default Setting Setting file
Interface 1

SIVA
Architecture



Where can SIVA help?

- *Non – monolithic GUI framework*
- *Allows for easy inclusion of legacy components from existing customer software to co-exist and operate in unison with the SIVA capabilities*
- *Minimizes expensive rework on already validated customer components*

What sets Soliton apart?

Thank You

Contact for more details

sales@solitontech.com

Agenda

Time	Topic	Presenter	Duration
08:30	Welcome and Introductions		
09:00	Keynote: An Overview of NI's Commitment to Semiconductor Test	Joris Donders (NI)	30 min
09:30	Importance of a post-Silicon Validation Automation Framework	Soliton Technologies	45 min
10:15	**Break**		30 min
10:45	Standardized software framework for test	AMSIMEC Group	45 min
11:30	Investments in Parametric testing capabilities with PXI	Jake Harnack (NI) Bart Dewachter (IMEC)	60 min
12:30	**Lunch**		60 min
13:30	Introduction to the PXI Platform	Tarek Safwan (NI)	30 min
14:00	Using a Modular Platform for Mixed-Signal Semiconductor Characterization	Tarek Safwan (NI) George Tsalavoutis (NI)	60 min
15:00	**Break**		30 min
15:15	Tips and Tricks to get the most out of the PXI platform	George Tsalavoutis (NI)	45 min
16:00	Wrap-up and summary	Alex Floor (NI) Joris Donders (NI)	30 min
16:30	**Finish**		

NATIONAL INSTRUMENTS

STANDARDIZED SOFTWARE FRAMEWORK FOR TEST

LORENZO RICOTTI

ABSTRACT

"To decrease cycle times, avoid reinventing the wheel and allow researchers at IMEC to quickly build test and measurements setups, IMEC's software test team hereby presents an insight into their plans to support IP reuse, best practices sharing and common workflows within IMEC's R&D test lab phases. The team explains the solution that they put forward and the challenges that this journey to a standardized test framework brings."

THE CURRENT LANDSCAPE :: 1/2

- Hardware
  - Dedicated to specific research lines.
  - Custom-assembled.
  - Many different vendors.
  - Issues:
    - Configurations may change (e.g. "borrowing" instruments, optional setups, ...)
    - Different degrees of maturity (old & new instruments, communication protocols, ...)
- Software
  - Largely non-uniform
    - Languages (TCL/TK, PERL, FORTRAN, C, C++, Python)
    - Environments (LabView, vendor-specifics, ...)
  - Maturity
    - Implementations
    - Functionalities
    - Usability
  - Designed by researchers (not SW engineers)
    - Drivers, drivers, drivers ...
    - Scripting flair
    - Maintainability

THE CURRENT LANDSCAPE :: 2/2

- Problems
  - Usage model
    - Interactive vs. batch
    - Remote vs. local
  - Maintain a large, heterogeneous code base
    - Non-negligible overhead to understand the legacy code
    - Familiarity with languages / tools / environments
    - Time to solution
  - Documentation
    - For the maintainers
    - For the users
  - Code quality
    - Lack of engineering
    - Less than ideal code structure

THE GOAL

- Tailored solution
  - Research oriented
    - Unique, specific needs
  - Focus on partners cooperation
- Build a solid development foundation
  - Reusability
  - Flexibility
  - Independence
  - Ownership
- Address different ways of working / needs
  - Clean, proper SW development
  - Scripting
  - Rapid application prototyping

THE MEANS

- Split the problem in smaller chunks
  - HW control
  - Measurement definitions
  - Measurement execution
  - Data management
  - Data integrity & security
  - User interface (not necessarily "Graphical ...")
- Engineering the software
  - Unified driver libraries
  - Rich basic functionalities
    - Measures
    - Workflows, conditional executions, ...
    - Software control style (CLI, GUI, WEB, ...)
- Pervasive automatic documentation
  - Code reference
  - Descriptions

CURRENT PROJECTS

IMF

- Hardware drivers
- Basic I/O
  - Application control
  - Data
- Configurations
- Basic instrument functions
- Written in C++
  - Native APIs
  - Python bindings

- User application for e-test
- Pilot project
- Uses ACME
- Written in C++
- Usage models:
  - Interactive
  - Client / Server (⚠)
- Intended targets:
  - Formal, official e-test
  - Replace legacy systems

- User application for e-test
- Python
- Uses ACME / SaM (⚠)
- Focuses on scripting capability
- Intended targets:
  - DIY-inclined people
  - Special applications
  - Prototyping

All of the above (will) interface with existing IMEC infrastructure (e.g. YoDa, etc...)

embracing a better life

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16:30	**Finish**		

NATIONAL INSTRUMENTS

NI DRIVEN IN-FAB PARAMETRIC TEST SETUP

BART DE WACHTER 3DSIP TEST ENGINEER

IN THIS PRESENTATION

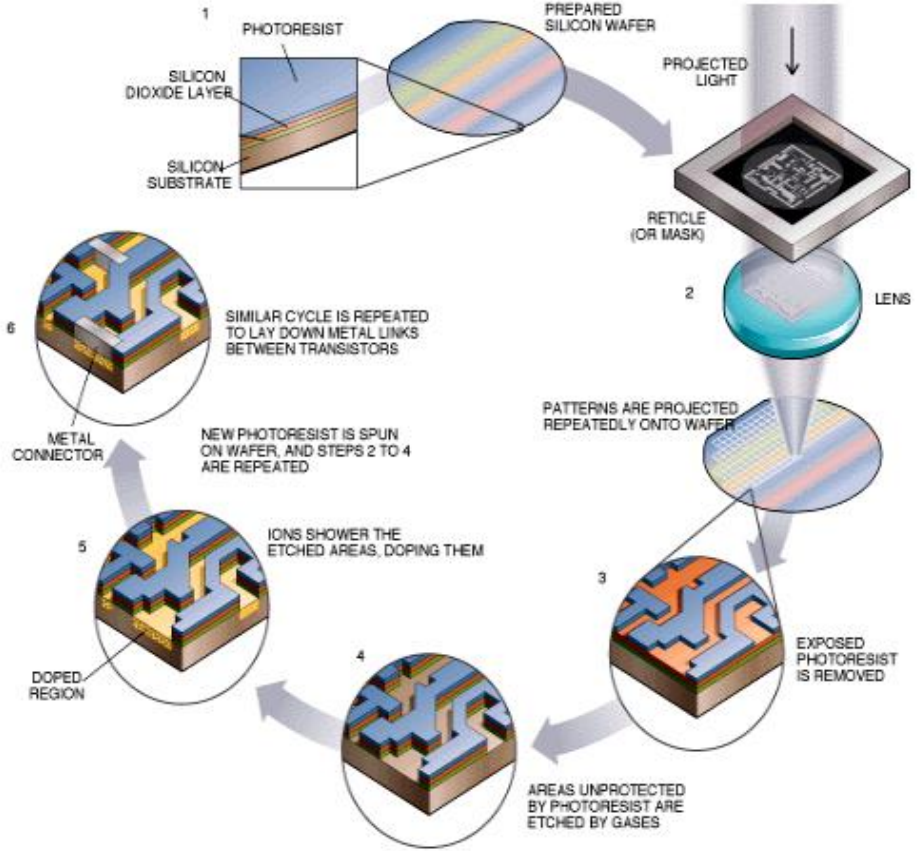
- The need for in-FAB parametric Etest
- Overview of the parametric test setup hardware & software
  - Traditional parametric test (2015-2017)
  - Highly parallel parametric test (2018-2019)
  - Traditional test vs highly parallel test
- Benchmark results NI SMUs
- Data logging / query / analysis
- Future work and challenges

THE NEED FOR IN-FAB PARAMETRIC ETEST

- Hundreds of dedicated process steps
- R&D environment, complexity ➔ process defects ➔ yield drop
- Electrical test at early process stage:
  - Very early feedback on device performance
  - monitoring of processes/tools (PCM)
  - Rework wafers
  - No need to take wafers out of FAB

➔ Speed up learning cycle

➔ Reduced wafer/processing cost

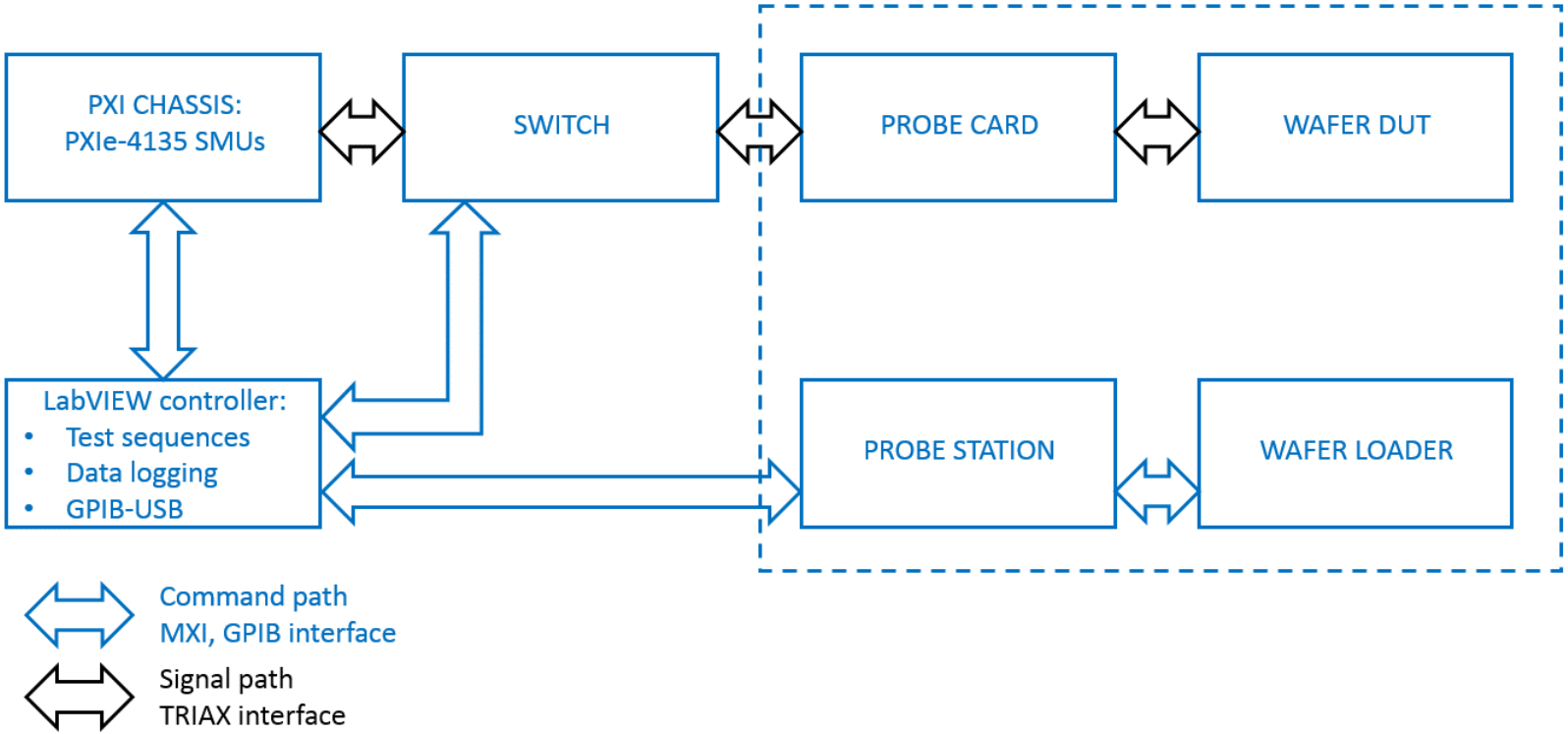


OVERVIEW OF THE TEST SETUP (VORTEX_2)

2015 – 2017 HOOKUP

1 Wafer loader
2 Wafer prober
3 Wafer prober software
4 Probe card
5 Triax cable interface
6 Low leakage switch matrix
7 National Instruments PXI chassis
8 LabVIEW controller PC:
test executive software – GUI – data logging / analysis

2015 – 2017 BLOCK DIAGRAM



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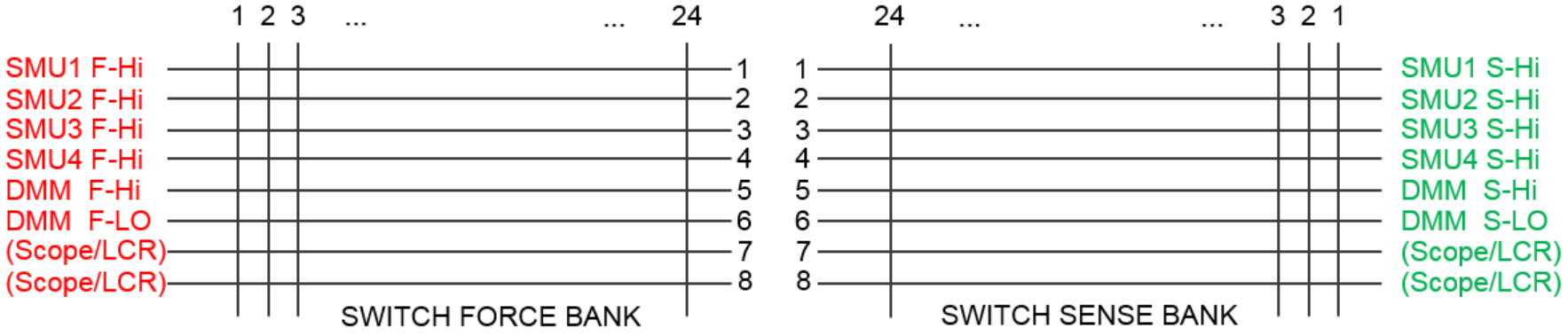
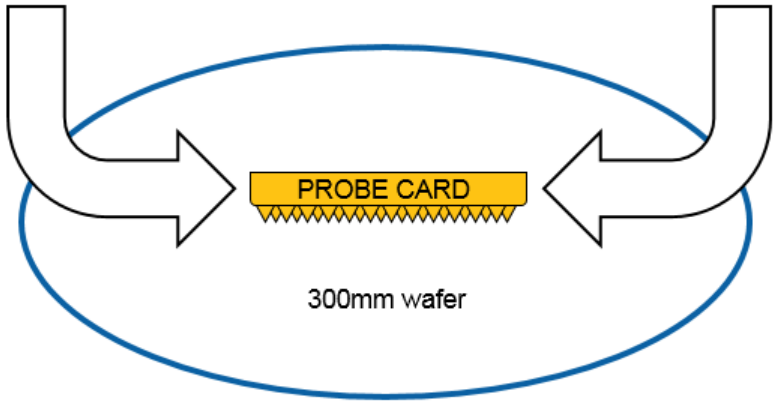
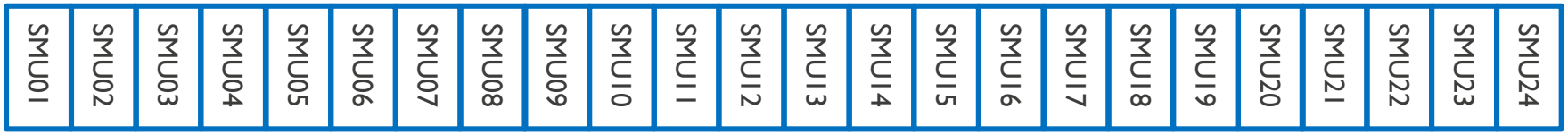
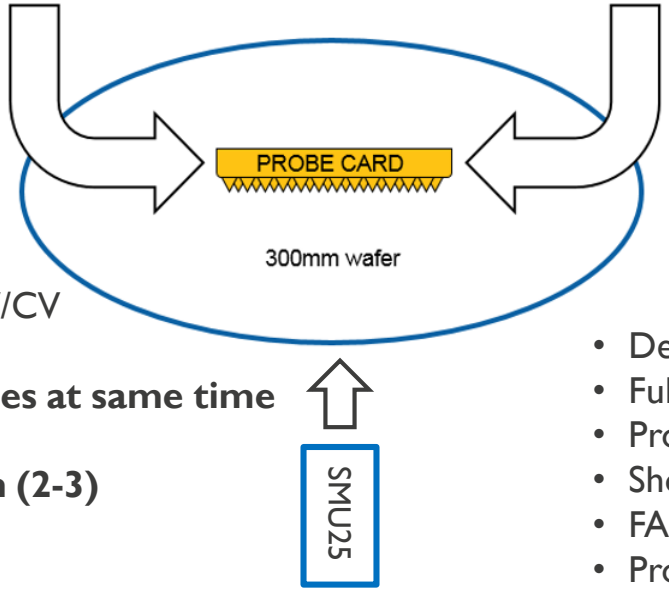
2015 – 2017 SIGNAL ROUTING





2018 – 2019 HIGHLY PARALLEL TEST SETUP





- Ditch the switch
- Per-pin-SMU
- Direct SMU-to-DUT connection
- One type of instrument does all IV/CV
- Ease of programming
- **Bias & measure multiple devices at same time**
- **Test time savings**
- **Test throughput multiplication (2-3)**

- Demand for inline Etest skyrocketed
- Full wafer map test: standard
- Process engineers require more statistics
- Shorter Tool Turnaround times required
- FAB cycle time
- Process ops are faster than Etest ops
- WLR

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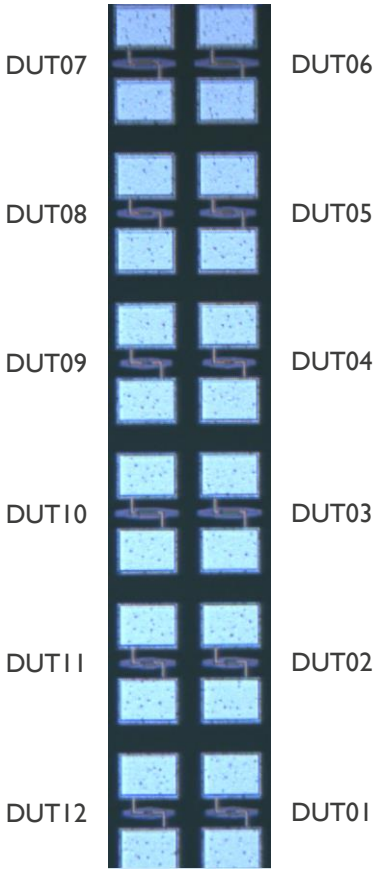
TRADITIONAL TEST VS HIGHLY PARALLEL TEST



TRADITIONAL PARAMETRIC TEST (TPT)

PARALLEL PARAMETRIC TEST (PPT)

TEST TIMING DIAGRAM

DUT01
DUT02 DUT02
DUT03 DUT03
DUT04 DUT04
DUT05 DUT05
DUT06 DUT06
DUT07 DUT07
DUT08 DUT08
DUT09 DUT09
DUT10 DUT10
DUT11 DUT11
DUT12 DUT12

TPT

PPT

TIME SAVINGS!

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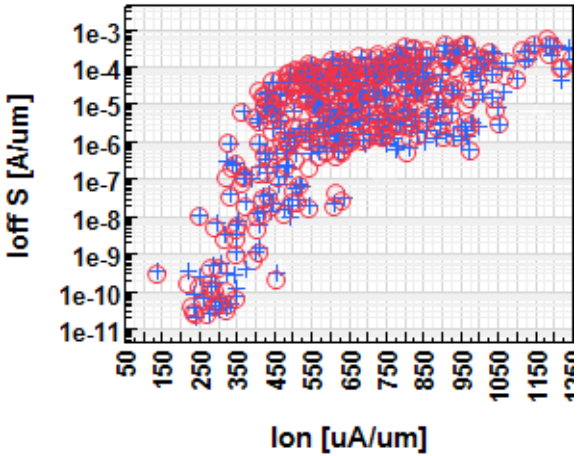
HIGHLY PARALLEL TEST

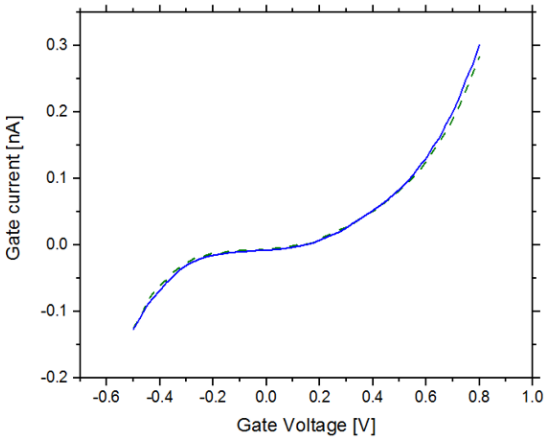
imec

BENCHMARK RESULTS WITH PXIE-4135 SMU



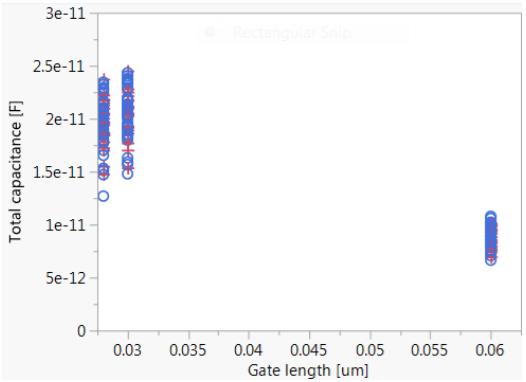
+ test results with PXIe-4135 SMUs
O test results with high-end third-party tools

Off-state / On-state transistor current measurements: excellent match!



+ test results with PXIe-4135 SMUs
-- test results with high-end third-party tools

Transistor gate sweeps (currents < pA): excellent match!



o test results with PXIe-4135 SMUs
+ test results with high-end third-party tools

Low-capacitance CV measurements for transistor gates: excellent match!!

imec

DATA LOGGING / QUERY / ANALYSIS

```
INLINE PARAMETRIC TEST SYSTEM VORTEX_2
DATE = 27/03/16
SAS DATE = 27mar2017:08:43:01.31
REQUEST ID = __001
TESTCHIP X SIZE = 25260
TESTCHIP Y SIZE = 13220
FILENAME = AL603682_D13
OPERATOR = BDW
REQUESTOR = SWK
AUTHOR = BDW
DOMAIN = 37999
KD = 00016
BOD
-1 10
27mar2017:08:43:21.40 80.957208E-12
27mar2017:08:43:25.63 1.127797E+0
27mar2017:08:43:29.63 1.255856E+0
27mar2017:08:43:33.64 1.405841E+0
27mar2017:08:43:35.43 70.820955E+6
27mar2017:08:43:35.72 43.354093E+6
27mar2017:08:43:36.03 72.400189E+6
27mar2017:08:43:36.30 69.375883E+6
27mar2017:08:43:36.94 1.828550E+0
27mar2017:08:43:37.36 68.511857E+6
27mar2017:08:43:37.62 68.997190E+6
27mar2017:08:43:37.89 42.723120E+6
27mar2017:08:43:38.18 43.494849E+6
27mar2017:08:43:38.82 2.705740E+0
27mar2017:08:43:39.29 3.915572E-9
27mar2017:08:43:40.90 42.791241E+6
27mar2017:08:43:41.19 45.096729E+6
27mar2017:08:43:41.46 71.721668E+6
27mar2017:08:43:41.73 62.296854E+6
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```
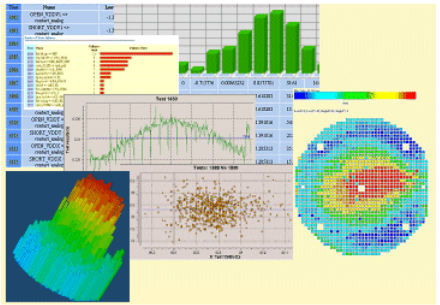
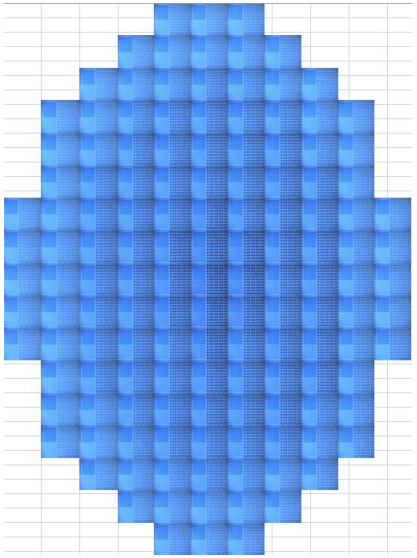

CSV

Quantix Examinator-Pro (Mentor)



SnapImages

Prober camera



yoda your data

- SAS based data warehouse
- Web Interface for data query
- Contains all imec metrology data
- Die index standardization ➔ overlay
- Calculations on datasets

- JMP
- Excel
- Matlab
- Labview
- ...

imec

FUTURE WORK / CHALLENGES

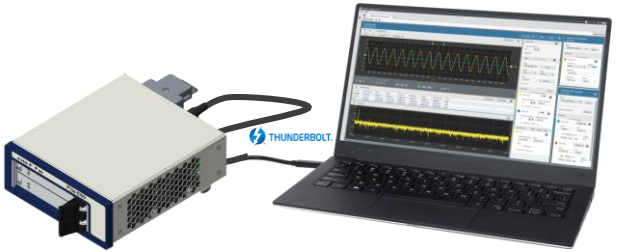
- Raise awareness to testchip designers to DFPT
- Measuring junction capacitances (<1pF)
- Expand parallel test towards WLR
- Examine more channels / bigger probe card solutions?
- New features

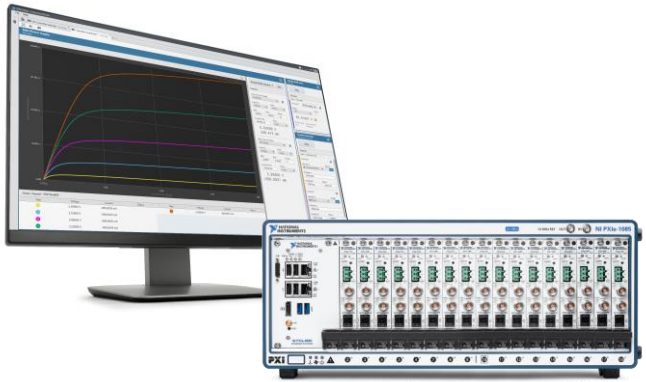
embracing a better life

NI Roadmap for DC Parametric Test

Jake Harnack | Senior Product Manager
National Instruments

What Does an NI Parametric Test System Look Like?





Hardware capabilities (SMU)
- Down to 10 fA sensitivity
- Up to 200 V maximum voltage
- Waveform generation and digitization

Supported O/S
- Windows
- Linux (roadmap)
- Linux RT (roadmap)

Supported languages
- LabVIEW & LabVIEW NXG
- C/C++
- .NET
- Python

NATIONAL INSTRUMENTS

NI SMUs Provide Core IV Requirements for Parametric Test

	Keysight B1500A HPSMU	NI PXI PXIe-4135
Maximum voltage	200 V	200 V
Maximum current	1 A DC	1 A DC, 3 A pulsed
Current sensitivity	10 fA	10 fA
Maximum sampling rate	10 kS/s	1.8 MS/s
Minimum pulse width	500 us	50 us
Connectivity	Triaxial	Triaxial
Maximum channels in chassis	4	17

Capability Comparison with Parameter Analyzer

	Keysight B1500A	NI PXI
Modular	√	√
High Power SMU	√	√
Medium Power SMU	√	√
High Resolution SMU (< 1 fA)	√ (w/ external pre-amplifier)	
10 MHz Capacitance Measurement Unit	√	ROADMAP
Medium Pulse Generator (50 µs)	√	√
Pulse Generator (< 1µs)	√	
Waveform Generator Fast Measure Unit	√	
Turnkey Application Software	√	
Programming APIs	√	√

Partner Solutions Based on NI PXI

- Company: YEA Engineering
- Product: Wafer-level-reliability toolkit for HCI and NBTI
- Available on the NI Tools Network as a software download, compatible with NI PXIe SMUs

- Company: Platform Design Automation (PDA)
- Product: FS-Pro Semiconductor Analyzer
- Sold via PDA channel (China and Taiwan)

Key Investment Areas for Semiconductor Parametric Test

- New PXIe hardware
  - SMUs and LCR meter
  - Digital instruments, precision DAQ, DMMs
  - New chassis
- Software
  - Driver features
  - Application software

Hardware

NI’s Evolving SMU Capability and Investment

PXI SMUs

Power: to 40 W, w/ aux power

Precision: to 10 pA

Speed: < 5 kS/s

4-CHANNEL SMUS

Power: < 3 W per channel

Precision: to 10 pA

Speed: to 600 kS/s sampling

SYSTEM SMUS

Power: 20 W DC, 500 W pulse

Precision: to 10 fA

Speed: to 1.8 MS/s sampling

12 & 24-CHANNEL SMUs

Power: <1 W per channel

Precision: 100 pA

Speed: to 100 kS/s

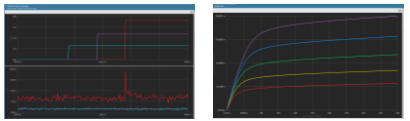
I/O CAPABILITY

2008 2009 2011 2012 2013 2014 2015 2016 2018

TECHNOLOGY BLOCKS

- HARDWARE TIMING AND TRIGGERING
- SOURCEADAPT DIGITAL CONTROL LOOP TECHNOLOGY

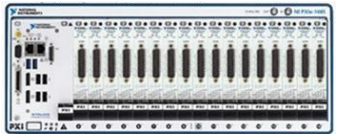
- INTERACTIVE SOFTWARE



NATIONAL INSTRUMENTS

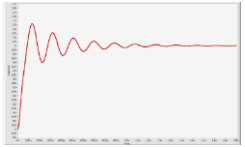
NI SMU Product Families

	System SMUs	4-channel SMUs	High density SMUs
Model numbers	4135:4139	4140:4145	4162:4163
Channels per model	1	4	12 or 24
Channels per chassis	17	68	408
Max voltage	200 V	24 V	24 V
Max current	3 A (10 A pulse)	500 mA	100 mA
Max power per channel	20 W (500 W pulse)	3 W	2.4 W
Best current sensitivity	0.01 pA	10 pA	100 pA
Driver API	NI-DCPower ← →		



CHANNEL DENSITY

up to 408 channels per chassis



SOURCEADAPT

minimize overshoot and oscillation

SOFTWARE & ECOSYSTEM

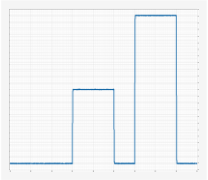
reduce development time

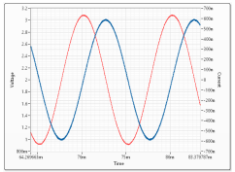
NI SMU TECHNOLOGY BLOCKS

EXECUTION SPEED

µs latency

Intel multicore processors





FAST SAMPLING AND STREAMING

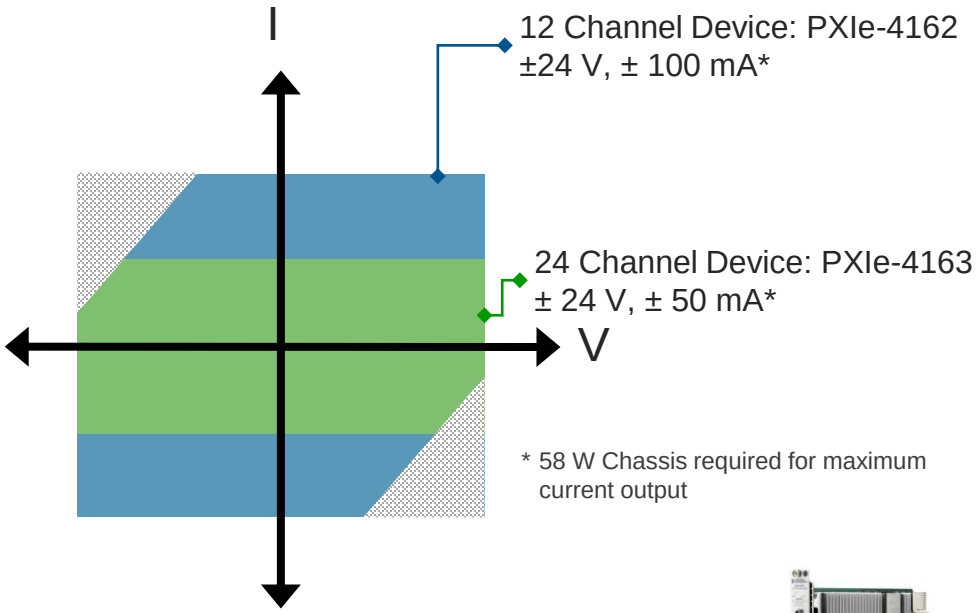
1.8 MS/s sampling rate

100 kS/s update rate

High-Density SMUs: PXIe-4162 and PXIe-4163

Released

- Single slot PXIe module
- 12 and 24 channel modules
- 100 pA current sensitivity
- 100 kS/s maximum sampling rate
- 100 kS/s maximum update rate
- SourceAdapt technology
- Hardware timing & triggering
- Up to 408 channels in a PXI chassis
- Supported in STS (calibration, cables, software, etc.)

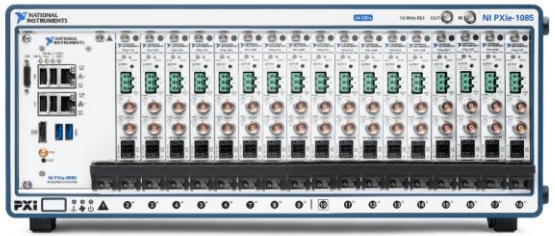


* 58 W Chassis required for maximum current output

Low Current System SMU: PXIe-4135

Released

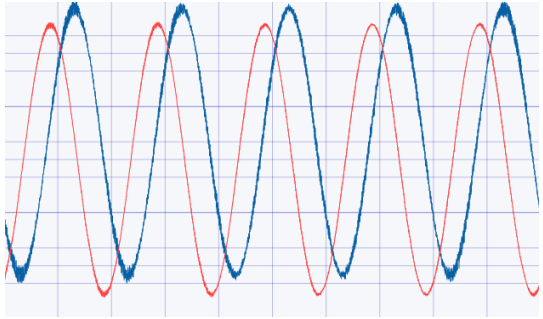
- Target applications: wafer parametric test, reliability, low current ICs and sensors
- IV Boundary
  - 200 V
  - 1 A DC, 3 A Pulse
  - 20 W DC, 500 W Pulse
- Current specs (10 nA range)
  - Sensitivity: 10 fA
  - Accuracy: 0.05% + 5 pA
- 1.8 MS/s maximum sampling rate
- 100 kS/s maximum update rate
- NI SourceAdapt™ Technology
- Hardware timing & triggering
- Triaxial connectivity



PXIe-4135 Spec and Functionality Improvements

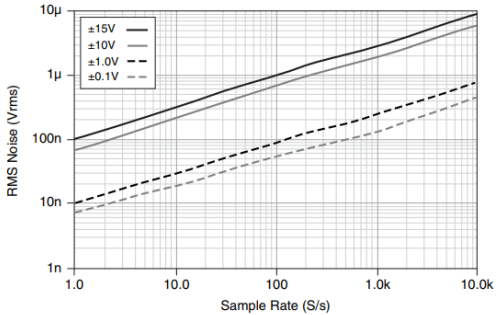
Released

- Description: Based on feedback from lead customers, improve the low current accuracy and enable CV measurements
- PXIe-4135 IV specifications
  - +/- 200 V DC output
  - 10 fA sensitivity
  - 0.05% + 5 pA accuracy >> 0.05% + 750 fA accuracy (10 PLC, w/ offset null)
- PXIe-4135 CV specifications, typical
  - DC to 1 kHz frequency
  - Nominal capacitance values between 1 pF and 10 nF
  - Typical resolution down to 10 fF
  - Typical accuracy down to 0.1%



Other High-Precision DC Instruments

Released



PXIe-4081: 7 ½ Digit DMM

1,000 V input
12 ppm voltage accuracy
100 nV voltage sensitivity
Up to 1.8 MS/s acquisition

PXIe-4309: 8 to 32-channel Analog Input

8 ADCs, each w/ internal 4x1 multiplexer
0.1 V to 15 V ranges
Down to 10 nV voltage sensitivity
Up to 2 MS/s acquisition

PXI Digital Pattern Instruments – PXIe-6570 and PXIe-6571

	PXIe-6570	PXIe-6571*
Module Width	2 slots	1 slot
Active Load	24 mA	16 mA
Pin Electronics	Digital: -2 V to +6 V, 32 mA PPMU measure voltage: -2 V to +6 V, 32 mA PPMU force voltage: -2 V to +7 V, 32 mA	
Channels	32 per module	
	256 maximum in a synchronized subsystem	512 maximum in a synchronized subsystem
Maximum Vector Rate	100 MHz (10 ns minimum vector period)	
Maximum Data Rate	200 Mb/s	
Maximum Clock Rate	160 MHz**	
Pattern Timing	31 time sets 39.0625 ps edge placement resolution	
Drive Formats	Non-return (NR), return to low (RL), return to high (RH) (100 MHz max), surround by complement (SBC) (50 MHz max)	
Vector Memory Depth	128 M/Channel	
Opcode Support	Flow control, sequencer flags and registers, signal, source and capture, subroutine	
Source and Capture Engines	Broadcast or site-unique Serial or parallel 8 per instrument	
SCAN Support	Flattened SCAN patterns, up to 128 M	

* Note that the PXIe-6571 requires a chassis with 82 W slot cooling capacity, such as the PXIe-1095. In STS, this requires the high-density test head revision.

** Clock rates >133 MHz will have a non-50% duty cycle.

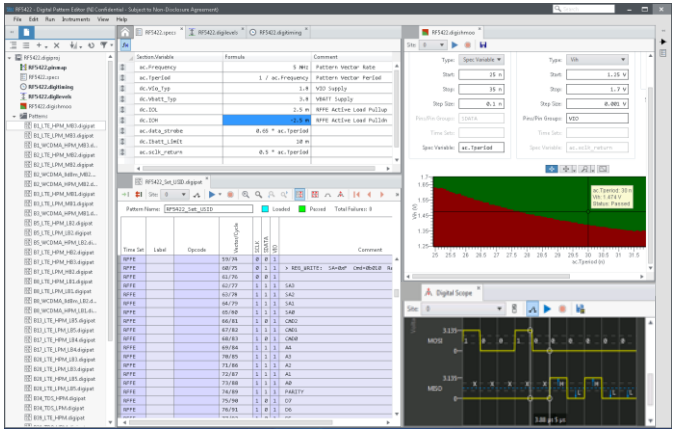
NATIONAL INSTRUMENTS

Continued Investment in Semiconductor Digital

PXIe-657x Firmware, NI-Digital Driver, and the Digital Pattern Editor

NI-Digital 18.0

- Edge Multiplier Mode enables data rates up to 200 Mbps and clock generation up to 160MHz (clock rates above 133MHz have uneven duty cycle)
- HRAM API allows programmatic collection of failures
- Sourcing Tri-State and Compares in source waveforms for open-drain protocols
- Independent Clock Generation enables free running clocks independent of pattern rates
- TCLK Fine Adjust supports multi-module synchronization outside of STS
- Extended PPMU range (to 7 V) for blowing fuses (OTP)



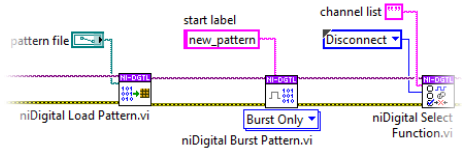
NI-Digital 19.0

- Faster API execution times around pattern bursts (certain driver call optimizations from 20 - 40%)
- Simulation Support
- Single driver session for simplified synchronization and programming of multi-device systems
- Compressed scan support for longer scan chains and improved failure analysis/visualization in DPE
- Ability for conditional opcodes to wait on PXI triggers for multi-instrument handshaking
- Having a DUT pin that can be shared across sites, to reduce wasted channels from automatic replication.
- API additions to improve programmatic shmooing
- Improved algorithm to provide digital scope results faster in DPE
- Ability to stream HRAM (History RAM) to collect more failure information

Future NI-Digital Releases (Concept)

- Ability to have separate synchronous digital subsystems in the same chassis
- TDR Sheets to store values for multiple load boards relevant to your project
- Multi-Clock period generation to create integer multiple clock signals of the vector rate
- DPE improvements targeted at completing more of an end users job completely in the DPE

Python support coming soon



Comparison of NI High Speed Serial Cards



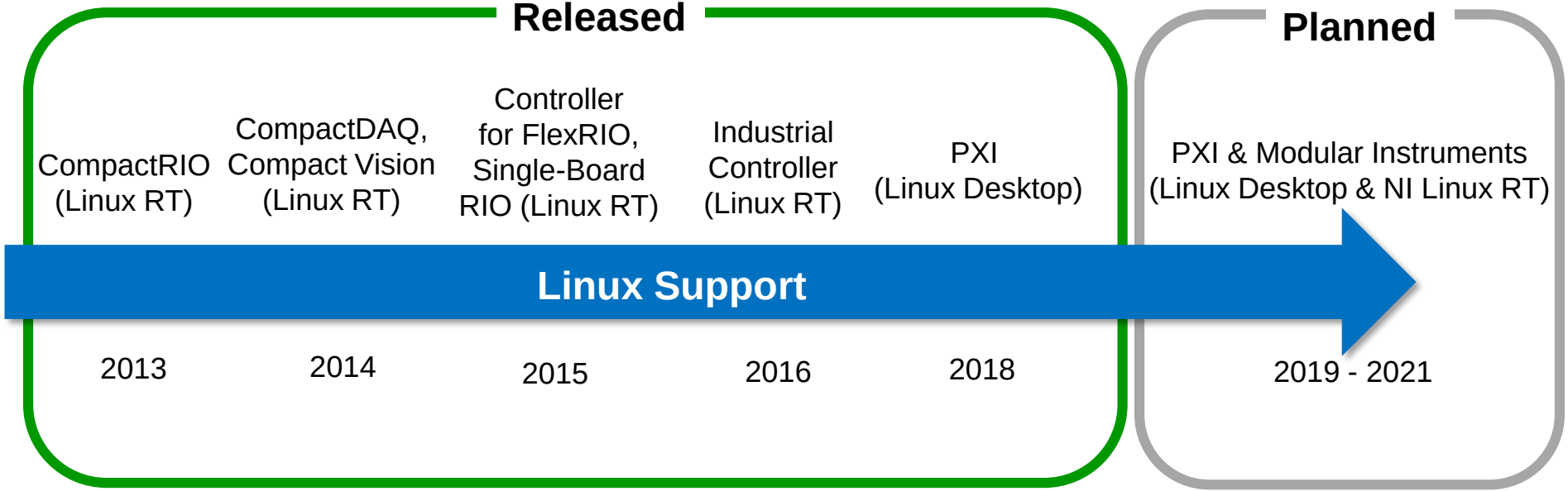


Specification	NI PXIe-7902	NI PXIe-6591	NI PXIe-6592	NI PXIe-6593	NI PXIe-6594
Release Date	Released	Released	Released	Q4 2019	Q4 2019
Line Rates	500 Mbps – 12.5 Gbps*	500 Mbps – 12.5 Gbps*	500 Mbps – 10.3125 Gbps*	500 Mbps – 16.3 Gbps	500 Mbps – 28.2 Gbps
Channels	24 TX/RX (GTX)	8 RX/TX (GTX)	4 RX/TX (GTX)	8 RX/TX (GTH)	8 RX/TX (GTY)
FPGA	Virtex-7 485T	Kintex-7 K410T	Kintex-7 K410T	Kintex Ultrascale KU40, KU60	Kintex Ultrascale + KU15P
DRAM	2 GB ~10GB/s	2 GB ~10GB/s	2 GB ~10GB/s	4 GB ~14 GB/s	8 GB ~40GB/s
Host Streaming Bandwidth	3.2 GB/s	3.2 GB/s	3.2 GB/s	7 GB/s	7 GB/s
Connector	Mini-SAS HD	Mini-SAS HD	SFP+	QSFP28	QSFP28
Cabling Options	Copper or Optical	Copper or Optical	Copper or Optical	Copper or Optical	Copper or Optical
Aux DIO	N/A	20 SE	4 SE	8 GPIO, 4 GTH	8 GPIO, 4 GTY

* Gap in achievable line rates between 8 Gbps and 9.8 Gbps

Software

NI Linux Investment Summary



redhat. LINUX

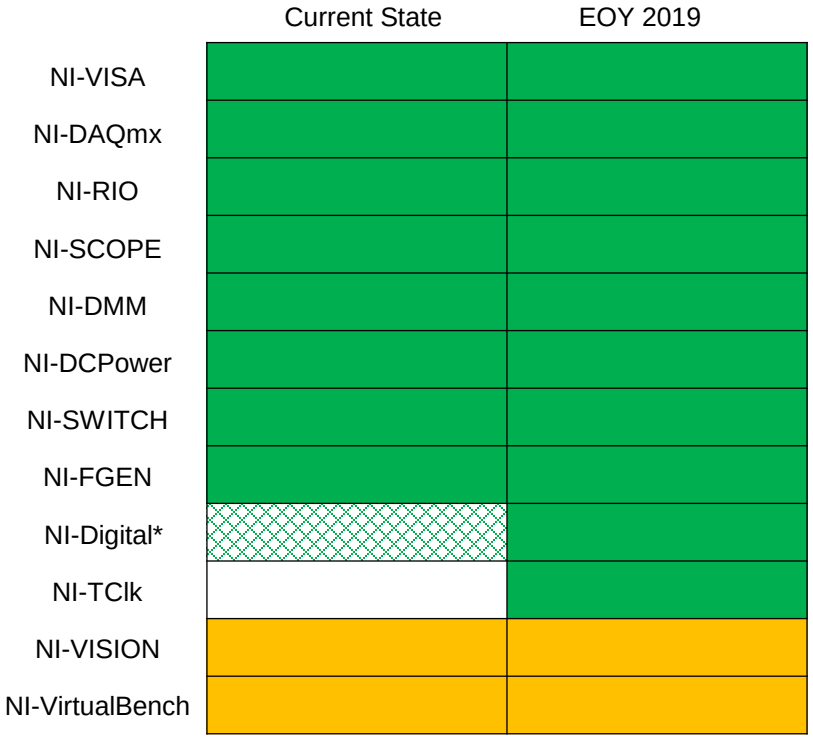
openSUSE

CentOS

NATIONAL INSTRUMENTS

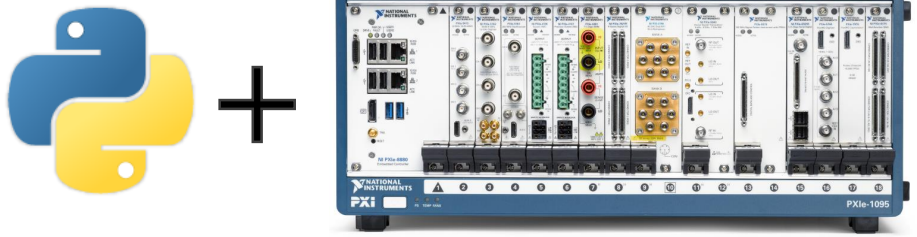
LINUX FOUNDATION
SILVER MEMBER

Python Driver Support Roadmap



Reduce development time with native Python APIs for DAQmx, VISA, RIO, and MI drivers

- Fully object oriented structure
- Supports Python warnings and exceptions
- Documentation and examples
- Free and open-source
- Installed through PyPI



New NI Driver and Application Software Features for Semiconductor

FEATURE SUMMARY

- Improved test execution times and parallel test efficiency (PTE)
- Faster code development with channel expansion
- Enhanced debugging experience by site/pin
- Advancements in offline development options
- Improved factory uptime

WHAT HAS CHANGED?

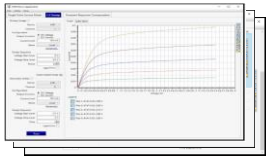
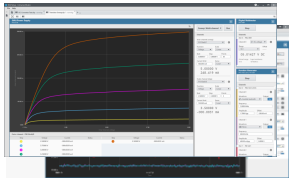
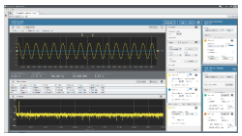
- STS Software 2019 release represents a culmination of significant investments into test execution times, test capability, programming efficiency, and factory operations
- While these features were developed primarily for STS users, many features are available by upgrading the device drivers to 19.0 or later

NATIONAL INSTRUMENTS

Software Roadmap and Potential Features for DCPower

Status	Feature	Description
v17.5	Python support	NI-developed Python bindings for DCPower, available as public beta on GitHub (v0.6.0)
v17.6.1	Asymmetric compliance	Set +/- compliance limits
v17.6.1	New DCPower Soft Front Panel	Interactive software for controlling multiple SMUs and power supplies and configuring IV sweeps
v18.1	Import configuration from InstrumentStudio	Configure DC instrument in InstrumentStudio and import that configuration into application code
v18.1	.NET installation w/ DCPower	Add .NET class libraries to the DCPower installation along with LabVIEW and C/C++
v18.1.1	Pre-load advanced sequences	Save up to 100 advanced sequences in memory and recall them without runtime config overhead
v18.2	Sequence step delta time for FGEN capability	Output low frequency pattern (sine, triangle, etc.) with better determinism
v19.1	Parallel test efficiency improvements	Reduced execution time for calls like Commit, Fetch, Wait for Event that improve PTE
H1 2020	Multi-instrument sessions	Combine DCPower channels across multiple devices into a single session
H1 2020	Linux Desktop	DCPower support for Linux 64-bit, distributions: Red Hat Enterprise, OpenSUSE, CentOS
	Measurement Autorange	Automatically switch ranges based on the measured value
	Digital slew rate control	Programmatically control the slew rate control w/ onboard FPGA
	“Power” compliance and CP mode	Ability to set a “power” compliance instead of voltage or current limits, also add constant power load
	Analog trigger/event	Trigger an SMU acquisition or event based on the SMU measurement (e.g. load current pulse)

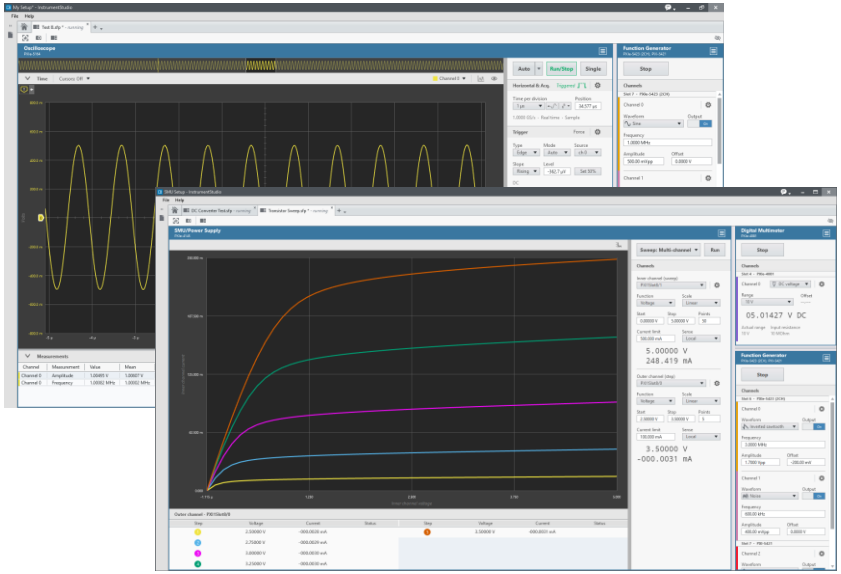
Interactive Software for SMUs and Power Supplies

	Soft Front Panel	SMU Demo App	DCPower 16.0.2	InstrumentStudio
Year introduced	2003	2015	2017	2018
Basic IV control & measure	●	●	●	●
Driver debug	● (2014)		●	●
Multiple DCPower modules		●	●	●
Sweeps		●	●	●
Installs w/ driver software				●
Integration w/ other instruments				●
Path to programming				●
SourceAdapt workflows		●		● (2019)
Digitizer/FGEN modes for SMU				● (2019)
Math channels				● (2019 SP1)

InstrumentStudio™

Next-Generation Soft Front Panels for NI PXI Modular Instruments



All your instruments in a single application
Take advantage of high-resolution monitors rather than small, integrated displays

Capture screenshots and export data
Store screenshots and measurement results from *all* of your instruments with a single click

Share projects with colleagues and between systems
Projects store your UI layout and instrument configuration for instant repeatability

Export configurations for programmatic use
Minimize code development and guarantee measurement correlation

Monitor and debug automated test systems
Pause test sequences for debug or simply monitor your instruments while they are running

InstrumentStudio 2019

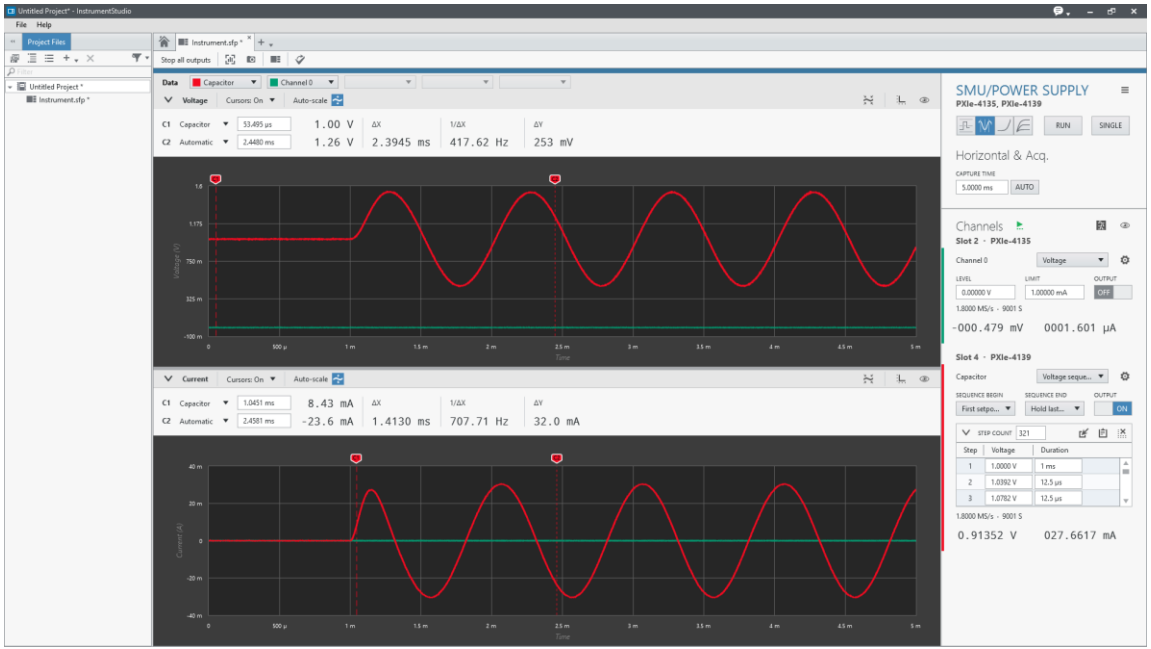
Released

SMU Enhancements

- Waveform/digitizer mode
- Trigger access
- Asymmetric limits and voltage protection
- Live monitoring
- Condensed channel view
- Math channels (2019 SP1 or later)

Other Enhancements

- Export to TestStand
- Pin and site awareness (DUT-centric debugging)
- Channel expansion for oscilloscopes
- Hosted LabVIEW applications



TestStand

New Features in 2019

- Adapter support for Python
- Parametric sweep and stream loops
- InstrumentStudio integration
- PDF reports and HTML5 graph control

Key Applications

- Automated production test
- Interactive, validation workflows

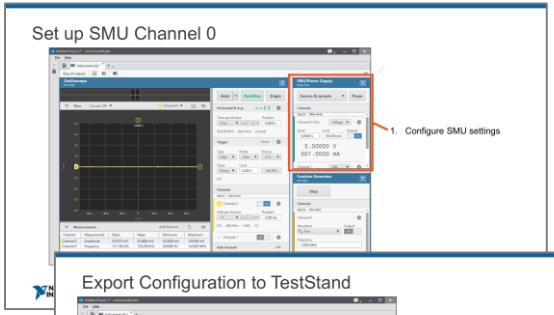
Other TestStand Features

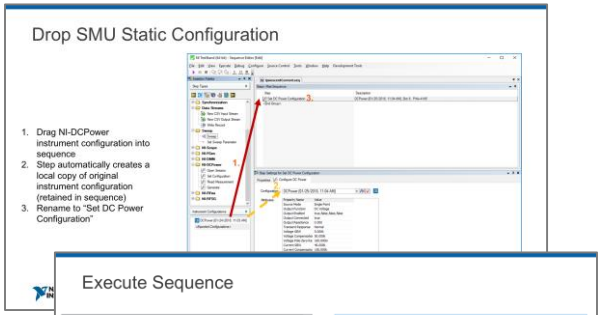
- Quick Drop
- Multicore scaling improvements
- LabVIEW 2019 and LabVIEW NXG 3.0 support
- Easily switch between source VIs and PPLs
- LabWindows/CVI 2019 – Source code navigation, auto-creation of enums from structs, and distinguish pointers from arrays

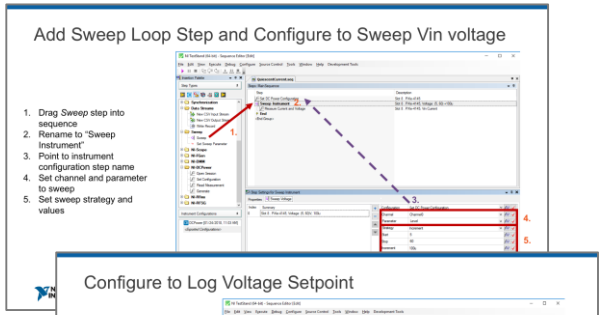
InstrumentStudio™ 2019 - TestStand Integration

Automation without programming for device validation

- InstrumentStudio exports instrument configuration to TestStand
- TestStand applies static instrument configuration and can sweep over common instrument settings (e.g. SMU voltage and current)
- TestStand can source instrument settings from and log results to CSV files (Data Streams)
- *Future:* configuration-based (no programming) TestStand steps for instrument-specific measurements







SystemLink™

Build systems faster. Manage them better.

Features at a glance

- System health and performance, with alarms and notifications
- Software deployments and software configuration management
- Automated test procedures with sequence monitoring and user-defined dashboards
- Data transmission and visualization with open APIs and graphical interfaces
- Data analysis and report scheduling with search, standardization, and 3rd-party plug-ins

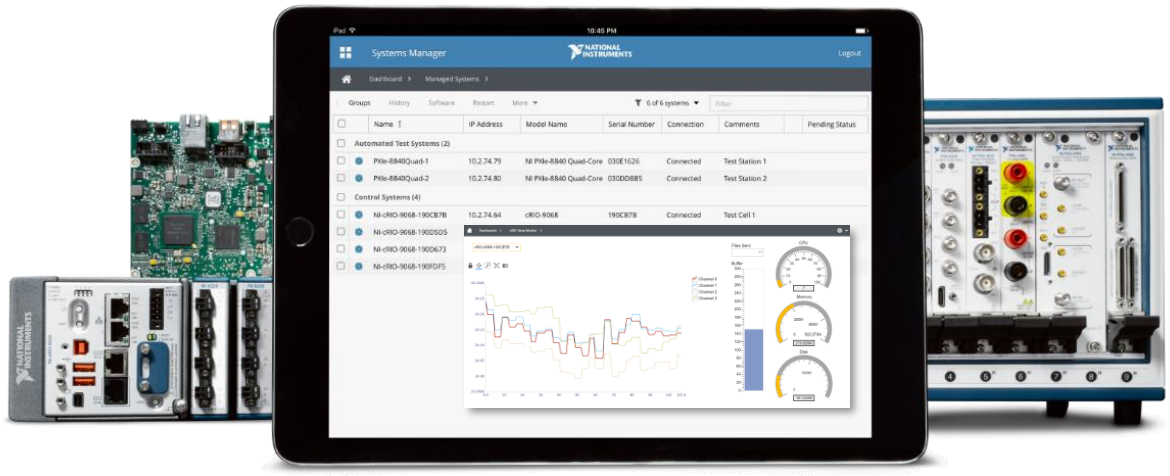
Customer Use Cases

Manufacturing test

Engineering verification & validation

Test cells / Physical systems test

Distributed DAQ & control



NATIONAL INSTRUMENTS

Agenda

Time	Topic	Presenter	Duration
08:30	Welcome and Introductions		
09:00	Keynote: An Overview of NI's Commitment to Semiconductor Test	Joris Donders (NI)	30 min
09:30	Importance of a post-Silicon Validation Automation Framework	Soliton Technologies	45 min
10:15	**Break**		30 min
10:45	Standardized software framework for test	AMSIMEC Group	45 min
11:30	Investments in Parametric testing capabilities with PXI	Jake Harnack (NI) Bart Dewachter (IMEC)	60 min
12:30	**Lunch**		60 min
13:30	Introduction to the PXI Platform	Tarek Safwan (NI)	30 min
14:00	Using a Modular Platform for Mixed-Signal Semiconductor Characterization	Tarek Safwan (NI) George Tsalavoutis (NI)	60 min
15:00	**Break**		30 min
15:15	Tips and Tricks to get the most out of the PXI platform	George Tsalavoutis (NI)	45 min
16:00	Wrap-up and summary	Alex Floor (NI) Joris Donders (NI)	30 min
16:30	**Finish**		

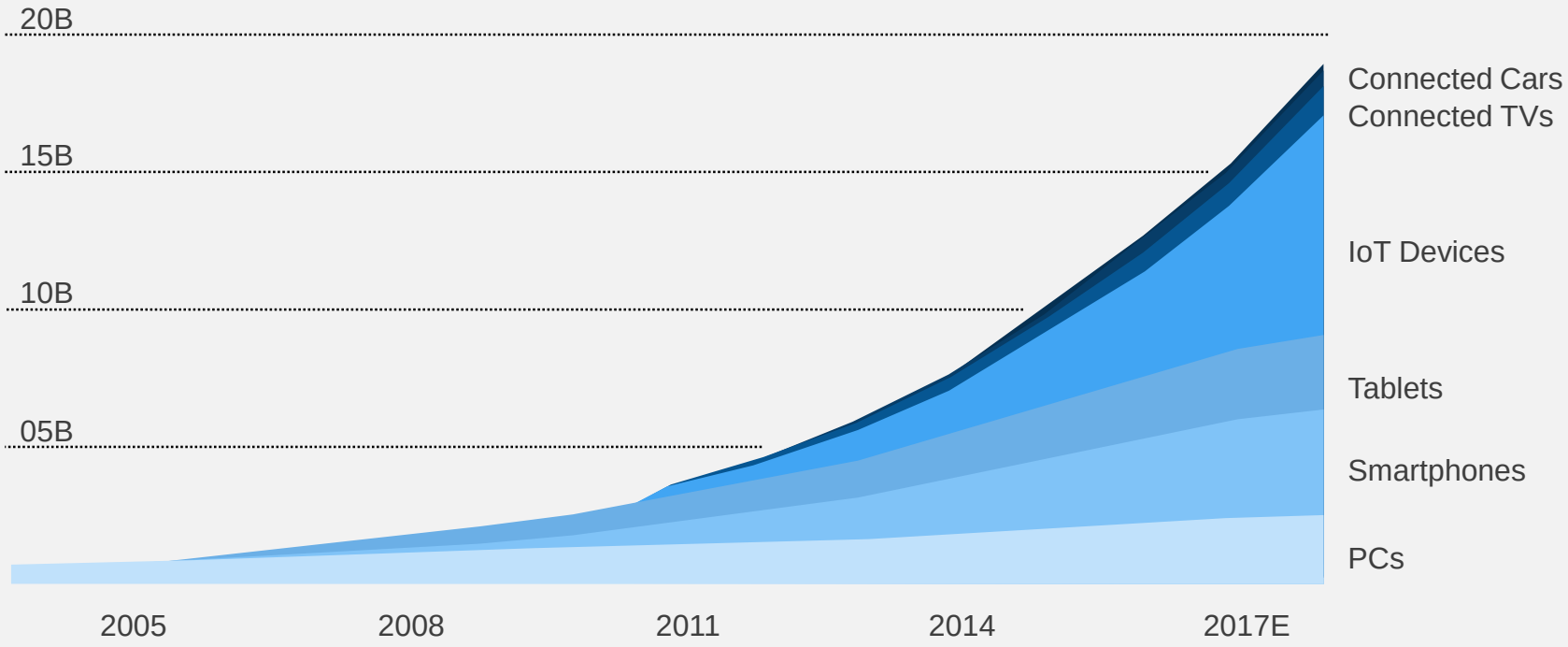
NATIONAL INSTRUMENTS

Introduction to the PXI Platform

Smarter Test From Characterization to Production

Tarek Safwan
Field Marketing, Semiconductor Test
National Instruments

The Big Bang of Smart Devices

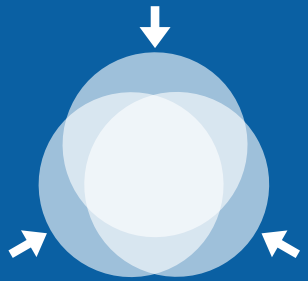


Source: BI Intelligence Estimates

NATIONAL INSTRUMENTS

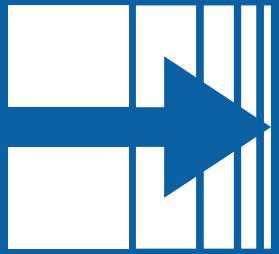
Unique Attributes of Smart Devices: Common Test Needs

CONVERGENCE



LOWER PRICE

RAPID CHANGE



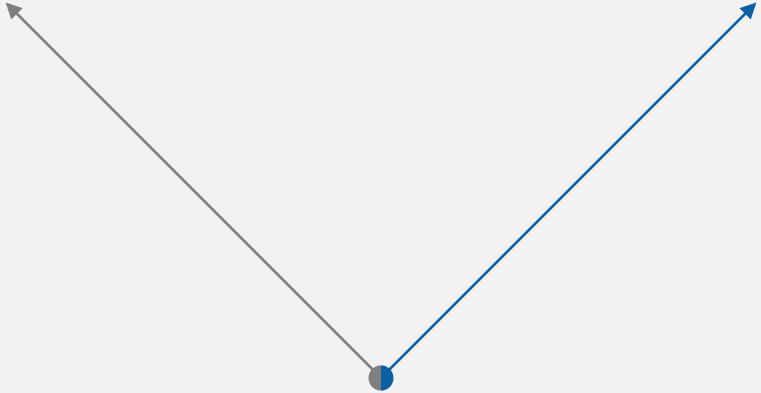
- More functionality
- High reliability
- Lowest cost
- Short time to market

NATIONAL INSTRUMENTS

Vendor Strategies for Test and Measurement

CLOSED

- “Vendor knows best”
- Fixed functionality
- Closed ecosystem
- Customer pays



PLATFORM

- “Customer knows best”
- Customizable solution
- Open, vibrant ecosystem
- Customer designs

NATIONAL INSTRUMENTS

Boxes Are Throttling Innovation

- Fixed Functionality
- Outdated Processors
- Communication Latency
- Little Data Streaming
- Closed Software

The old, closed approach to test just isn’t smart;
it can’t keep pace with innovation.

NATIONAL INSTRUMENTS

Smarter Test System

- Open, Flexible Software
- Modular Hardware
- Vibrant Ecosystem
- “Customer Knows Best”

A smart test system is more than a fixed-functionality instrument; it is built for automation and customization.

PXI

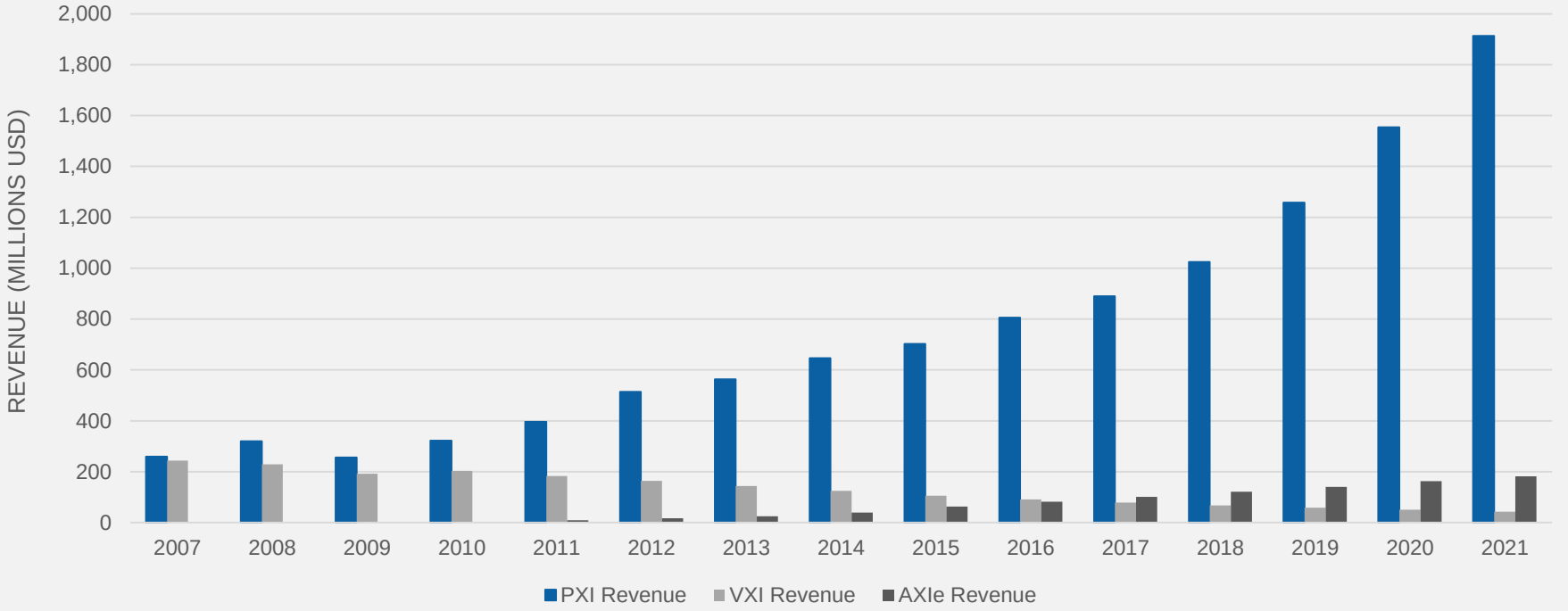
Systems Alliance

NATIONAL INSTRUMENTS

Characteristics of the Stable PXI Platform

- Founded in 1997
- 60+ Vendors
- 2000+ Modules
- Latest Technology
- Growing Market Share

Continued Innovation in PXI Platform



Source: Frost & Sullivan

NATIONAL INSTRUMENTS

Anatomy of a PXI Test and Measurement System

Software

Test Management and Code Development
Code sequencing, database reporting, user management, operator interface, parallel execution, signal processing; LabVIEW, C/C++, .NET, Python

Timing and Synchronization

PXI Chassis
PCI Express Gen 3 throughput up to 24 GB/s, subnanosecond latency, P2P streaming, integrated triggering

Computer

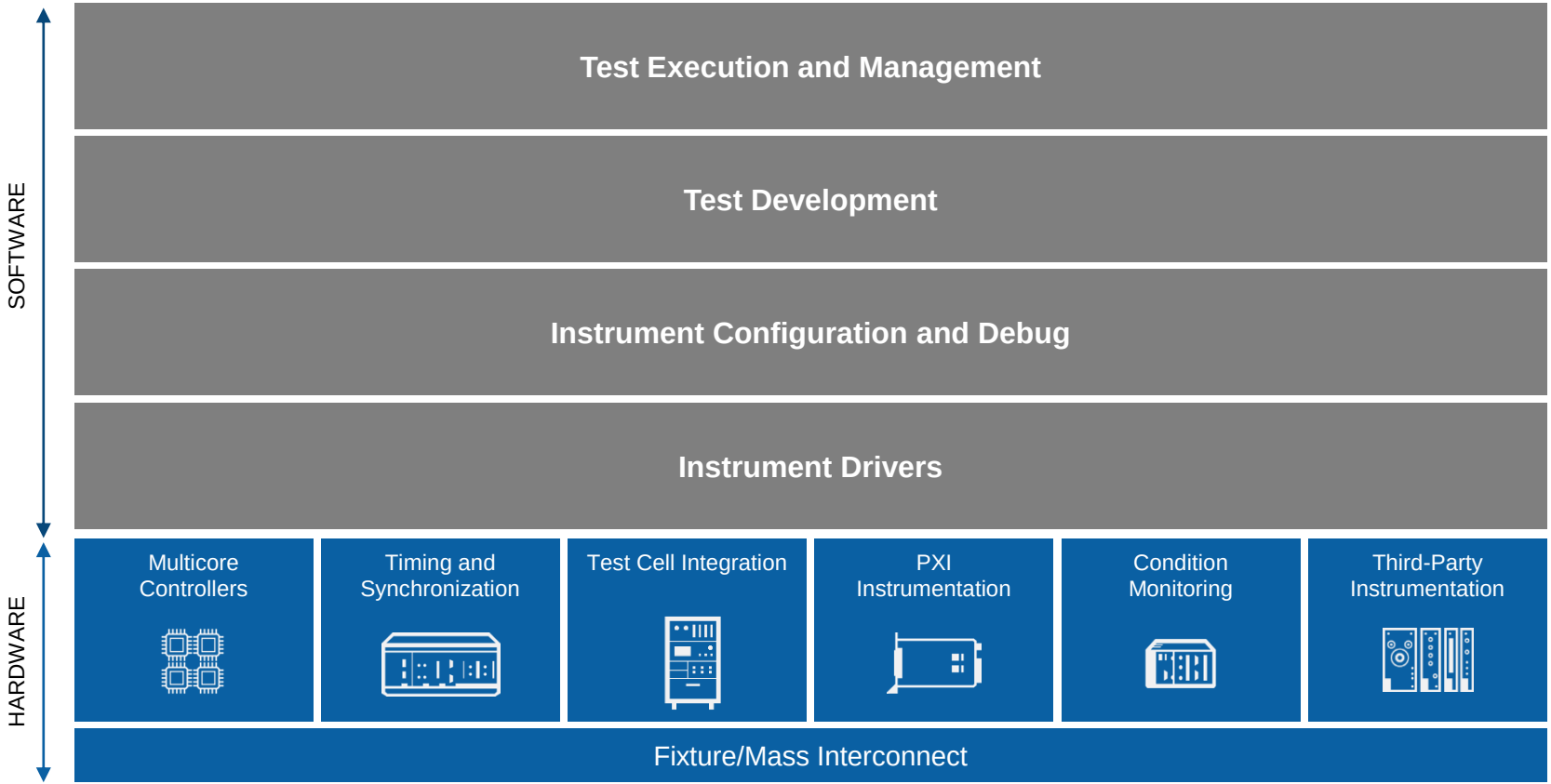
PXI Embedded Controller
Windows and real-time OS options, Intel Xeon processing, peripheral ports, display output, integrated hard drive

Instrumentation

PXI Modules
DC to mmWave, oscilloscope, programmable power supply, switch/MUX, DMM, VSA, VSG, VST, AWG, SMU, DAQ

NATIONAL INSTRUMENTS

Architecture of an Automated Test System



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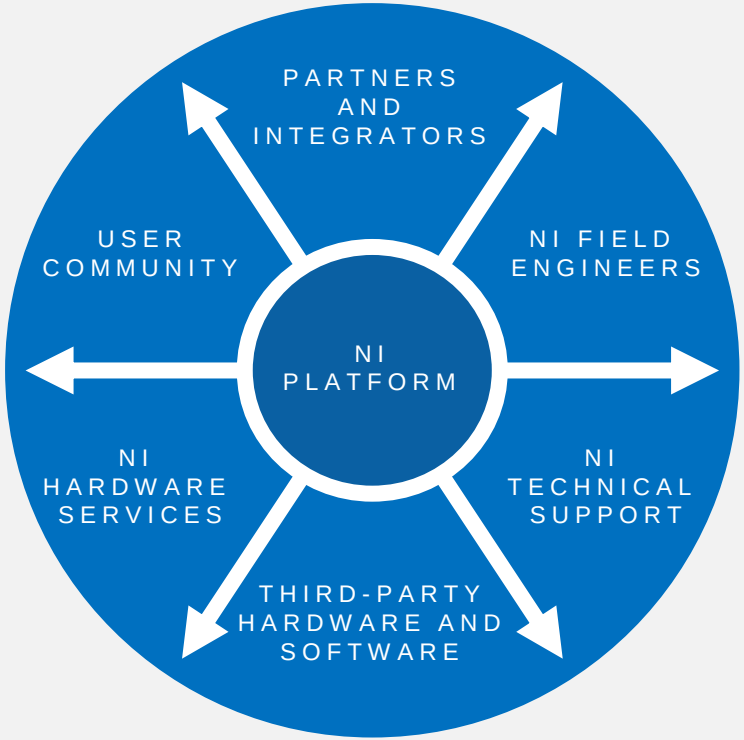
An Ecosystem Built on the NI Platform

300k+
Users

30+
Service Centers

350+
Software Toolkits



1000+
Partners

700+
Field Engineers

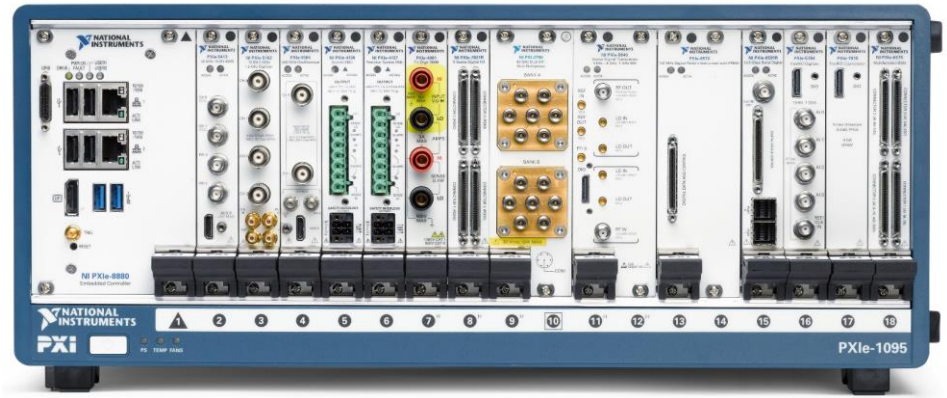
700+
Support Engineers

NATIONAL INSTRUMENTS

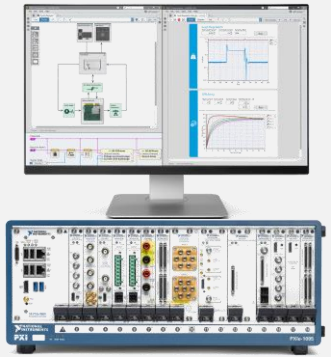
PXI Integrates All Instrumentation Protocols

Broad Modular Instrumentation Portfolio

DAQ and Control	Instrumentation	Interfaces
Multifunction I/O	Oscilloscopes	GPIB, USB, LAN
Counter/Timer/Clock	High-Speed Digital I/O	RS232/RS485
Digital I/O	DMM and SMU	CAN, LIN, DeviceNet
Analog Input/Output	Signal Generators	SCSI, Ethernet
Vision and Motion	Switching	VXI/VME
FPGA/Reconfigurable I/O	RF Analyzers and Generators	Boundary Scan/JTAG



NATIONAL INSTRUMENTS



Advantages of PXI Instrumentation

- High Measurement Quality
- Low Latency and High Throughput
- Software-Defined Functionality
- Integrated Timing and Sync
- High-Performance Processing
- Reduced Size, Weight, and Power
- Complete Instrumentation Portfolio

NATIONAL INSTRUMENTS

Industry-Leading Test and Measurement Platform

PXIe-5162
4 ch, 1.5 GHz,
10-bit digitizer

PXI-4081
7½-digit, 1 kV
precision DMM

PXIe-5668
26.5 GHz VSA with
765 MHz bandwidth

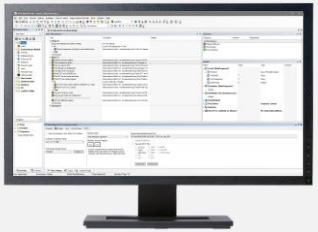
PXIe-4135
precision system SMU
10 fA sensitivity

PXIe-5840
6 GHz VST with
1 GHz bandwidth

PXIe-1095
PXI chassis
24 GB/s throughput

PXIe-8880
PXI Express controller
8-core Intel Xeon

LabVIEW
system design
software

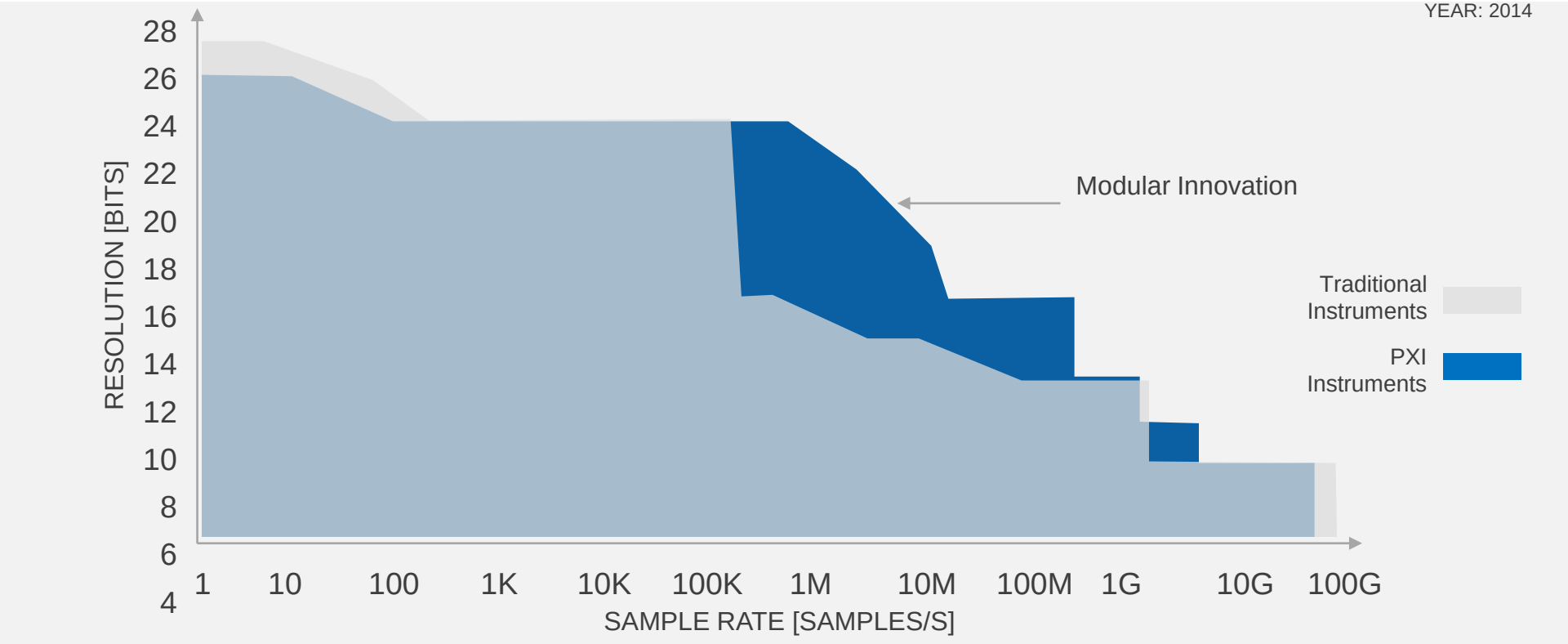


TestStand
test management
software

PXIe-2543
6 GHz, 8 ch, solid-state
multiplexer

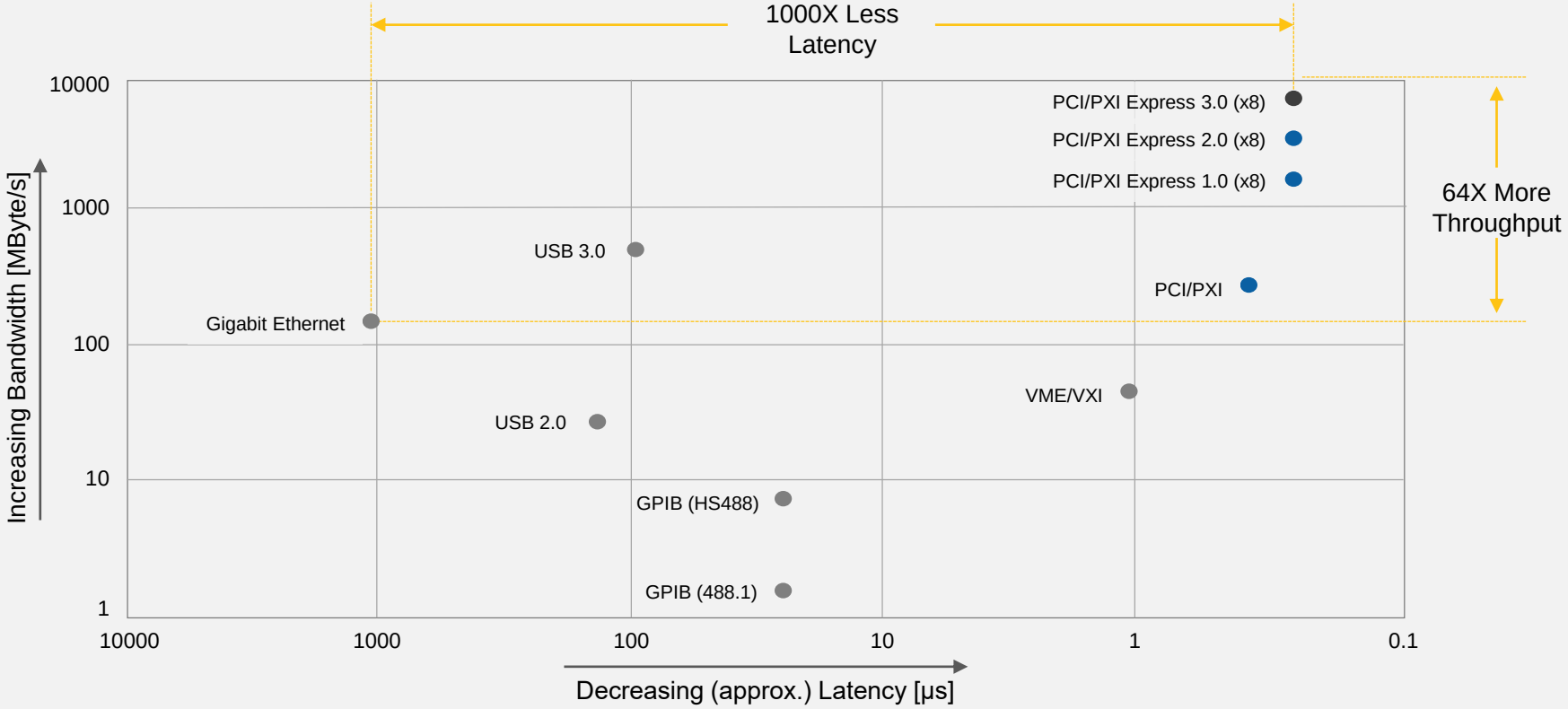
NATIONAL INSTRUMENTS

Trusted Measurement Quality



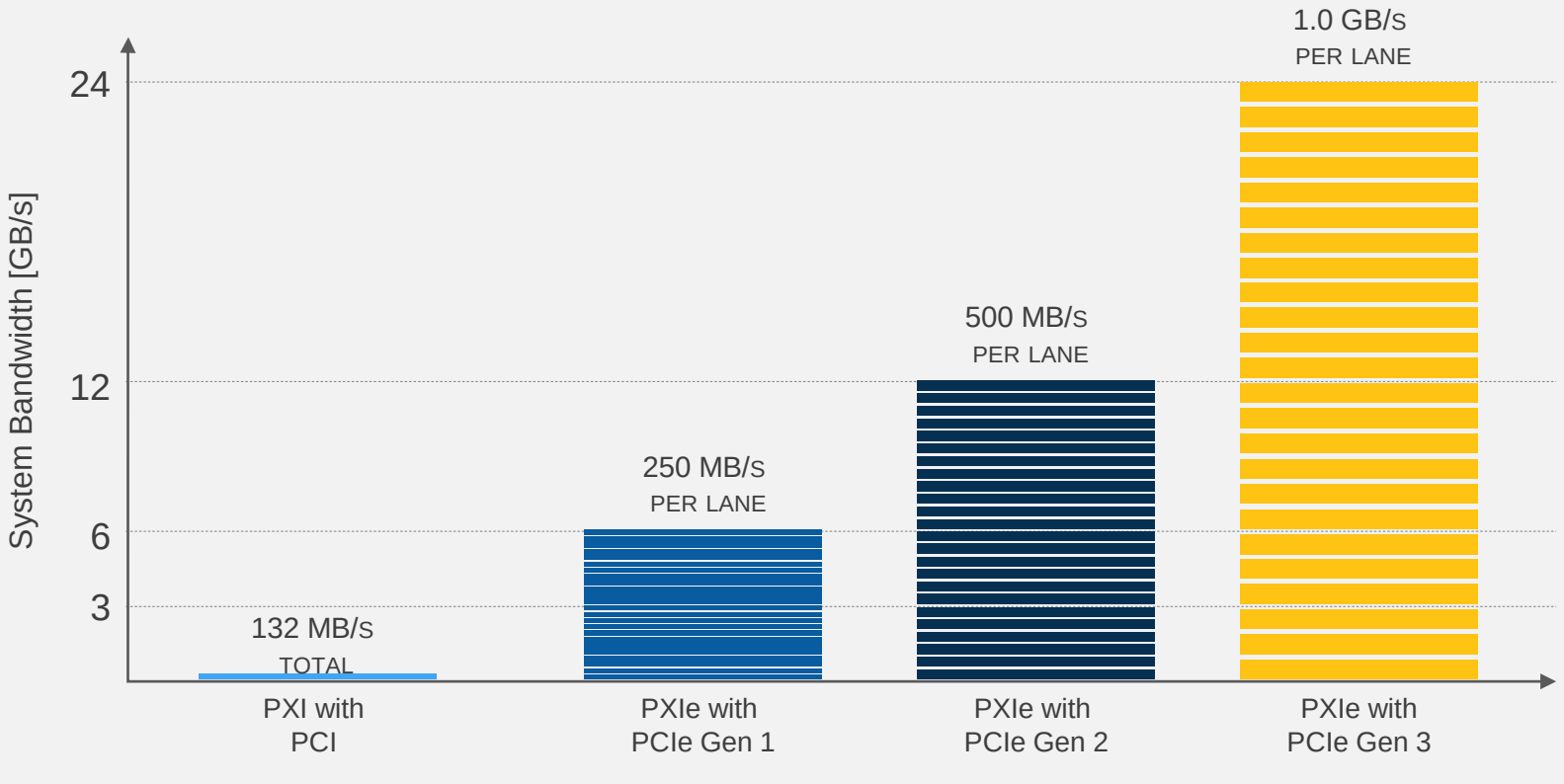
NATIONAL INSTRUMENTS

High Throughput and Low Latency With PXI



NATIONAL INSTRUMENTS

Continually Increasing System Bandwidth



NATIONAL INSTRUMENTS

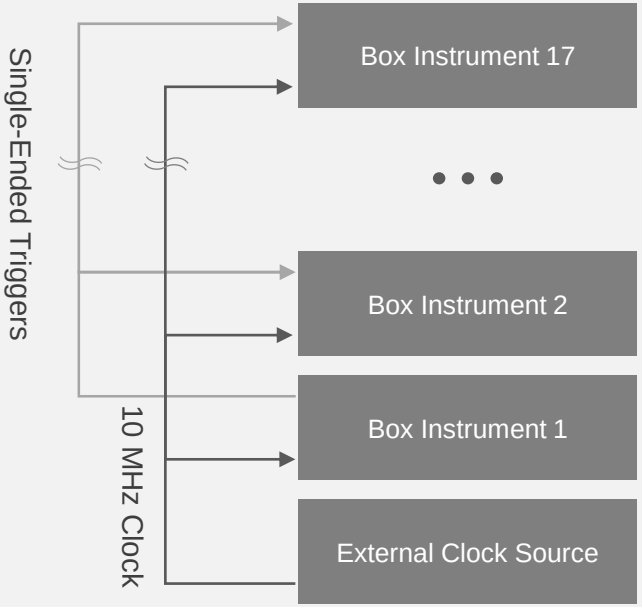
PXIe-1095

Industry's first chassis with 82 W of power and cooling in every slot

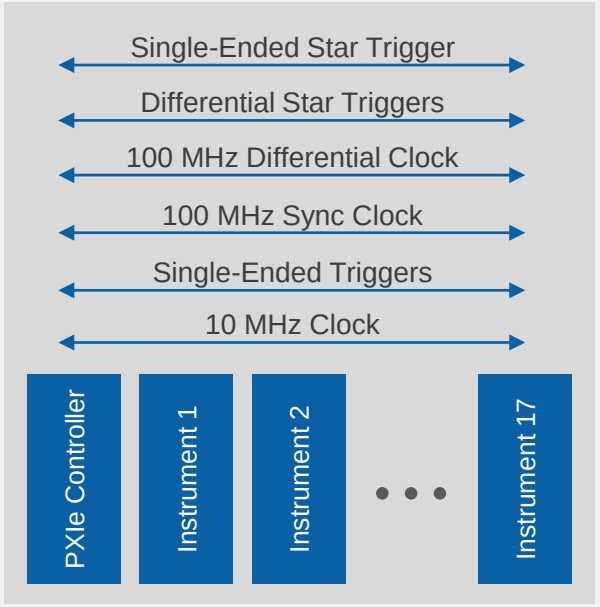
- 18-slot, 24 GB/s system bandwidth
  - 5 PXI Express hybrid slots, 12 PXI Express only (including one system timing slot)
- 2 hot-swappable, easily serviceable, 1,200 W power supplies
- 2 distinct, software-selectable cooling profiles
- Significant reduction in fan noise in 38 W profile
- Optional timing and synchronization upgrade
  - Built-in OCXO, external clock, and trigger routing

NATIONAL INSTRUMENTS

Advanced Timing and Synchronization With PXI



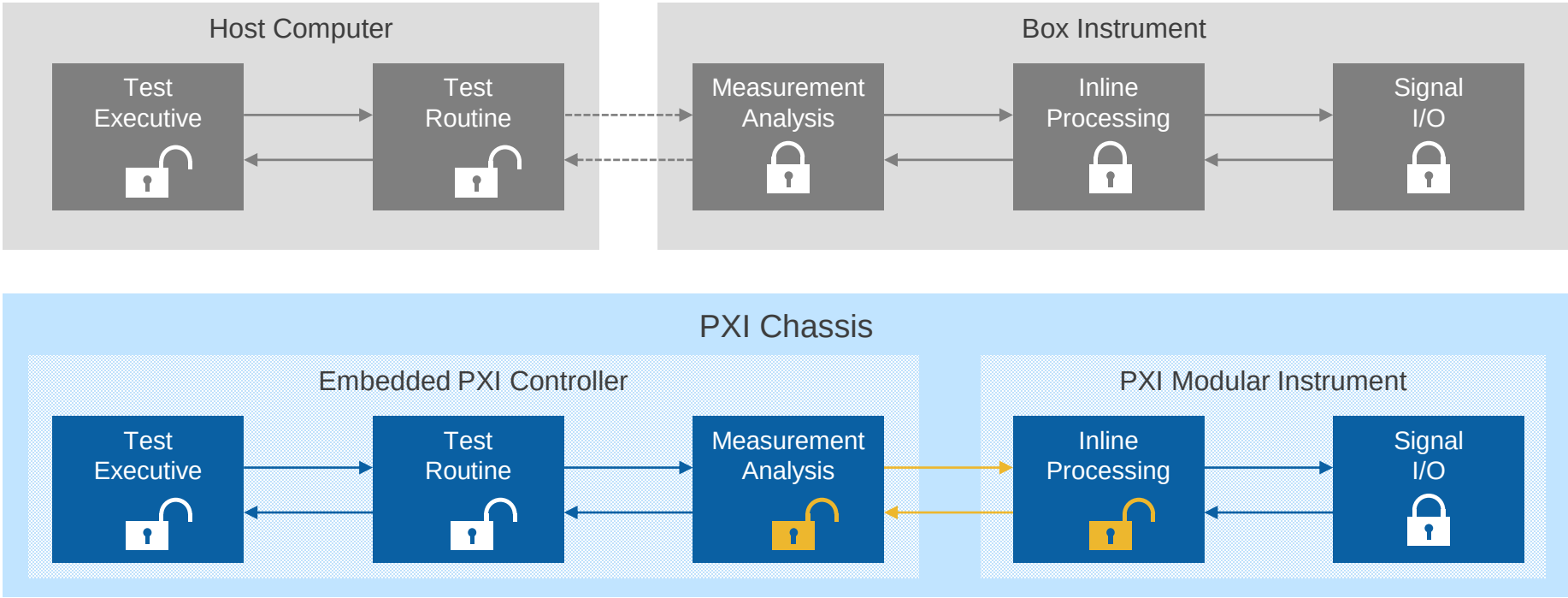
Box Instruments



PXI

NATIONAL INSTRUMENTS

Highest Flexibility With Software-Defined Instruments



NATIONAL INSTRUMENTS

Software-Designed Instruments

PXIe-5668
26.5 GHz, >765 MHz BW
RTBW vector signal analyzer

PXIe-5840
6 GHz VST with
1 GHz bandwidth

PXIe-5624
2 GS/s, 12-bit
IF digitizer

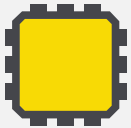
PXIe-6591/92
12.5 Gbps, 4–8 ch.
high-speed serial

PXIe-5170/71/72
250 MS/s, 14-bit, 4–8 ch.
oscilloscope

PXIe-7976
3.5 GB/s streaming
K410T K7 FlexRIO

"Fully functional instrument out of the box"

Customize functionality with



LabVIEW FPGA

NATIONAL INSTRUMENTS

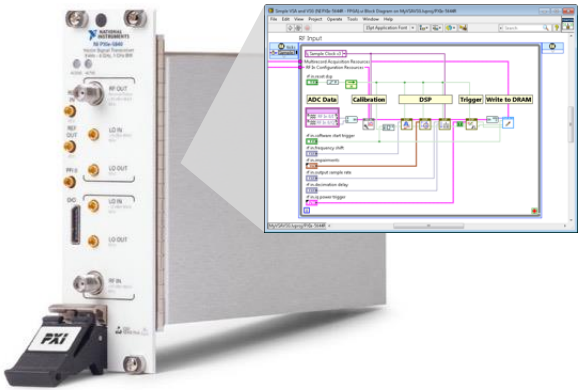
Second-Generation Vector Signal Transceiver

FEATURES AT A GLANCE

- User-programmable FPGA with LabVIEW
- 1 GHz of instantaneous bandwidth for advanced digital predistortion test and wideband signals
- Excellent accuracy enables measurement of 802.11ax error vector magnitude performance of -50 dB
- FPGA enables measurement speeds up to 10X faster than traditional instrumentation
- Small size and tight synchronization allow for up to 8x8 MIMO configuration in a single 18-slot chassis

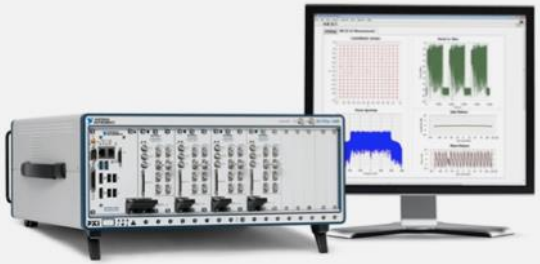
APPLICATION AREAS

- Wireless test
- Semiconductor test
- Automotive radar



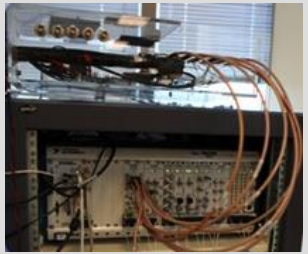
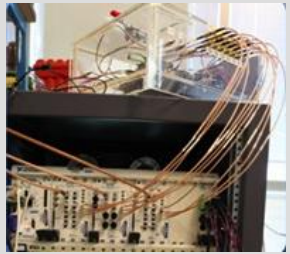
NATIONAL INSTRUMENTS

Qualcomm Reduces Test Times



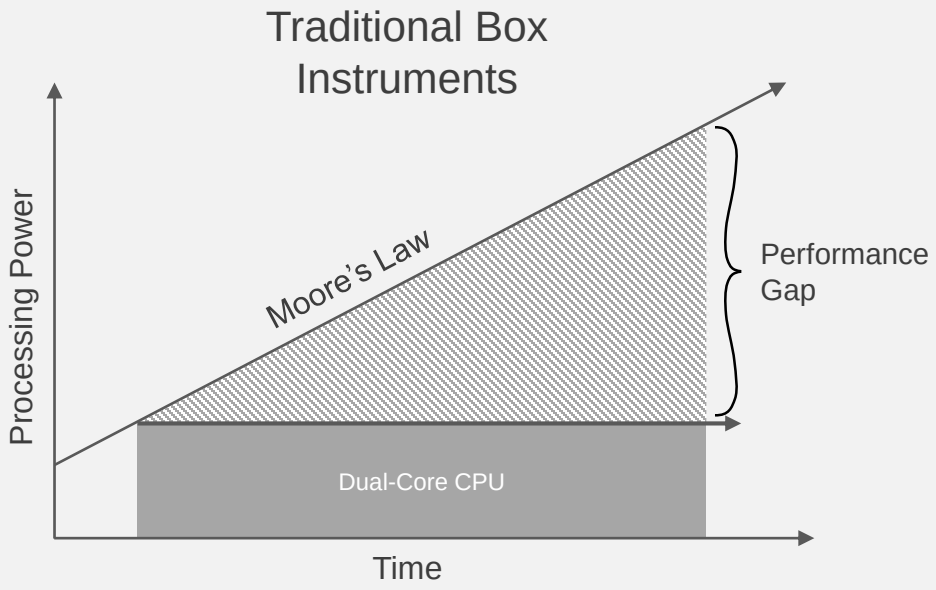
Qualcomm ATHEROS

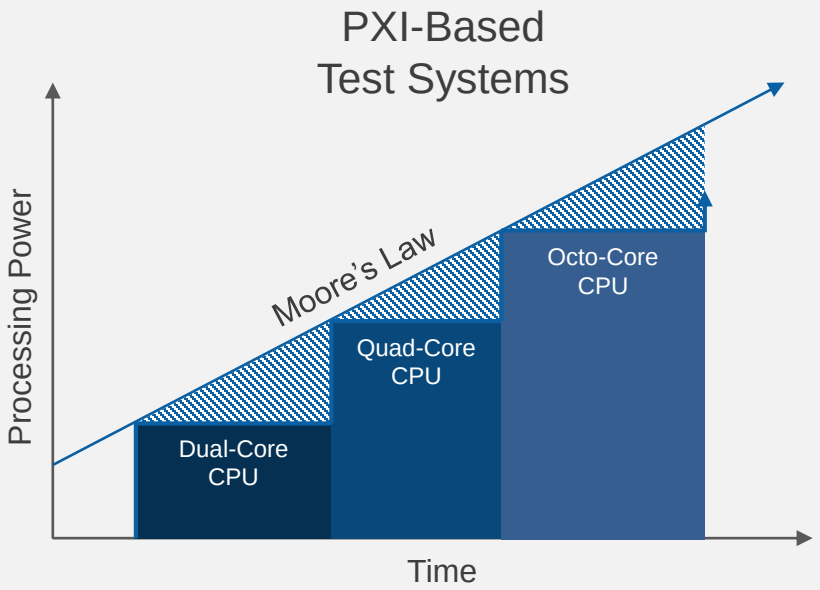
“We improved test speeds by more than 200X compared to traditional rack-and-stack instruments while significantly improving test coverage.”

	Previous	PXI Phase 1	PXI Phase 2
			
Technology	Traditional Box Instrumentation	NI PXI RF Instrumentation	NI Vector Signal Transceiver
Year	Early 2000s	2007	2012
Test Time Reduction	1X	10X	200X
WLAN Protocols Tested	802.11a 802.11b 802.11g	802.11a 802.11b 802.11g 802.11n	802.11a 802.11b 802.11g 802.11n 802.11ac

NATIONAL INSTRUMENTS

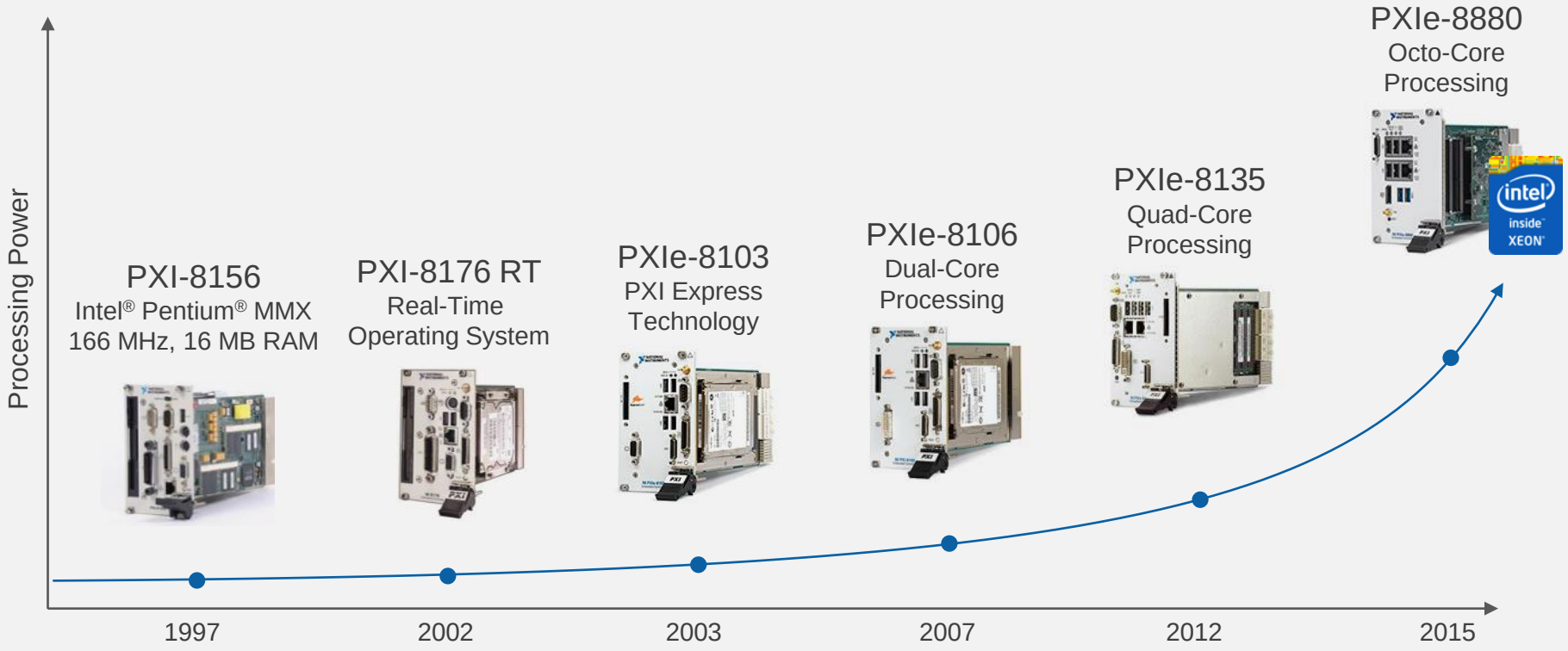
Reducing Test Times With Latest CPUs and FPGAs





NATIONAL INSTRUMENTS

Industry-Leading NI PXI Controller Portfolio



NATIONAL INSTRUMENTS

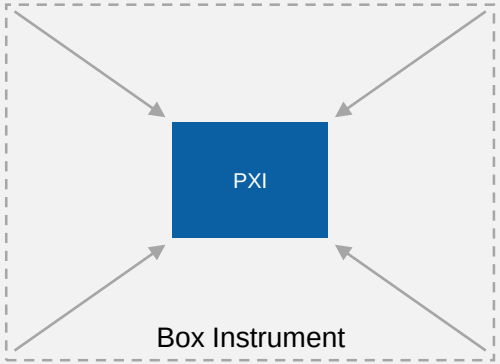
PXIe-8880 Embedded Controller

Embedded controller with Intel Xeon technology

- Intel® Xeon® E5-2618L v3 processor
- 2.3 GHz (base) and 3.4 GHz (Turbo Boost)
- 8 physical and 16 logical CPU cores
- 8 GB DDR4 1866 MHz RAM (standard); 24 GB max
- Up to 24 GB/s system bandwidth (each direction)
- 240 GB, 1.8 in. SSD hard drive
- Windows 7 64-bit or LabVIEW Real-Time OS
- PXI Express with PCI Express Gen 3 technology

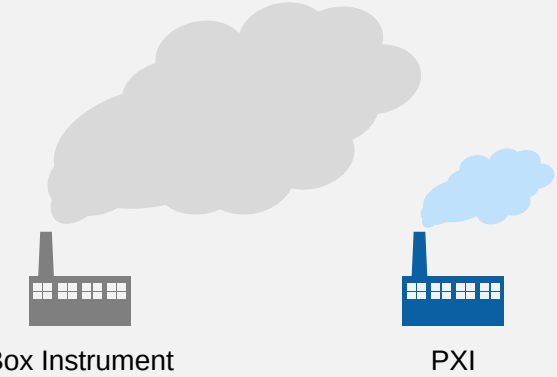
NATIONAL INSTRUMENTS

Reduced Overhead With PXI Form Factor



Size/Footprint

Weight/Portability



Power Consumption

NATIONAL INSTRUMENTS

Analog Devices Reduces MEMS Test Cost

ANALOG DEVICES

“Using PXI and LabVIEW, we were able to test our MEMS devices at a fraction of the cost, weight, power consumption, and footprint of our previous ATE system.”

	Previous ATE	PXI System	Reduction
Cost	$450k	$40k	11X
Footprint	277 ft^3	1.75 ft^3	158X
Weight	4000 lb	60 lb	66X
Energy	10 kW	0.6 kW	16X

NATIONAL INSTRUMENTS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16:30	**Finish**		

NATIONAL INSTRUMENTS

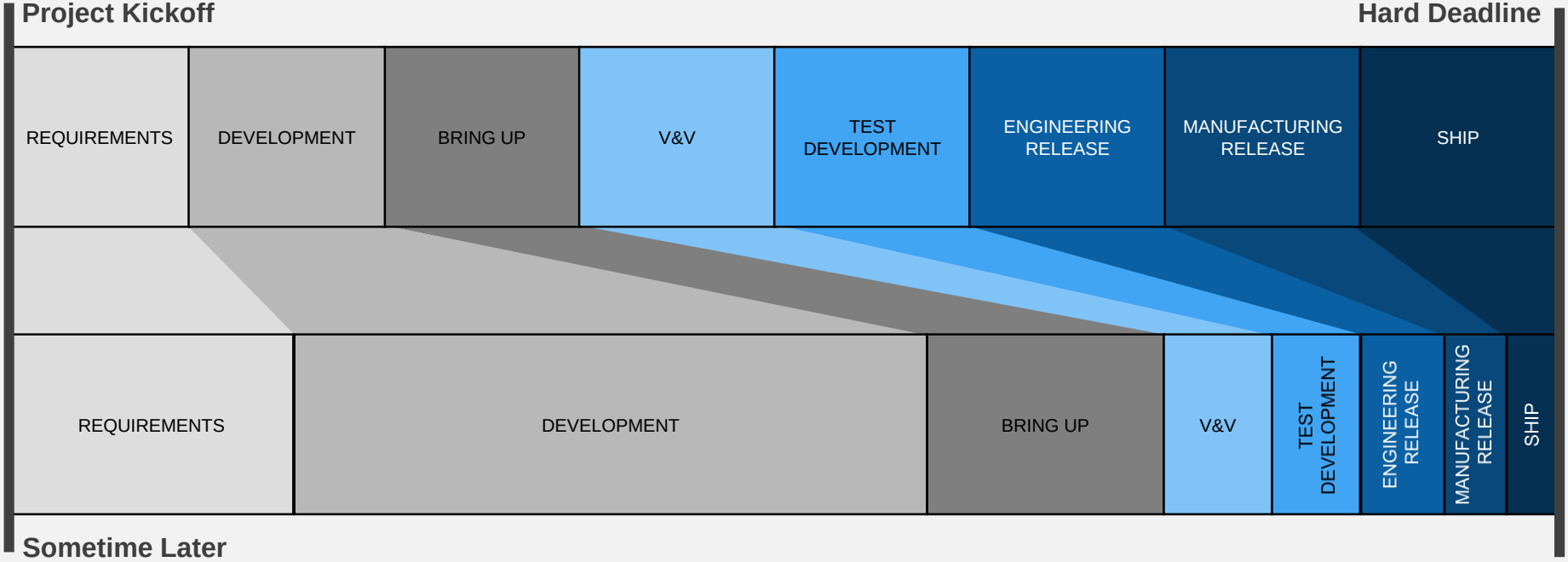
Using a Modular Platform for Mixed-Signal Semiconductor Characterization

Smarter Test From
Characterization to Production

George Tsalavoutis
Senior Applications Engineer, Automated Test
National Instruments

NATIONAL INSTRUMENTS

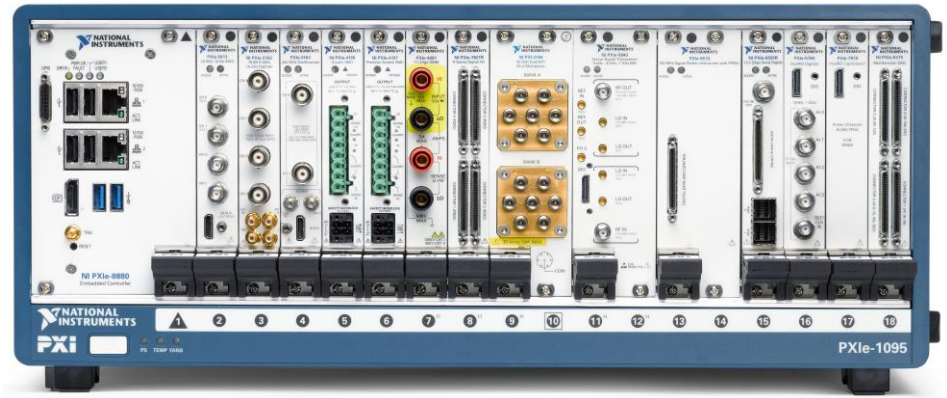
Does this ever happen to your projects?



NATIONAL INSTRUMENTS

Broad Modular Instrumentation Portfolio

DAQ and Control	Instrumentation	Interfaces
Multifunction I/O	Oscilloscopes	GPIB, USB, LAN
Counter/Timer/Clock	High-Speed Digital I/O	RS232/RS485
Digital I/O	DMM and SMU	CAN, LIN, DeviceNet
Analog Input/Output	Signal Generators	SCSI, Ethernet
Vision and Motion	Switching	VXI-VME
FPGA/Reconfigurable I/O	RF Analyzers and Generators	Boundary Scan/JTAG



NATIONAL INSTRUMENTS

PXI Instrumentation for Mixed-Signal IC Test

NI Source Measure Units (SMUs)

- Broad IV range up to 200 V and 3 A (20 W DC)
- Pulse up to 10 A (500 W)
- Current resolution to 10 fA
- Max sampling to 1.8 MS/s
- NI SourceAdapt technology for fast settling in presence of capacitive loads
- Best-in-class channel density

NI Digital Pattern Instrument

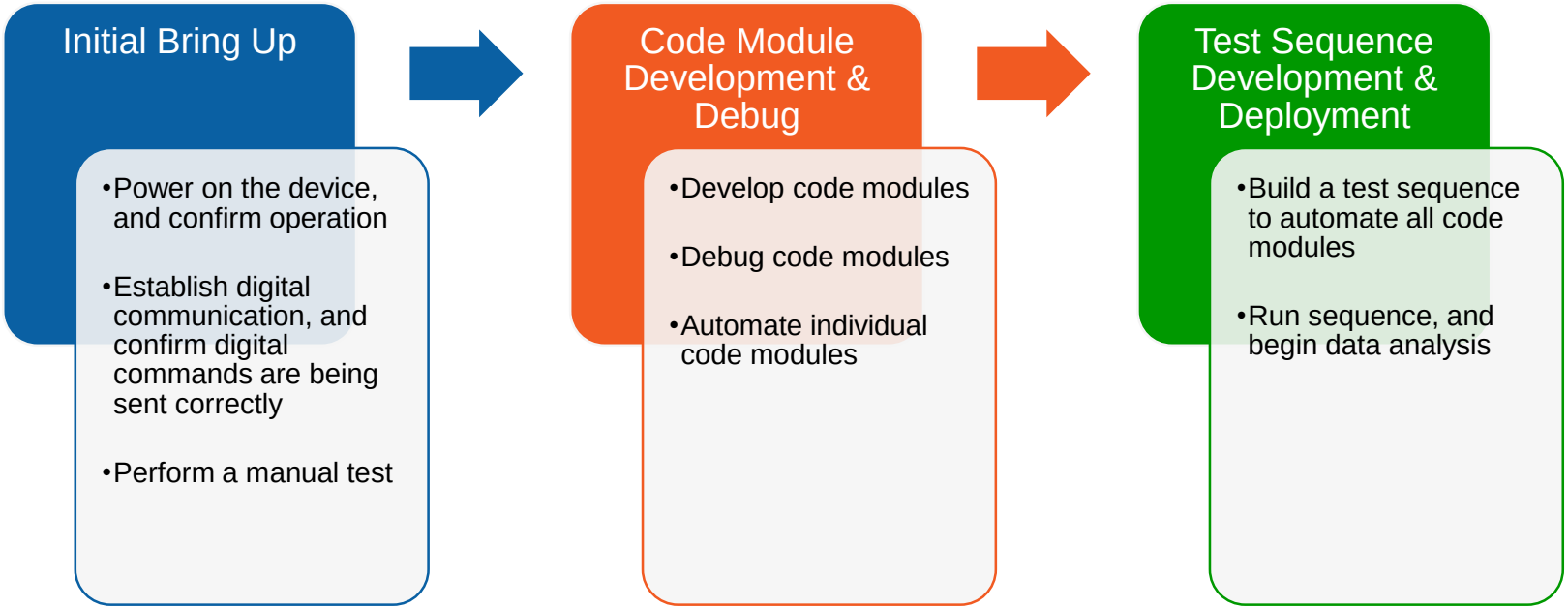
- ATE-class digital (with PPMU) in PXI
- Out-of-the-box Digital Pattern Editor software for configuration, interactive tests, and debugging
- Time sets, drive formats, opcodes, source and capture, history RAM, Shmoo

Other Instrumentation

- General-purpose analog and digital I/O for AC measurements and peripheral control
- General-purpose power supplies for peripherals
- Arbitrary waveform generators and oscilloscopes

NATIONAL INSTRUMENTS

Demo Workflow



Demo Workflow

InstrumentStudio

Power on Device, Confirm Operation

Confirm Commands From Digital Instrument

Perform Manual Test

Debug Test Code

Digital Pattern Editor

Establish DUT Communication

LabVIEW

Develop Test Code

Automate Single Test

NI TestStand

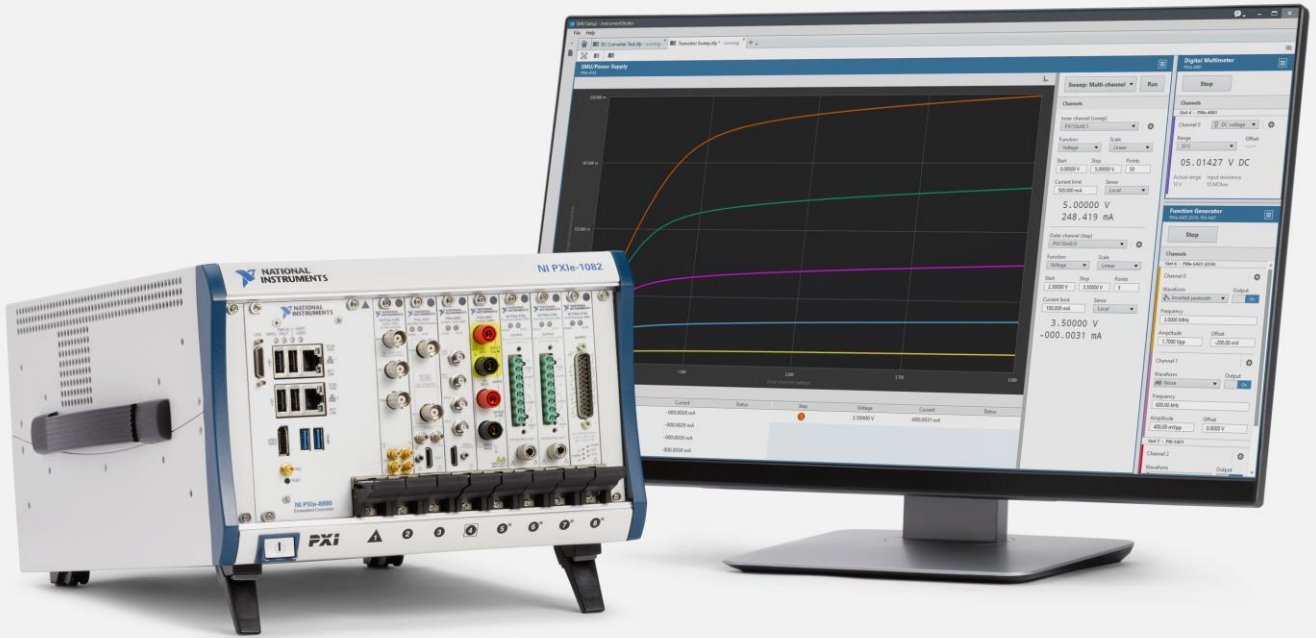
Build Sequence

Run Sequence and Begin Analysis

NATIONAL INSTRUMENTS

What is InstrumentStudio and why is it relevant to me?

It is all about adding an Integrated UI to the PXI Platform



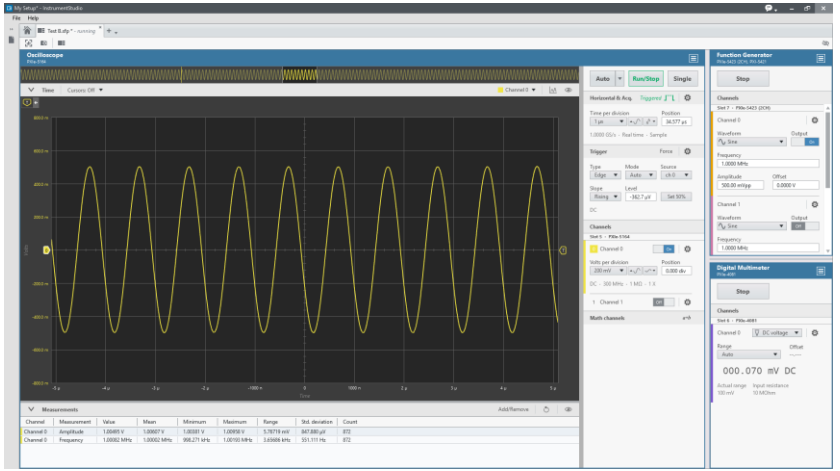
NATIONAL INSTRUMENTS

InstrumentStudio™

Oscilloscopes, AWGs and FGens, DMMs, SMUs, and Power Supplies

Enhanced interactive use

- Familiar but modern UI and UX with common functionality across instrument types
- Multi-instrument tabbed interface
  - Multidevice channel expansion within an SFP
  - One or many instruments per tab
  - Multiple tabs and multiple screens per instance
- Export data and screenshots
  - PNG, TDMS, clipboard
- Save UI configuration and share across systems



Streamlined transition from interactive to automated measurements

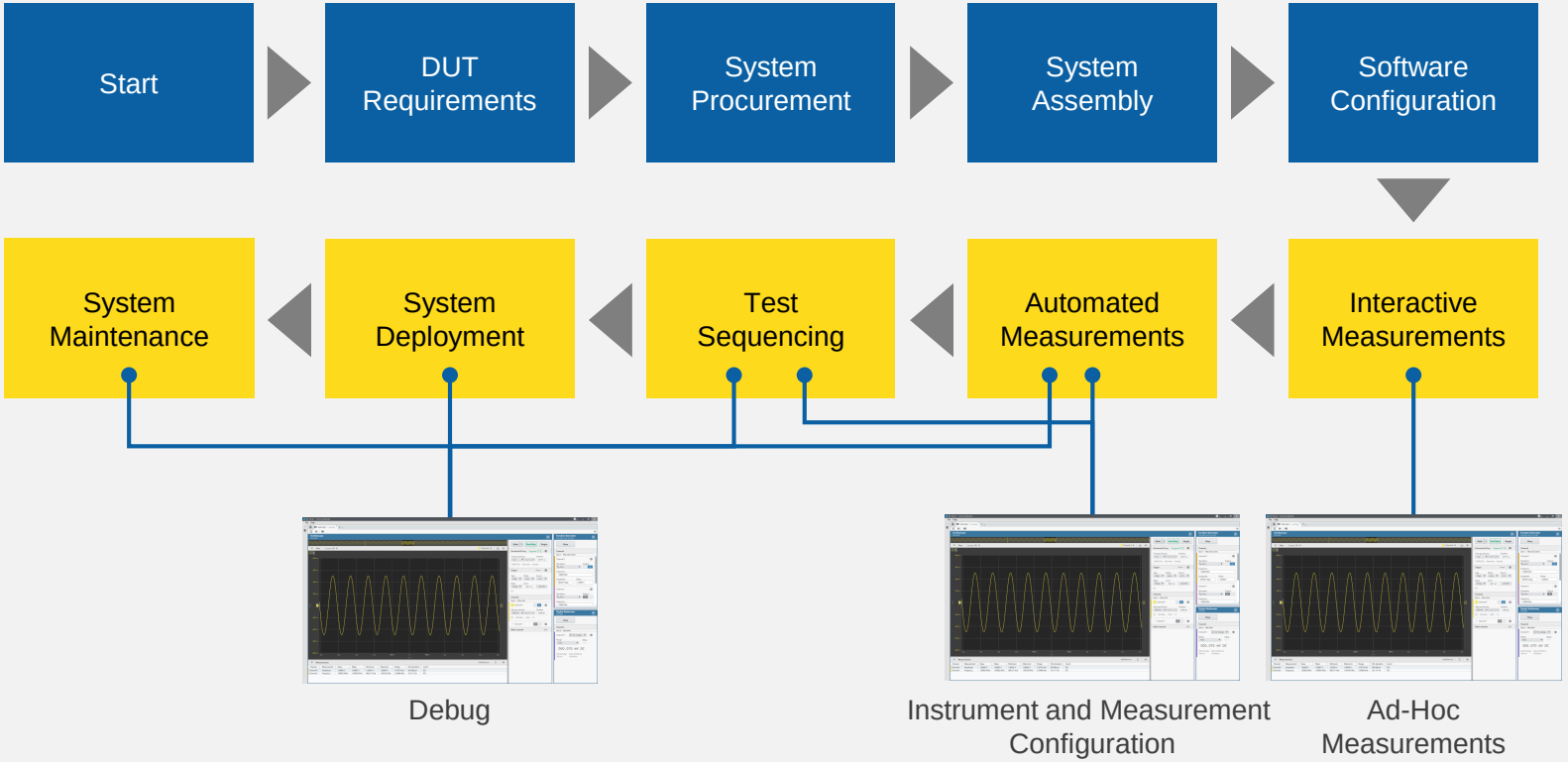
- Export instrument configuration for programmatic use

Simplified automated test system debug

- Debug driver session—monitor and control

NATIONAL INSTRUMENTS™

Interactive Measurements in an Automated Workflow



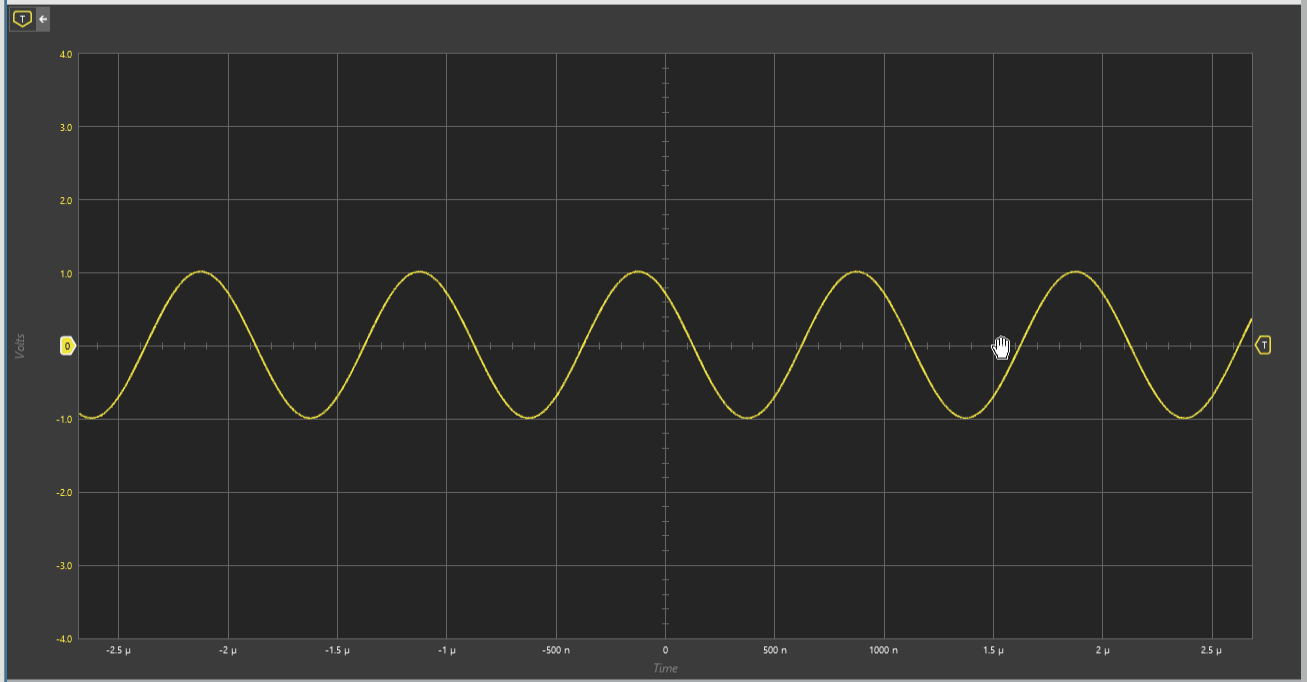
Untitled Project* - InstrumentStudio

File Help

Instrument.sfp * - running

Oscilloscope
PXIe-5164

Time | Cursors: Off | Channel 0



Measurements | Add/Remove

Channel	Measurement	Value	Mean	Minimum	Maximum	Range	Std. deviation	Count
Channel 0	Amplitude	2.01584 V	2.01501 V	2.01167 V	2.02019 V	8.52017 mV	1.49861 mV	87
Channel 0	Frequency	1.00018 MHz	999.947 kHz	998.943 kHz	1.00086 MHz	1.91638 kHz	399.002 Hz	87

Auto | Run/Stop | Single

Horizontal & Acq. Triggered

Time per division: 500 ns | Position: 28.376 µs

1.0000 GS/s · Real time · Sample

Trigger Force

Type: Edge | Mode: Auto | Source: ch 0

Slope: Rising | Level: 16.61 mV | Set 50%

DC

Channels

Slot 5 · PXIe-5164

Channel 0 — On

Volts per division: 1 V | Position: 0.000 div

DC · 300 MHz · 1 MΩ · 1 X

1 Channel 1 — Off

Math channels *a+b*

Function Generator
PXIe-5423 (2CH), PXI-5421

Stop

Channels

Slot 7 · PXIe-5423 (2CH)

Channel 0

Waveform: Sine | Output: On

Frequency: 1.0000 MHz

Amplitude: 1.0000 Vpp | Offset: 0.0000 V

Channel 1

Waveform: Sine | Output: Off

Frequency: 1.0000 MHz

Digital Multimeter
PXIe-4081

Stop

Channels

Slot 6 · PXIe-4081

Channel 0 — DC voltage

Range: Auto | Offset: --.---

000.065 mV DC

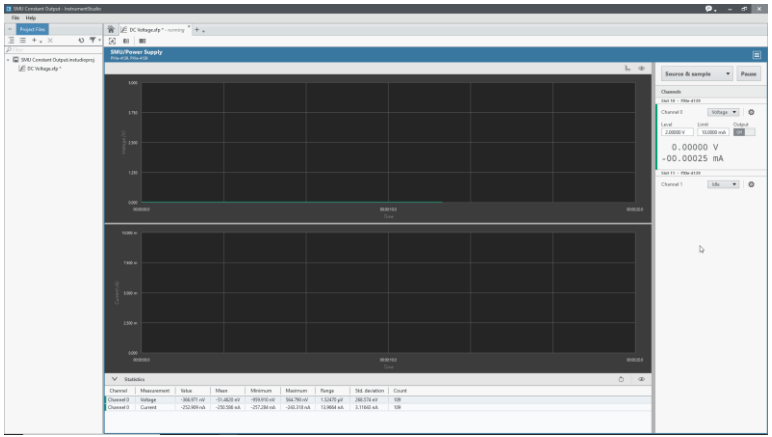
Actual range: 100 mV | Input resistance: 10 MOhm

InstrumentStudio™

Oscilloscopes, AWGs and FGens, DMMs, SMUs, and Power Supplies

Enhanced interactive use

- Familiar but modern UI and UX with common functionality across instrument types
- Multi-instrument tabbed interface
  - Multidevice channel expansion within an SFP
  - One or many instruments per tab
  - Multiple tabs and multiple screens per instance
- Export data and screenshots
  - PNG, TDMS, clipboard
- Save UI configuration and share across systems



Streamlined transition from interactive to automated measurements

- **Export instrument configuration for programmatic use**

Simplified automated test system debug

- Debug driver session—monitor and control

NATIONAL INSTRUMENTS™

SMU Constant Output - InstrumentStudio

File Help

Project Files

Filter

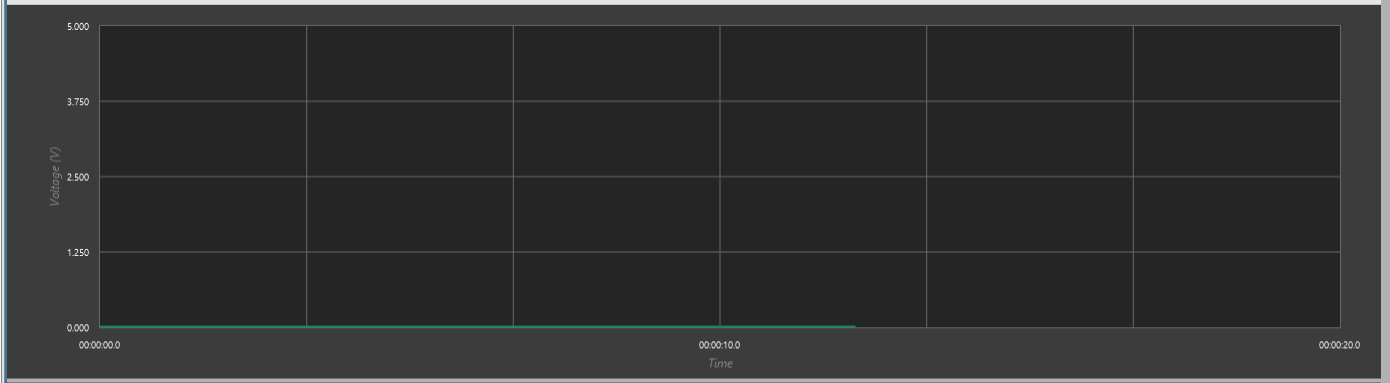
SMU Constant Output.instudioproj

DC Voltage.sfp *

DC Voltage.sfp * - running

SMU/Power Supply

PXIe-4139, PXIe-4139



Source & sample

Pause

Channels

Slot 10 · PXIe-4139

Channel 0 Voltage

Level 2.00000 V

Limit 10.0000 mA

Output Off

0.00000 V

-00.00025 mA

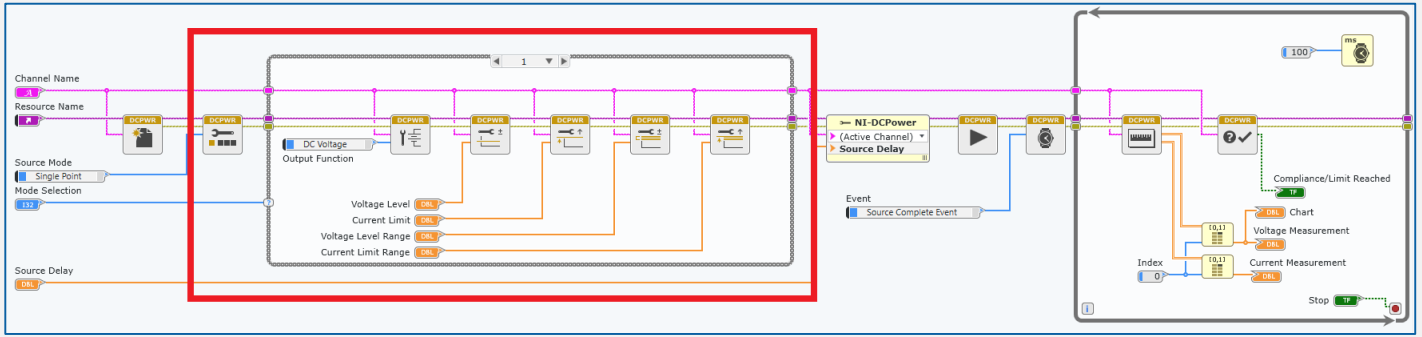
Slot 11 · PXIe-4139

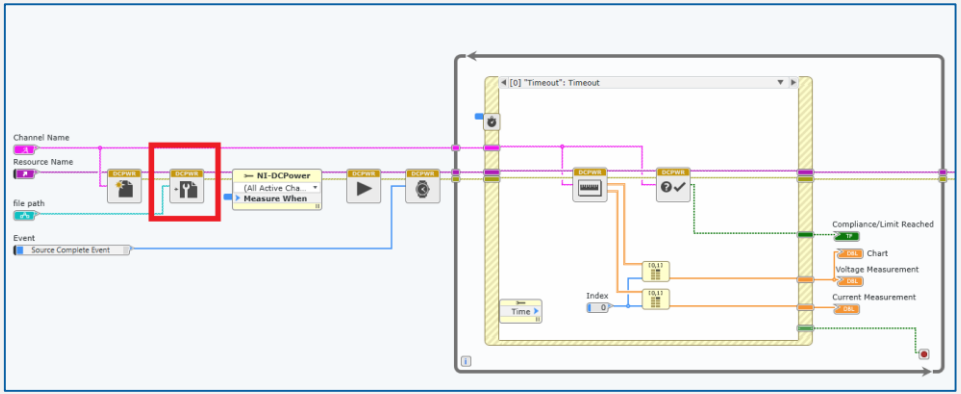
Channel 1 Idle

Statistics

Channel	Measurement	Value	Mean	Minimum	Maximum	Range	Std. deviation	Count
Channel 0	Voltage	-366.971 nV	-51.4620 nV	-959.910 nV	564.790 nV	1.52470 µV	268.574 nV	109
Channel 0	Current	-252.909 nA	-250.586 nA	-257.284 nA	-243.318 nA	13.9664 nA	3.11643 nA	109

Simplifying Your Code





NATIONAL INSTRUMENTS

NI-DCPower: Source and Sample Mode

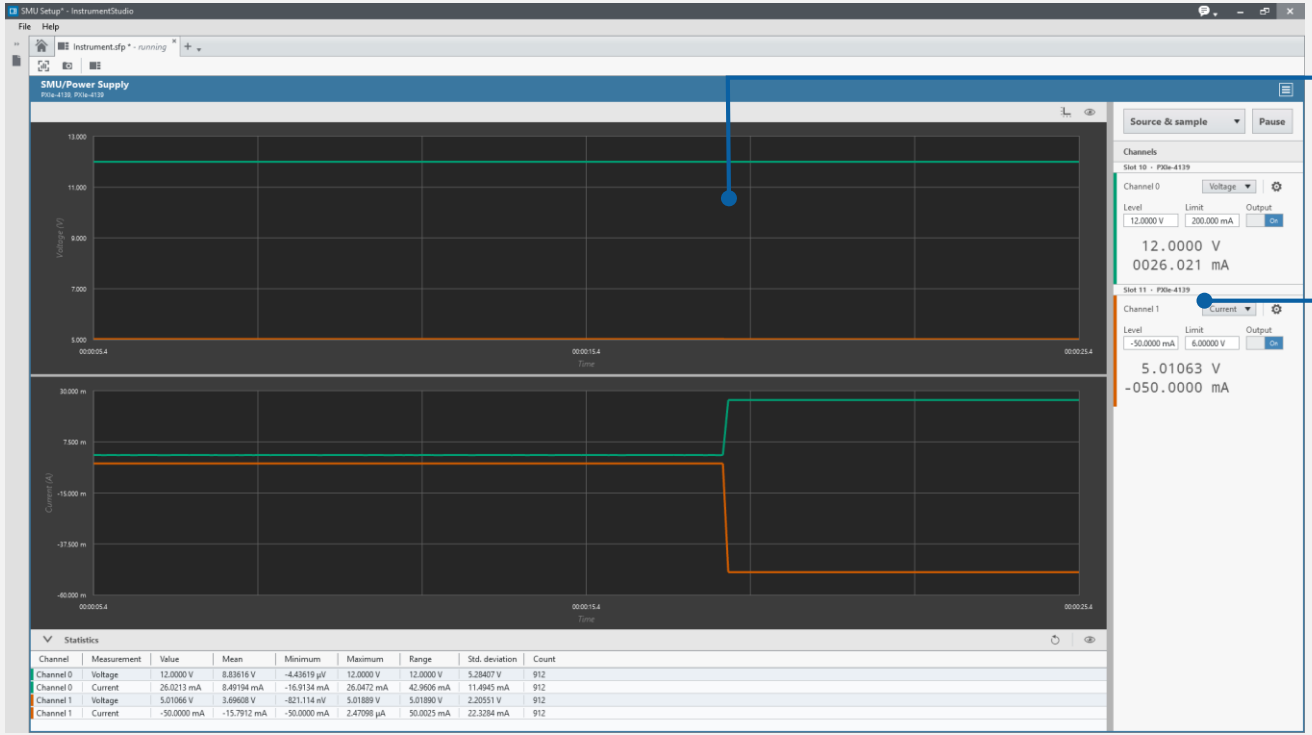
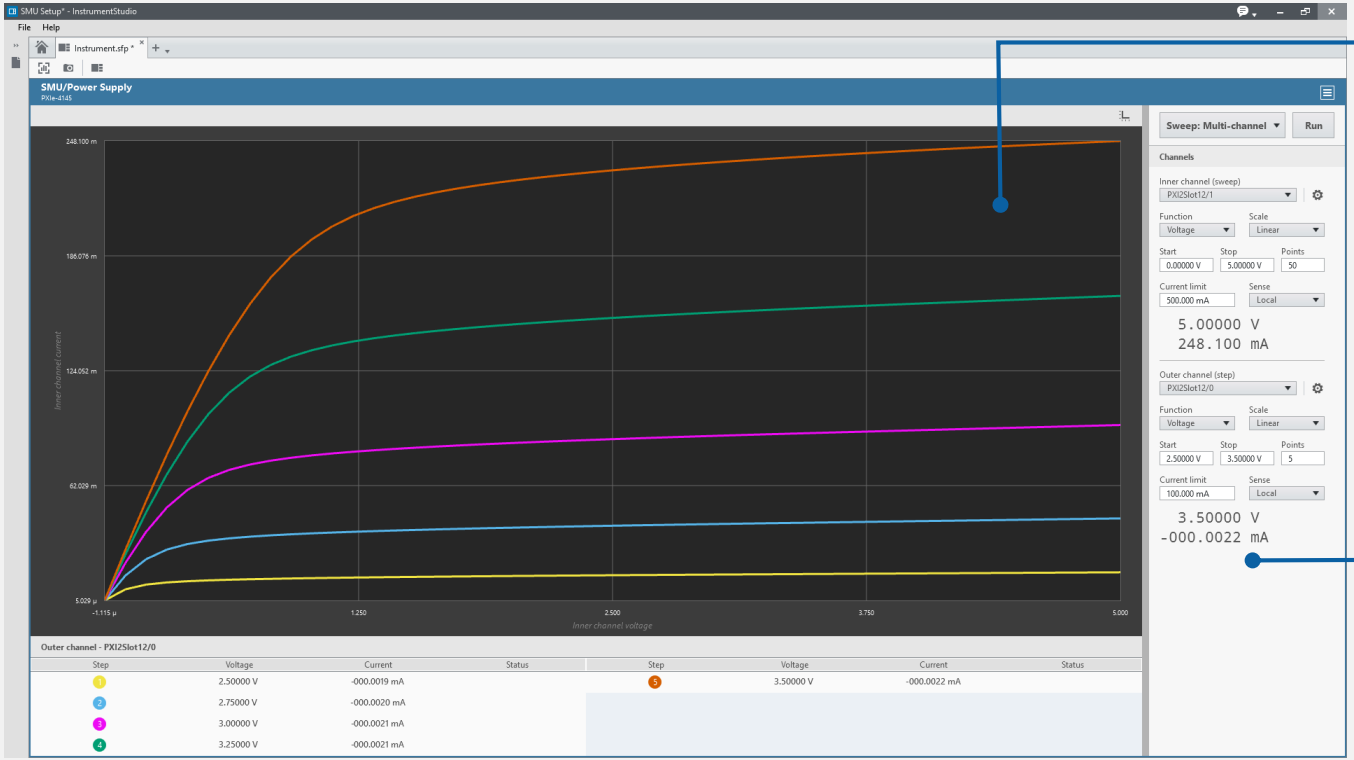


Chart voltage and current over time

Manage multiple devices in a single window

NATIONAL INSTRUMENTS

NI-DCPower: Sweep Mode



Run 1- or 2-channel sweeps

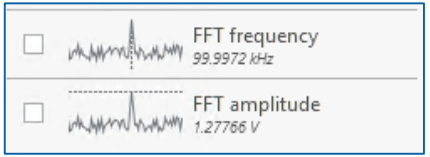
Access advanced timing and measurement settings

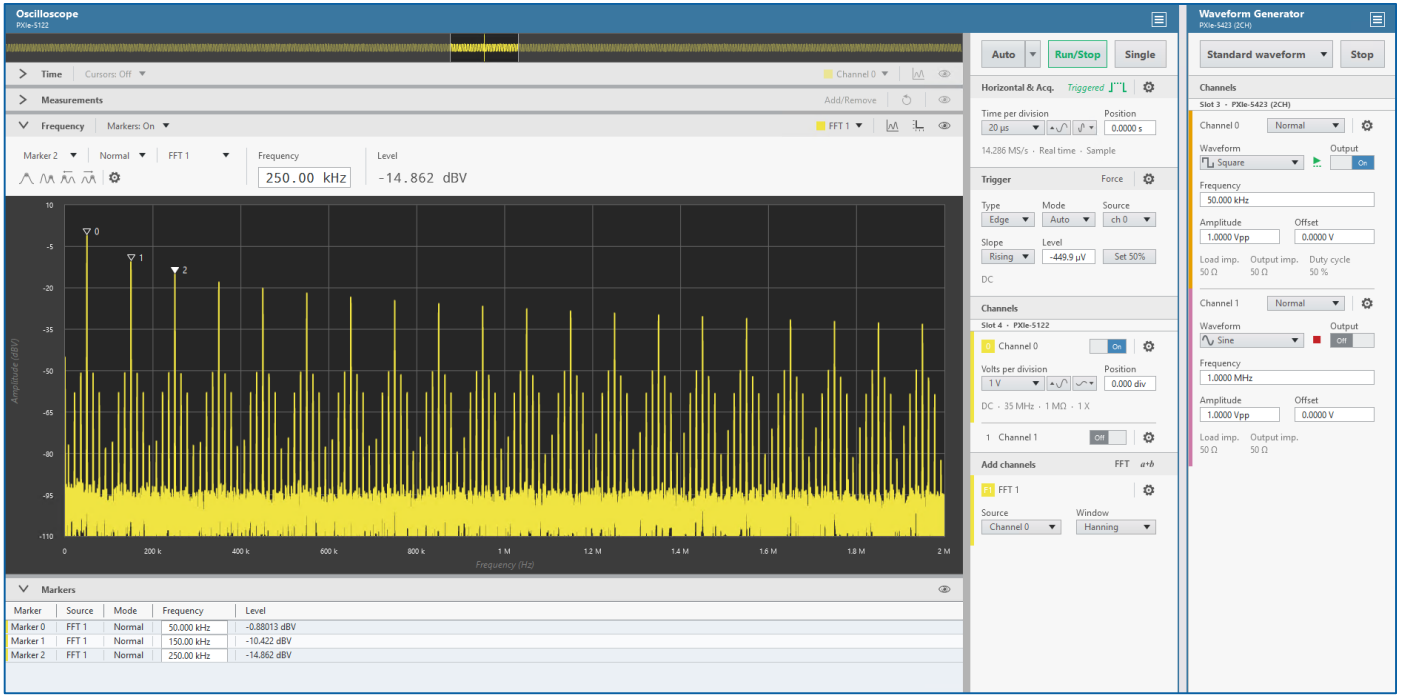
NATIONAL INSTRUMENTS

Recent Updates & Improvements

Oscilloscope Panel: FFT Channels

Plus frequency markers, peak search, and FFT measurements

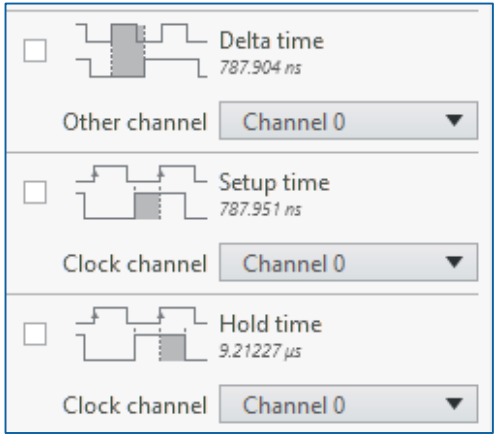


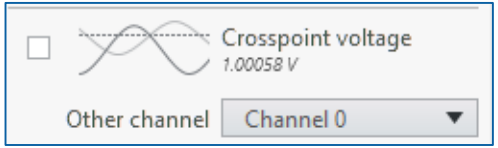


NATIONAL INSTRUMENTS

Oscilloscope Panel: Two-Channel Measurements

- Specify “other channel” to measure against primary channel
- Delta time, setup time, hold time, and crosspoint voltage

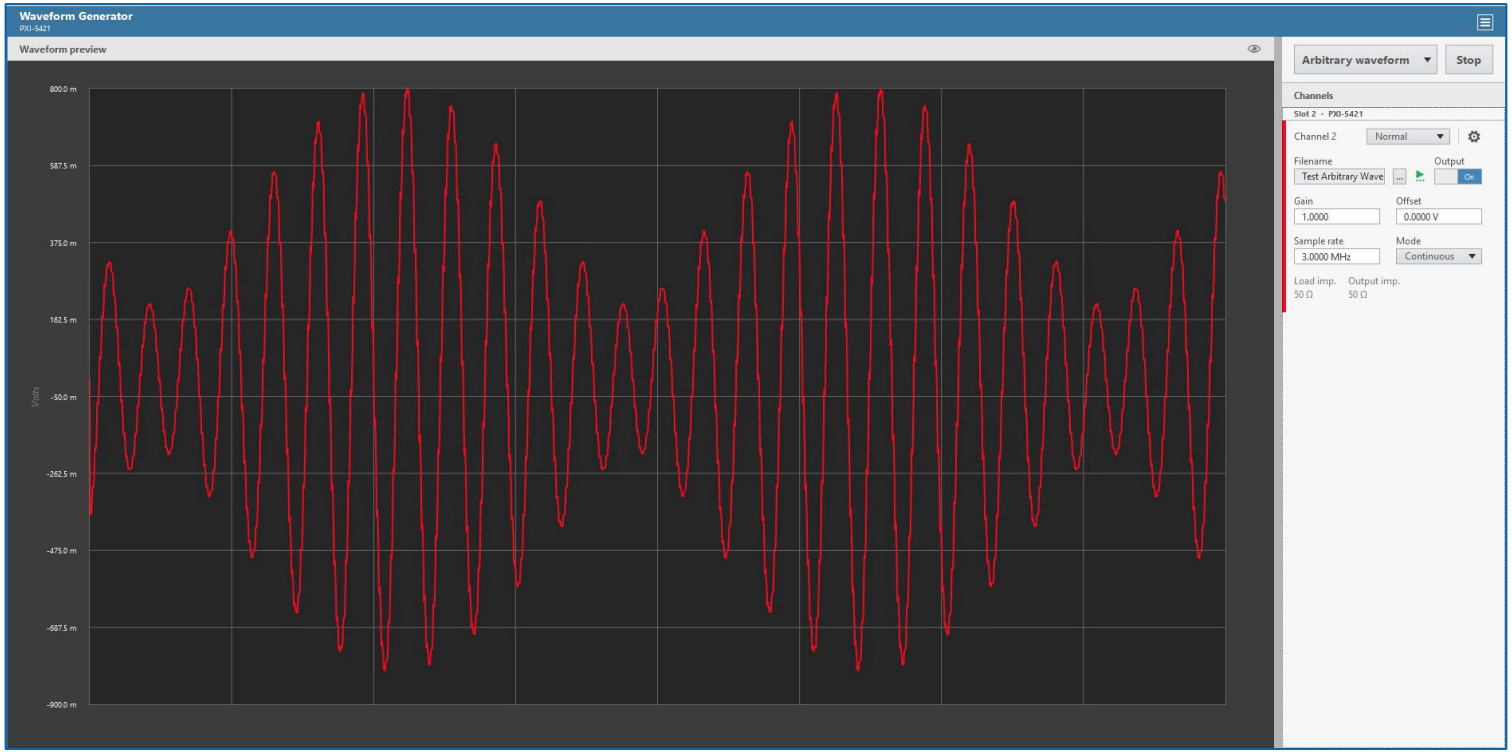




NATIONAL INSTRUMENTS

Waveform Generator Panel: Arbitrary Waveform Mode

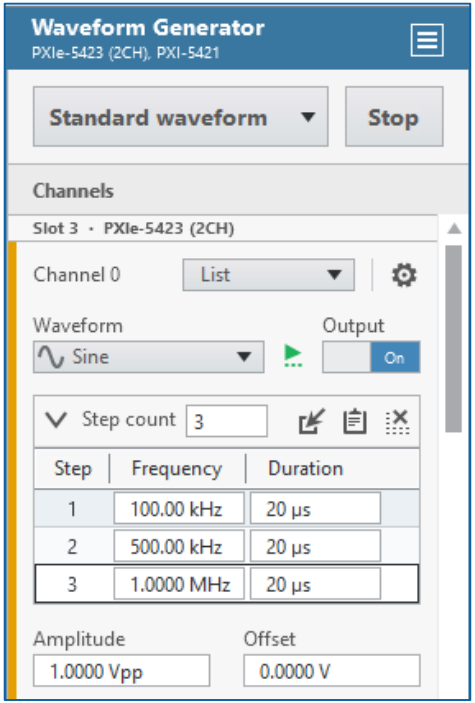
See a preview in the large panel view

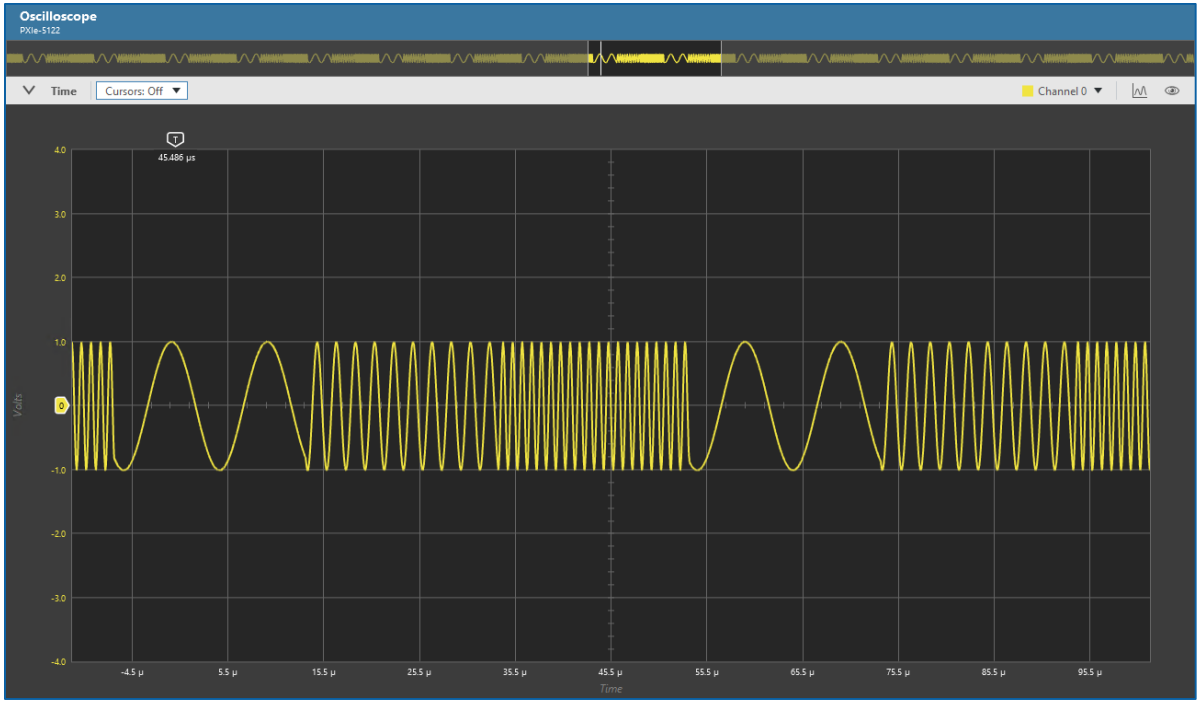


NATIONAL INSTRUMENTS

Waveform Generator Panel: List Mode

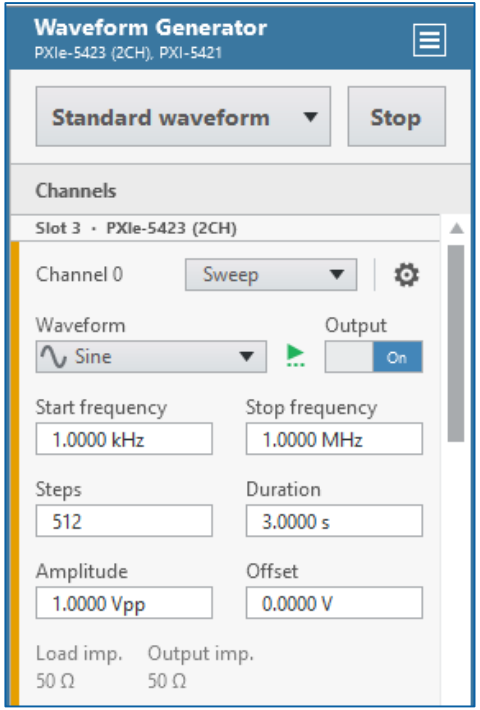
Specify a list manually or from file

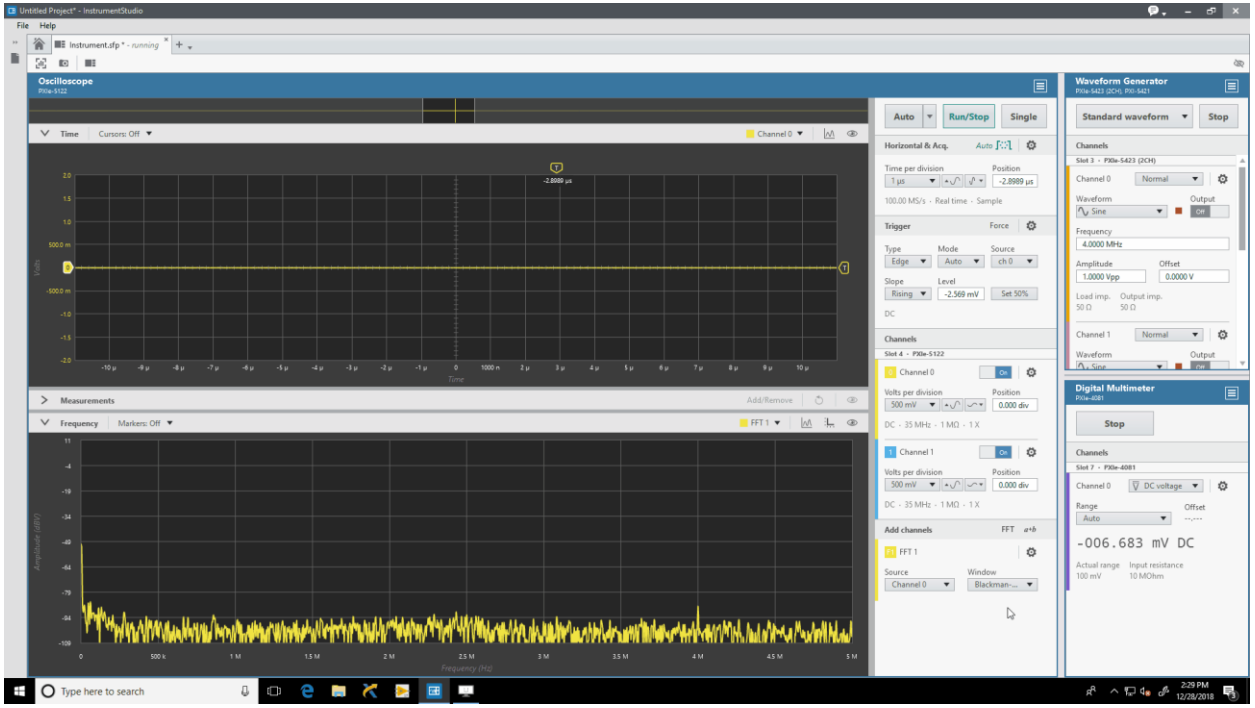




Waveform Generator Panel: Sweep Mode

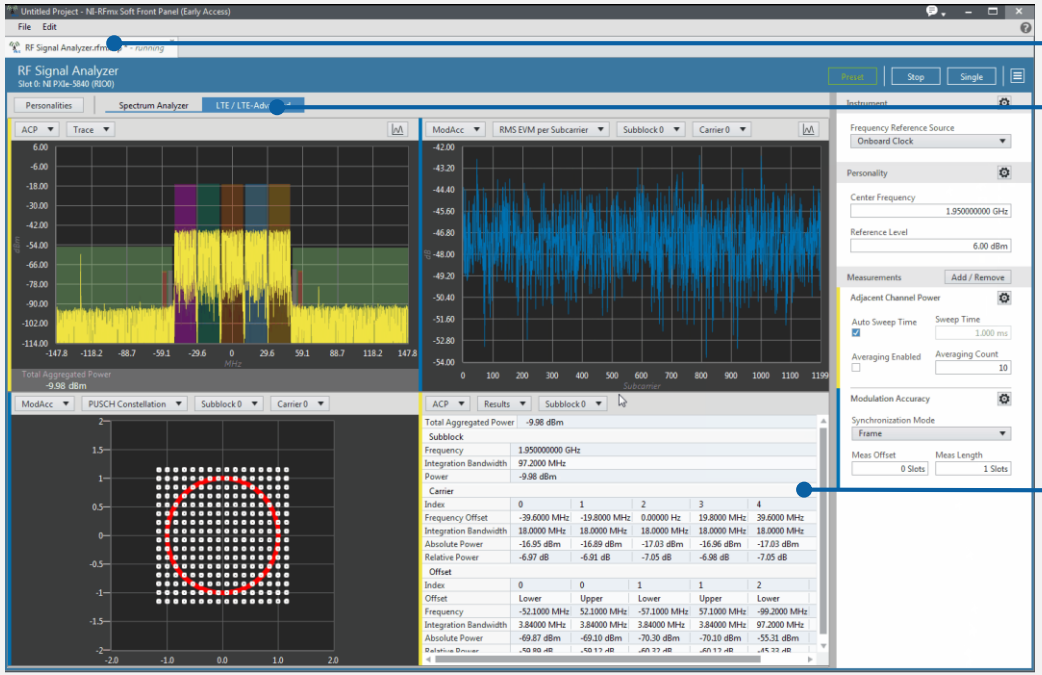
Animation: FGEN Sweep + Scope FFT





NI-RFmx Soft Front Panel: SpecAn and LTE/LTE-A

Similar interactive software for RF instrumentation



Multiple instances/tabs

Multiple personalities/standards

Multiple measurements and traces

NATIONAL INSTRUMENTS

Demo Workflow

InstrumentStudio

Power on Device, Confirm Operation

Confirm Commands From Digital Instrument

Perform Manual Test

Debug Test Code

Digital Pattern Editor

Establish DUT Communication

LabVIEW

Develop Test Code

Automate Single Test

NI TestStand

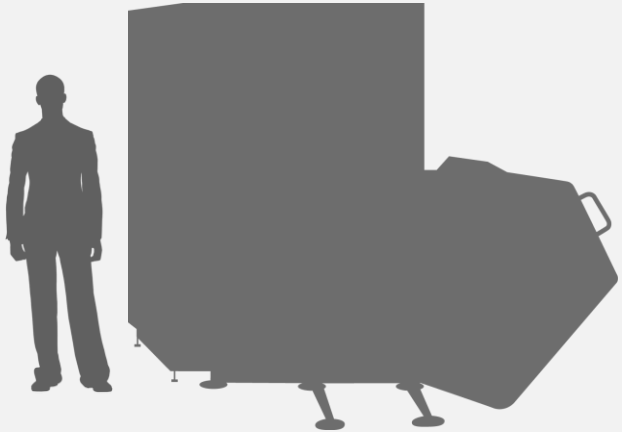
Build Sequence

Run Sequence and Begin Analysis

NATIONAL INSTRUMENTS

ATE Not Designed to Serve Validation

- Too expensive
- Custom cooling
- High-power connections
- Designated space in labs
- I/O options are fixed and aging
- Renting ATE from other groups
- Trying to partner overseas to use production ATE
- Lack of ATE availability limits test productivity



NATIONAL INSTRUMENTS

Lab Test System

ATE

Scalable ATE-Class Digital

Modular hardware

Timing and DC parametric measurements

ATE digital patterns

Production test speed

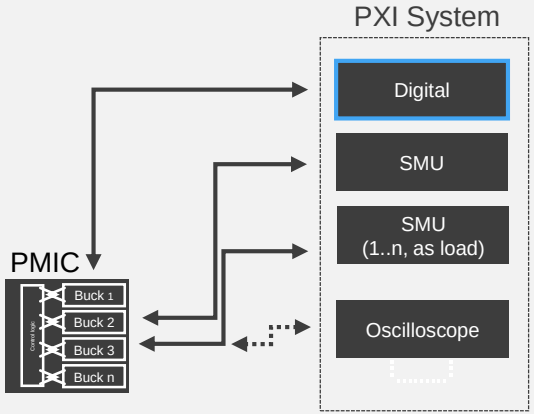
NATIONAL INSTRUMENTS

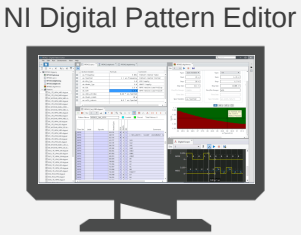
Digital: Consistent Terminology With ATE

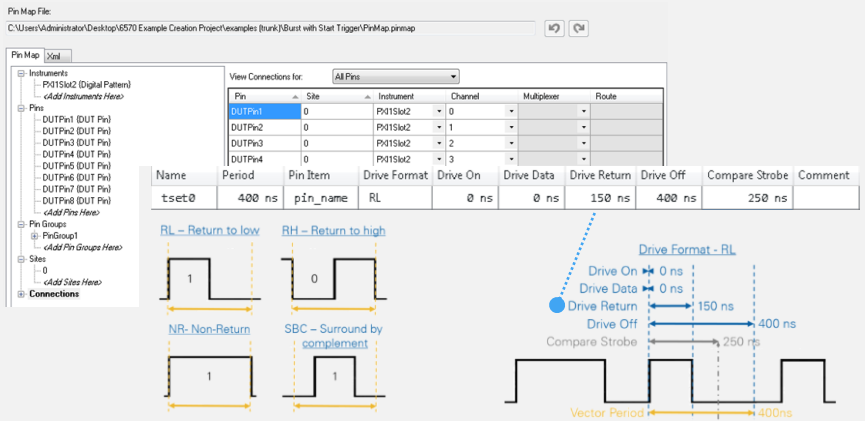
- DUT-centric programming by pin
- Time sets with cycle-to-cycle edge placement and drive formats
- Pin electronics for edge placement and IV measurements

Why it matters

- Paradigm consistency paves the way for reuse (patterns, code modules) and easier correlation with production ATEs







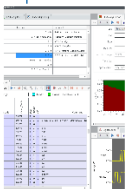
NATIONAL INSTRUMENTS

PXI Digital Pattern Instruments

PXIe-6570 and PXIe-6571

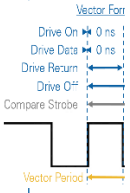
Built for Semiconductor Device Test

- RFICs and Transceivers
- Power Management ICs
- MEMS
- IoT Devices with Integrated MCUs and Sensors



ATE Development and Debug Features

- Digital Pattern Editor
- Source and Capture Memory
- History RAM, Digital Scope, Pin View, and System View
- Shmoo Plots



ATE Test Capability

- Time Sets and Edge Placement
- Opcodes
- Multi-site Support
- Integrated Per-Channel PPMU
- Up to 512 Synchronized Channels

NATIONAL INSTRUMENTS

PXI Digital Pattern Instruments: PXIe-6570 and PXIe-6571

	PXIe-6570	PXIe-6571*
Module Width	2 slots	1 slot
Active Load	24 mA	16 mA
Pin Electronics	Digital: -2 V to +6 V, 32 mA PPMU measure voltage: -2 V to +6 V, 32 mA PPMU force voltage: -2 V to +7 V, 32 mA	
Channels	32 per module	
	256 maximum in a synchronized subsystem	512 maximum in a synchronized subsystem
Maximum Vector Rate	100 MHz (10 ns minimum vector period)	
Maximum Data Rate	200 Mb/s	
Maximum Clock Rate	160 MHz**	
Pattern Timing	31 time sets 39.0625 ps edge placement resolution	
Drive Formats	Non-return (NR), return to low (RL), return to high (RH) (100 MHz max), surround by complement (SBC) (50 MHz max)	
Vector Memory Depth	128 M/channel	
Opcode Support	Flow control, sequencer flags and registers, signal, source and capture, subroutine	
Source and Capture Engines	Broadcast or site-unique Serial or parallel 8 per instrument	
SCAN Support	Flattened SCAN patterns, up to 128 M	

* Note that the PXIe-6571 requires a chassis with 82 W slot cooling capacity, such as the PXIe-1095. In STS, this requires the high-density test head revision.
** Clock rates >133 MHz will have a non-50% duty cycle.

NATIONAL INSTRUMENTS

A Modular Approach to Digital Test

Synchronized PXI Instruments

- Subnanosecond synchronization with other PXI modules
- Full suite of instruments from DC to mmWave

PXIe-8880 Controller

- Intel Xeon 8-core processor (2.3 GHz)
- 24 GB/s system bandwidth
- Up to 24 GB DDR4 1866 MHz RAM
- Gen 3 PCI Express technology

PXIe-6571 Digital Pattern Instrument

- 32 channels per module
- Up to 512 synchronized channels in digital subsystem
- 31 time sets
- 100 MHz vector rate
- 128 M vector memory

PXIe-1095 Chassis

- 18 PXI Express slots
- Up to 24 GB/s system bandwidth
- 82 W slot cooling capacity
- Peer-to-peer data streaming
- Gen 3 PCI Express technology

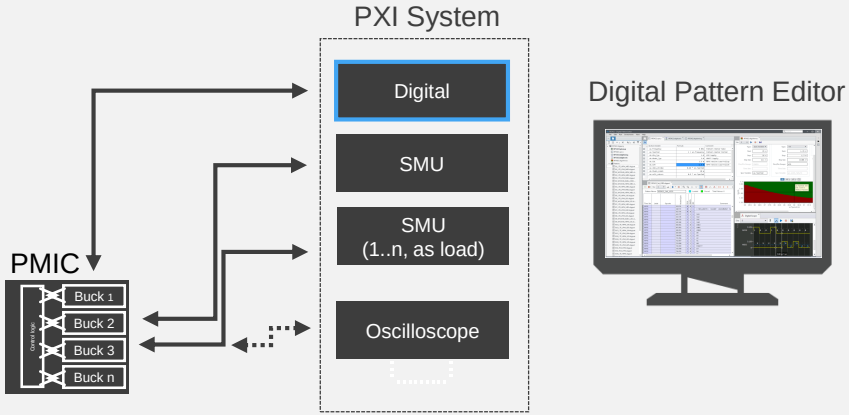
NATIONAL INSTRUMENTS

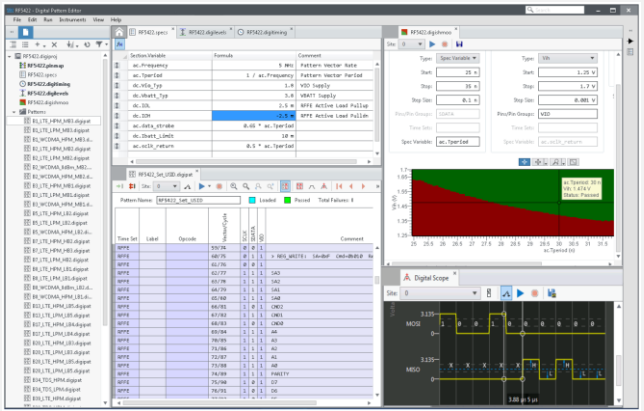
Digital: Pattern Editor Software

- Create, edit, and import digital test patterns
- Debug tools like History RAM and Digital Scope
- Shmoo plotting for margining and characterization

Why it matters

- Out-of-the-box functionality to import/create, debug, and burst patterns
- Go from configuration to test faster with out-of-the-box application software





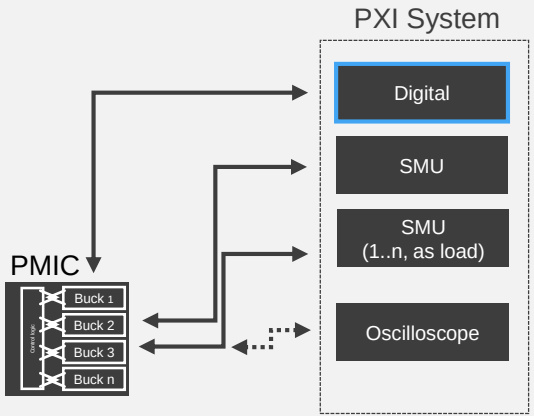
NATIONAL INSTRUMENTS

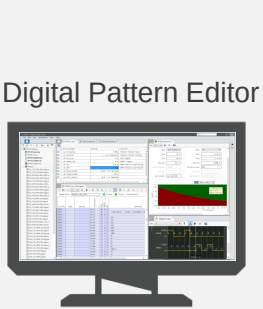
Digital: Test System Integration

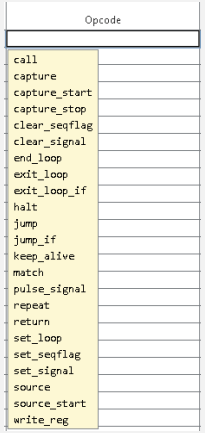
- Logical operations within patterns like looping, jumping, and matching
- Multimodule, cross-module, and cross-instrument operations

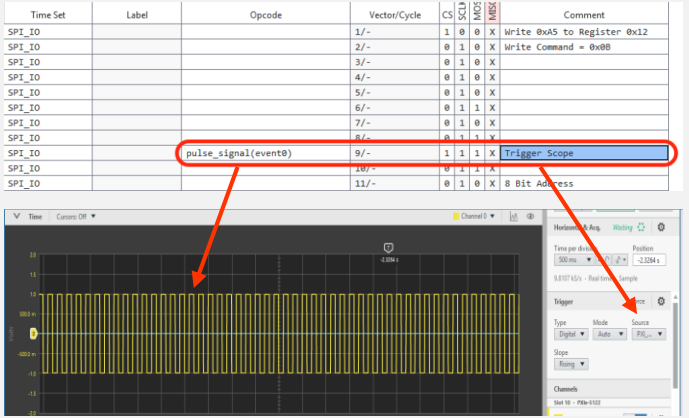
Why it matters

- Flexible execution of patterns including dynamic source and capture memory operations
- Integrated measurement capability of all instruments within a digital pattern

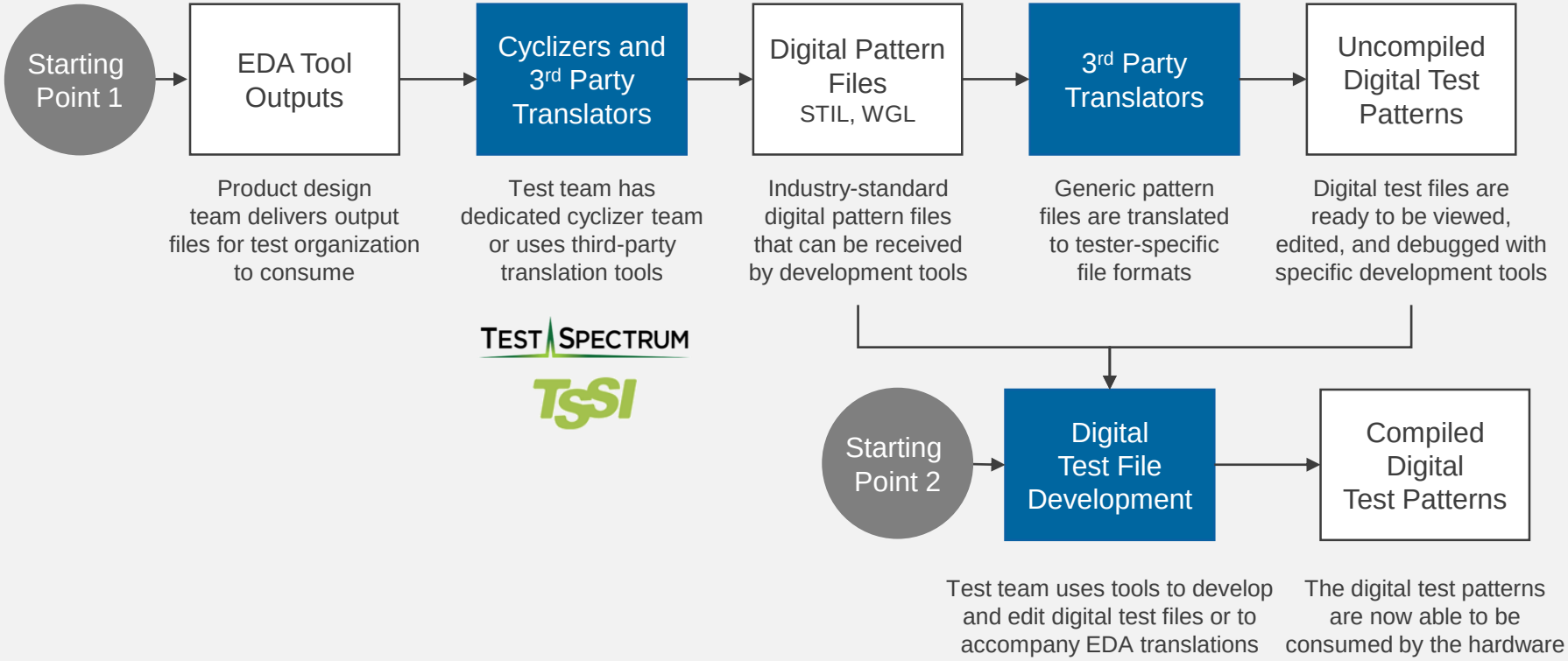








Semiconductor Digital Pattern Workflow



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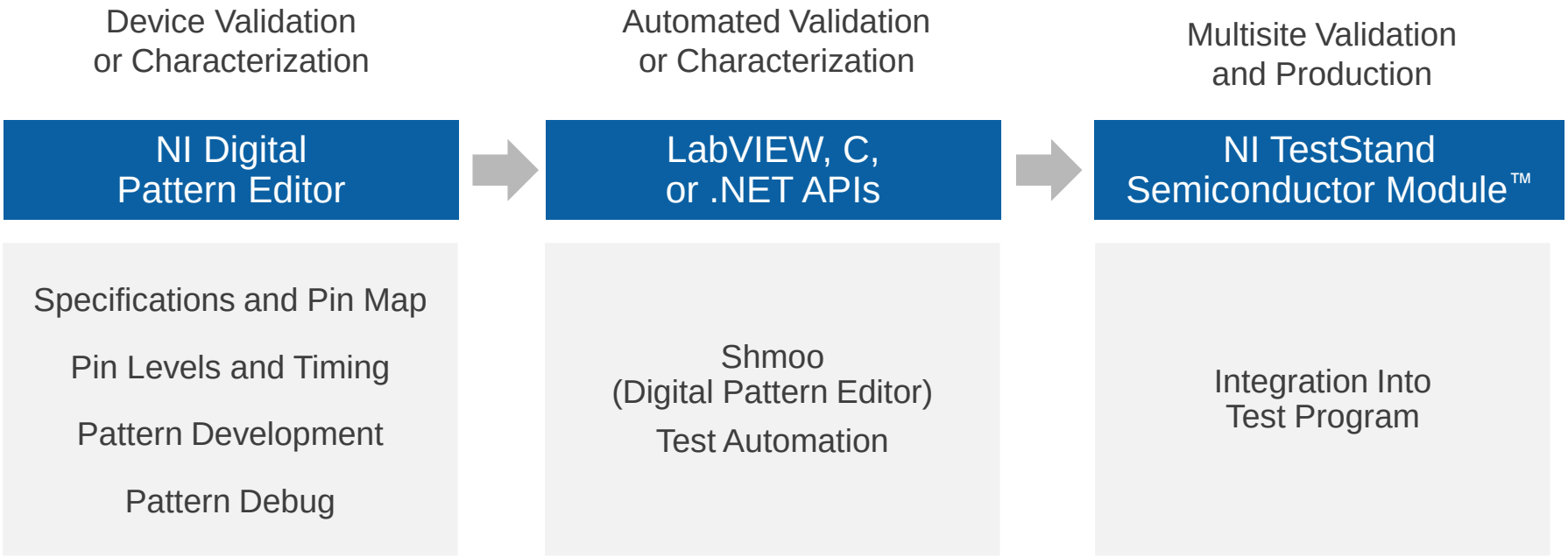
Test Engineer Workflow With NI



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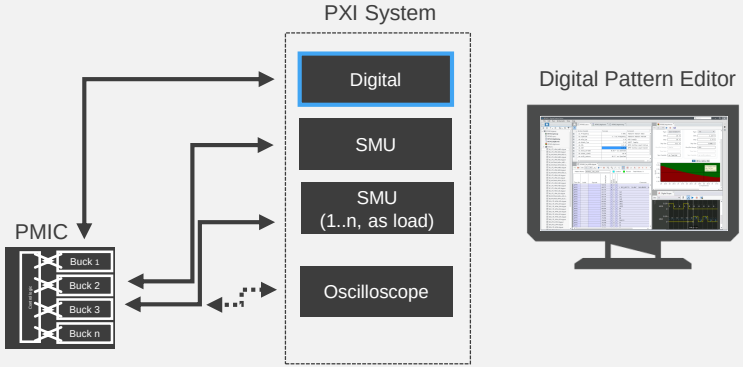
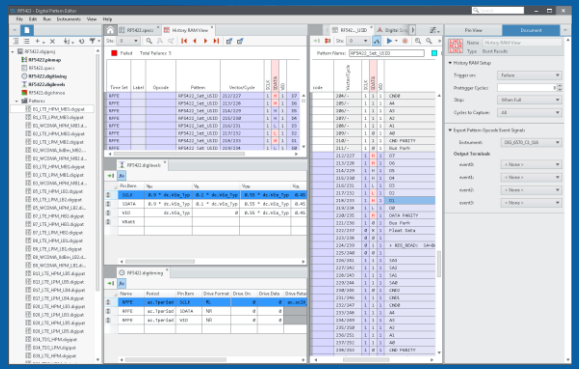


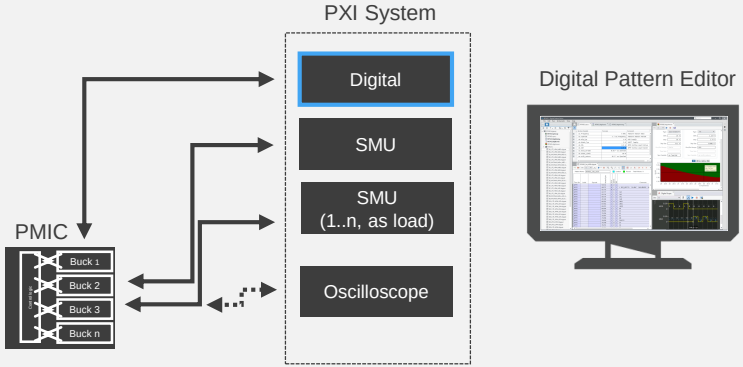
Digital Pattern Editor

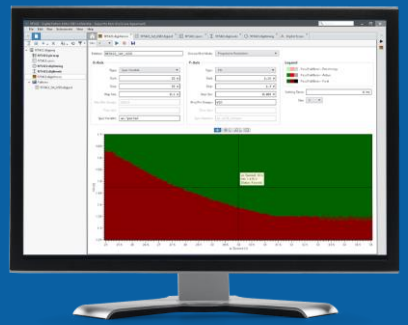


DEMO: Create and Edit Digital Patterns

- Develop digital patterns with the Digital Pattern Editor
- Create pin and channel maps
- Set specifications, timing, and levels
- Standard ASCII format for pattern files

NATIONAL INSTRUMENTS





DEMO: Debug Digital Patterns and Create Shmoo Plots

- History RAM overlay and viewer
- Pin and system views
- Digital scope
- Shmoo plot

NATIONAL INSTRUMENTS

Demo Workflow

InstrumentStudio

Digital Pattern Editor

LabVIEW

NI TestStand

Power on Device, Confirm Operation

Establish DUT Communication

Confirm Commands From Digital Instrument

Perform Manual Test

Debug Test Code

Develop Test Code

Automate Single Test

Build Sequence

Run Sequence and Begin Analysis

NATIONAL INSTRUMENTS

LabVIEW™

Integrate Hardware. Visualize Data. Accelerate Engineering.

Rapidly connect to and configure instrumentation

Minimize test sequence development time

Quickly reuse existing source code, scripts, and libraries

Instantly visualize measurement results

Reduce test station deployment and rework costs

NATIONAL INSTRUMENTS™

NI TestStand™

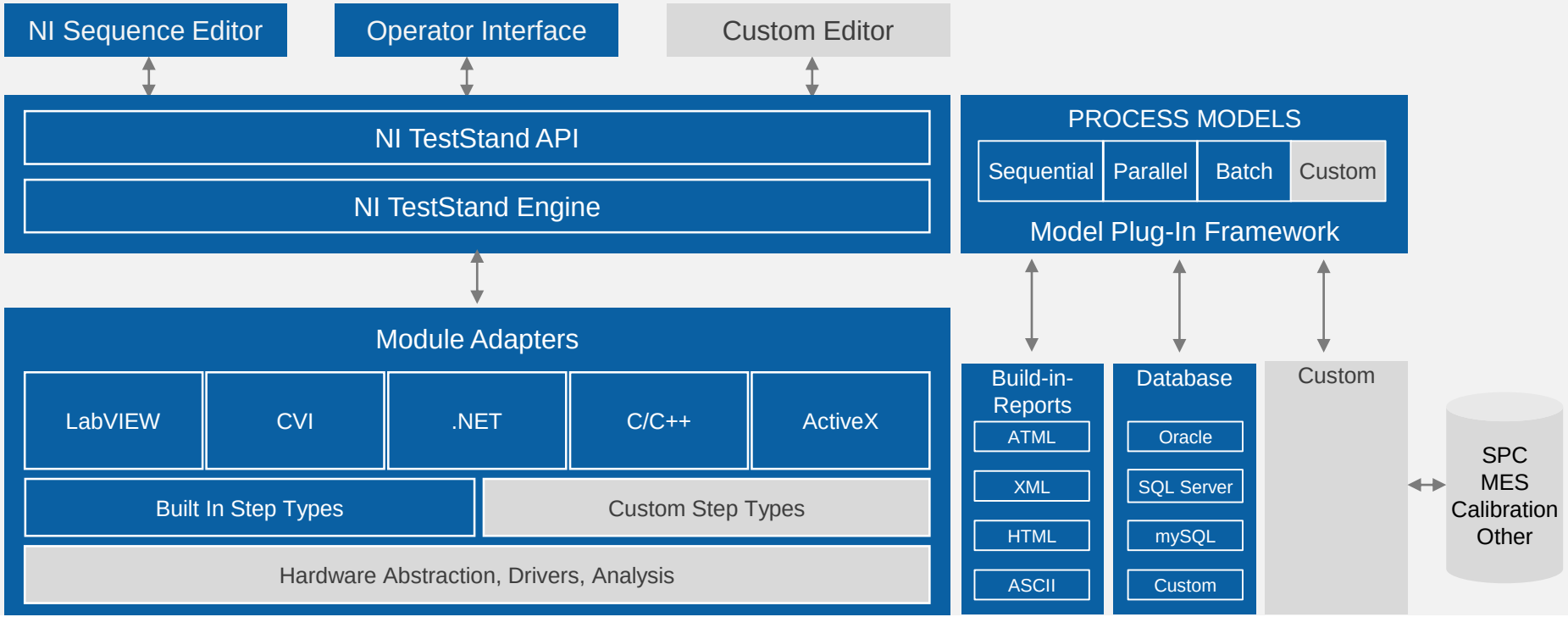
Industry-Standard Test Management Software

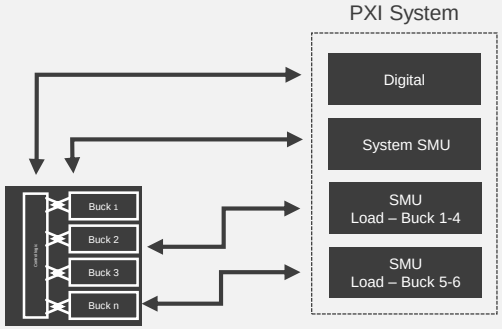
FEATURES AT A GLANCE

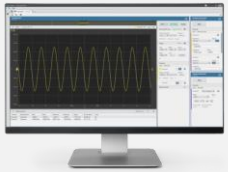
- Author, execute, and debug test sequences
- Leverage test code developed in any language
- Test many devices in parallel
- Generate reports
- Integrate with databases
- Extend the software to meet custom requirements
- Develop professional operator interfaces

NATIONAL INSTRUMENTS

TestStand Architecture





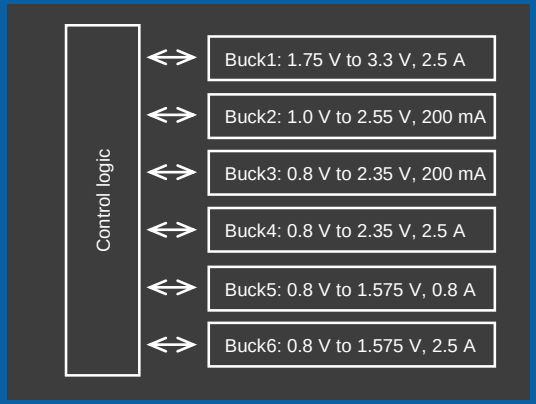


InstrumentStudio

LabVIEW

Digital Pattern Editor

NI TestStand



DEMO: Develop a Sample Automated Test Sequence for Power Efficiency and Load Regulation

- Use InstrumentStudio to confirm DUT functionality and debug
- Use Digital Pattern Editor to develop patterns to communicate with DUT
- Automate tests with LabVIEW
- Sequence numerous tests and generate reports with TestStand

NATIONAL INSTRUMENTS

Using NI Hardware with Python

2019 Update

George Tsalavoutis

Senior Applications Engineer, Automated Test

National Instruments

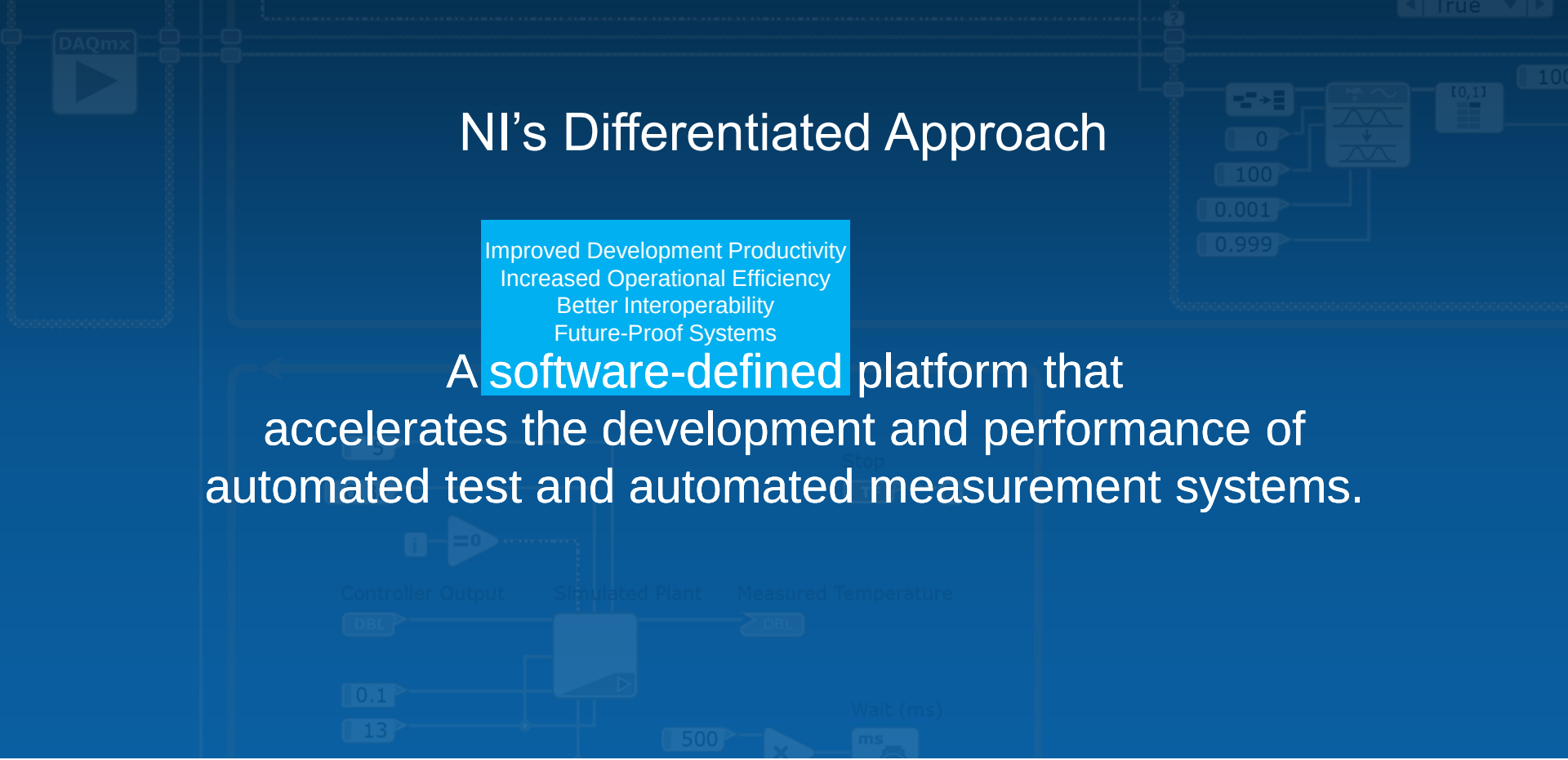
Disclaimers

- Some information applies specifically to this site
- Some comments are George's opinion, rather than official NI corporate strategy

NI's Differentiated Approach

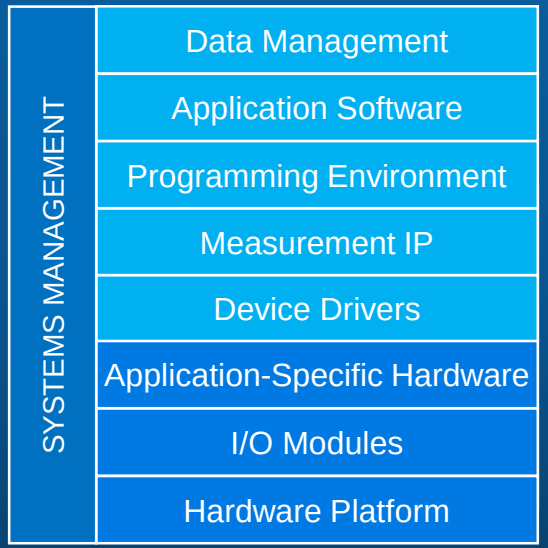
Improved Development Productivity
Increased Operational Efficiency
Better Interoperability
Future-Proof Systems

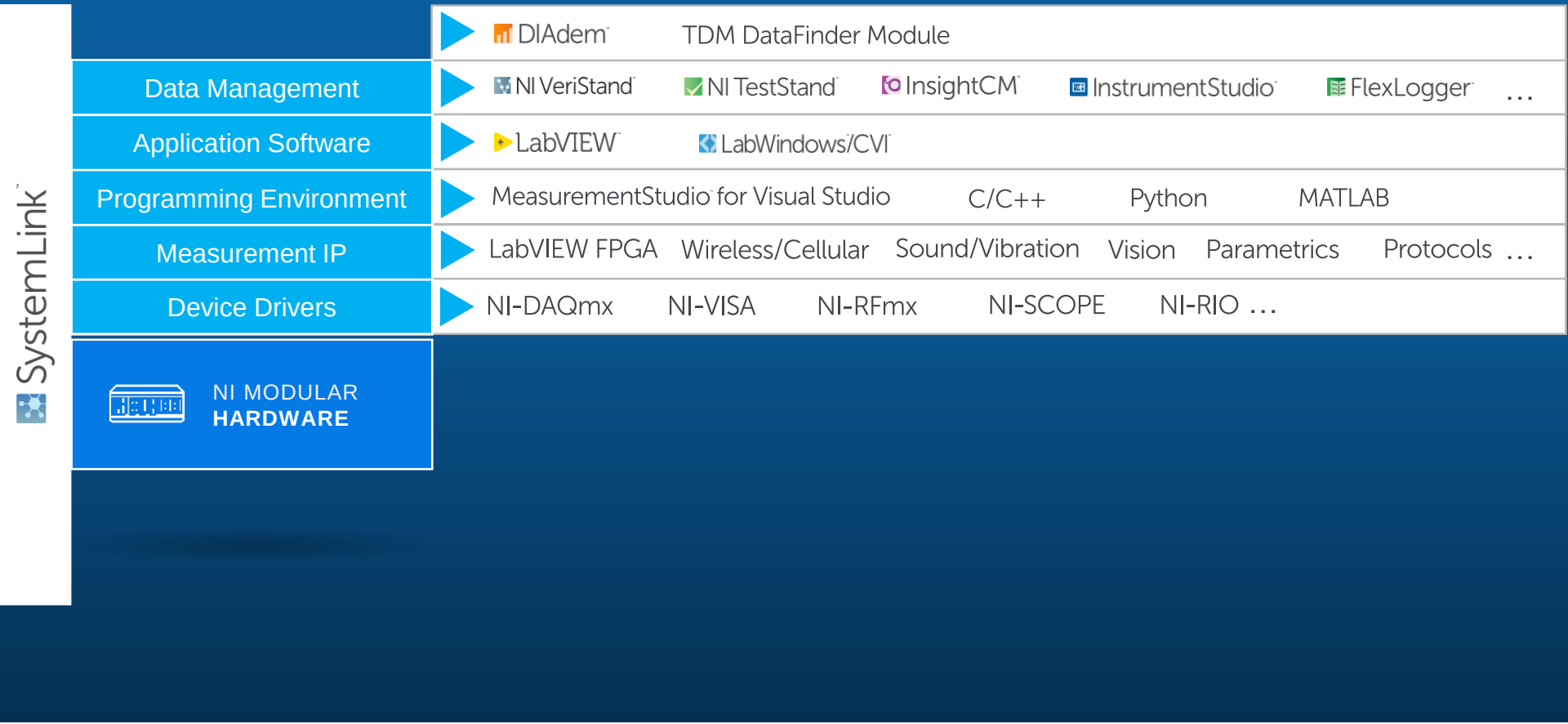
A software-defined platform that accelerates the development and performance of automated test and automated measurement systems.



NATIONAL INSTRUMENTS

NI PLATFORM


SYSTEMS MANAGEMENT
Data Management
Application Software
Programming Environment
Measurement IP
Device Drivers
Application-Specific Hardware
I/O Modules
Hardware Platform

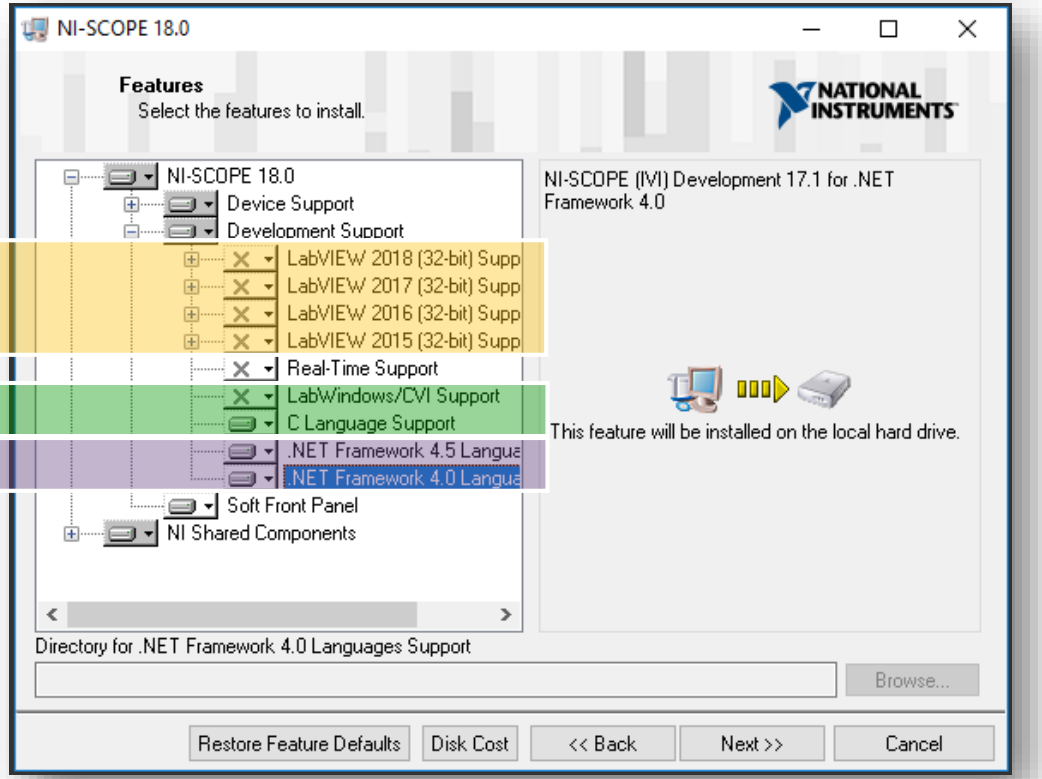


Typical NI Hardware Driver installer

NI LabVIEW Support

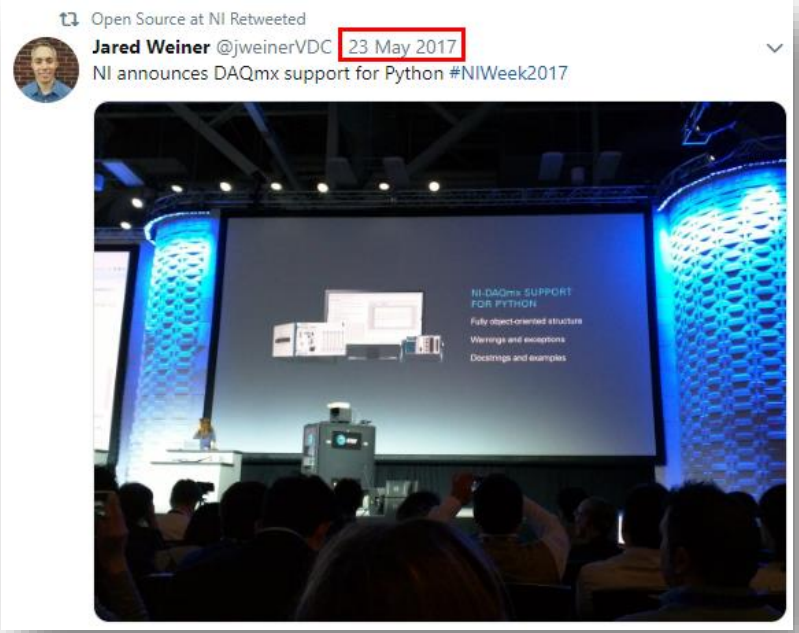
C language Support

.NET language Support



NATIONAL INSTRUMENTS

NI-DAQmx Python Support



https://nidaqmx-python.readthedocs.io/en/latest/

Python APIs for NI Instruments

- Interface with the Python drivers through a Python API that is:
  - concise
  - object-oriented
  - best-in-class
- Easy access to:
  - Properties
  - device-specific parameters
  - exception handling
- Get dynamic, real-time device feedback through interactive scripting

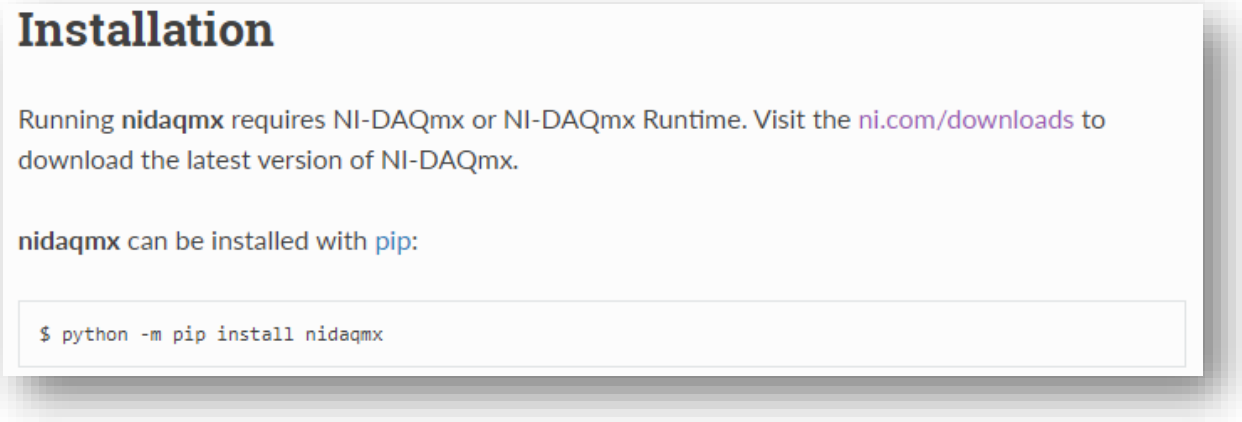
```
import nidaqmx


task = nidaqmx.Task()
task.ai_channels.create_voltage_channel('cDAQ1Mod1/ai0')
print task.read(number_of_samples_per_channel=10)
task.clear()
```

NATIONAL INSTRUMENTS

How to get Python Support

1. Search online [My Driver] Python Support
2. Read the documentation for NI's Python support on readthedocs.io
3. Download and install NI's latest driver for the hardware of interest
4. Use `pip`, or other preferred method, to pull the Python support library
5. Begin working with Python and the supported NI Hardware



Installation

Running **nidaqmx** requires NI-DAQmx or NI-DAQmx Runtime. Visit the ni.com/downloads to download the latest version of NI-DAQmx.

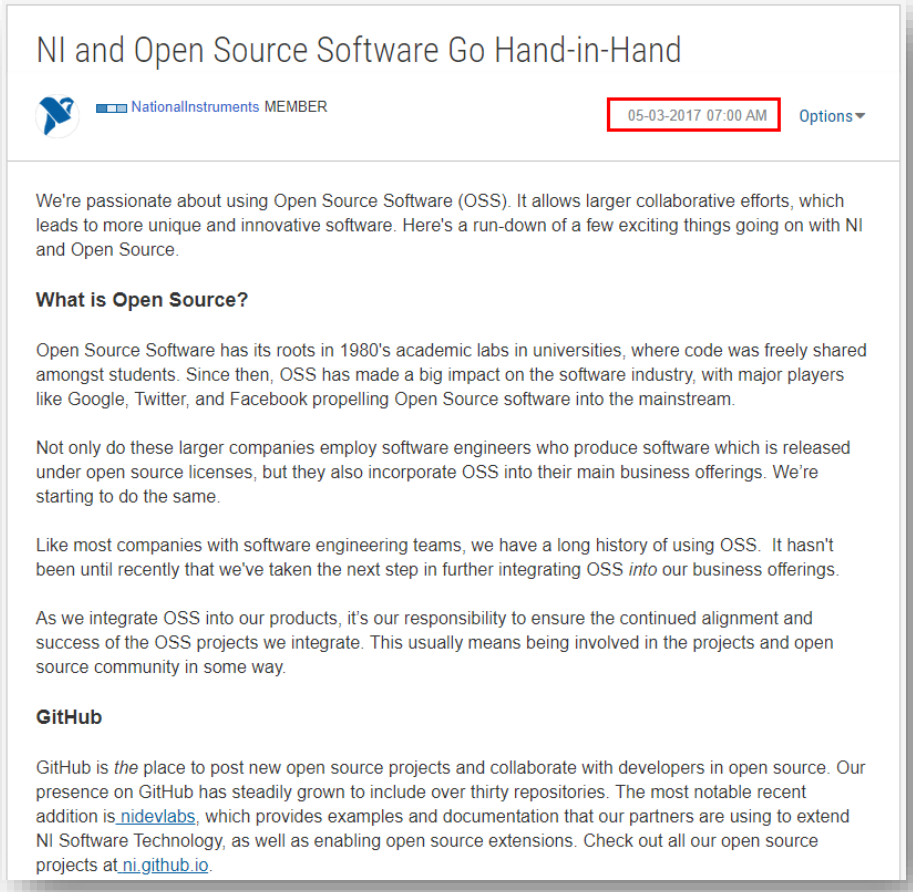
nidaqmx can be installed with pip:

```
$ python -m pip install nidaqmx
```

https://nidaqmx-python.readthedocs.io/en/latest/

NI’s Open-source efforts

Publicly discussed since 2017



NI and Open Source Software Go Hand-in-Hand

NationalInstruments MEMBER

05-03-2017 07:00 AM Options

We're passionate about using Open Source Software (OSS). It allows larger collaborative efforts, which leads to more unique and innovative software. Here's a run-down of a few exciting things going on with NI and Open Source.

What is Open Source?

Open Source Software has its roots in 1980's academic labs in universities, where code was freely shared amongst students. Since then, OSS has made a big impact on the software industry, with major players like Google, Twitter, and Facebook propelling Open Source software into the mainstream.

Not only do these larger companies employ software engineers who produce software which is released under open source licenses, but they also incorporate OSS into their main business offerings. We're starting to do the same.

Like most companies with software engineering teams, we have a long history of using OSS. It hasn't been until recently that we've taken the next step in further integrating OSS *into* our business offerings.

As we integrate OSS into our products, it's our responsibility to ensure the continued alignment and success of the OSS projects we integrate. This usually means being involved in the projects and open source community in some way.

GitHub

GitHub is *the* place to post new open source projects and collaborate with developers in open source. Our presence on GitHub has steadily grown to include over thirty repositories. The most notable recent addition is nidevlabs, which provides examples and documentation that our partners are using to extend NI Software Technology, as well as enabling open source extensions. Check out all our open source projects at ni.github.io.

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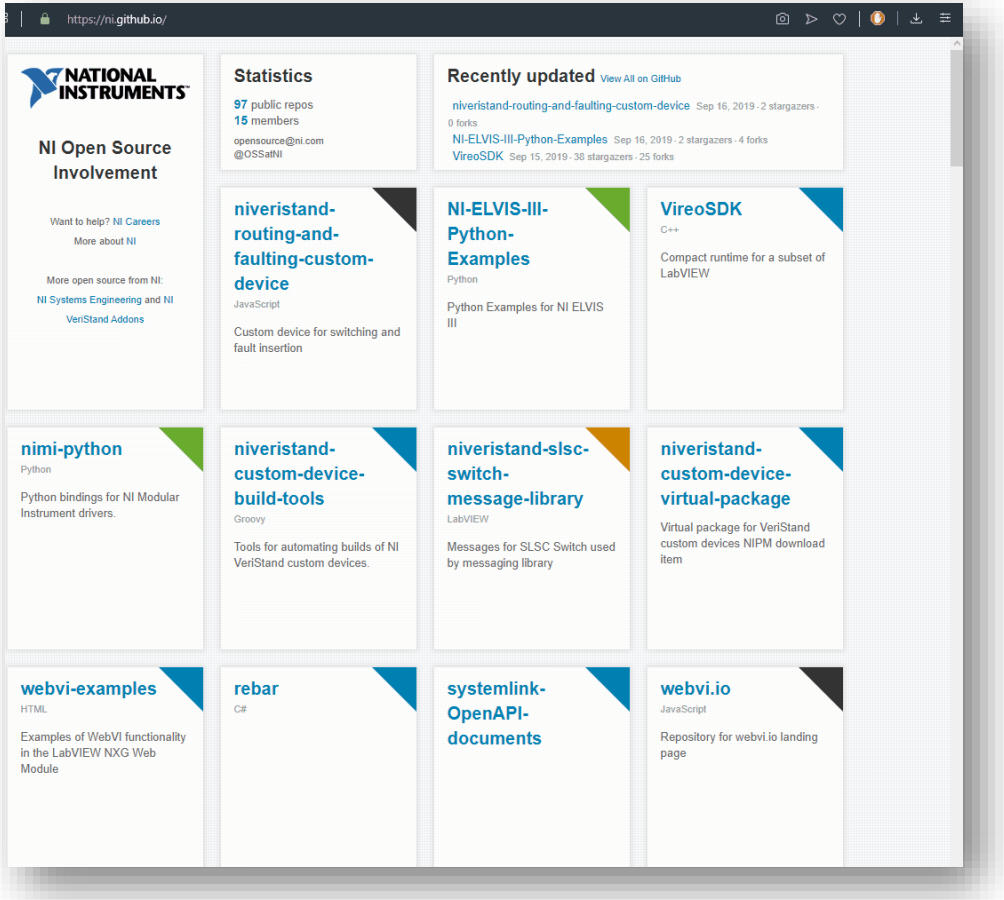
NI’s Open-source Projects

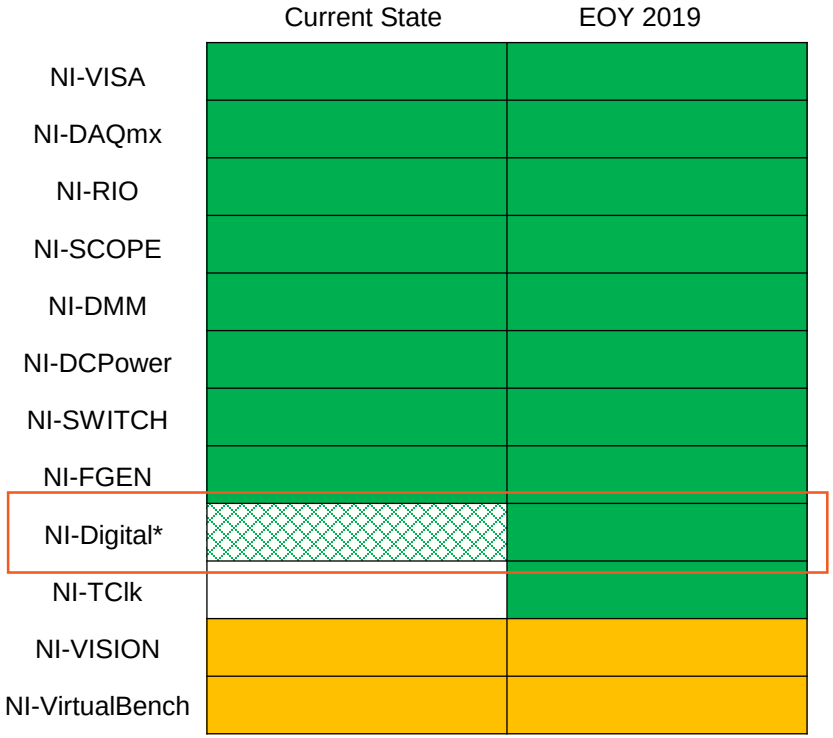


NATIONAL INSTRUMENTS

https://ni.github.io/

NI PXI Modular Instruments

Python Driver Support Roadmap



Reduce development time with native Python APIs for DAQmx, VISA, RIO, and MI drivers

- Fully object-oriented structure
- Supports Python warnings and exceptions
- Documentation and examples
- Free and open-source
- Installed through PyPI

*NI-Digital is currently released on GitHub with a subset of full functionality

PXI Digital Pattern Instruments: PXIe-6570 and PXIe-6571

	PXIe-6570	PXIe-6571*
Module Width	2 slots	1 slot
Active Load	24 mA	16 mA
Pin Electronics	Digital: -2 V to +6 V, 32 mA PPMU measure voltage: -2 V to +6 V, 32 mA PPMU force voltage: -2 V to +7 V, 32 mA	
Channels	32 per module	
	256 maximum in a synchronized subsystem	512 maximum in a synchronized subsystem
Maximum Vector Rate	100 MHz (10 ns minimum vector period)	
Maximum Data Rate	200 Mb/s	
Maximum Clock Rate	160 MHz**	
Pattern Timing	31 time sets 39.0625 ps edge placement resolution	
Drive Formats	Non-return (NR), return to low (RL), return to high (RH) (100 MHz max), surround by complement (SBC) (50 MHz max)	
Vector Memory Depth	128 M/channel	
Opcode Support	Flow control, sequencer flags and registers, signal, source and capture, subroutine	
Source and Capture Engines	Broadcast or site-unique Serial or parallel 8 per instrument	
SCAN Support	Flattened SCAN patterns, up to 128 M	

* Note that the PXIe-6571 requires a chassis with 82 W slot cooling capacity, such as the PXIe-1095. In STS, this requires the high-density test head revision.
** Clock rates >133 MHz will have a non-50% duty cycle.

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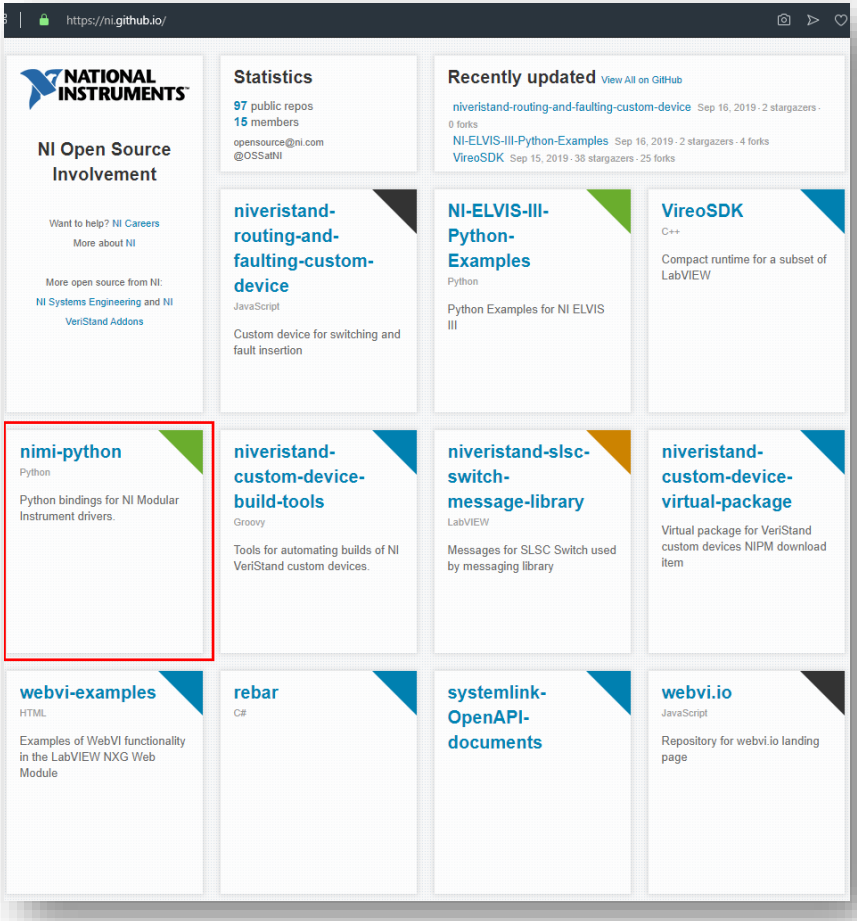
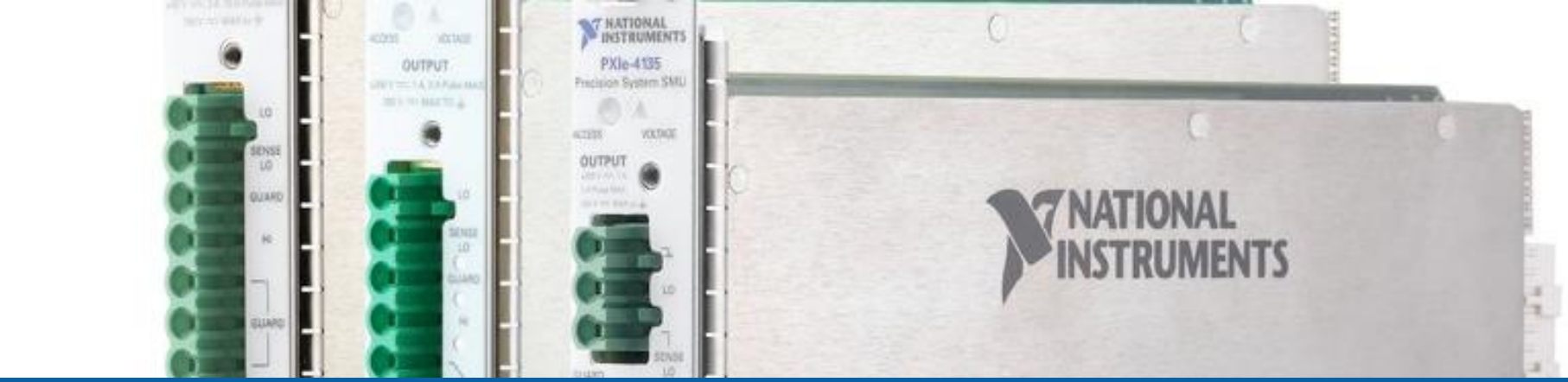
NI's Open-source Projects



NATIONAL INSTRUMENTS

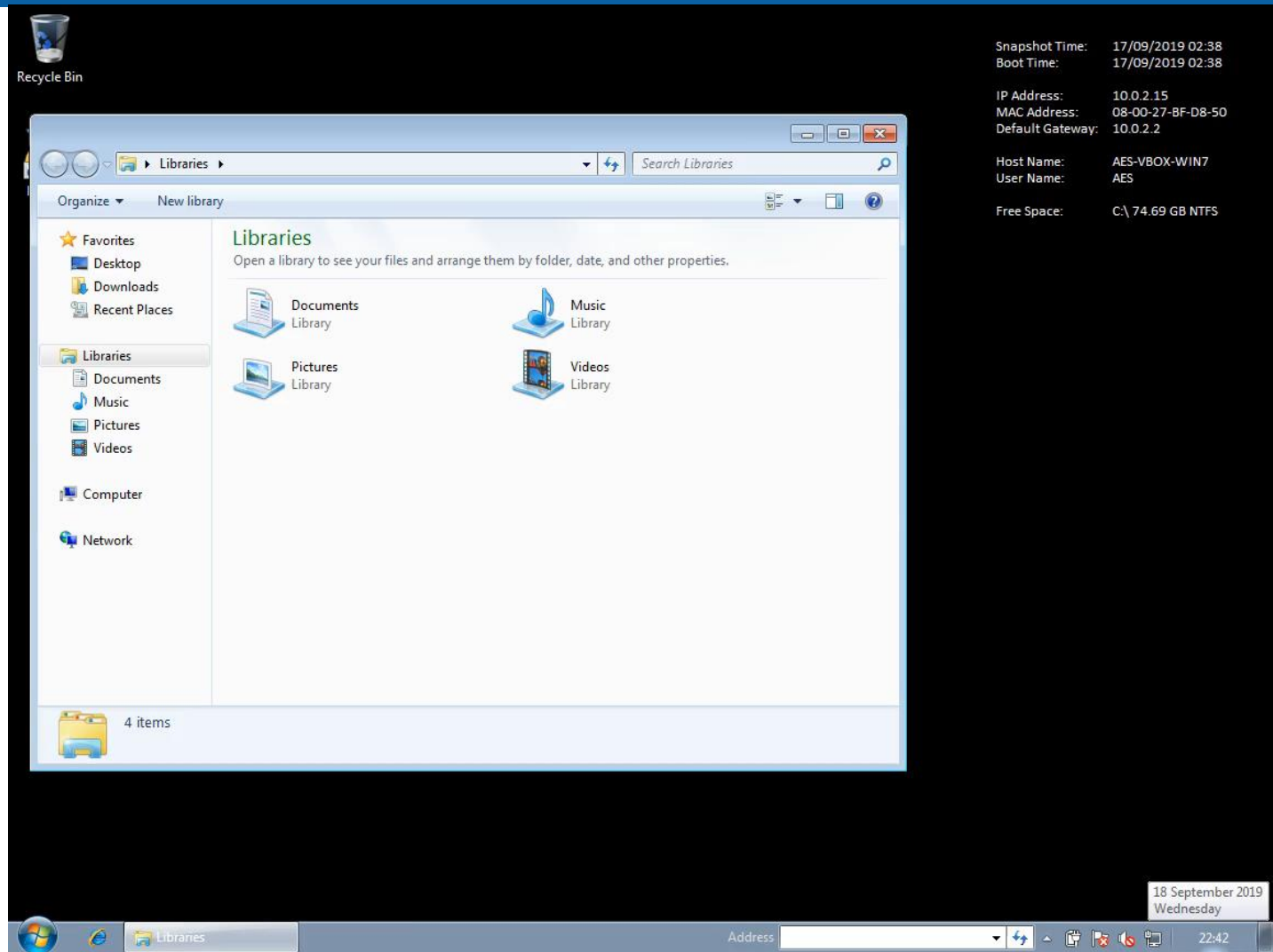
https://ni.github.io/



Demo

- Using `pip` to install NI-DCPower (Power supplies and SMU) support for Python

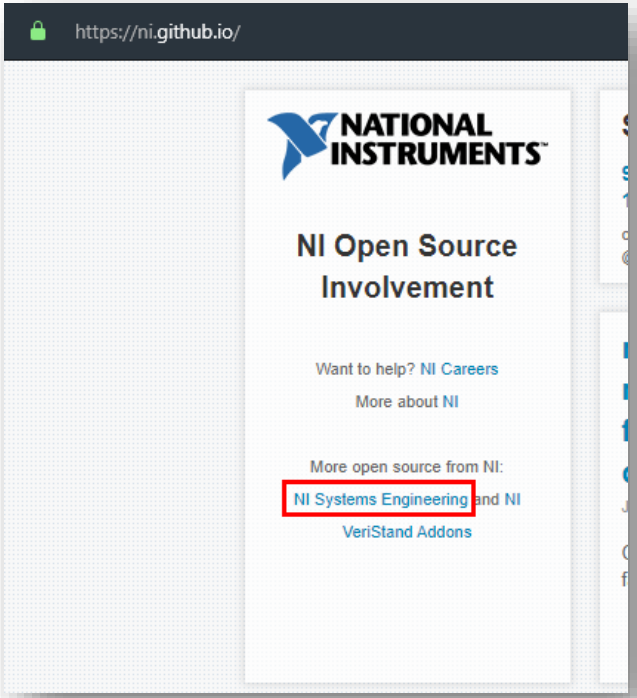
Demo
(2x playback)

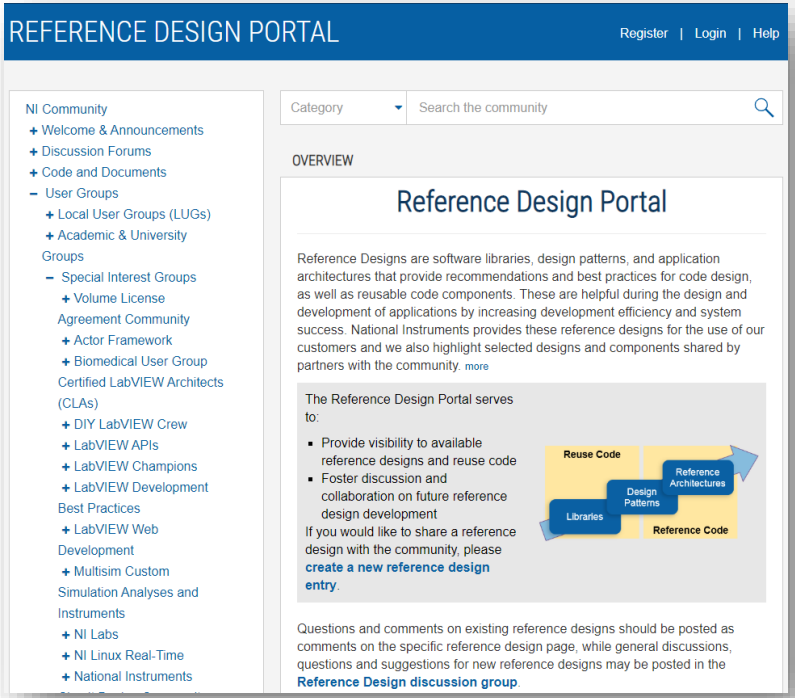


NATIONAL INSTRUMENTS

Other NI Efforts for Python development

Additional repositories from groups internal to NI





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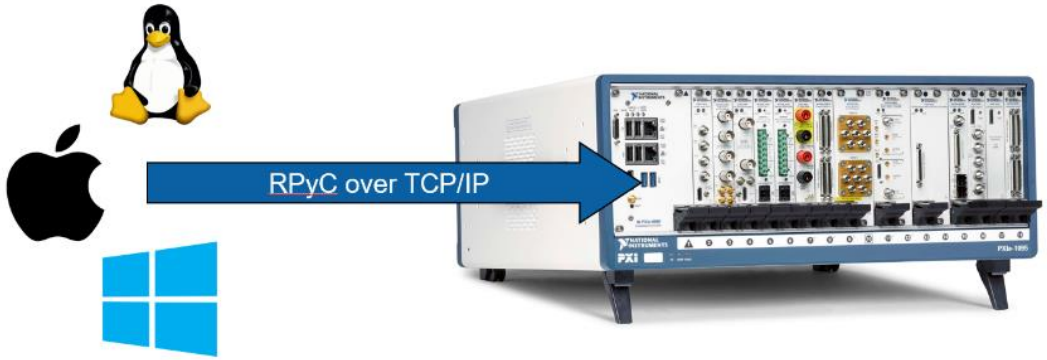
RPyC for RFmx Remoting

Value Statement

Using Python, we can remotely execute NI instrument drivers running on a Windows system (PXIe controller for example) from a client that supports Python.



Supported Clients

- Windows
- Macintosh
- Linux
- Any others that can run Python and RPyC

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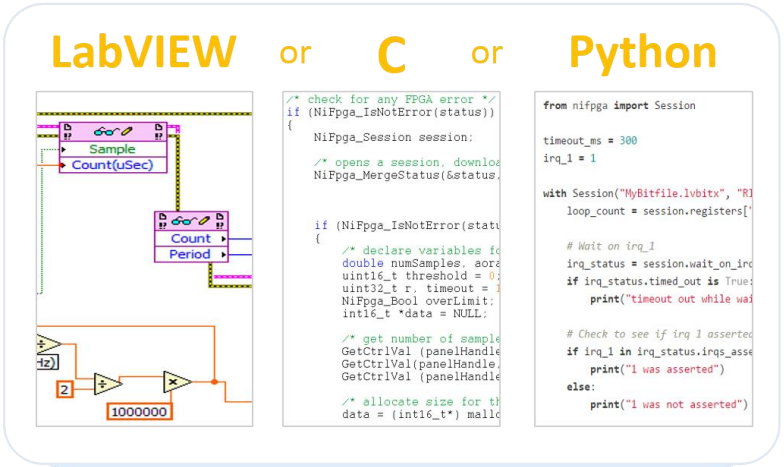
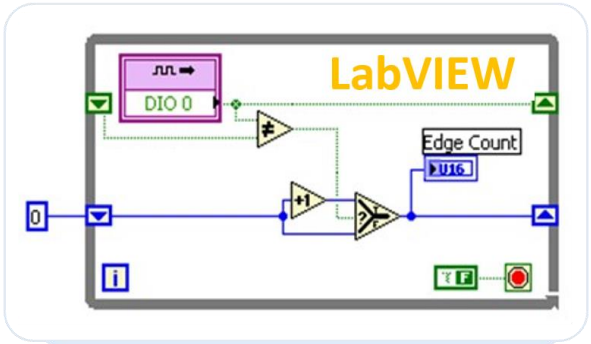
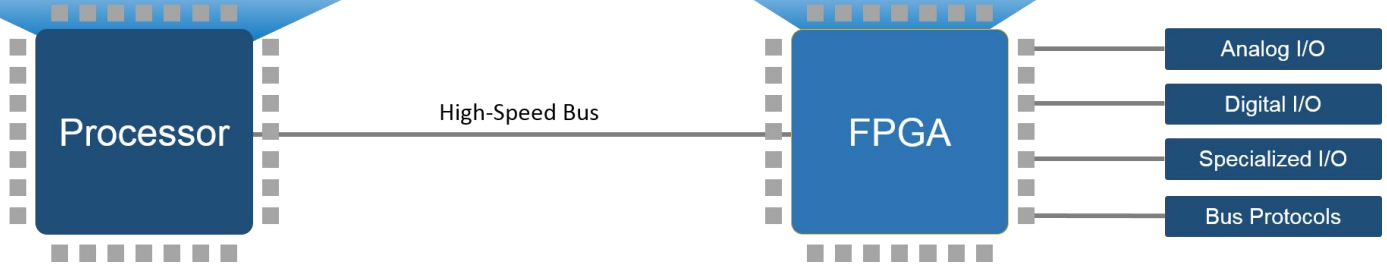
FPGA Interface APIs







NATIONAL INSTRUMENTS

Python Integration

TestStand

New Features in 2019

- Adapter support for Python
- Parametric sweep and stream loops
- InstrumentStudio integration (August 2019)
- PDF reports and HTML5 graph control

Key Applications

- Automated production test
- Interactive, validation workflows

Other TestStand Features

- Quick Drop
- Multicore scaling improvements
- LabVIEW 2019 and LabVIEW NXG 3.0 support
- Easily switch between source VIs and PPLs
- LabWindows/CVI 2019 – Source code navigation, auto-creation of enums from structs, and distinguish pointers from arrays

NATIONAL INSTRUMENTS

imec – Goals and Measures

Introduction

Goal of this pilot is to assess if the NI teststand solution can be used to schedule and execute existing test applications available in imec. The pilot should demonstrate that NI Teststand can help to

- automate the execution of test programs
- facilitate logging and data management
- enable reporting on test data
- provide a standard user interface to the test programs

The available test applications are all applications intended to perform device characterization and are based on different programming languages and hardware platforms.

Overall measures for success of pilot

1. Can NI Teststand interface with existing applications? Can it handle different HW/SW/OS configurations?
    a. Other than LV applications is important
    b. How to go from existing code to a Teststand module?

2. Can NI Teststand enable standardization of input (files) / output (result data)?

3. Can NI Teststand enable/facilitate parallelism / multi threading of existing test modules?

4. Can NI Teststand enable a uniform user interface to different applications?

5. Can NI Teststand enable/facilitate automated reporting?

imec – Pilot Candidates

#		Application	Hardware	Software	OS
1	NewMeasure (Chris)	Command line application for IV sweeps Input: test sequence via text file	B1500	Meas application (C++ or Python) drivers (C++)	Lin/Win
2	Measure (Albert)	Command line application General parametric test (FEOL, BEOL, memory, ...) Input: test sequence via text file	TEL prober KS 4082F ATE B1500 Keithley SMU's KS LCR ...	meas application (C) VISA drivers (C)	Lin only
3	RRAM LV (Sidd)	Labview application for RRAM characterisation (Resistance, IV-sweep, endurance cycling, ...)	Cascade PA300 HP8110A pulser Keithley SMU + switch box LeCroy osci	Labview	Win
4	RRAM_SCR? (Lorenzo)	Command line application for RRAM characterization	B1530	C	
5	Vortex_2 LV (Bart)	LV Application for FEOL/BEOL device characterisation Input: test sequence via text file	CM300 prober PXI rack	Labview	Win
6	Pymeasure (Jeroen) Bo to be informed	Command line application for optical device characterization Input: test sequence via text file	CM300 prober Keysight 8164B optical mainframe PI Hexapod motion controller B1530 ...	Python Two main modules to interface with: 1- Thor.py: encapsulates all commands related to wafer and fiber movements 2- Optical_instruments.py: commands to perform optical measurements.	Win
7	Other?				

imec people for testing: 12 weeks (9/11/18 – 15/2/19)

	application	Role	Name	Total Commitment [man days]
Test case 1	New Measure (C++)	Lead	Chris.Jansen@imec.be	12
		Backup	Albert.Vanhelmont@imec.be	3
Test case 2	Vortex2 (Labview)	Lead	Ferenc.Fodor@imec.be	12
		Backup	Bart.Dewachter@imec.be	3
Test case 3	OIO Pymeasure (python)	Lead	Jeroen.Decoster@imec.be	8
		Backup	Bo.Wang@imec.be	3

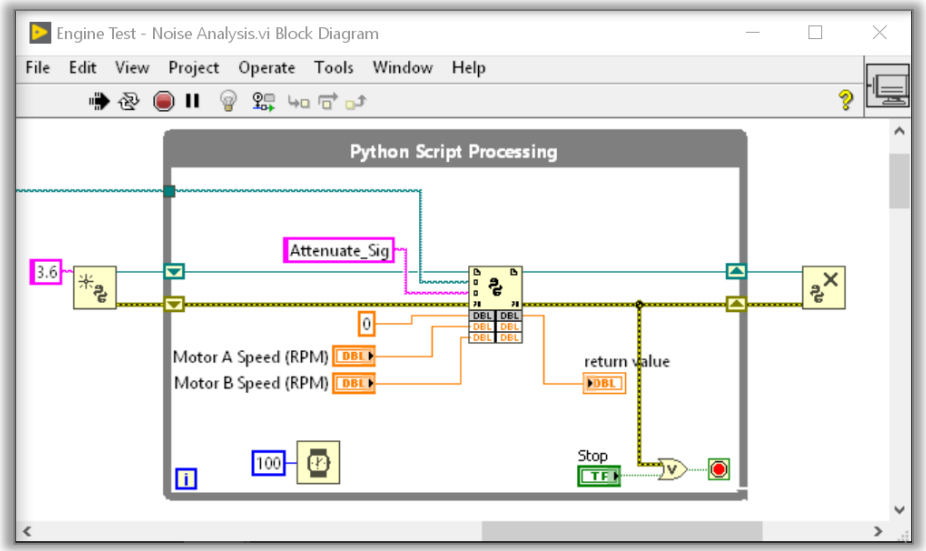
NATIONAL INSTRUMENTS

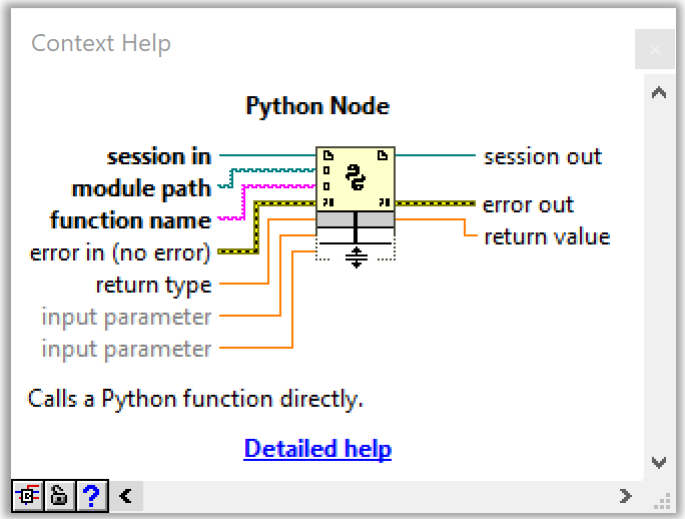

LabVIEW 2018
Version 18.0 (32-bit) - Finishing initialization
NATIONAL INSTRUMENTS

Reuse More IP

Python Node

Natively call Python functions and pass parameters within the LabVIEW environment



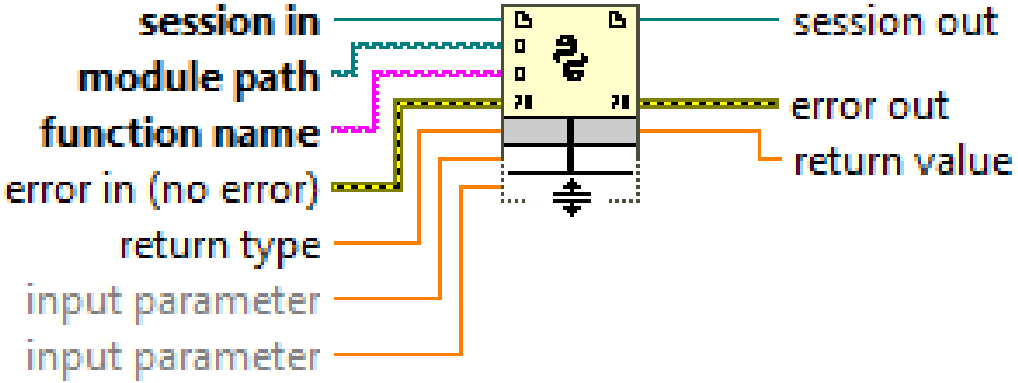


Program with Purpose

LabVIEW 2019

Python Node

LabVIEW 2019 Python Node supports NumPy arrays and Booleans



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Choosing the right language

Program with Purpose

New Data Collection Types

LabVIEW 2019

Maps

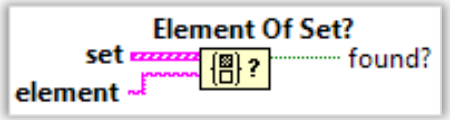
Implement key-value lookup tables

Key	Value
Darth Vader	512-555-1122
Leia Organa	713-555-2133
Luke Skywalker	415-555-4455
Lando Calrissian	617-555-8796
Chew Bacca	312-555-3968

Key	Value
Object A	{metadata cluster…}
Object B	{metadata cluster…}
Object C	{metadata cluster…}
Object D	{metadata cluster…}
Object E	{metadata cluster…}

Sets

Self-sorting unique lists



Instruments in use

`{DMM, Power Supply, Scope}`

Unique emails

`{kimberly@lab.com, victor@test.com, larry@test.com, erika@tools.com, …}`

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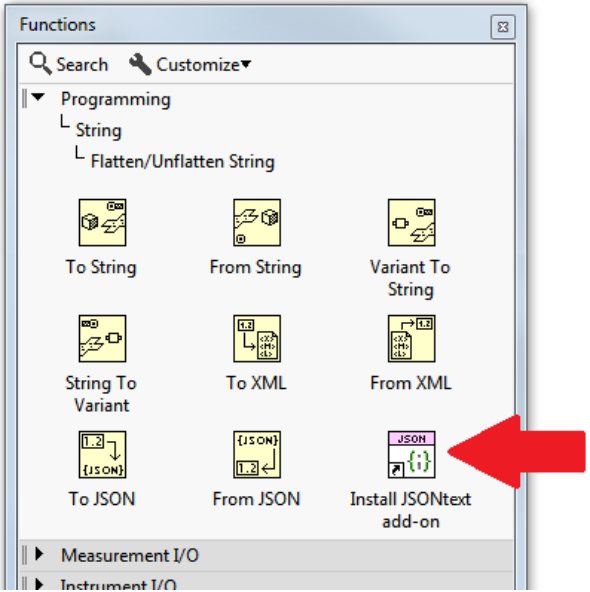
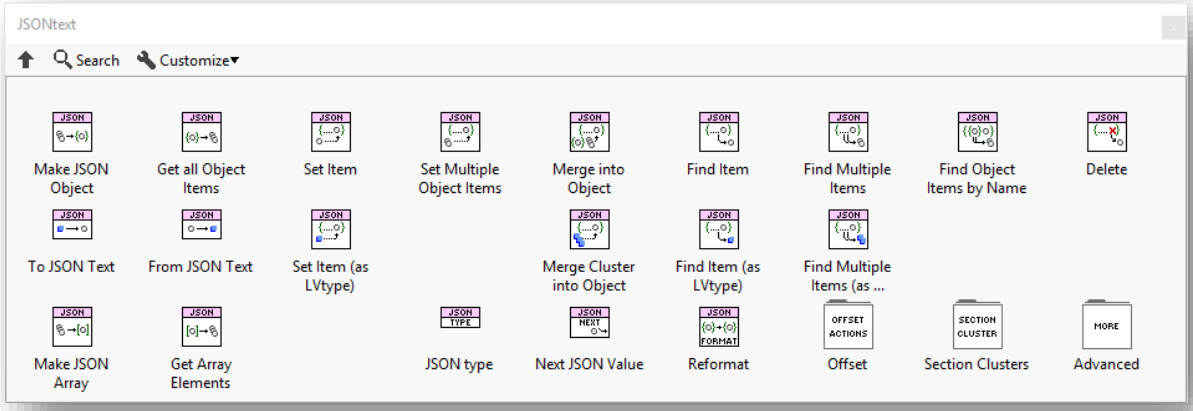
Program with Purpose

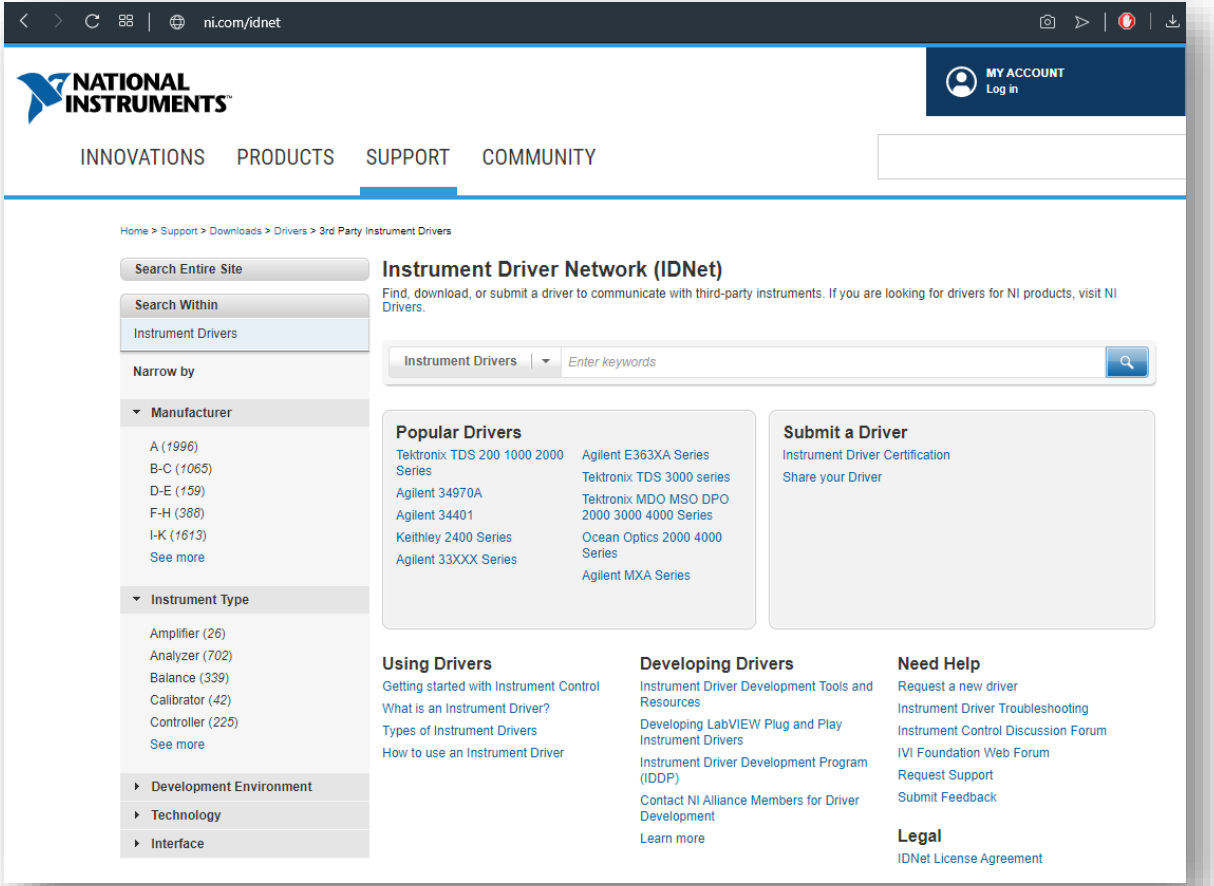
Expand JSON functionality

- Searchable palette item links to JSONtext toolkit

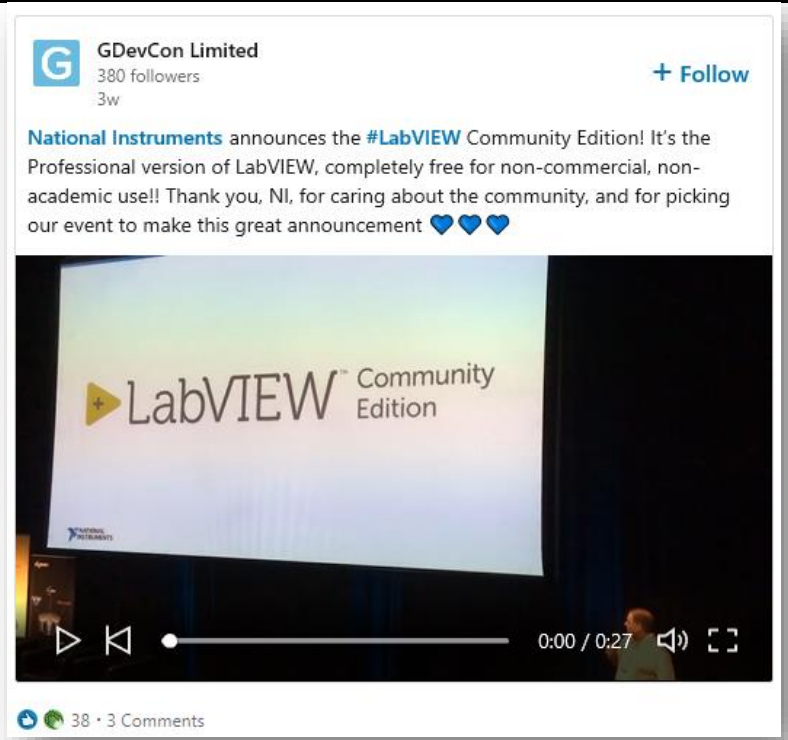




3rd Party Instrument Interfaces



LabVIEW™ Community Edition



NATIONAL INSTRUMENTS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Agenda

Time	Topic	Presenter	Duration
08:30	Welcome and Introductions		
09:00	Keynote: An Overview of NI's Commitment to Semiconductor Test	Joris Donders (NI)	30 min
09:30	Importance of a post-Silicon Validation Automation Framework	Soliton Technologies	45 min
10:15	**Break**		30 min
10:45	Standardized software framework for test	AMSIMEC Group	45 min
11:30	Investments in Parametric testing capabilities with PXI	Jake Harnack (NI) Bart Dewachter (IMEC)	60 min
12:30	**Lunch**		60 min
13:30	Introduction to the PXI Platform	Tarek Safwan (NI)	30 min
14:00	Using a Modular Platform for Mixed-Signal Semiconductor Characterization	Tarek Safwan (NI) George Tsalavoutis (NI)	60 min
15:00	**Break**		30 min
15:15	Tips and Tricks to get the most out of the PXI platform	George Tsalavoutis (NI)	45 min
16:00	Wrap-up and summary	Alex Floor (NI) Joris Donders (NI)	30 min
16:30	**Finish**		

NATIONAL INSTRUMENTS

Optimizing SMUs for High-Throughput Test

Smarter Test From Characterization to Production

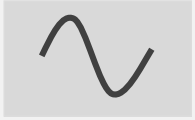
George Tsalavoutis
Senior Applications Engineer, Automated Test
National Instruments

Functionality of Source Measure Units

DC VOLTAGE SOURCE

DC CURRENT SOURCE

PULSE GENERATOR



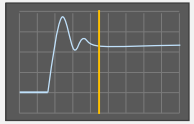
WAVEFORM GENERATOR

VOLTMETER

AMMETER

OHMMETER

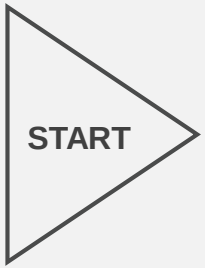
ISOLATED DIGITIZER

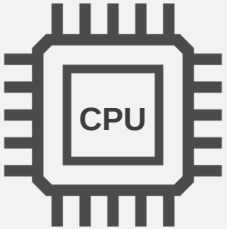


PROGRAMMABLE LOAD

NATIONAL INSTRUMENTS

SMU Measurement Flow





TRIGGER → SOURCE → MEASURE → PROCESS

You can take high-precision measurements quickly.

Removing small inefficiencies in timing can reduce your cost of test.

Demo Configuration

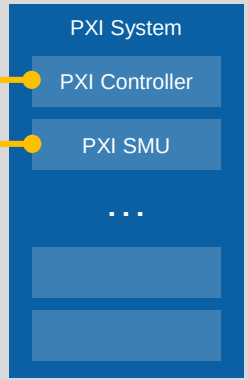
LED

Example
High-Power LED Array

PXI System and LabVIEW

Industry-Leading PC

Source and Measure
I-V Curve of LED



Common Bottlenecks

1. Bus communication latency
2. Sequencing: hardware versus software timing
3. Source and measure cycle
4. Transient response and rise time
5. Serial versus parallel test

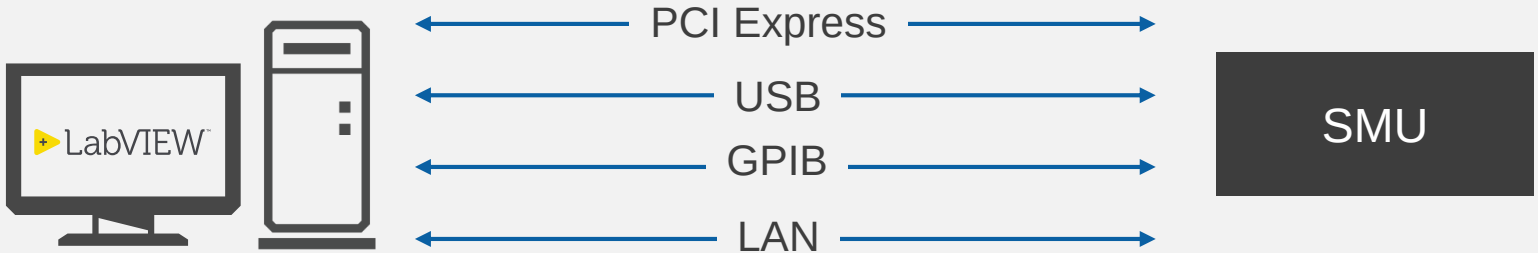
TEST CHALLENGE

Execute a sequence as fast as possible

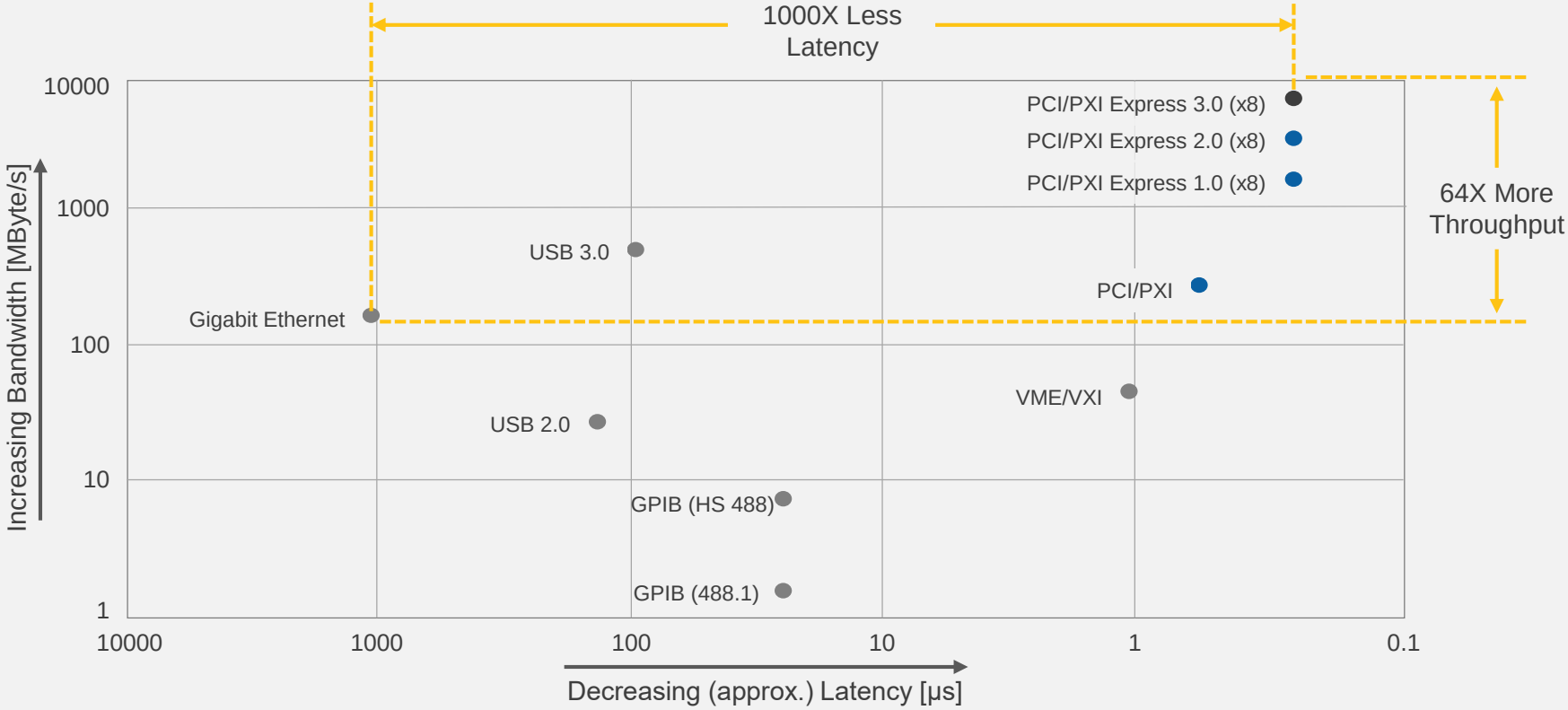
SYSTEM SPECIFICATIONS

3 A, 60 V SMU
Up to 1.8 MS/s sample rate
Up to 100 kS/s update rate
NI SourceAdapt technology
Hardware timing and triggering

1. Bus Communication

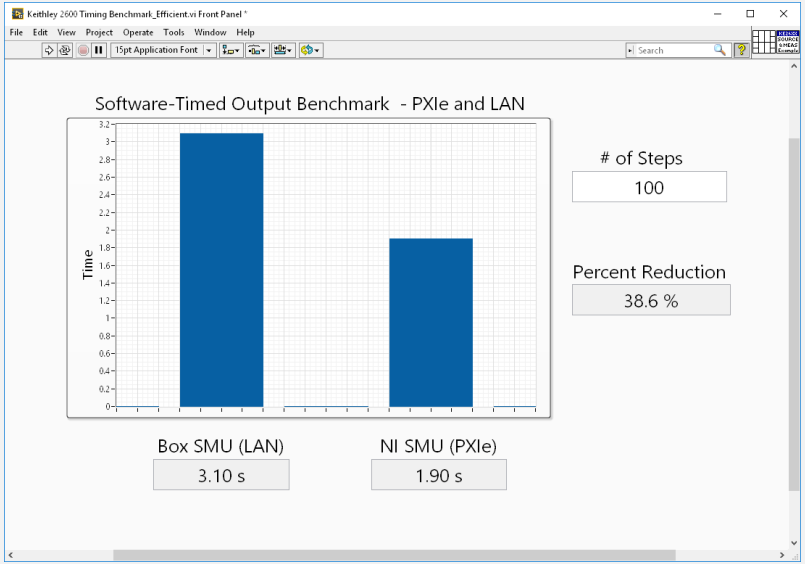


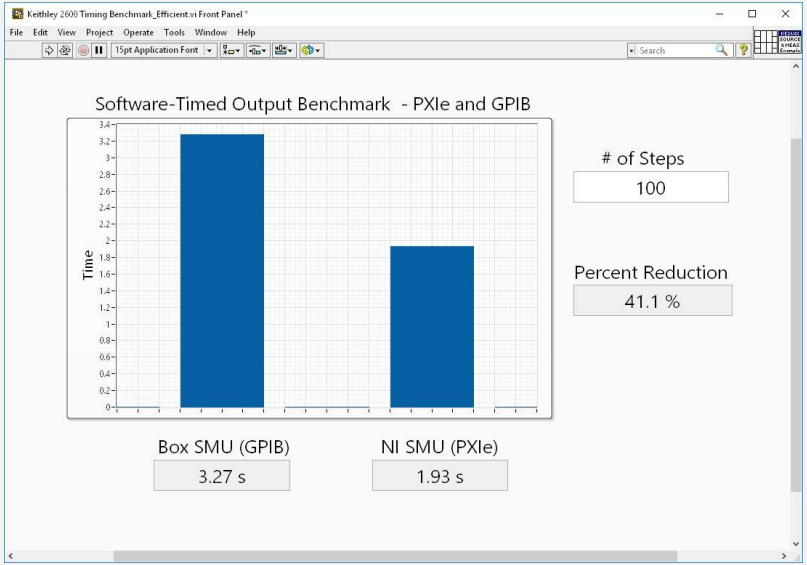
High Throughput and Low Latency With PXI



NATIONAL INSTRUMENTS

SMU Benchmarks Timing by Bus Type





2. Sequencing

Optimized Software Timing

Basic Software Timing

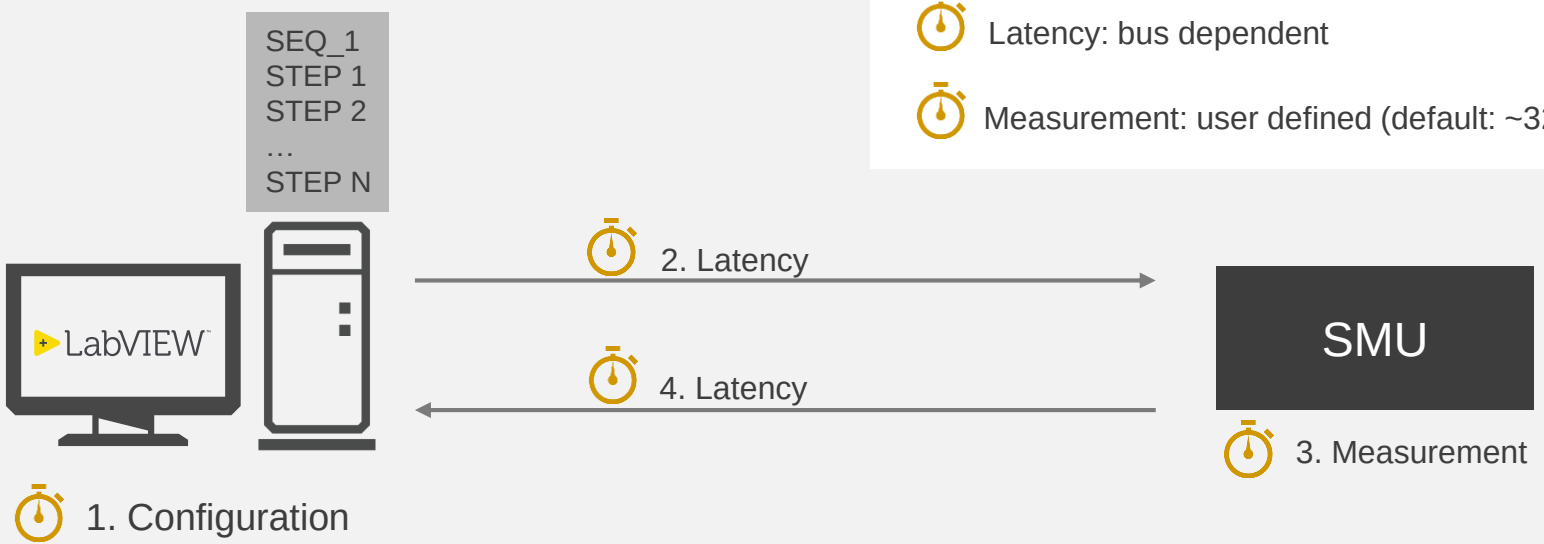
Hardware Timing

Sequencing: Software Timing

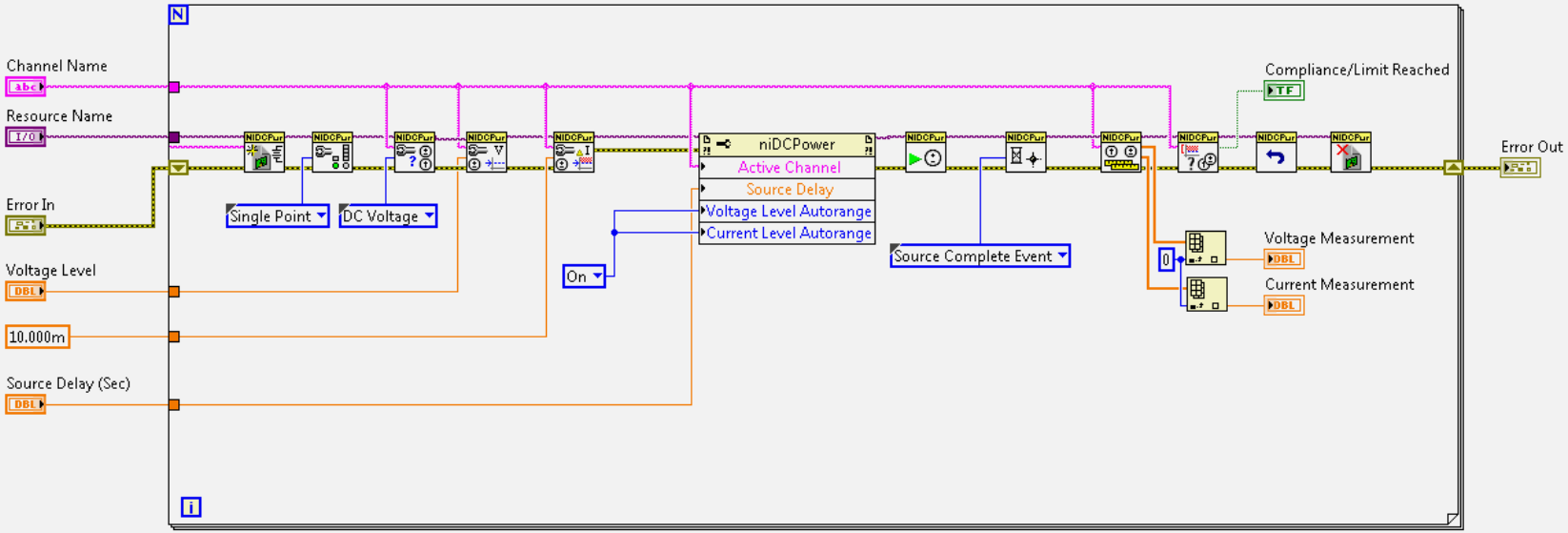
Configuration: variable

Latency: bus dependent

Measurement: user defined (default: ~32 ms)



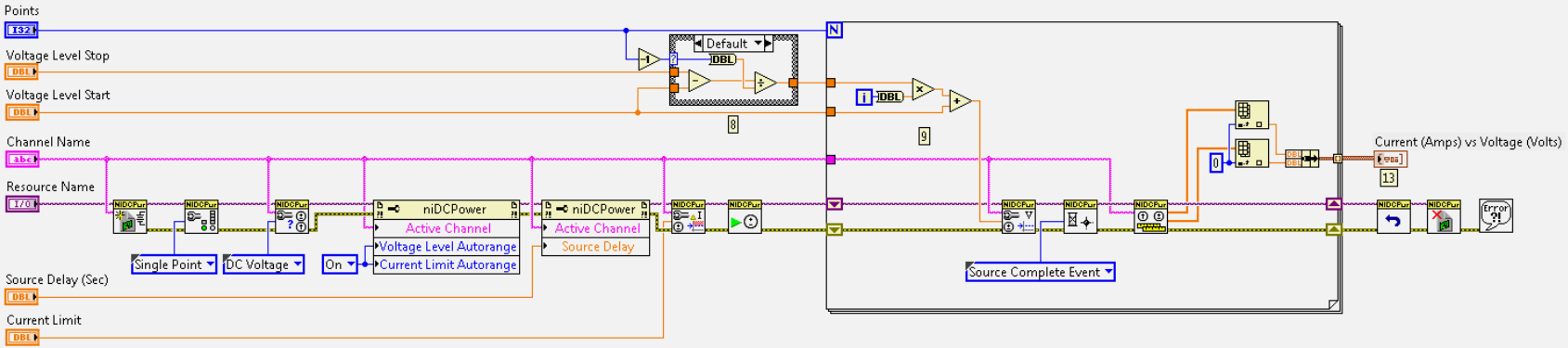
Basic Software Timing



LabVIEW Example—Output DC Voltage

NATIONAL INSTRUMENTS

Efficient Software Timing



LabVIEW Example—Software-Timed DC Voltage Sweep

NATIONAL INSTRUMENTS

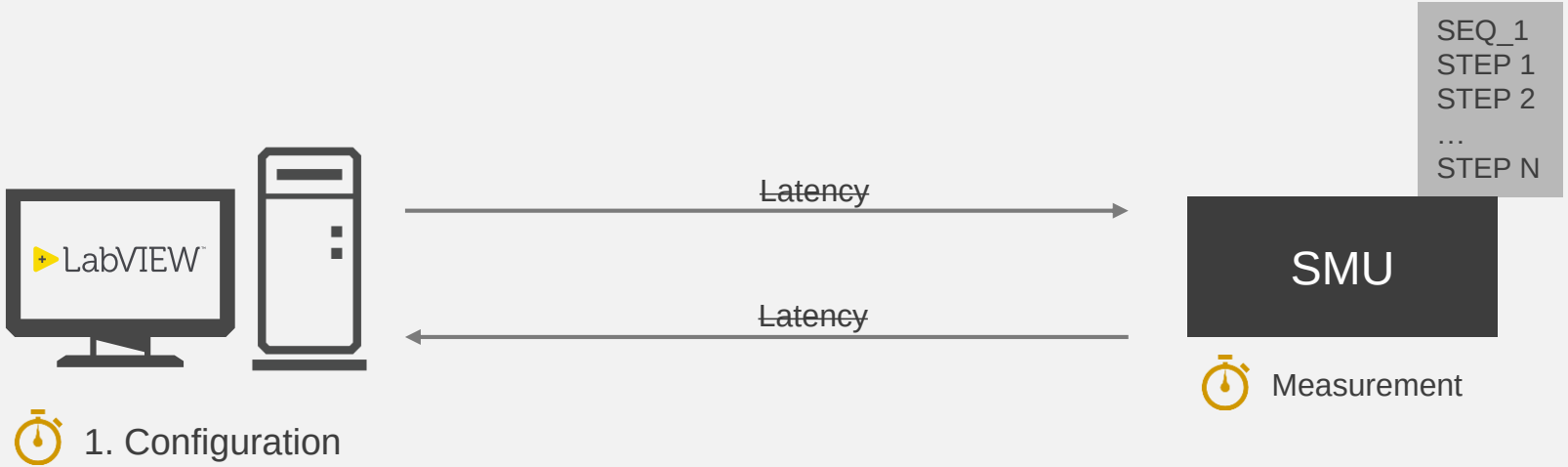
Sequencing

Optimized Software Timing

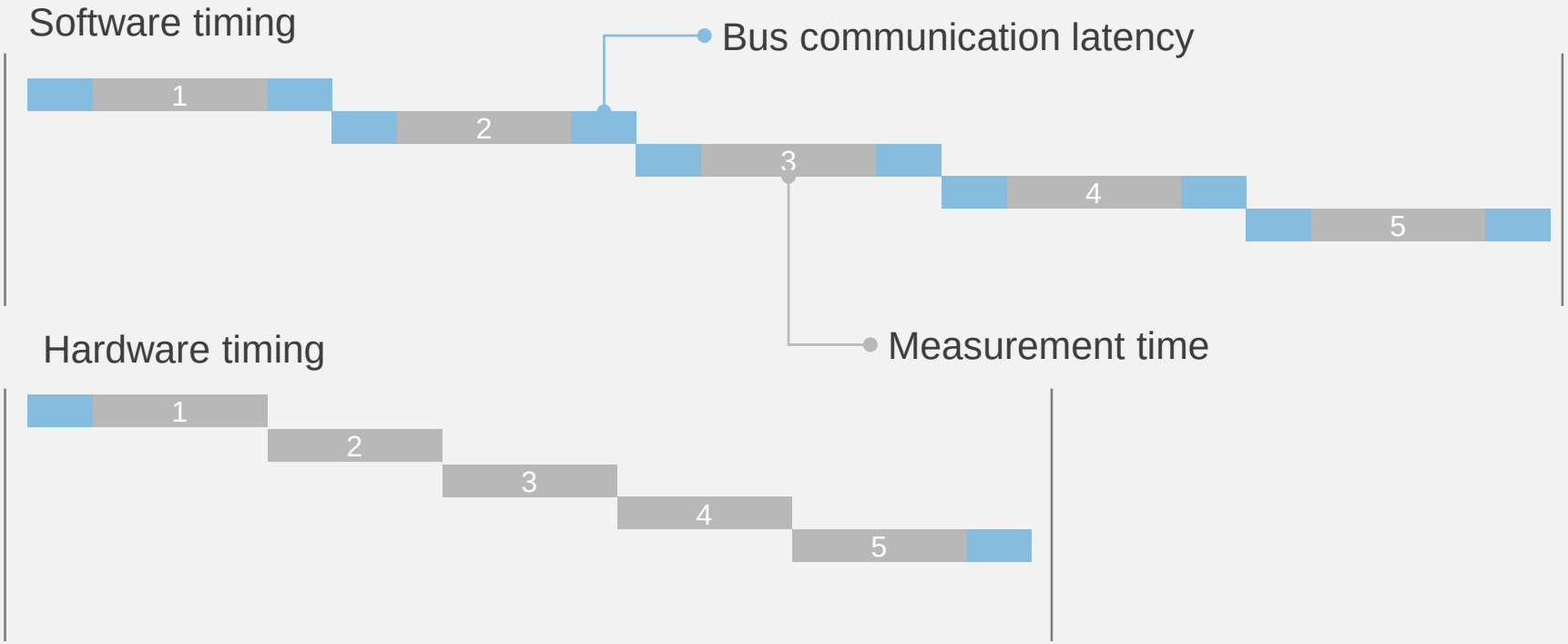
Basic Software Timing

Hardware Timing

Sequencing: Hardware Timing



Sequencing: Software Versus Hardware Timing



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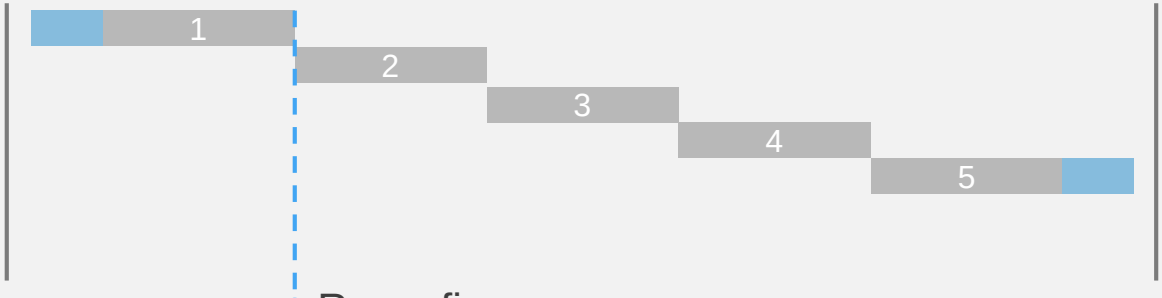
Hardware-Timed Sequencing



Reconfigure

- Output level
- Source delay

“basic” sequence

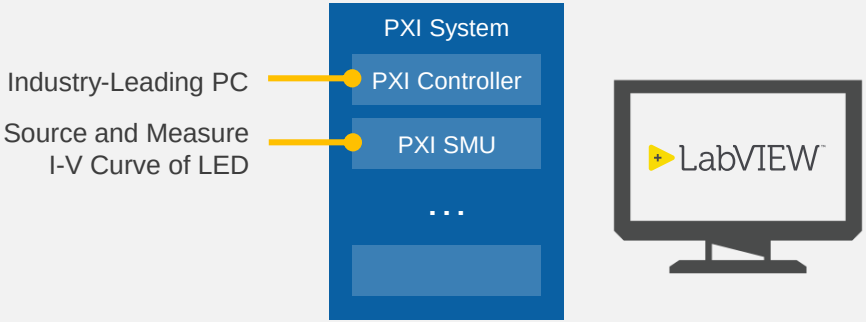
- Aperture time
- Measurement range
- Compliance limit
- Output mode (I or V)
- …

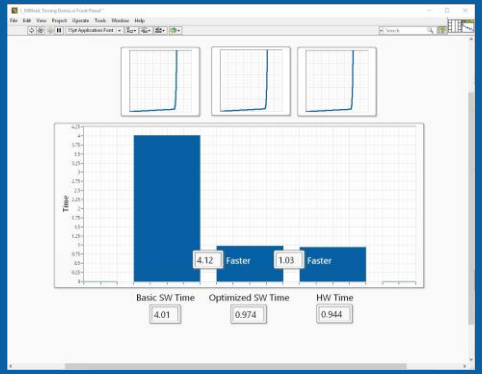
“advanced” sequence (>30 properties)

LED

Example
High-Power LED Array

PXI System and LabVIEW





DEMO: SMU Sequence Execution Time

Three I-V sweeps with identical measurement settings

- Software timing
- Optimized software timing
- Hardware timing

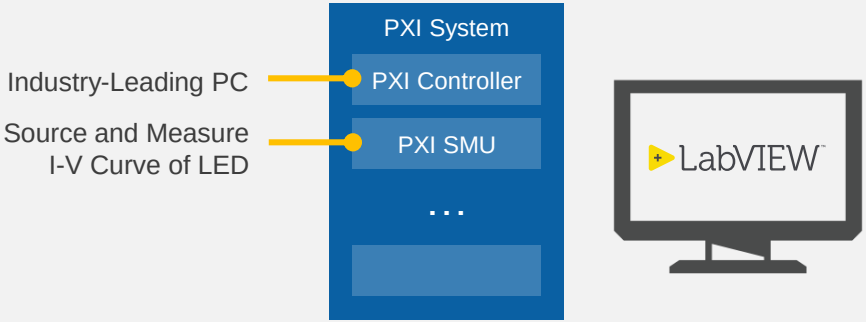
Unnecessary, repetitive function calls add significant overhead to your sequence

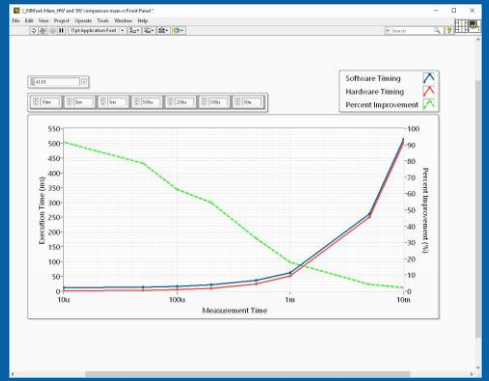
NATIONAL INSTRUMENTS

LED

Example
High-Power LED Array

PXI System and LabVIEW



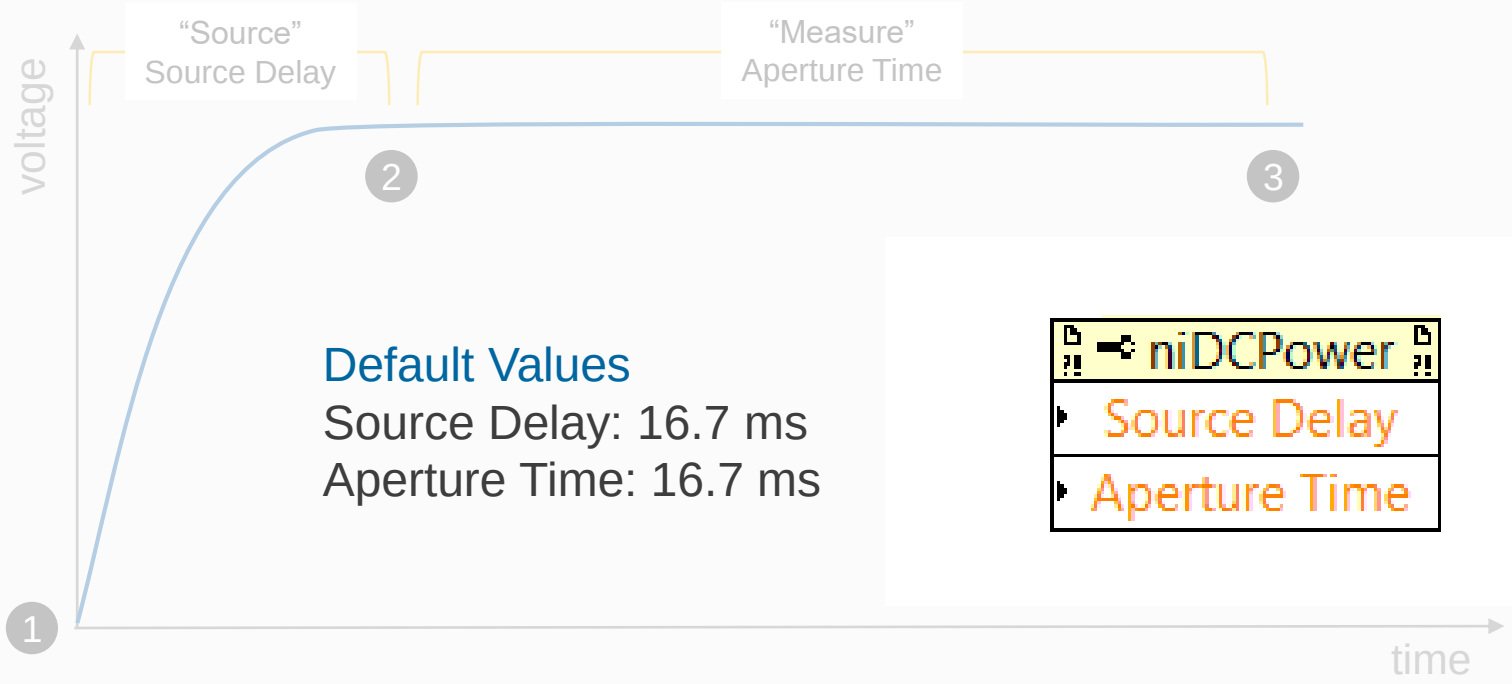


DEMO: SMU Test Time Reduction With Hardware-Timed Sequences

- Compares software timing and hardware timing as a function of the total measurement time of the SMU
- Hardware timing removes overhead of bus latency and software
- As measurement time decreases, hardware timing can significantly improve test execution time

NATIONAL INSTRUMENTS

3. Source and Measure Cycle

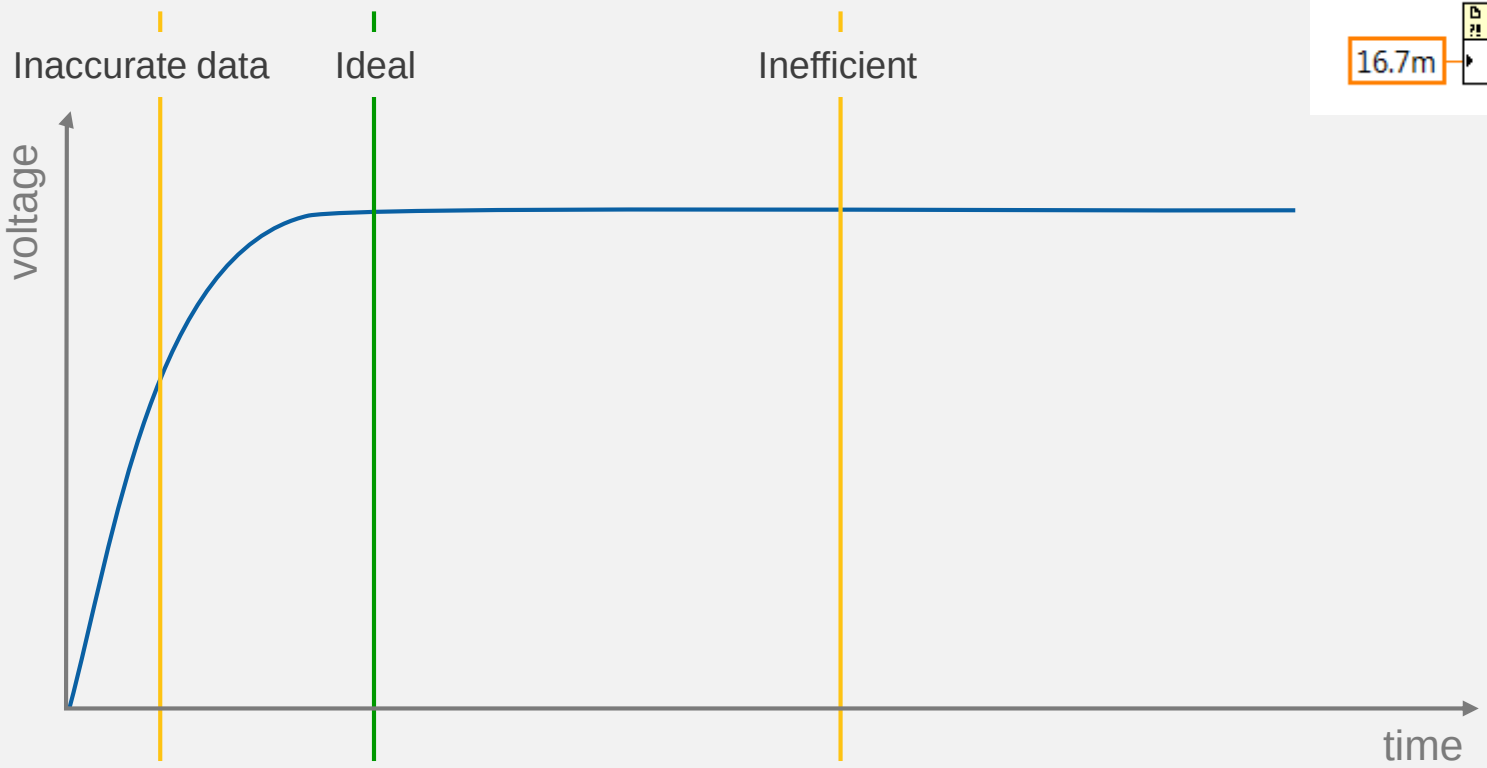


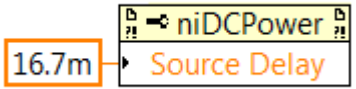
Default Values
Source Delay: 16.7 ms
Aperture Time: 16.7 ms

Source and Measure Cycle

NATIONAL INSTRUMENTS

Source Delay

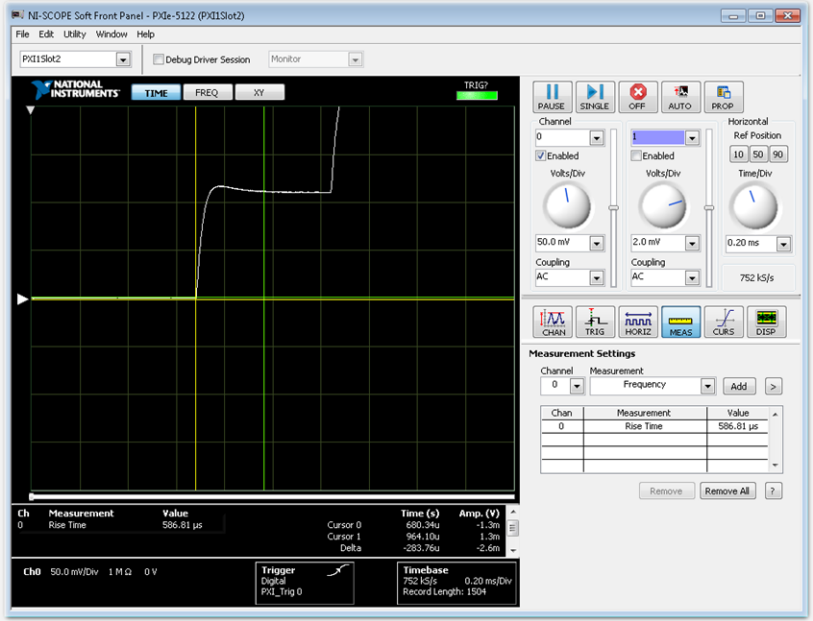




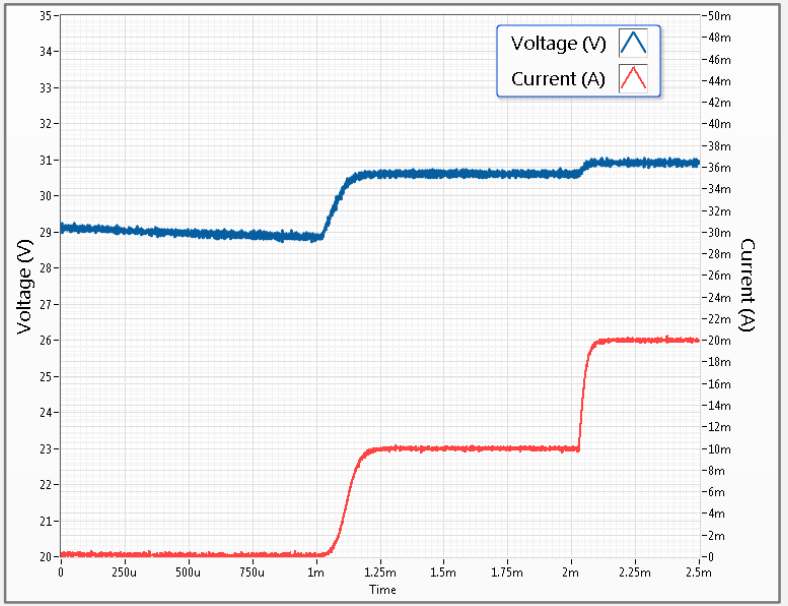
NATIONAL INSTRUMENTS

Determining Ideal Source Delay

Method 1: Oscilloscope



Method 2: SMU built-in digitizer

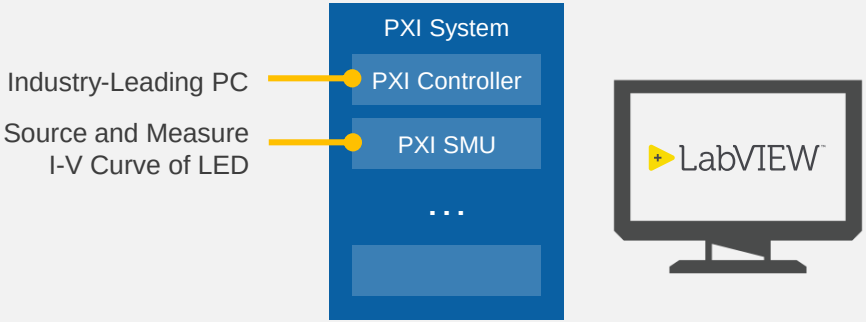


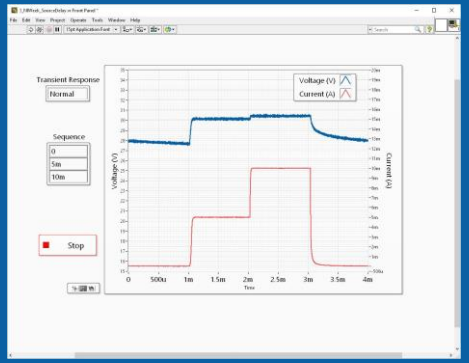
NATIONAL INSTRUMENTS

LED

Example
High-Power LED Array

PXI System and LabVIEW



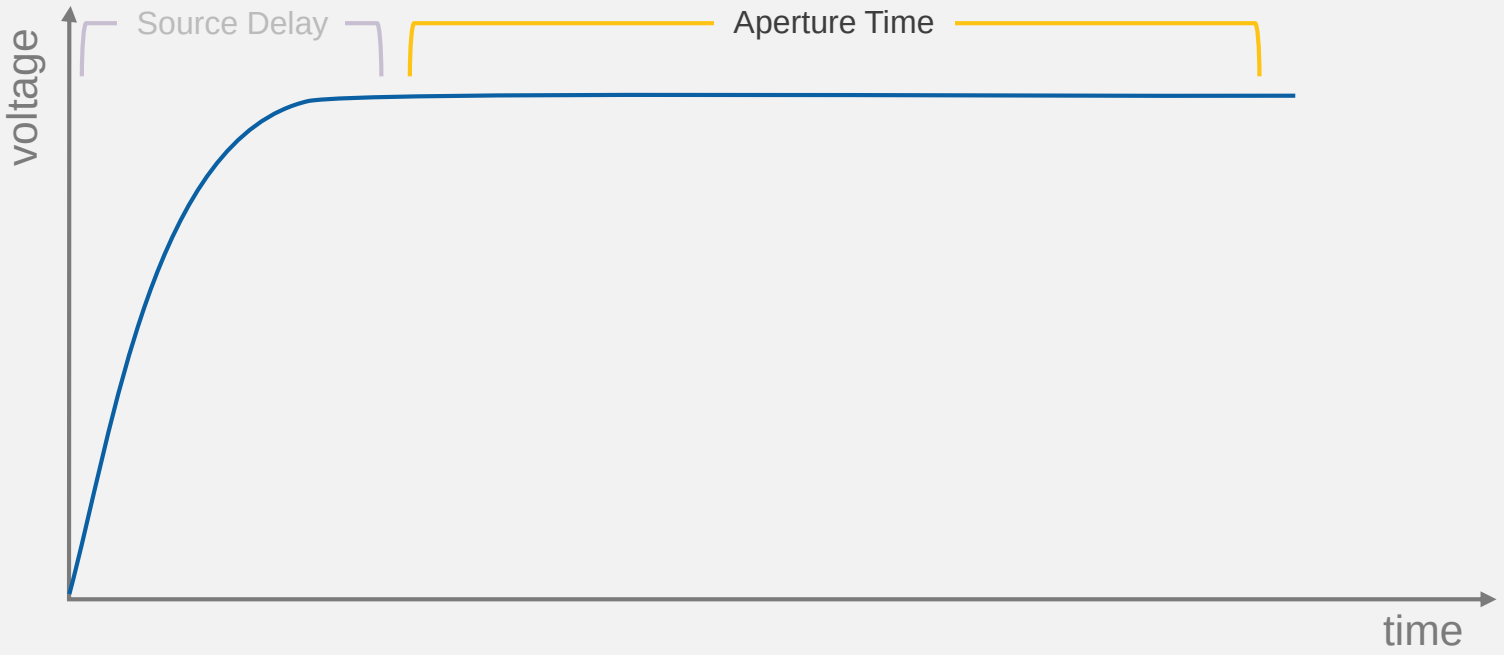


DEMO: SMU Source Delay

- Allow for signal to settle before the beginning of the measurement
- Optimize delay based on settling time
- Ensure high-quality measurements without extra delay
- Experiment with Slow, Normal, Fast transient response to improve settling time

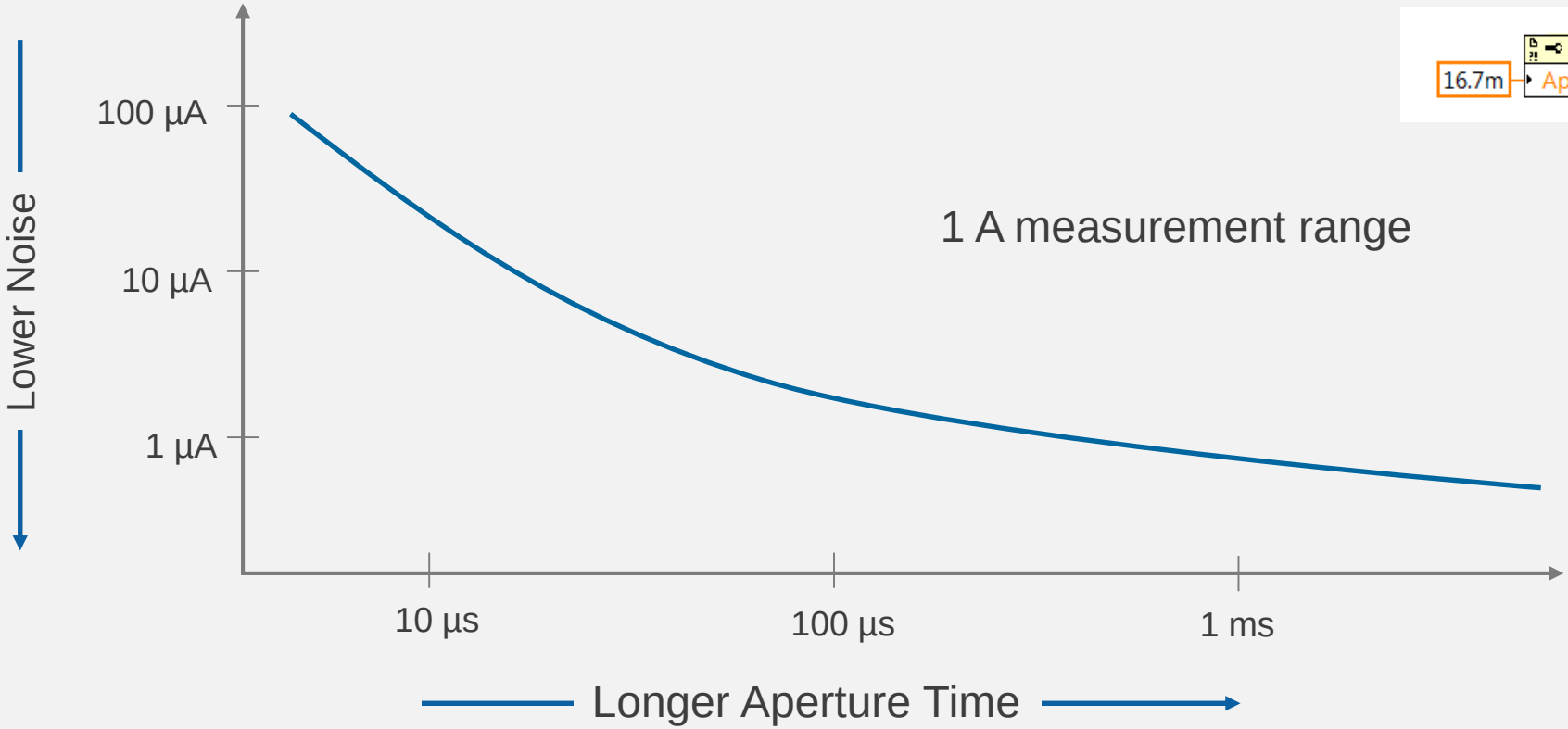
NATIONAL INSTRUMENTS

Source and Measure Cycle

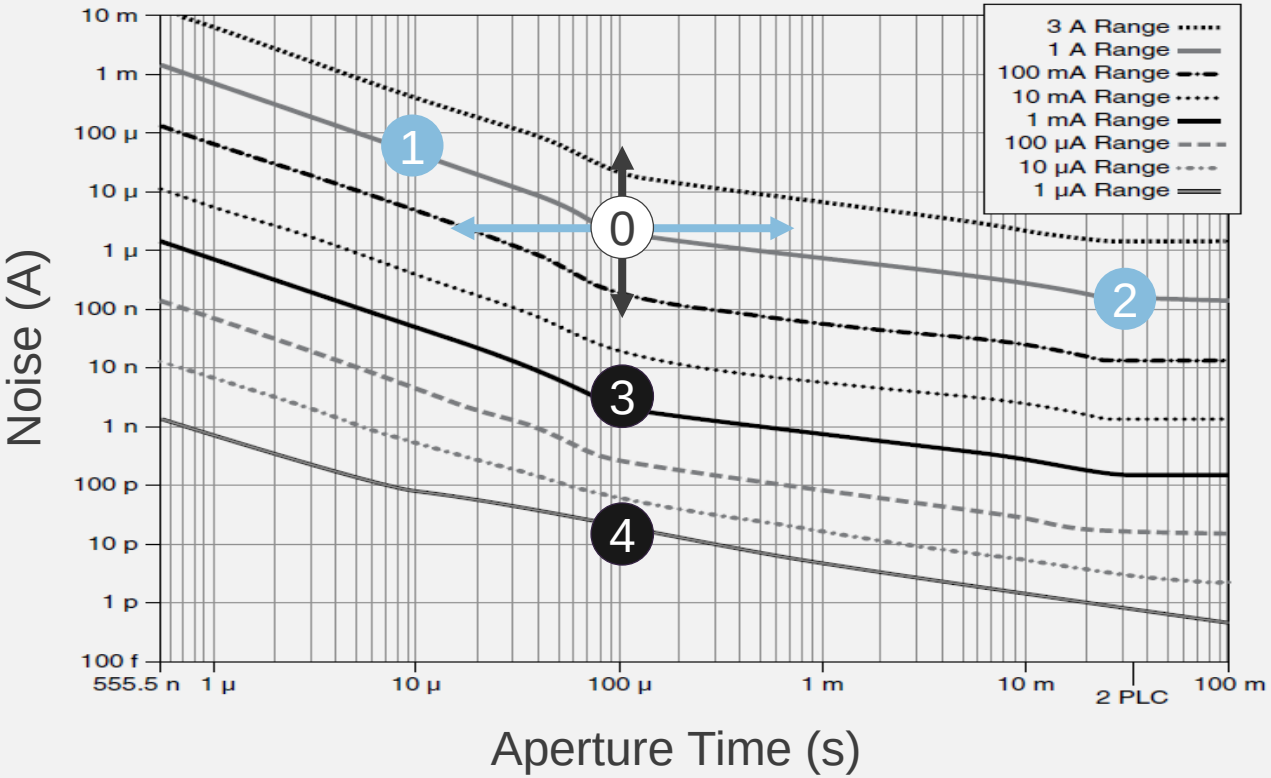


NATIONAL INSTRUMENTS

Property: Aperture Time



Noise Versus Aperture Time



Noise

0	1 µA
1	100 µA
2	100 nA
3	1 nA
4	10 pA

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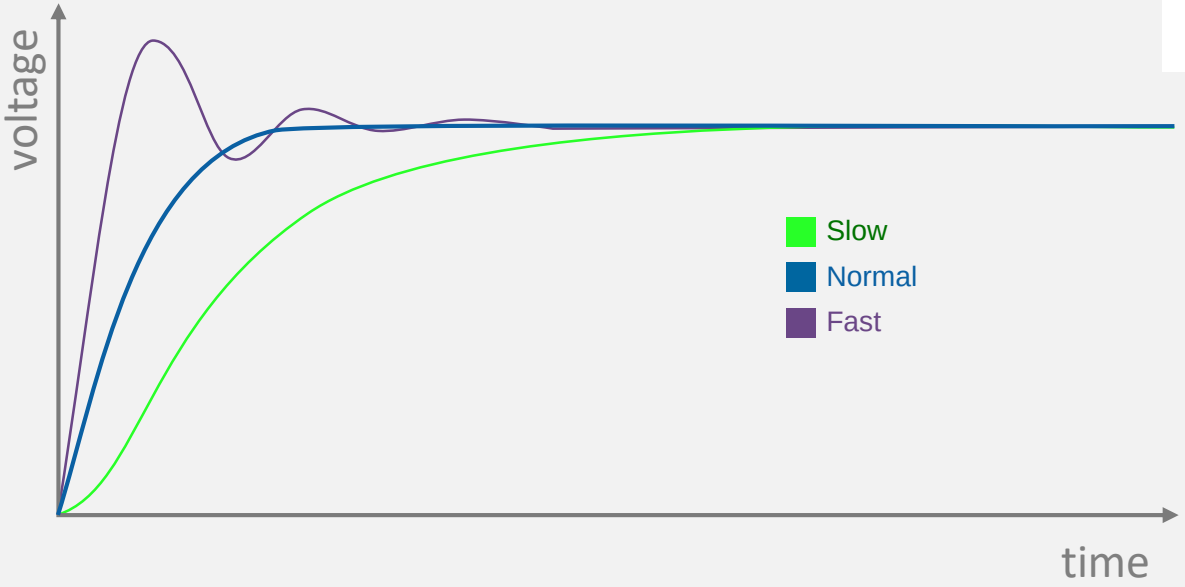
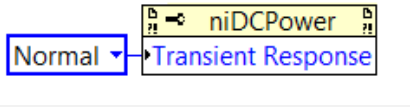
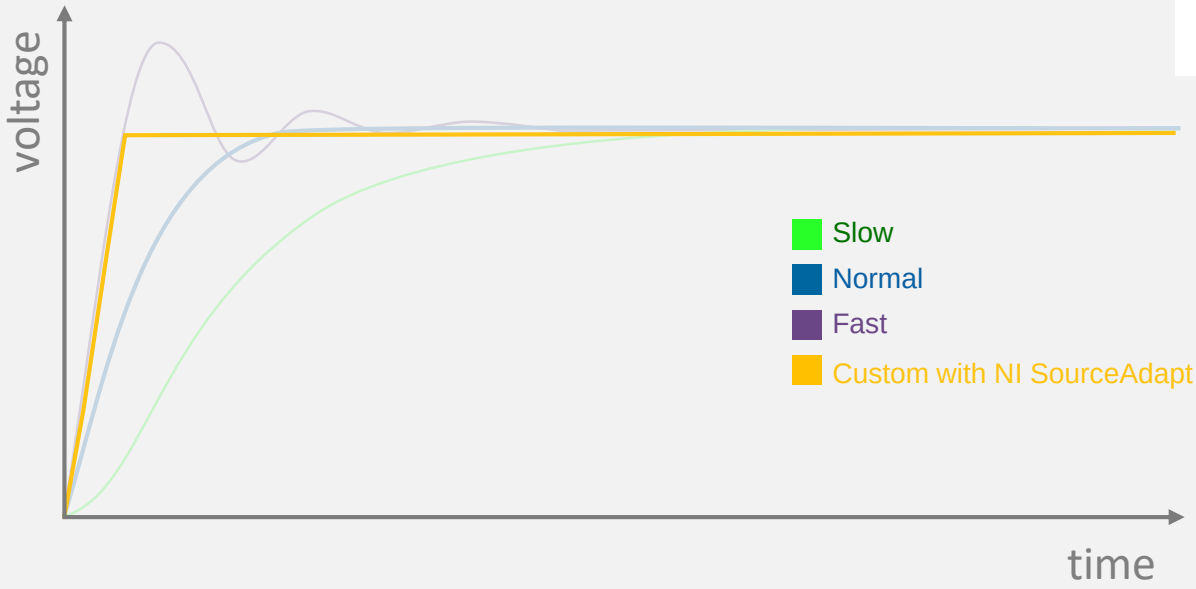
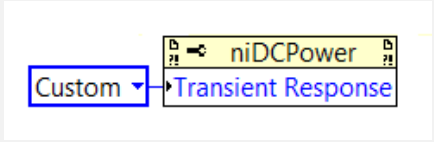
4. Transient Response and Rise Time



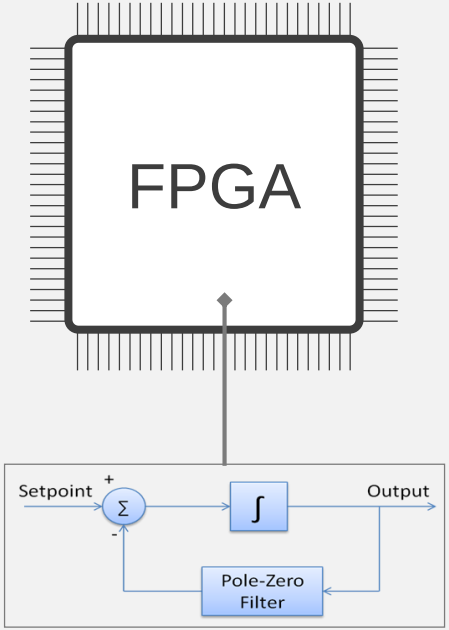


4. Transient Response and Rise Time





SourceAdapt: Digital Control Loop



ADC 1.8 MS/s

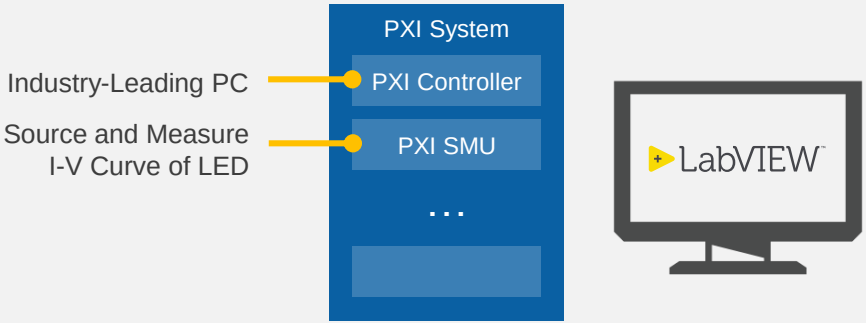
DAC 100 kS/s

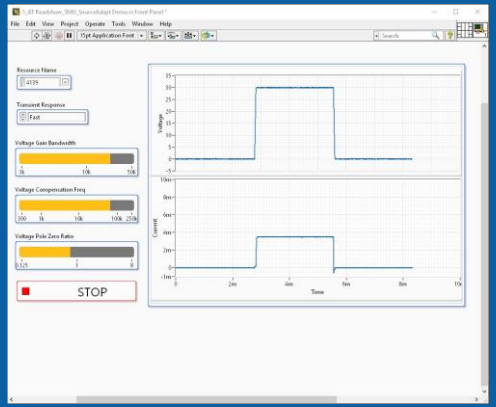
V/I CONTROL

Capacitor

Example
10 µF Capacitor

PXI System and LabVIEW



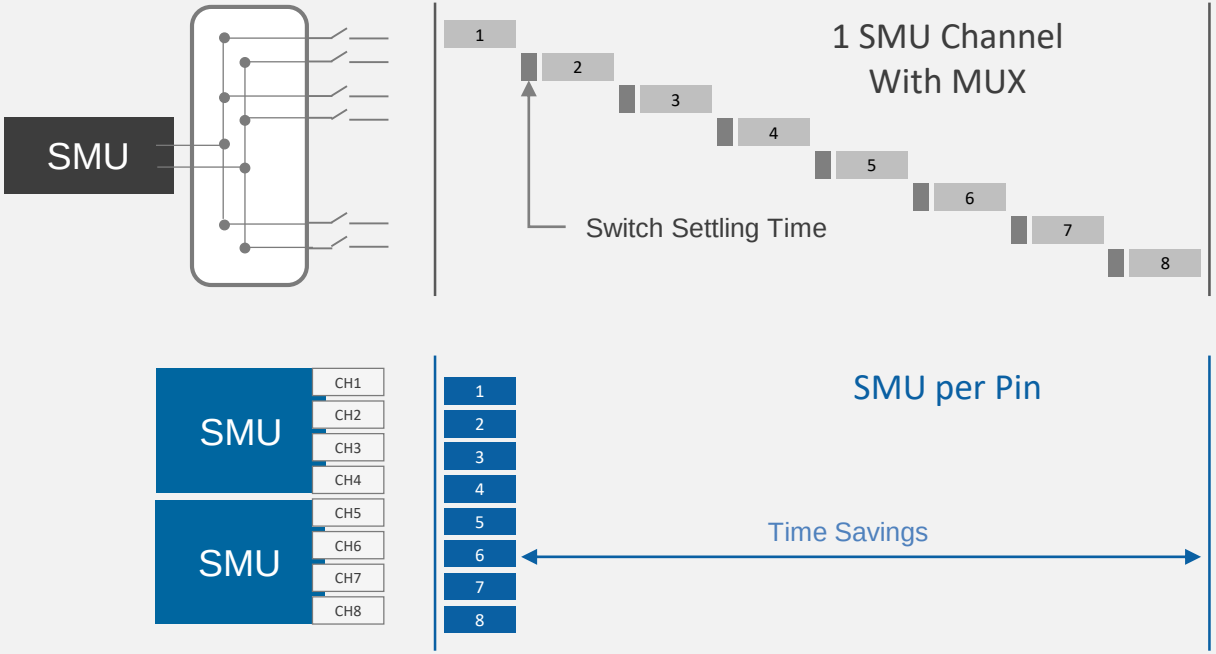


DEMO: SMU SourceAdapt

- Full control of transient response through software
- "Custom" setting gives you maximum control of rise time, overshoot, and oscillation
- Unique to NI SMUs

NATIONAL INSTRUMENTS

5. Parallel Versus Serial SMU Channels



24-Channel SMUs

400+ channels in PXI chassis
Parallel execution in LabVIEW and TestStand

NATIONAL INSTRUMENTS

Summary for Optimizing Test Time

1. Choose a low-latency bus
2. Implement efficient software or hardware sequencing
3. Reduce source delay and aperture time to achieve desirable noise performance and measurement speed
4. Optimize transient response for each DUT
5. Use multichannel SMU architecture and multithreaded application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