

Developing Monitoring and Control Systems with NI LabVIEW and NI CompactRIO

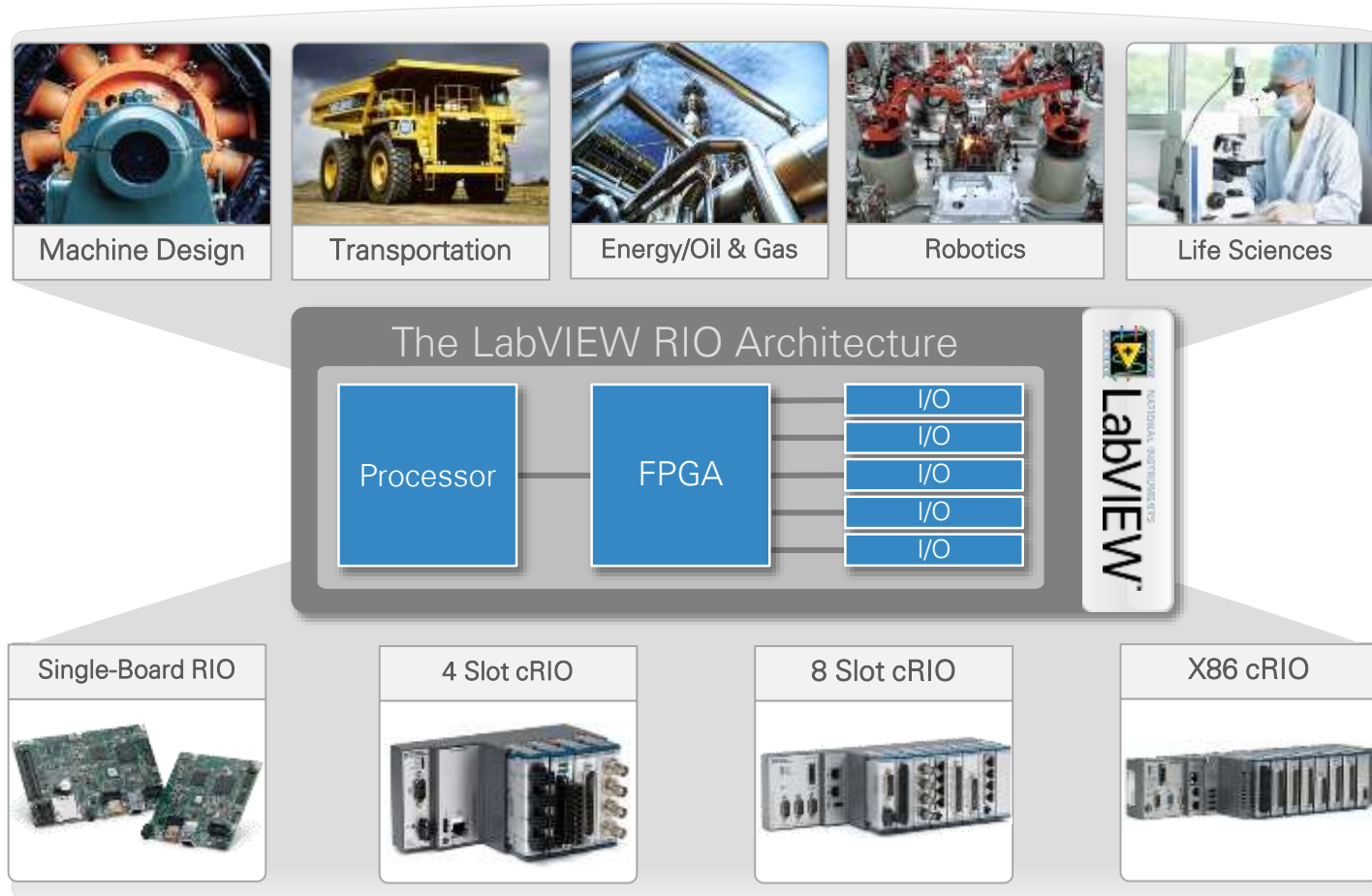


We all have a challenge to solve...



Graphical System Design

A platform-based approach for measurement and control



The NI CompactRIO System

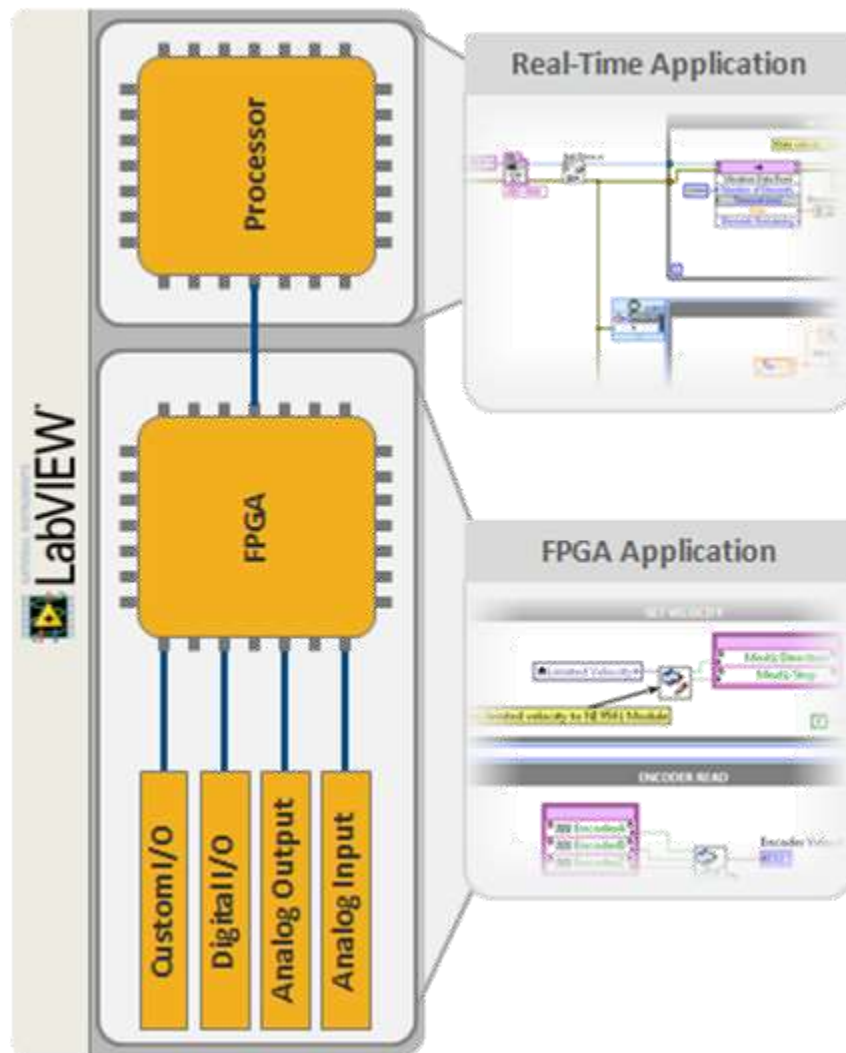
REAL-TIME
CONTROLLER

FPGA CHASSIS



MEASUREMENT
MODULES

The LabVIEW RIO Architecture



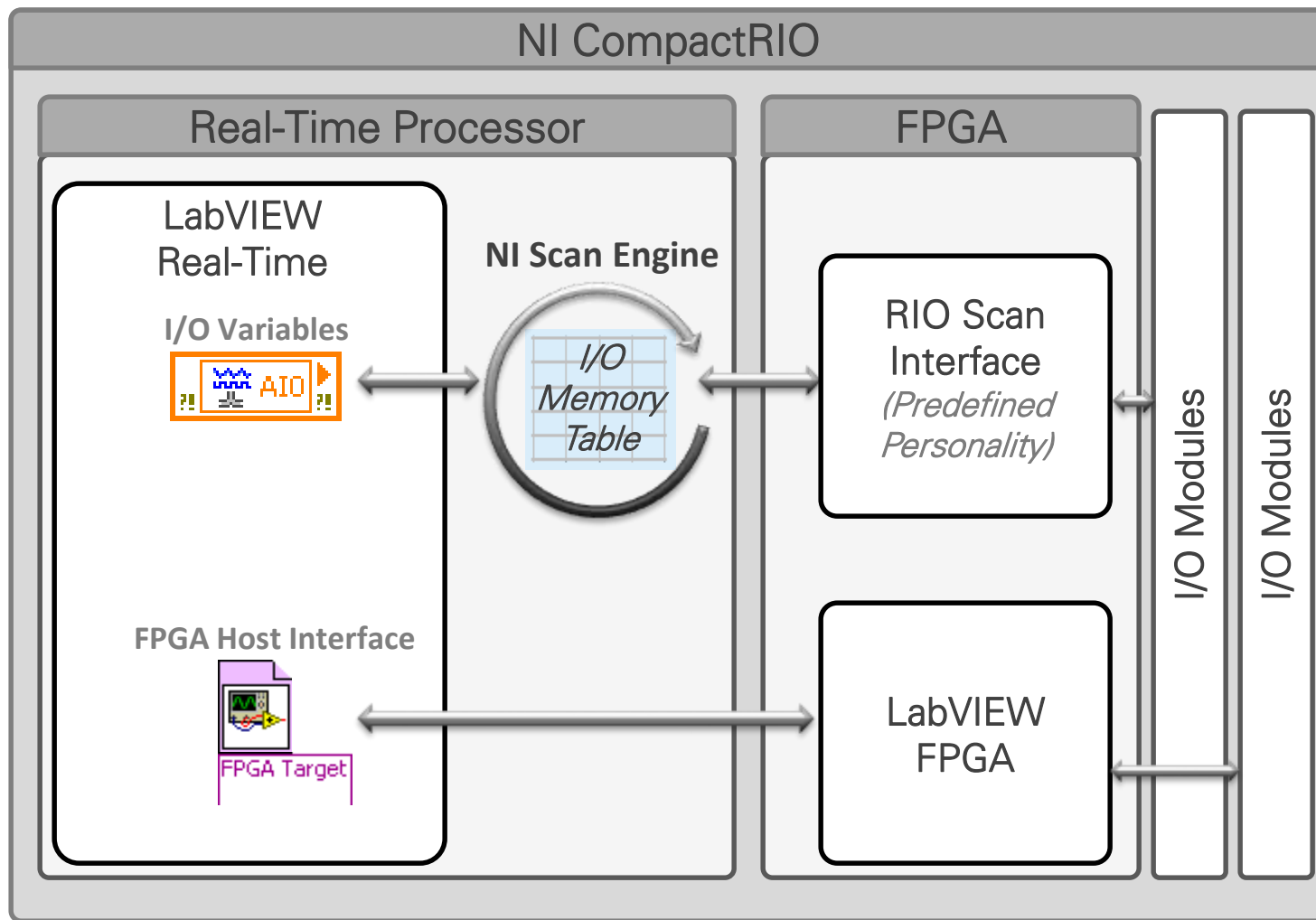
- Real-time OS
- Application software
- Networking and peripheral I/O drives
- DMA, interrupt, and bus control drivers

- Application IP
- Control IP
- DSP IP
- Specialized I/O drivers and interface
- DMA controller

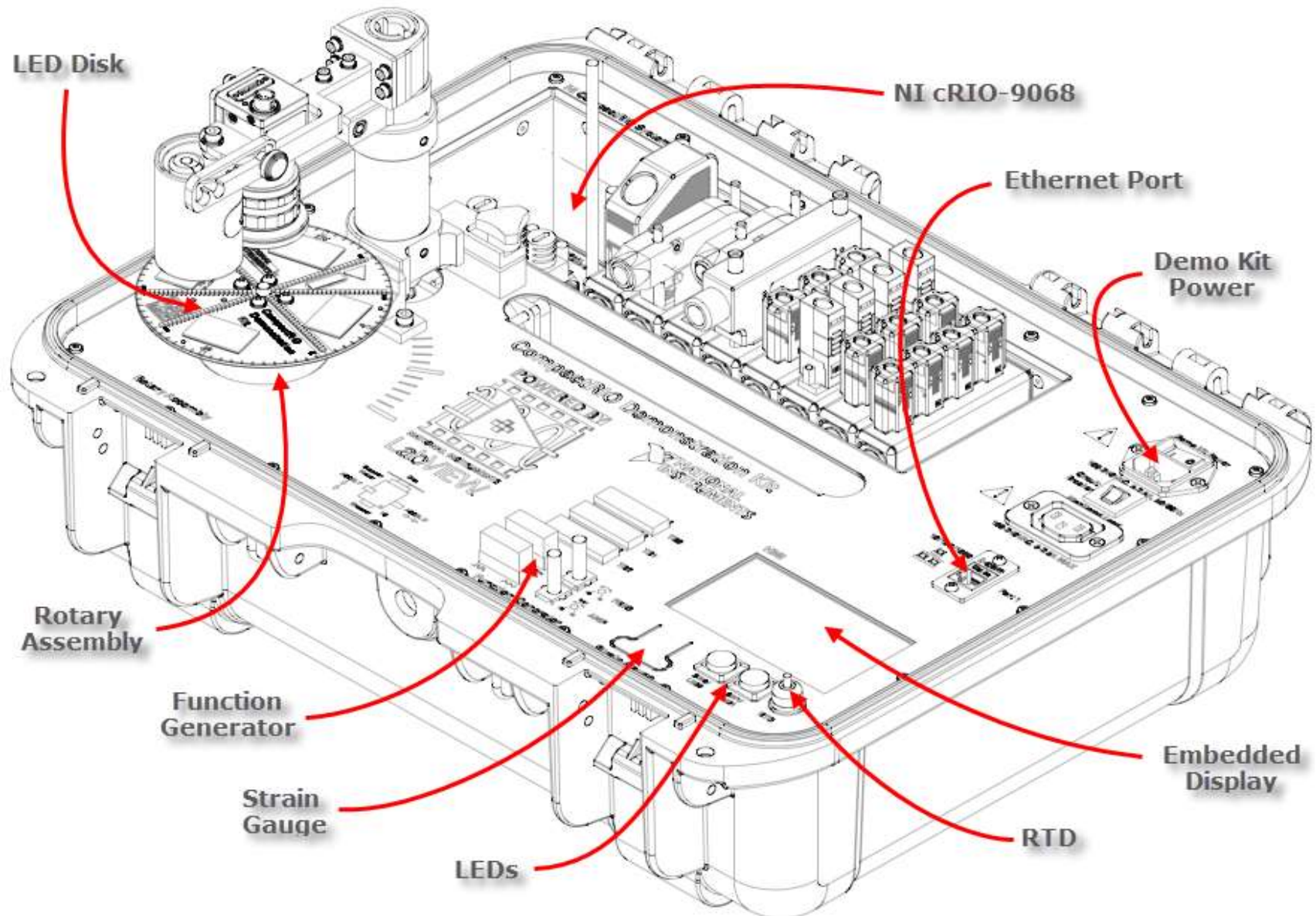
Operating System Characteristics

	<i>Loop Rate</i>	<i>Jitter</i>
General Purpose OS <ul style="list-style-type: none">• High-priority tasks can be preempted by lower-priority tasks• Extraneous background programs<ul style="list-style-type: none">- Screen savers, disk utilities, virus software, and so on• Peripheral Interrupts<ul style="list-style-type: none">- Mouse, keyboard, and so on	<i>10-100 Hz</i>	<i>Unbounded</i>
Real-Time OS <ul style="list-style-type: none">• Scheduler ensures high-priority tasks execute first• Direct control over all tasks• Stand-alone<ul style="list-style-type: none">• no mouse, keyboard, and so on	<i>Up to 50 kHz</i>	<i>Bounded</i>

LabVIEW Programming Model for CompactRIO

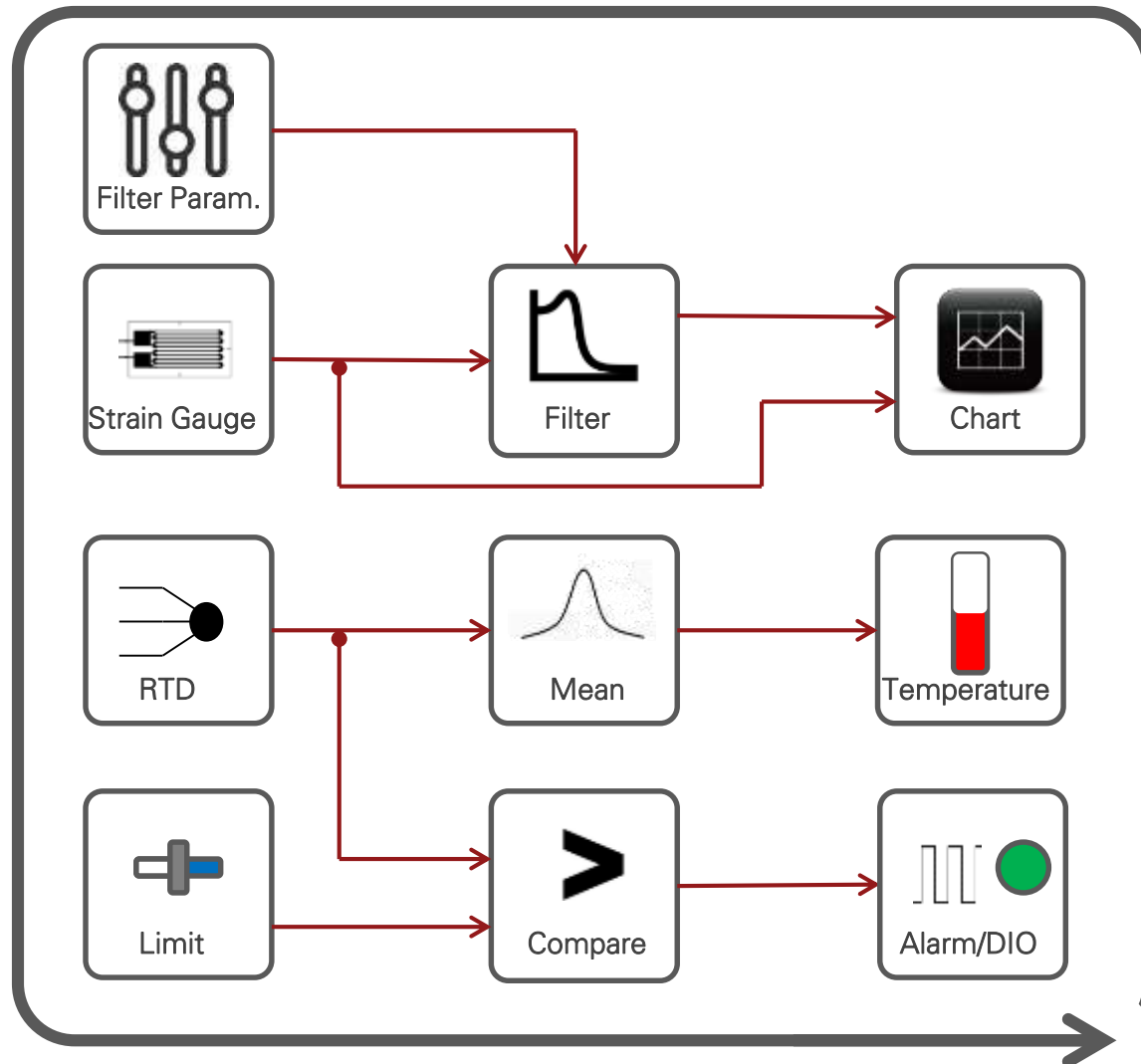


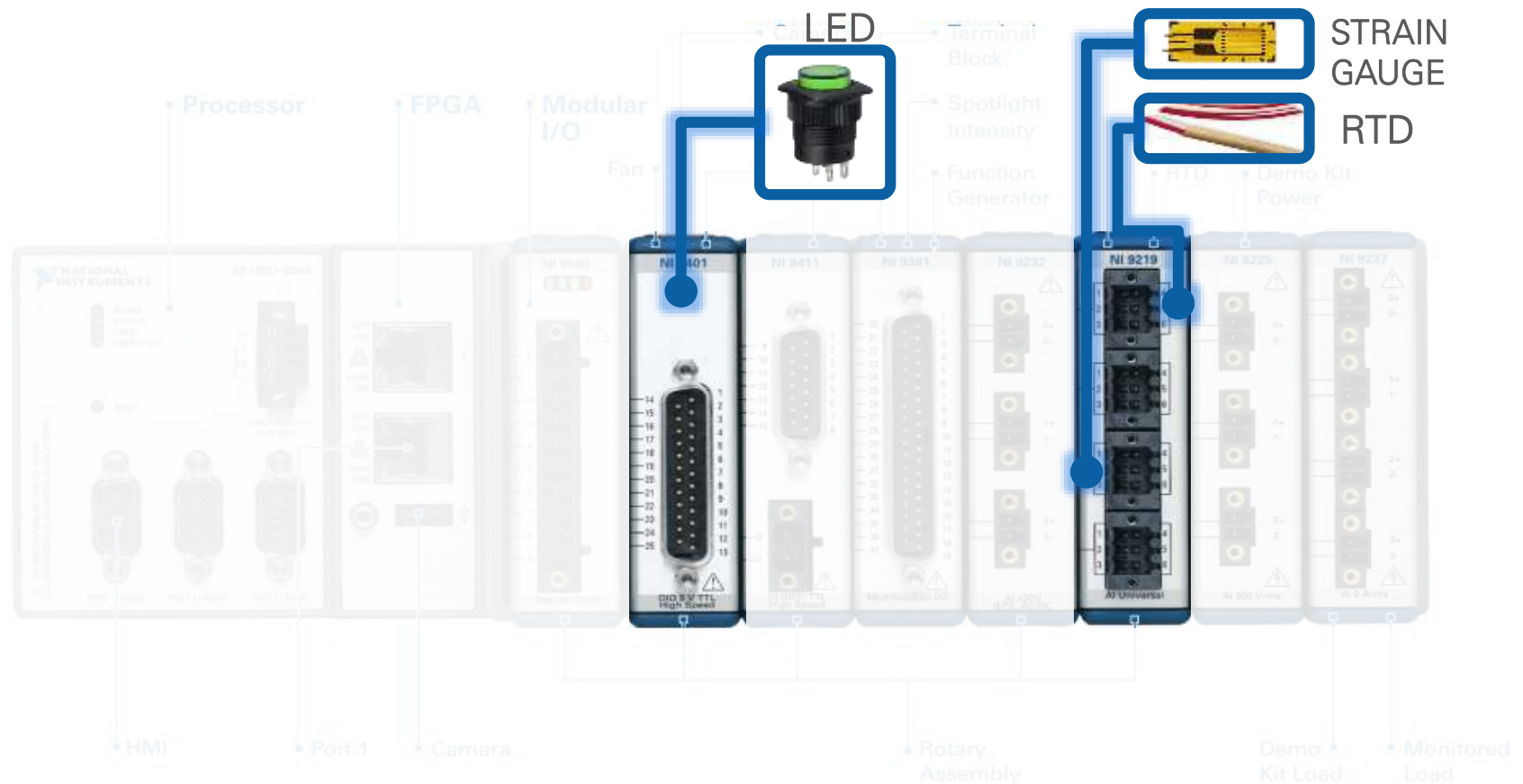
NI CompactRIO Demonstration Kit



Exercise

Temperature and Strain Monitoring





Inputs:

Slot 6: NI 9219—24 Bit Universal Analog Input
(4 DIFF · 100 S/s/ch)

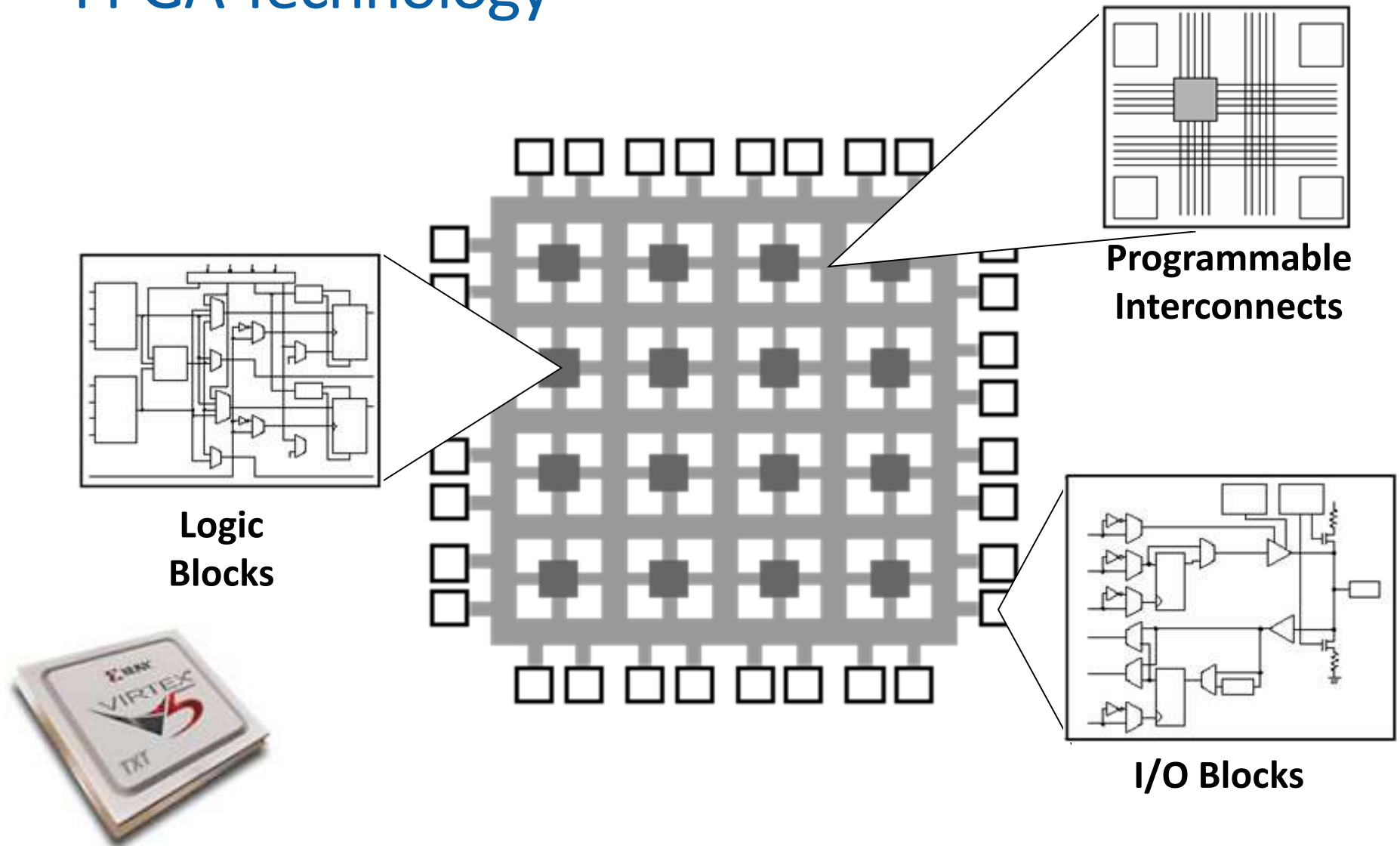
Analog Input 0 (AI0) → RTD
(3 Wire Pt100-TCR3851)

Analog Input 2 (AI2) → Strain Gauge
(Quarter Bridge / 350 Ohms)

Outputs:

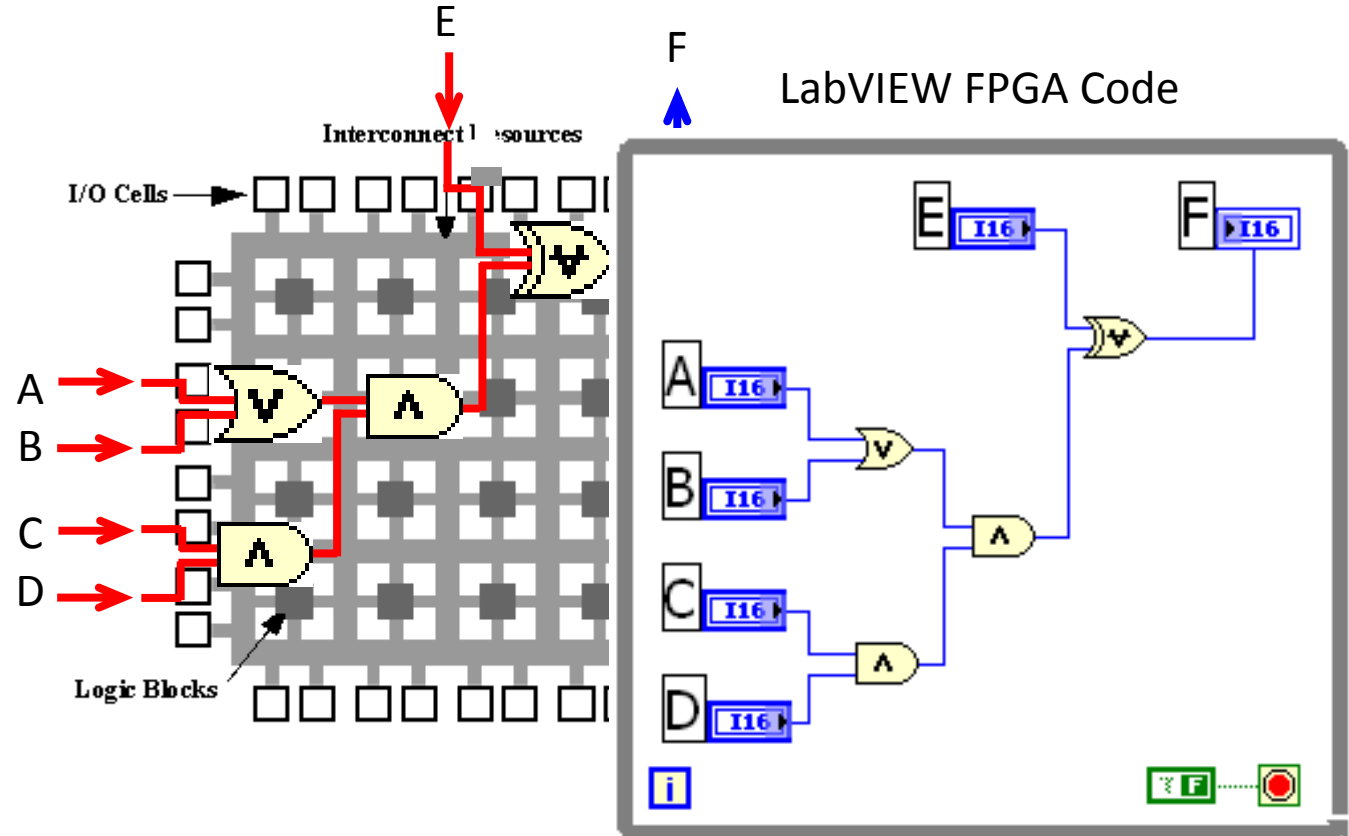
Slot 2: NI 9401—8 Ch, 5 V/TTL High-Speed
Bidirectional Digital I/O Module
Digital IO 5 (DIO5) → LED1

FPGA Technology

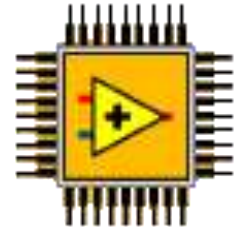


FPGA Logic Implementation

Implementing Logic on FPGA: $F = \{(A+B)CD\} \oplus E$



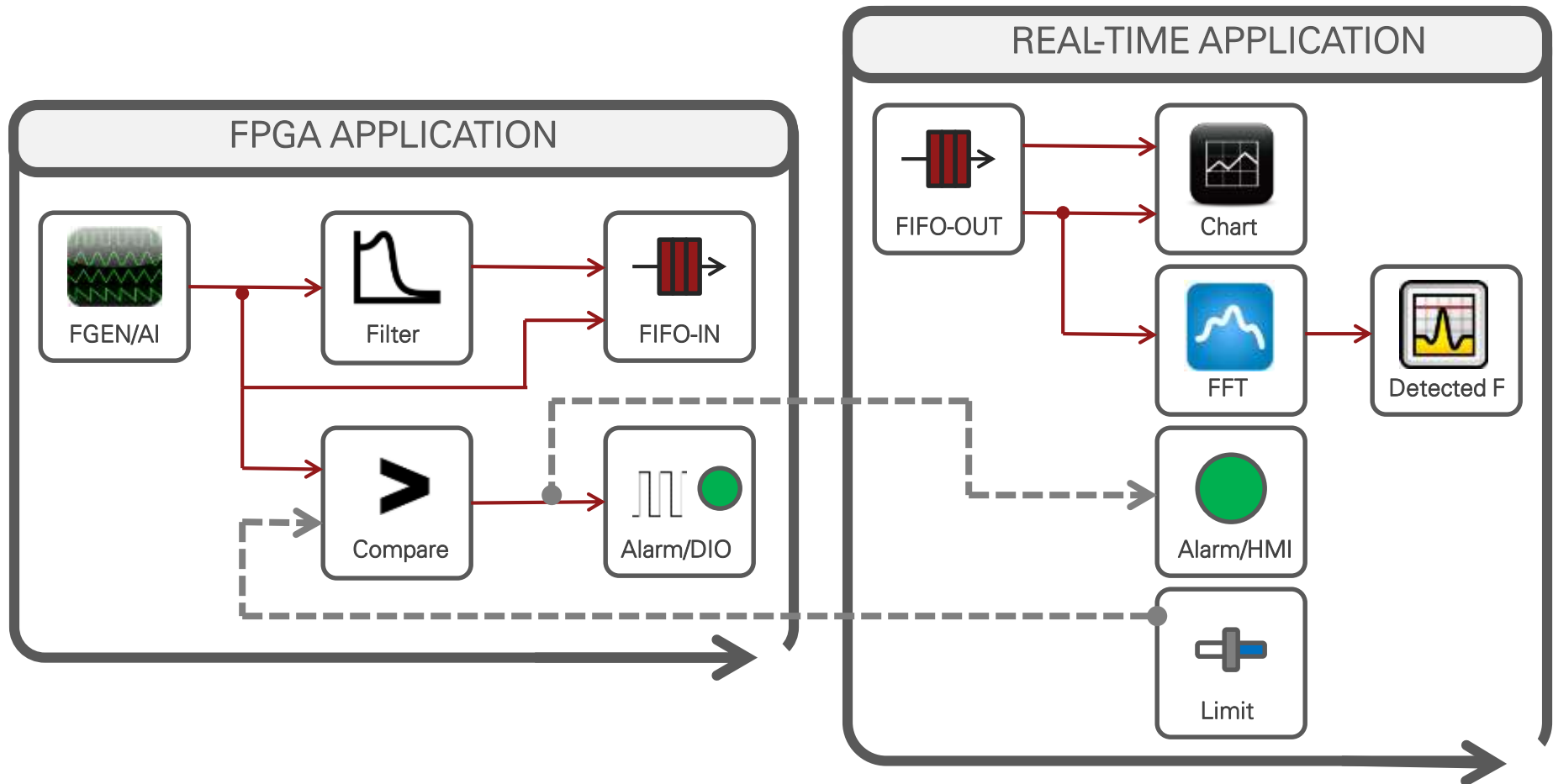
FPGA Technology Benefits

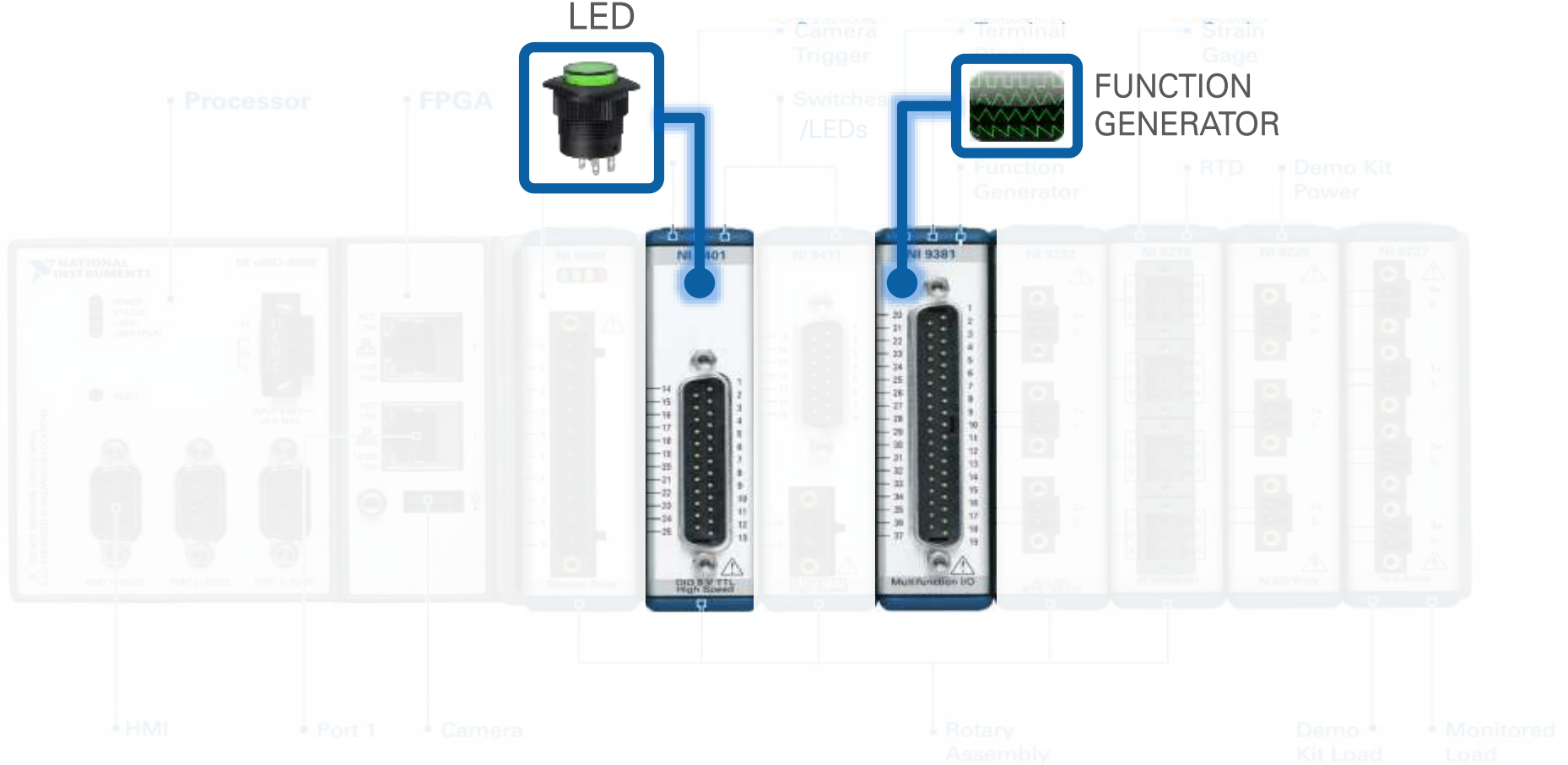


- **True Parallelism** – Enables parallel tasks and pipelining
- **High Reliability** – Designs become a custom circuit
- **High Determinism** – Runs algorithms at deterministic rates down to 25 ns (faster in many cases)
- **Reconfigurable** – Create new and alter existing task-specific personalities

Exercise

FPGA-Based Butterworth Filter





Inputs:

Slot 4: NI 9381— 0 V to 5 V AI/AO Module With 4 LVTTTL DIO Lines

Mod4/AI7→Function Generator

Sampling Period→ 20 kS/s

Resolution→12-bit

Outputs:

Slot 2: NI 9401— 8 Ch, 5 V/TTL High-Speed Bidirectional Digital I/O Module

Digital IO 4 (DIO4)→LED0

CompactRIO Developer's Guide

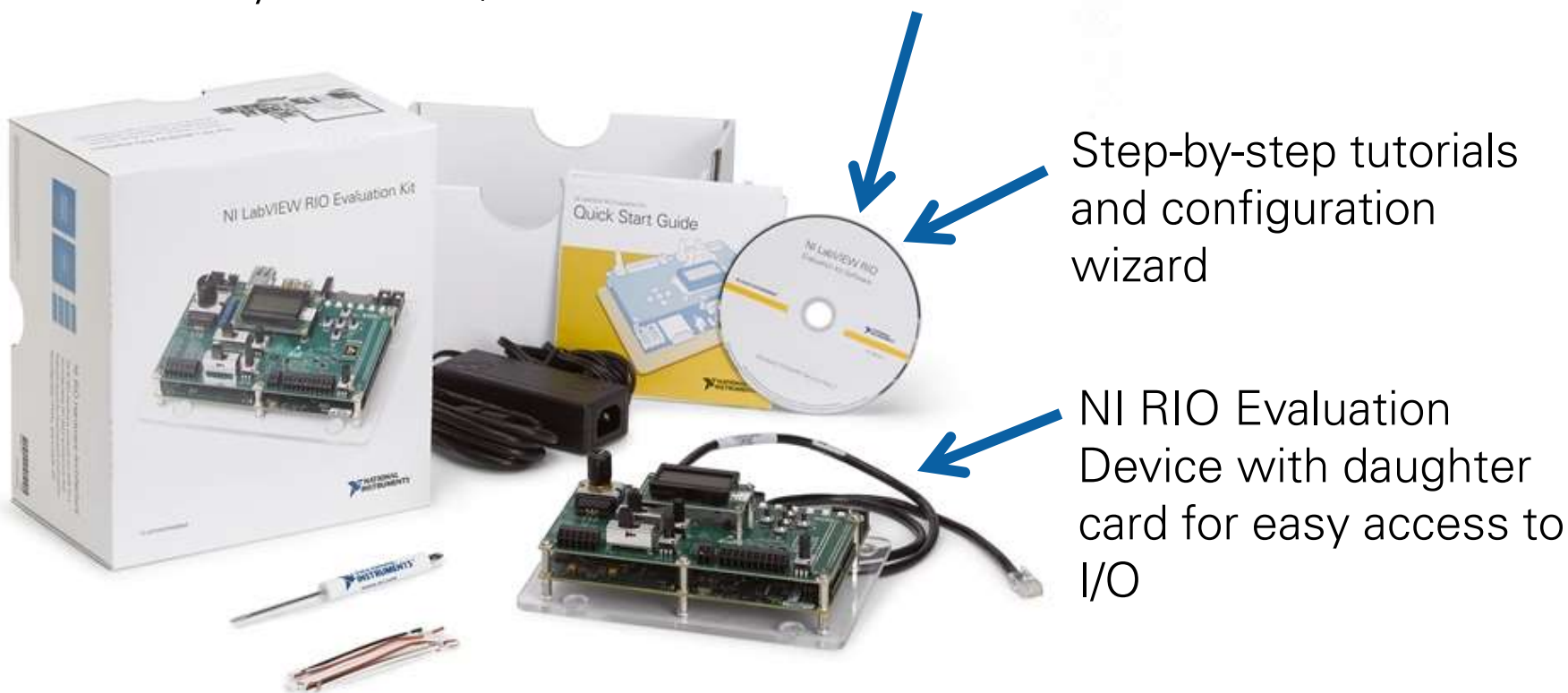
NI LabVIEW for CompactRIO Developer's Guide

Recommended LabVIEW Architectures and Development Practices
for Control and Monitoring Applications

<http://www.ni.com/compactriodevguide/>

NI LabVIEW RIO Evaluation Kit

90-day LabVIEW, LabVIEW FPGA & LabVIEW Real-Time evaluation



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wizard

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- LabVIEW FPGA
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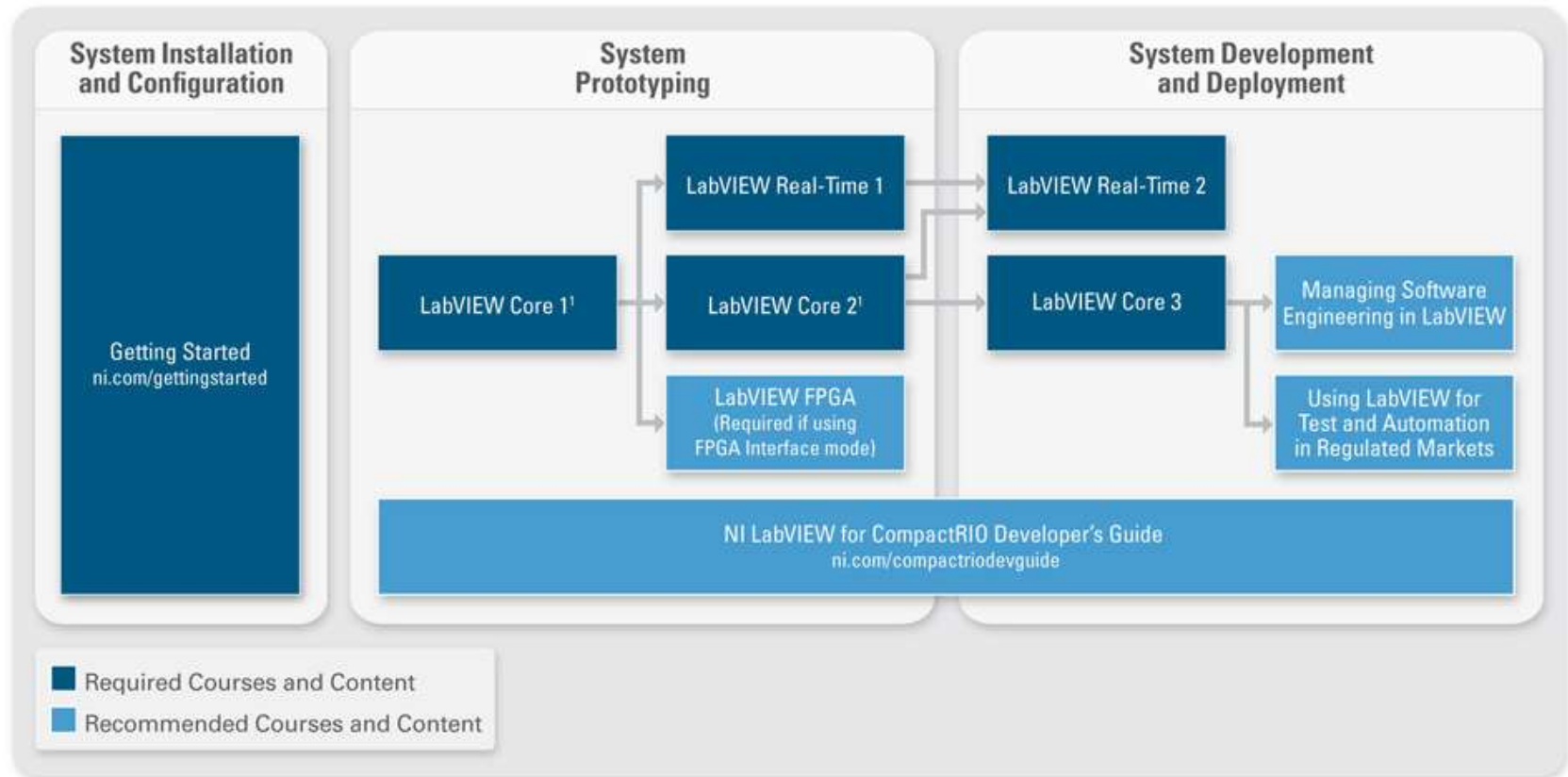
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