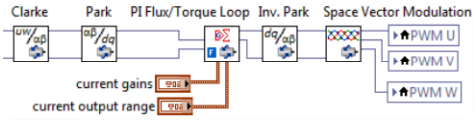
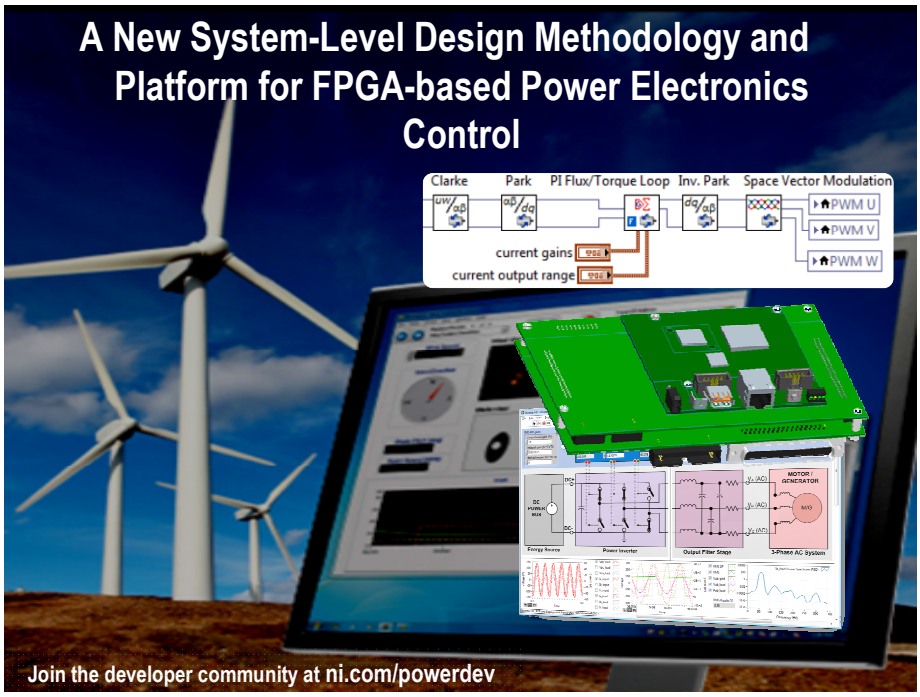


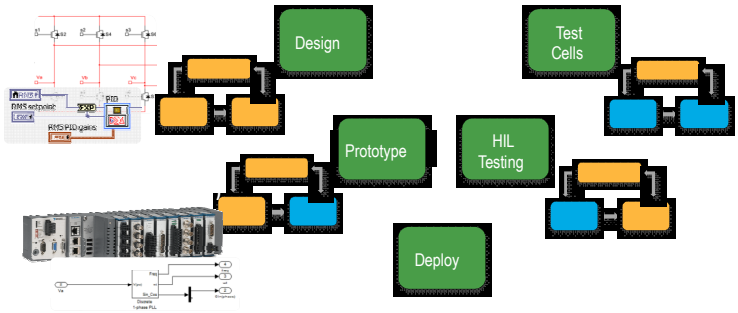
Design Tutorial

Smart Grid Control Systems

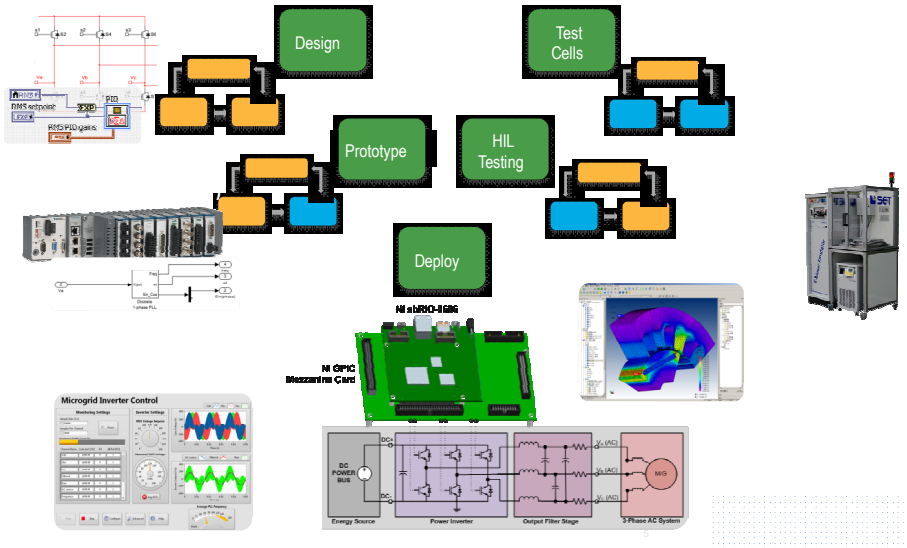
A New System-Level Design Methodology and Platform for FPGA-based Power Electronics Control



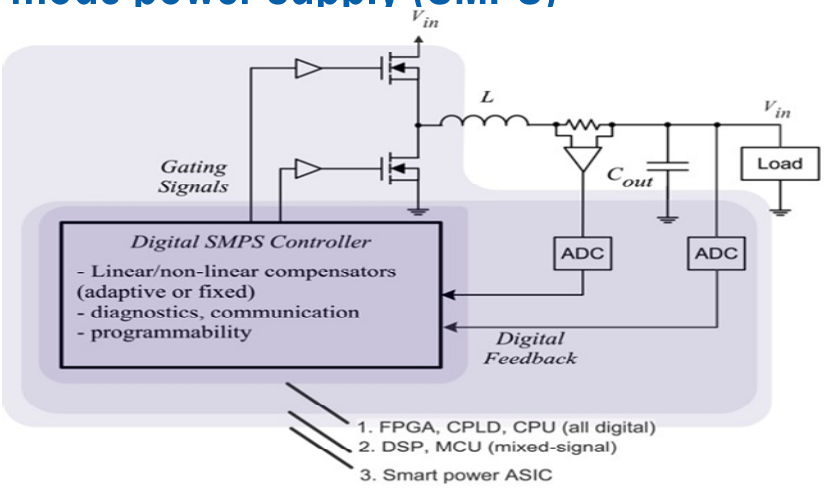
NI Vision for Power Electronics



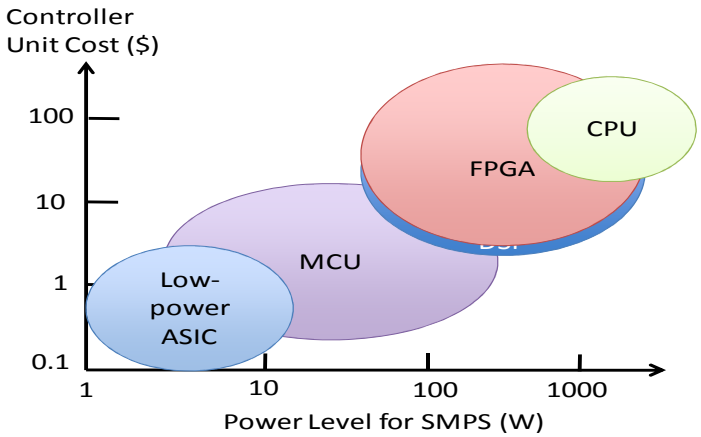
NI Vision for Power Electronics



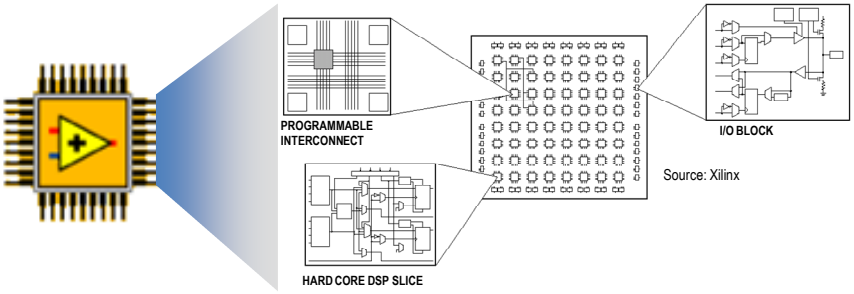
Generic digitally-controlled switched-mode power supply (SMPS)



Spectrum of suitable control targets for high volume mass production



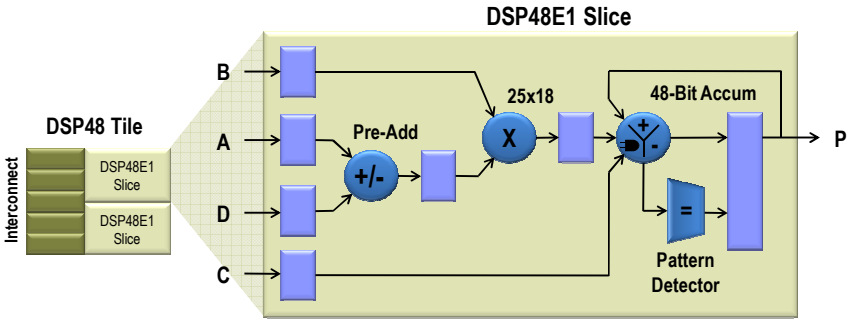
What is an FPGA?



Field Programmable Gate Array (FPGA)

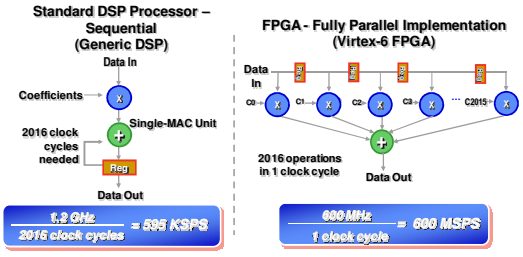
DSP Performance through the DSP48E1 Slice

Virtex-6, Artex-7, Kintex-7, Virtex-7

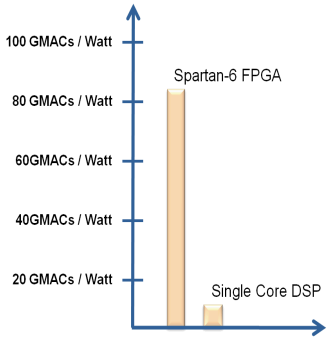


- 2 DSP48E1 Slices / Tile
- Input Flexibility through 5 Shared interconnect
- 638 MHz Fmax
  - 20% faster than competing FPGAs

Modern FPGAs utilize hard-core DSP processing elements integrated in fabric



Performance per Chip



Performance per Watt

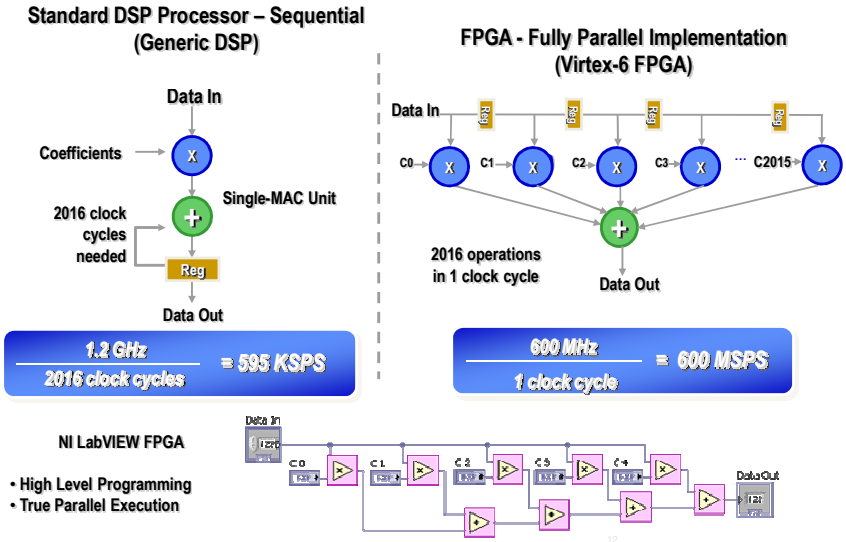
Modern FPGAs are often lower cost per MAC compared to single-core processors and DSPs

Part	Description	DSP Performance	MACs/$*
DSP A	32-bit, 100 MHz, fixed pt	100 MMACs	6.48e6
DSP B	300 MHz, fixed pt	600 MMACs	6.98e6
Xilinx Spartan-6 LX45 FPGA	FPGA, 250 MHz, fixed pt, 58 DSP48A1 multipliers	22,600 MMACs (250 MHz) 4,600 MMACs (40 MHz)	5.58e8 8.85e7

* Multiply-accumulate (MAC) operations per dollar

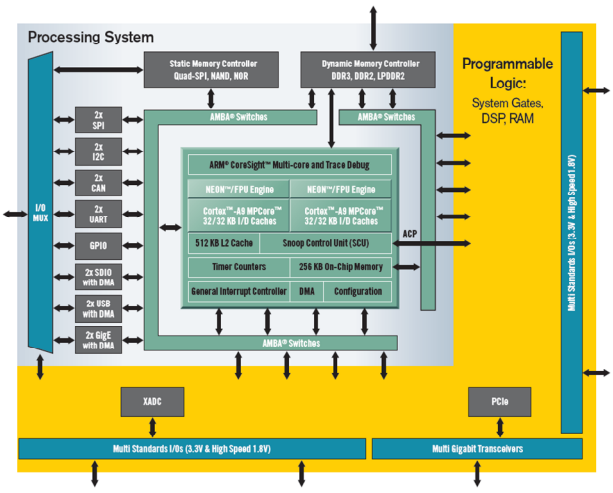
Performance per Dollar

Sequential vs. Parallel DSP Processing



The Next Paradigm: Floating Point Processors Integrated in FPGA Fabric

ZYNQ EXTENSIBLE PROCESSING PLATFORM



The Next Paradigm: Floating Point Processors Integrated in FPGA Fabric

ZYNQ EXTENSIBLE PROCESSING PLATFORM

Zynq-7000 Product Table (Software View)

	Device Name	Z-7010	Z-7020	Z-7030	Z-7045
	Part Number	XC7Z010	XC7Z020	XC7Z030	XC7Z045
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™			
	Processor Extensions	NEON™ and Single/Double Precision Floating Point			
	Maximum Frequency	800 MHz			
	L1 Cache	32 KB Instruction, 32 KB Data per processor			
	L2 Cache	512 KB			
	On-Chip Memory	256 KB			
	External Memory Support	DDR3, DDR2, LPDDR2			
	External Static Memory Support	2x QSPI-SPI, NAND, NOR			
	DMA Channels	8 (4 dedicated to Programmable Logic)			
	Peripherals	2x USB 2.0 (OTG) w/DMA, 2x Tri-mode Gigabit Ethernet w/DMA, 2x SD/SDIO w/DMA, 2x UART (2), 2x CAN2.0B, 2x I2C, 2x SPI, 4x 32b GPIO			
	Security	AES and SHA 256b for secure boot			
	Peripherals and Static Memory Multiplexed I/O[1]	54			
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave, 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts			
Programmable Logic	Xilinx 7 Series Programmable Logic Equivalent	Artix™-7 FPGA	Artix™-7 FPGA	Kintex™-7 FPGA	Kintex™-7 FPGA
	Programmable Logic Cells (Approximate ASIC Gates[3])	28K Logic Cells (~430K)	85K Logic Cells (~1.3M)	125K Logic Cells (~1.9M)	350K Logic Cells (~5.2M)
	Extensible Block RAM (# 36 Kb Blocks)	240KB (60)	560KB (140)	1,060KB (265)	2,180KB (545)
	Programmable DSP Slices (18x25 MACCs)	80	220	400	900
	Peak DSP Performance (Symmetric FIR)	58 GMACS	158 GMACS	480 GMACS	1080 GMACS
	PCI Express® (Root Complex or Endpoint)	—	—	Gen2 x4	Gen2 x8
	Agile Mixed Signal (AMS)/XADC	2x 12 bit, 1 MSPS ADCs with up to 17 Differential Inputs			
	Security	AES and SHA 256b for secure configuration			
	Multi-Standards 3.3V I/O[2]	100	200	250	350
	Serial Transceivers[2]	—	—	4	16

Notes:
1. Static memory interface combined with the usage of many peripherals could require more than 54 I/Os. A designer can use the Programmable Logic I/Os.
2. Total Number of I/O and Transceivers depends on package used.
3. Equivalent ASIC gate count is dependent of the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.
4. Preliminary product information. Subject to change. Please contact your Xilinx representative for the latest information.

14

Requirements for System Level Methodology and Platform

This section examines the application-specific needs of SMPS designers and researchers in regards to system-level FPGA programming tools and introduces a new platform developed through significant commercial R&D effort in consultation with researchers and commercial design engineers.

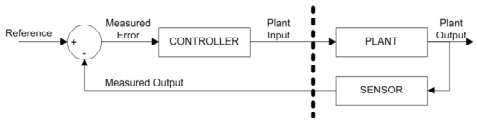
15

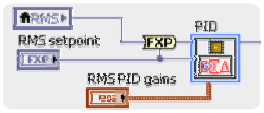
A New Platform and Methodology for System-Level Design of Next-Generation FPGA-based Digital SMPS

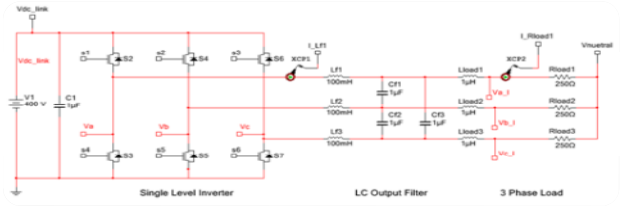
1. The system-level FPGA design tool must integrate with a full-featured power electronics circuit simulator
2. The software development flow should be bi-directional rather than unidirectional
3. The FPGA resource utilization efficiency must be comparable to hand written register transfer level (RTL) code
4. The FPGA code used in the final target must be exactly identical to the code used for design validation simulations
5. The tool must include fixed-point math blocks and power electronics IP libraries that enable efficient development of fixed-point control, signal processing and power analysis algorithms.

A New Platform and Methodology for System-Level Design of Next-Generation FPGA-based Digital SMPS

6. The tool must target pre-validated COTS control boards which meet the specific control, I/O and performance and cost needs of modern high volume commercial SMPS products
7. The tool should also be suitable for developing fast, real-time hardware-in-the-loop (HIL) SMPS simulators for the purpose of enabling comprehensive validation of the production control system







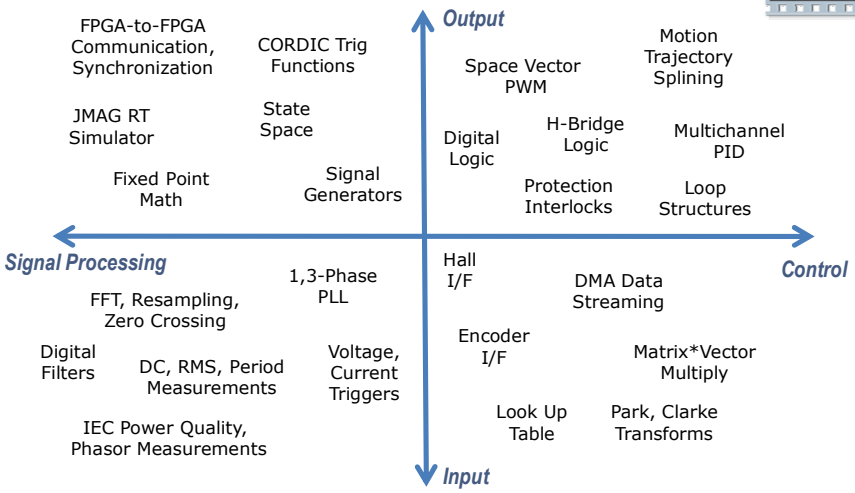
NEW PLATFORM AND METHODOLOGY

DEMONSTRATION

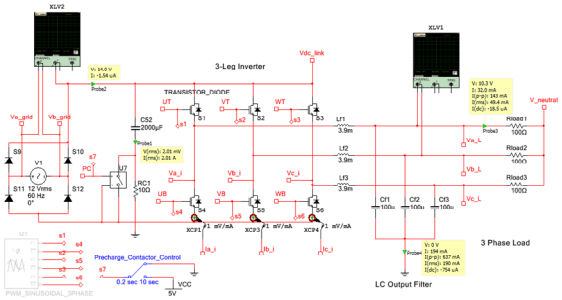
New! LabVIEW Electrical Power Measurement Suite

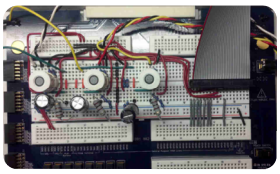
Voltage and Current	Power and Energy	Power Quality
Three Phase RMS (V and I)	Power per Phase	Voltage Sag (dip)
THD	Three Phase or Total	Voltage Swell
Harmonic (up to 64th)	Power Factor	Impulsive Transient (V + I)
Interharmonics (0.5 to 63.5th)	Active Power Total	Oscillatory Transient (V + I)
Voltage Unbalance	Active Power Harmonic	Overvoltage and undervoltage
Frequency Oscillation	Apparent Power Total	Overcurrent
Flicker	Apparent Power Harmonic	Phasor Imbalance
DC Portion	Reactive Power	Three Phase Voltage Harmonic
	Reactive Power Harmonic	Four Current Harmonic
	Energy Active Total	Harmonic per sec and per cycle
	Energy Apparent Total and +/-	Synchrophasor IEEE-C37.118
	Energy Reactive Total and L/C	

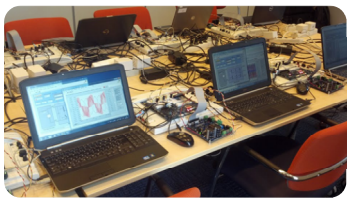
LabVIEW FPGA Power Electronics IP

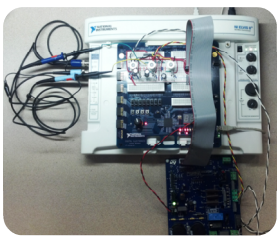


Three Phase Inverter: Co-Simulation vs. Physical Measurements



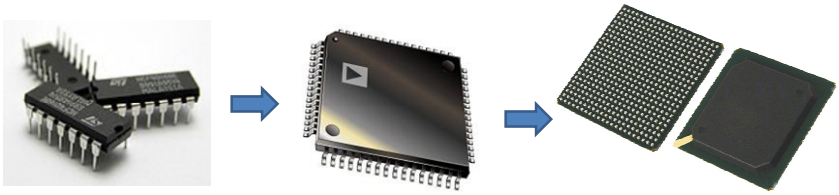






The Problem with Embedded Design

1. Moore's Law
   - Transistor count doubles every 18 months
   - Performance per dollar doubles every 11 months
   - Full custom embedded design takes 13 months
   - Number of pins on the devices increases with the number of transistors > PCB layout increasingly complex, risky, costly



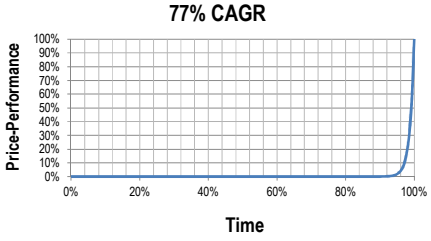
DIP Package | Low Profile Quad Flat Package | Ball Grid Array (BGA) Package

Performance per dollar

Moore's Law

PRICE-PERFORMANCE = PERFORMANCE / PRICE

41% CAGR / 53% CAGR = 77% CAGR (11 MONTHS)

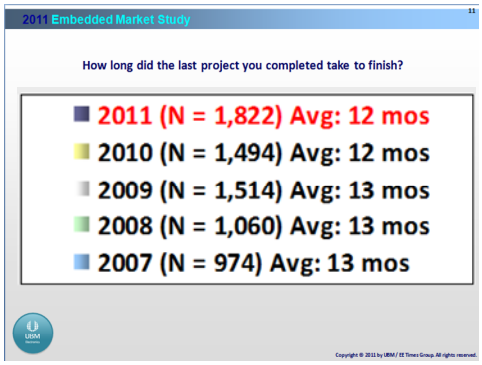


Full custom development time is not improving: 12-13 months since 2007

UBM Electronics

2011
EMBEDDED MARKET STUDY

EE Times
Embedded Systems Design
Embedded.com

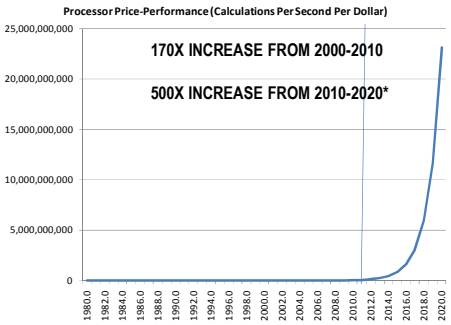


Full custom development cost & risk is not improving: 2009-2011 data

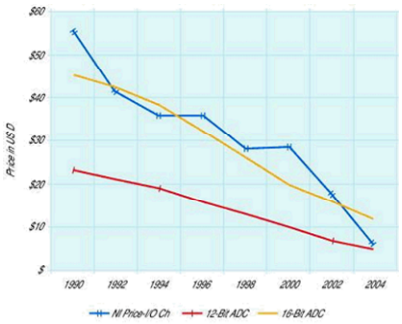
- Average of 15 engineers/project:
  - 7 software engineers (± 1.9 standard deviation)
  - 5 hardware engineers (± 0.6 standard deviation)
  - 3 firmware engineers (± 0.8 standard deviation)
- 57% of projects finished late (no change from 2009-2011):
  - 43% of all projects finished on or ahead of schedule
- What will be your greatest technology challenges next year (managers only):
  1. Integrating new technology or tools
  2. Managing code size/complexity
  3. Building higher quality development process

Managing Moore's Law

- Leveraging COTS technology keeps your business "on the curve", delivering exponentially increasing price-performance



Moore's Law for Processors and FPGAs



Moore's Law for analog to digital converters (ADCs)- historical

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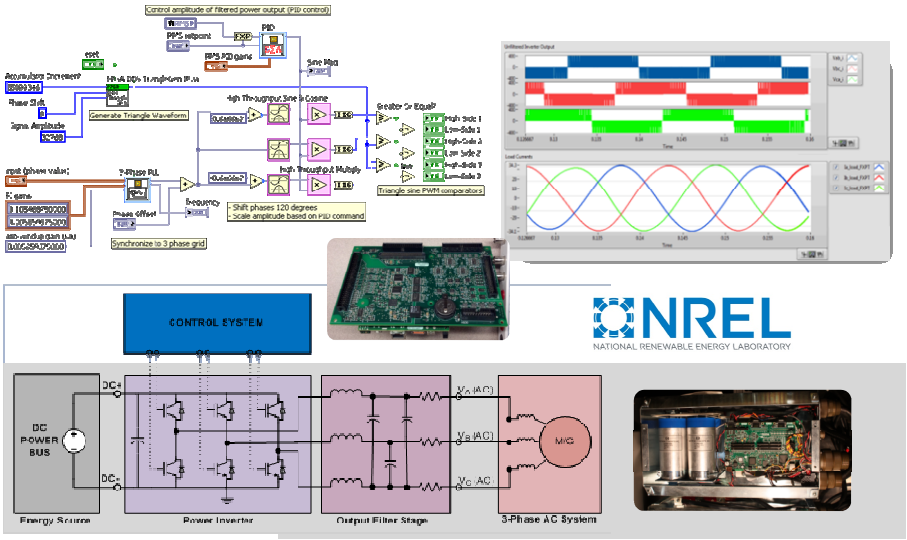
NI RIO Hardware Platform

	CompactRIO & Single-Board RIO			PXI/PC RIO
	 Value	 Ultra Rugged	 Performance	 High Performance
Processor Performance	Up to 400MHz	Up to 800 MHz	Up to 1.33 GHz Dual-Core	Up to 2.26 GHz Quad-Core
FPGA Performance	Up to 43,661 logic cells, up to 58 DSP cores	Up to 110,592 logic cells, up to 64 DSP cores	Up to 147,443 logic cells, up to 180 DSP cores	Up to 94,208 logic cells, up to 640 DSP cores
Analog I/O Speed	Up to 1 MS/s	Up to 1 MS/s	Up to 1 MS/s	Up to 250 MS/s
Operating System	Real-Time OS	Real-Time OS	Window/Real-Time OS	Windows/Real-Time OS
Ruggedness	-20 to 55° C*, passively cooled	-40 to 70° C, passively cooled	0 to 55° C, passively cooled	0 to 55° C, actively cooled
Size	Starts at 17.8x9.3x8.7 cm.3*	Starts at 18x9.3x8.7cm.3	Starts at 40.4x13.4x8.7 cm.3	Starts at 25.7x21.4x18.4 cm.3
Target Application Examples	• Smart grid analyzer • Environmental Monitoring • Mobile robotics • Medical diagnostics & device control • Special Purpose Machines (SPM) • Chemical Process Control • Motion control	• In-vehicle logging • Machine Condition Monitoring • Industrial Machine Control • Oil & Gas Monitoring • Power Monitoring • Structural Monitoring • Automated Welding Control	• Machine Vision • Power Distribution/Control • ECU Prototyping • Analytical Instruments • Turbine Control • Industrial Robotics • Rapid Control Prototyping • Big physics & research	• Hardware-in-the-Loop (HIL) Test • Medical Imaging • High-end Simulation • Protocol Aware Test • Wireless Test • Software Defined Radio • Signal Intelligence

*Single-Board RIO versions are available that operate from -40 to 85° C and start at 10.3x9.7x2.4 cm3

NI Single-Board RIO General Purpose Inverter Controller (GPIC)



ALL SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

NI General Purpose Inverter Control (GPIC) System

NATIONAL INSTRUMENTS

NI Single-Board RIO General Purpose Inverter Controller *IN DEVELOPMENT*

- Deployment-ready commercial embedded system for high-volume grid-tied inverter, DC/DC converter and motor/generator drives
- High level graphical system design tools and reconfigurable FPGA enable rapid development of highly differentiated control algorithms
- Complete, industry proven LabVIEW tool chain with I/O drivers, IP libraries and tightly integrated simulation tools
- FPGA-based control logic for ultra fast pin-to-pin response time, lifetime upgradeability and IP protection
- Xilinx Spartan-6 LX45 FPGA with 58 DSP cores yielding 4,600 MMAC computing performance and hardware parallel execution
- 400 MHz PowerPC processor with VxWorks RTOS for hard real-time floating point processing, networking, and event capture data logging
- Smart grid utility network protocol support (DNP3, IEC 60870, IEC 61850, Modbus, CAN, ...) and onboard real-time 3-phase power and IEC 61000-4-7:2002 harmonic spectra analysis
- 10/100BASE-TX Ethernet port with FTP, HTTP, HTTPS and SSL support and SNTP or IEEE1588 time synchronization
- DMA data scope capabilities for high speed waveform capture and automatically triggered event recording
- Options for depopulation, LEM-style 20-100 mA current sense AI, 16-bit calibrated AI, real-time clock battery, conformal coating, top/bottom/side connectors
- I/O signal compatibility with most standard IGBT intelligent power modules— FUJI, Infineon, Hitachi, Mitsubishi, Powerex, SEMIKRON (SKiiP 3 and 4), Toshiba, ...

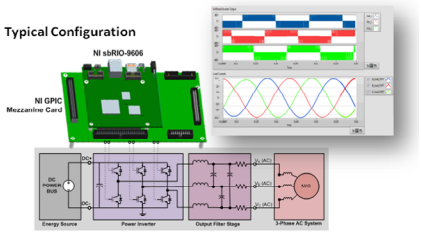
LabVIEW Development Software

- LabVIEW Real-Time (VxWorks) 2011 SP01 or higher
- LabVIEW FPGA 2011 SP01 or higher

Recommended Software

- NI MultiSim Co-Simulation Interface for LabVIEW FPGA (design guide)
- NI Power Electronics IP Library (included with NI SoftMotion 2011 f1)
- NI Electrical Power Measurement Suite
- NI Veristand (for automated real-time virtual/physical testing)
- NI Simulation Interface Toolkit (interface to 3rd party simulator)

Typical Configuration



The Problem with Embedded Design

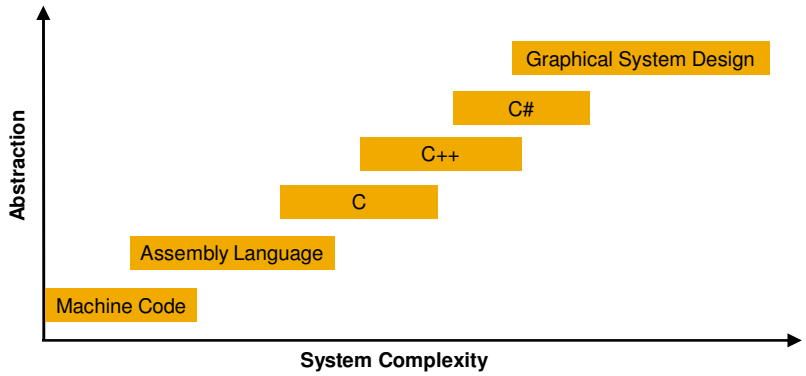
2. System design complexity is increasing
   - The sophistication of the tools must increase
   - We can't manually do the things we used to do
   - System level tools are needed to grapple with complex non-linear, multi-domain design tradeoffs

Power Electronics Design Goals & Tradeoffs

- Optimize for multiple design goals simultaneously, including:
  - Energy efficiency
  - Cost
  - Component lifetime
  - Systematic reliability
  - Regulatory compliance
  - Smart grid ready
  - Differentiated features
  - …
  - …

Automated Engineering

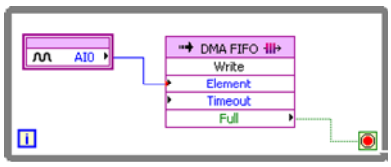
- 90% of engineering work should be automated

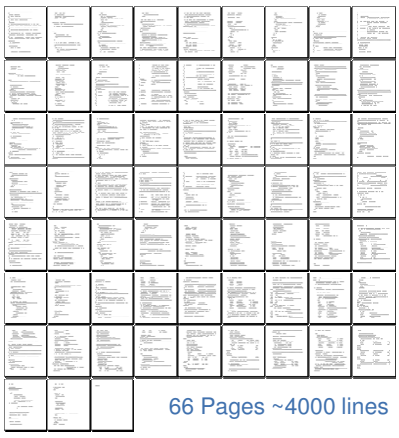


The Problem with Embedded Design

3. FPGAs are ideal for digital control of SMPS
   - Pros
     - Nanosecond control of timing, completely parallel execution
     - Now contain dozens to hundreds of mini hard-core DSPs, emerging FPGAs have hard-core floating point processors
     - Orders of magnitude higher DSP performance per dollar and per watt compared to single core DSPs
     - Field reconfigurable at the silicon gate level (SGL)
   - Cons
     - Orders of magnitude more complex to program
     - PCB layout is becoming increasingly complex and costly due to fine-pitch parts
     - 70% of software development cost is I/O interface development (rather than algorithms)

LabVIEW FPGA vs VHDL





66 Pages ~4000 lines

Counter **Analog I/O** **Streaming**

The Problem with Embedded Design

4. Parallelism: Moore's Law has gone parallel
   - The performance of a single-core has gone flat
   - Must have design tools for a parallel world – a very difficult problem:
     - Synchronization
     - Simultaneous parallel loops
     - Multirate loops
     - Handshaking, semaphores, triggers
     - Data producers & consumers
   - FPGAs help a lot with these issues because they are actually truly parallel in hardware

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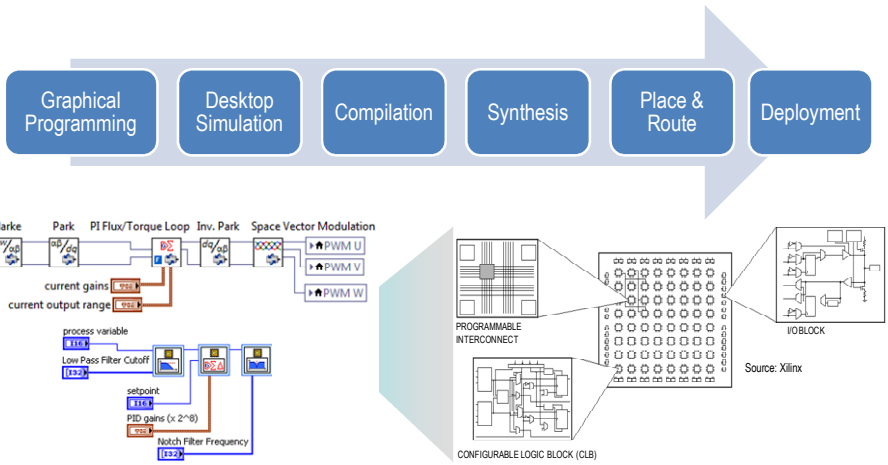
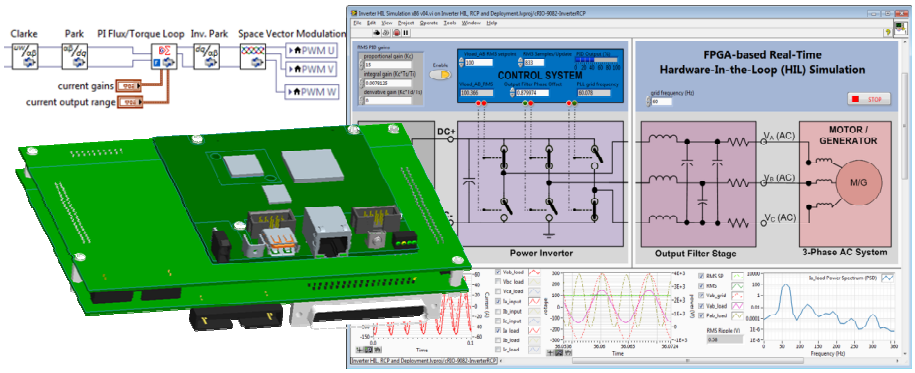
Graphical System Design



LabVIEW FPGA

Reconfigurable I/O (RIO) Hardware



NEXT STEP

JOIN THE DEVELOPER COMMUNITY AT

NI.COM/POWERDEV