NIDays09

WORLDWIDE GRAPHICAL SYSTEM DESIGN

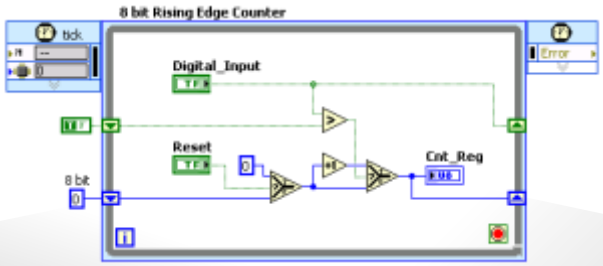
CONFERENCE

NATIONAL INSTRUMENTS

Benefits of FPGA Technology

Agenda

- What Are FPGAs and Why Are They Useful?
- Programming FPGAs
- Common Applications for FPGAs
- FPGA Hardware
- How to Learn More



LabVIEW Real-Time

LabVIEW FPGA

LabVIEW Touch Panel

LabVIEW for ADI Blackfin

LabVIEW for ARM

NI LabVIEW Embedded Technology

Real-Time Processor

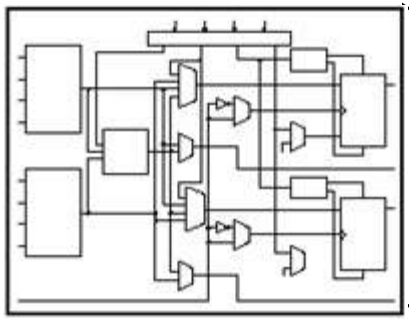
FPGA

PDA/HMI

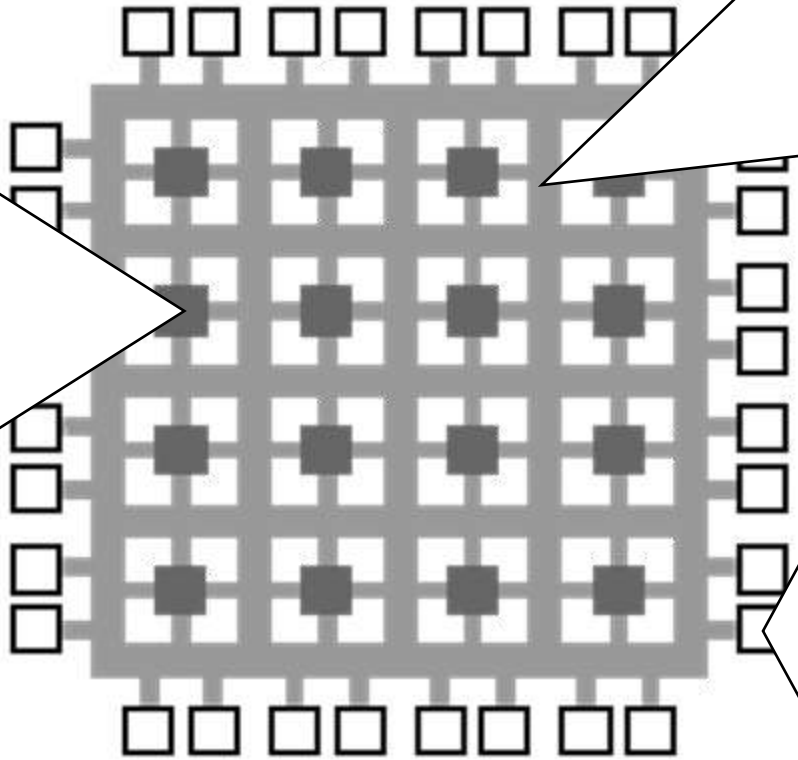
Microprocessor

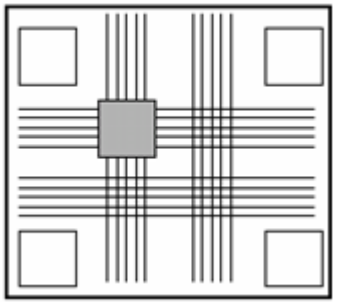
Microcontroller

FPGA Technology

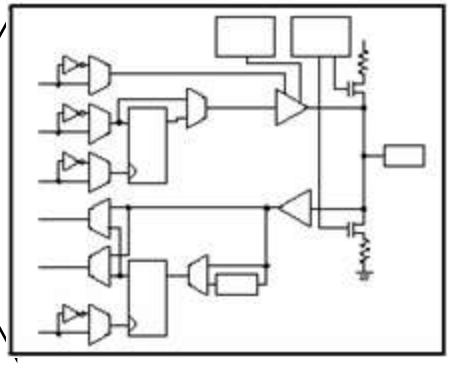


Logic Blocks



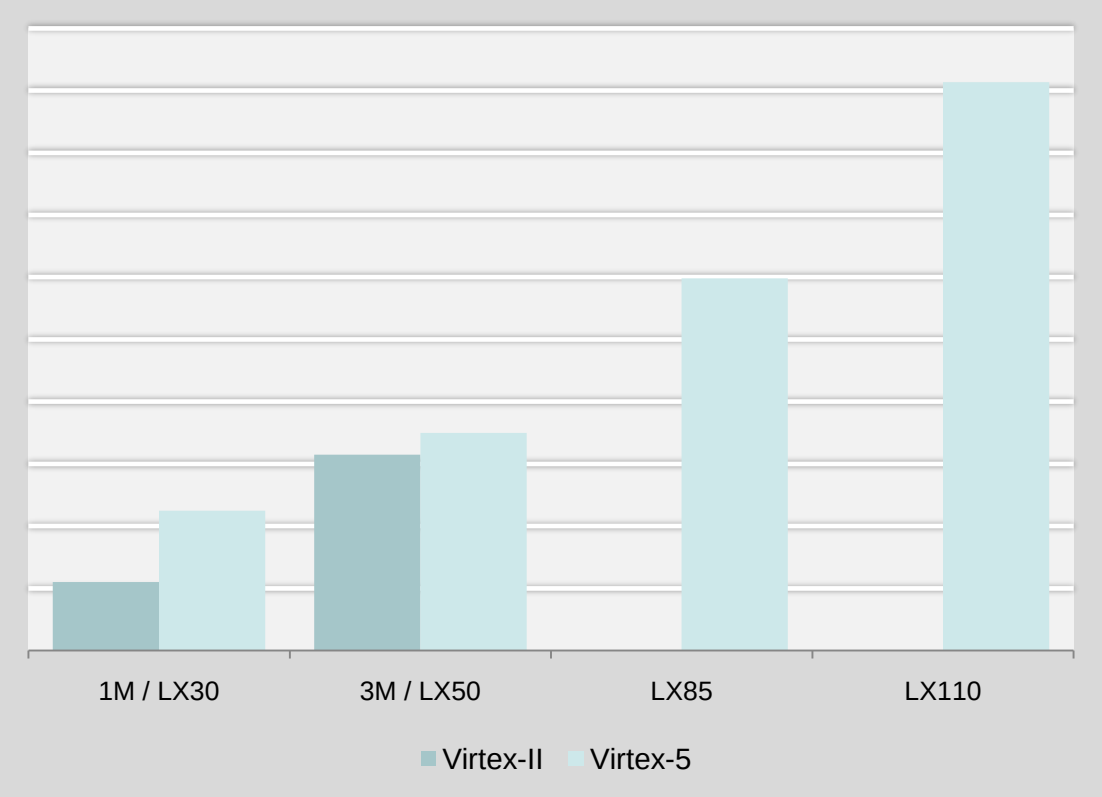


Programmable Interconnects

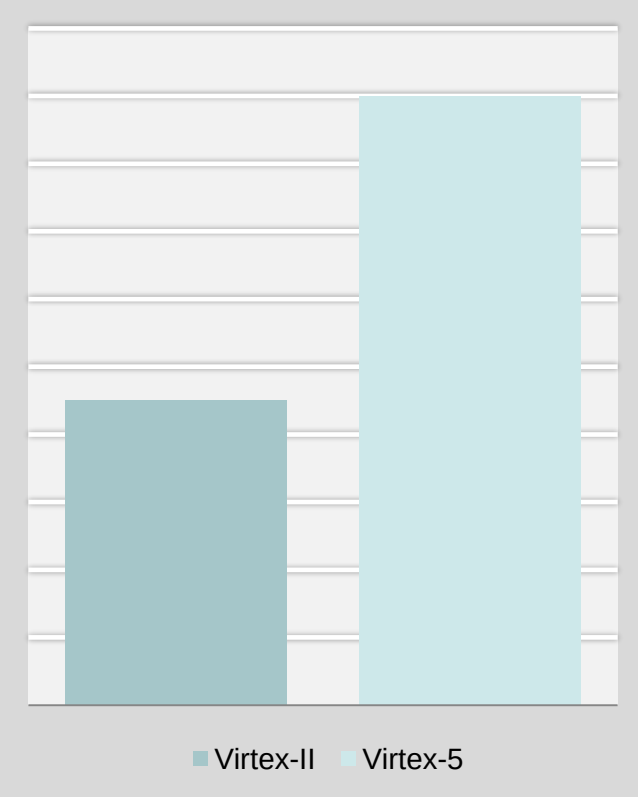


I/O Blocks

FPGA Families / Sizes

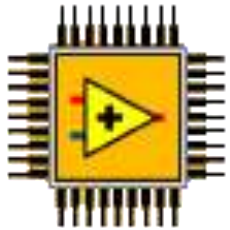


FPGA Logic Resources



FPGA Execution Speed

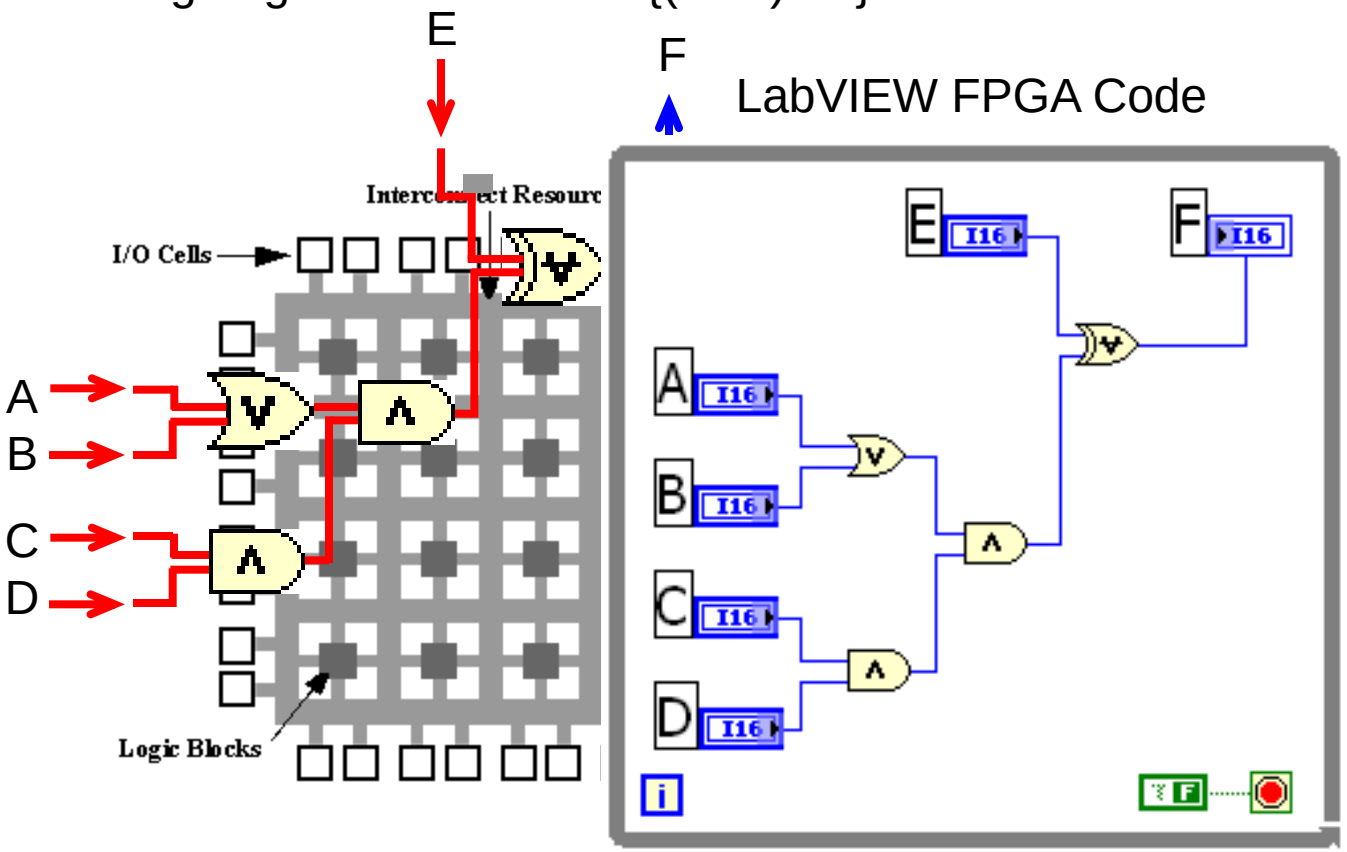
Why Are They Useful?



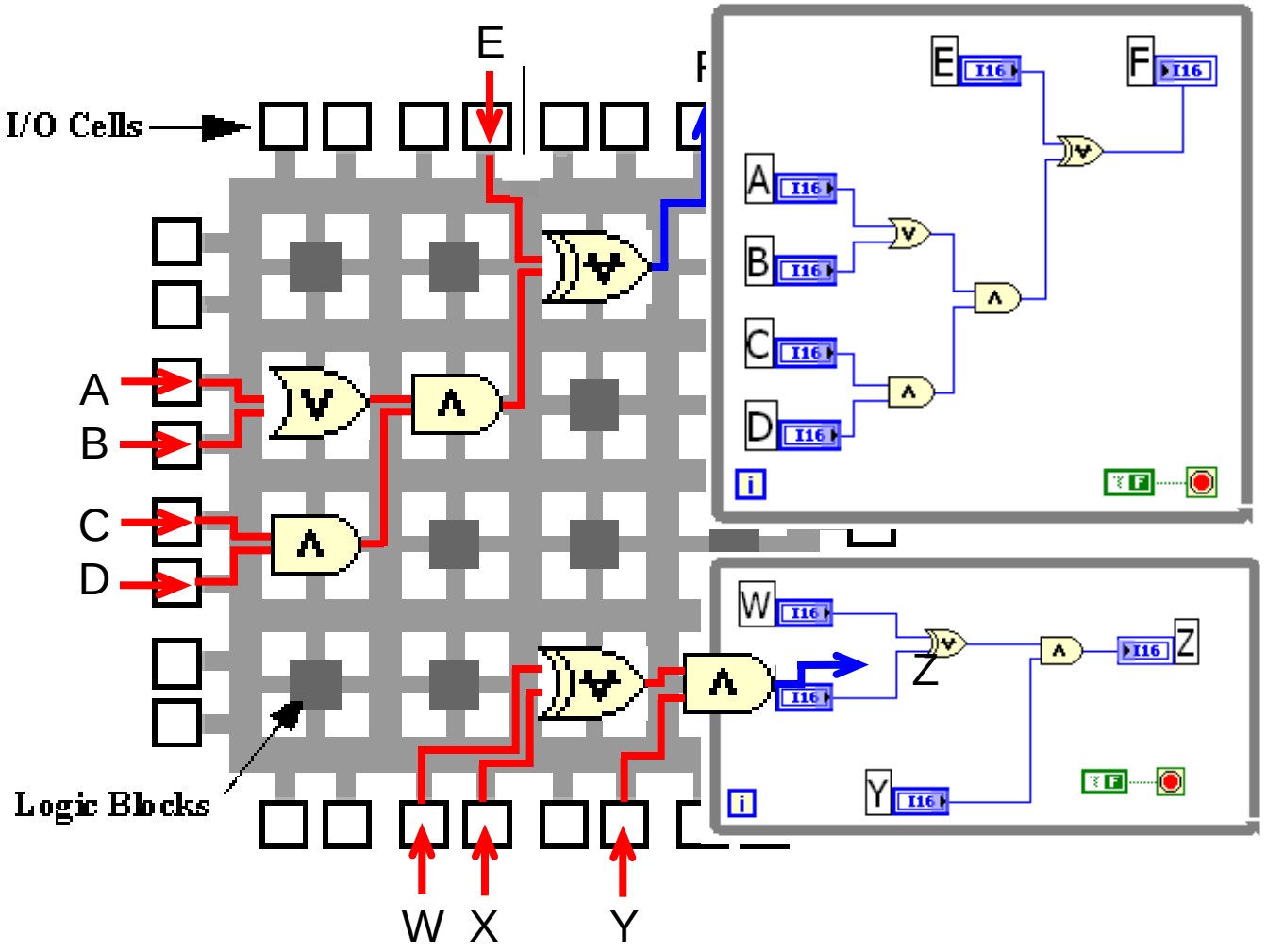
True Parallelism	Provides parallel tasks and pipelining
High Reliability	Designs become a custom circuit
High Determinism	Runs algorithms at deterministic rates down to 25 ns (faster in many cases)
Reconfigurable	Create new and alter existing task-specific personalities

FPGA Logic Implementation

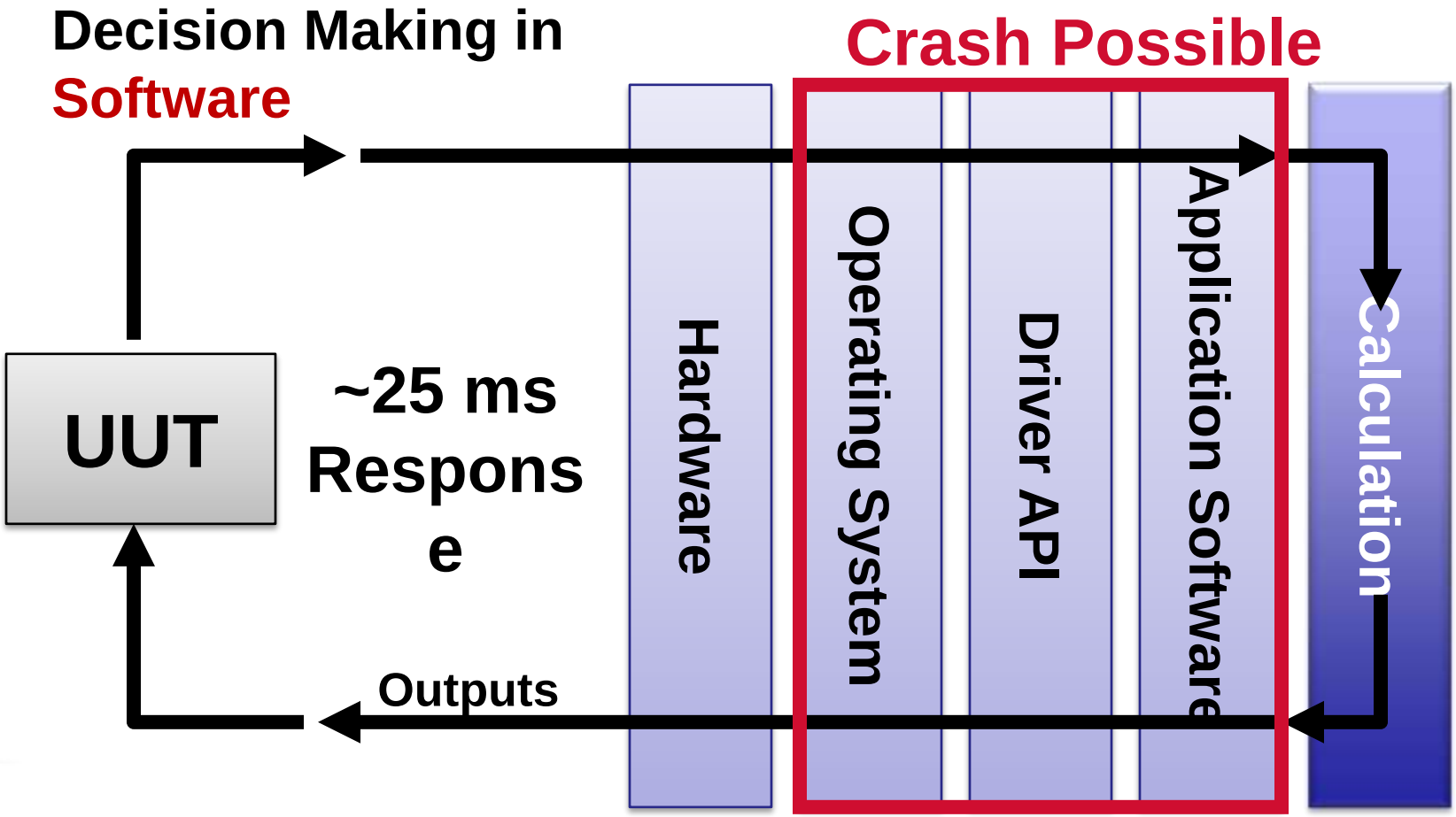
Implementing Logic on FPGA: F = {(A+B)CD} ⊕ E



True Parallelism



High Reliability and Determinism



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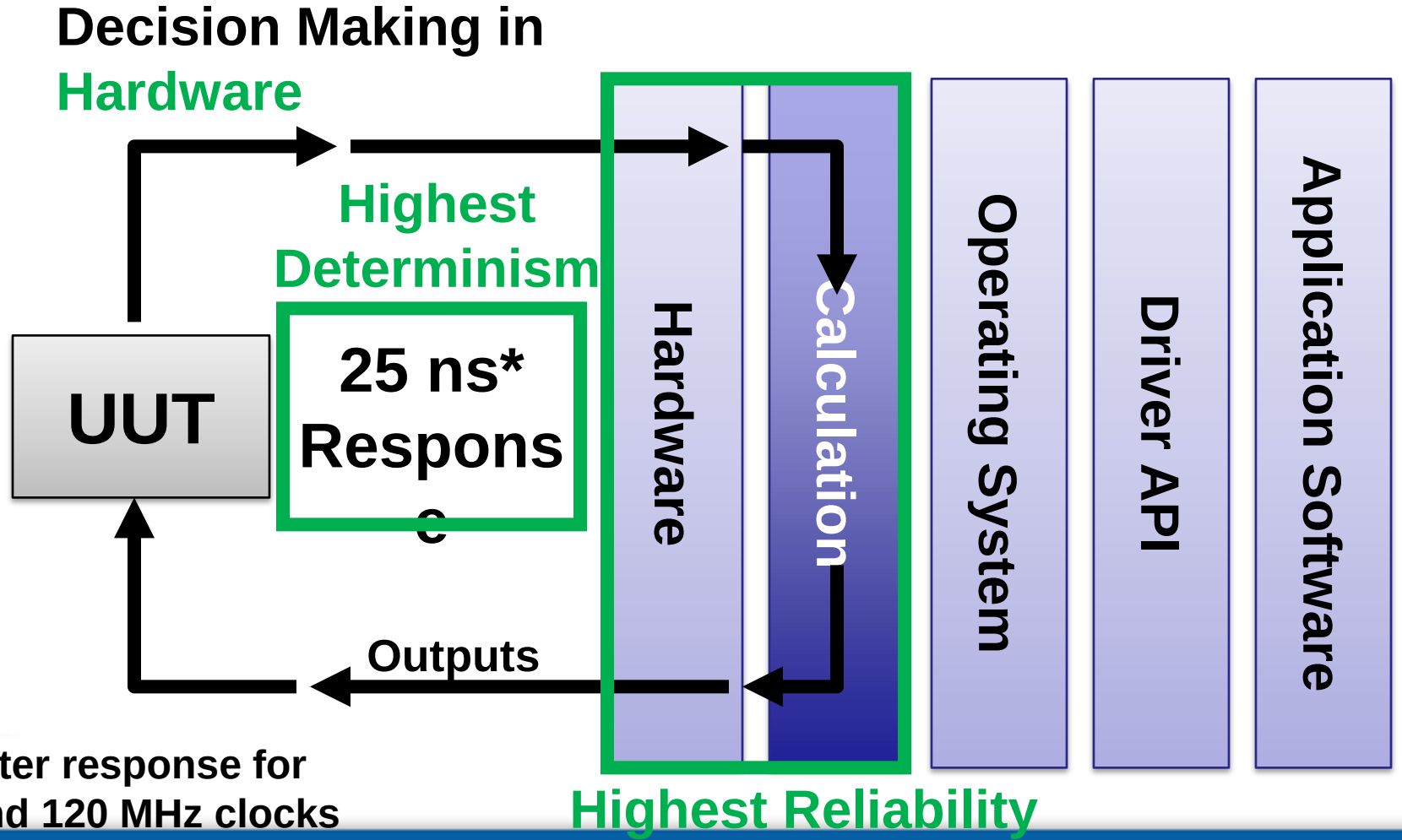

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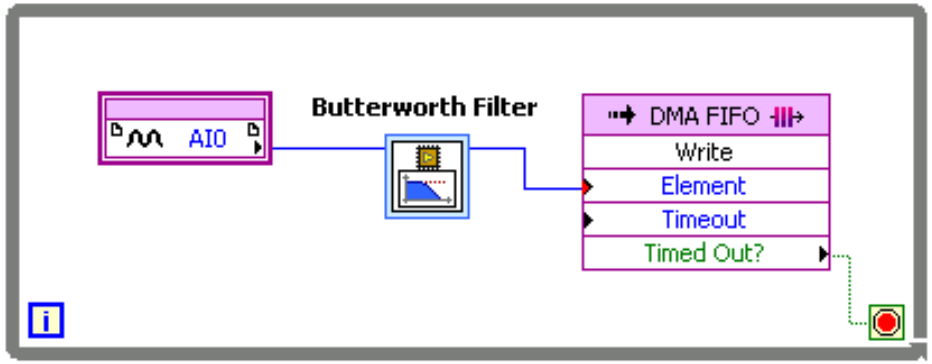
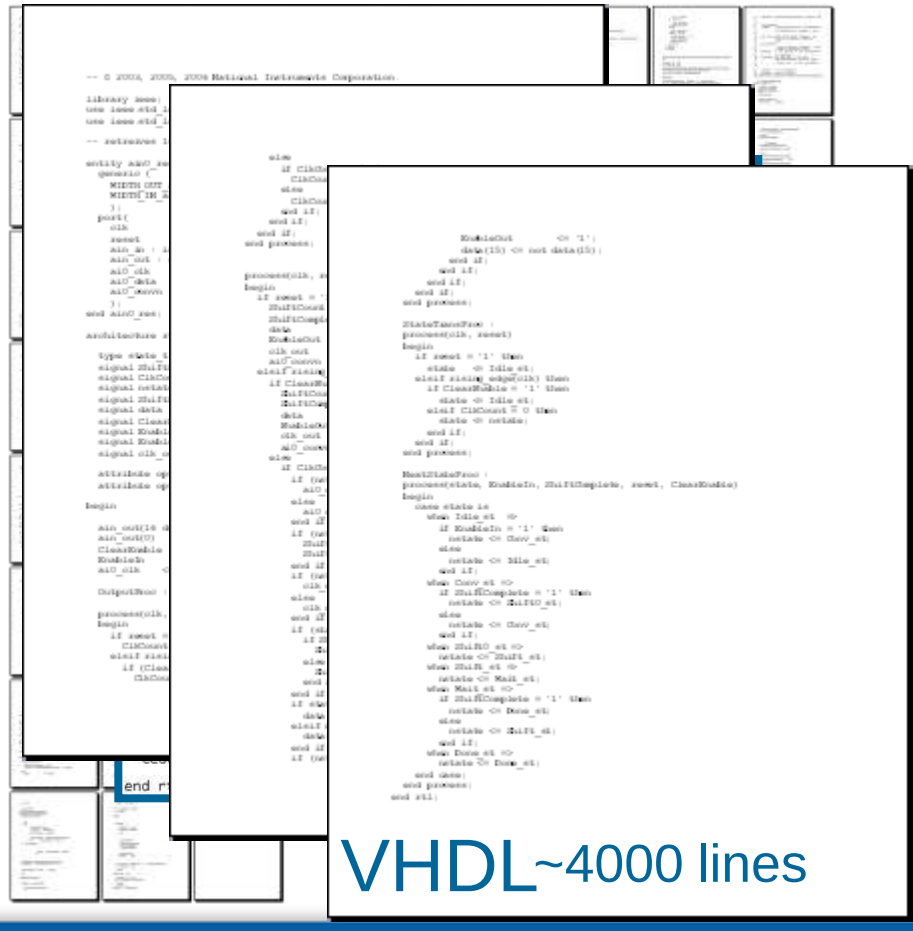
LabVIEW FPGA Code Abstraction

Counter | **Analog I/O** | **I/O with DMA**

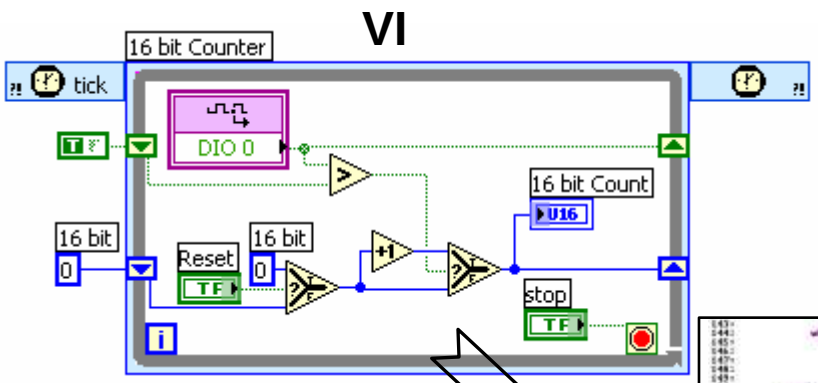


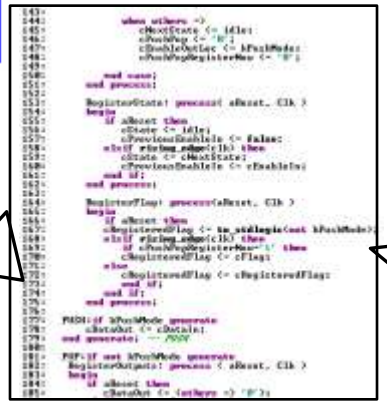
LabVIEW FPGA



VHDL~4000 lines

From LabVIEW to hardware





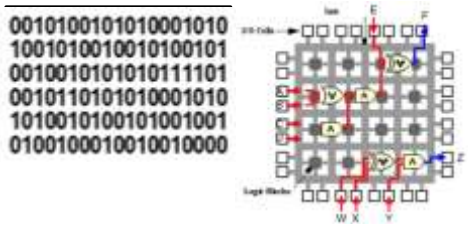
LabVIEW FPGA

Compilation

Synthesis

Xilinx

BitStream

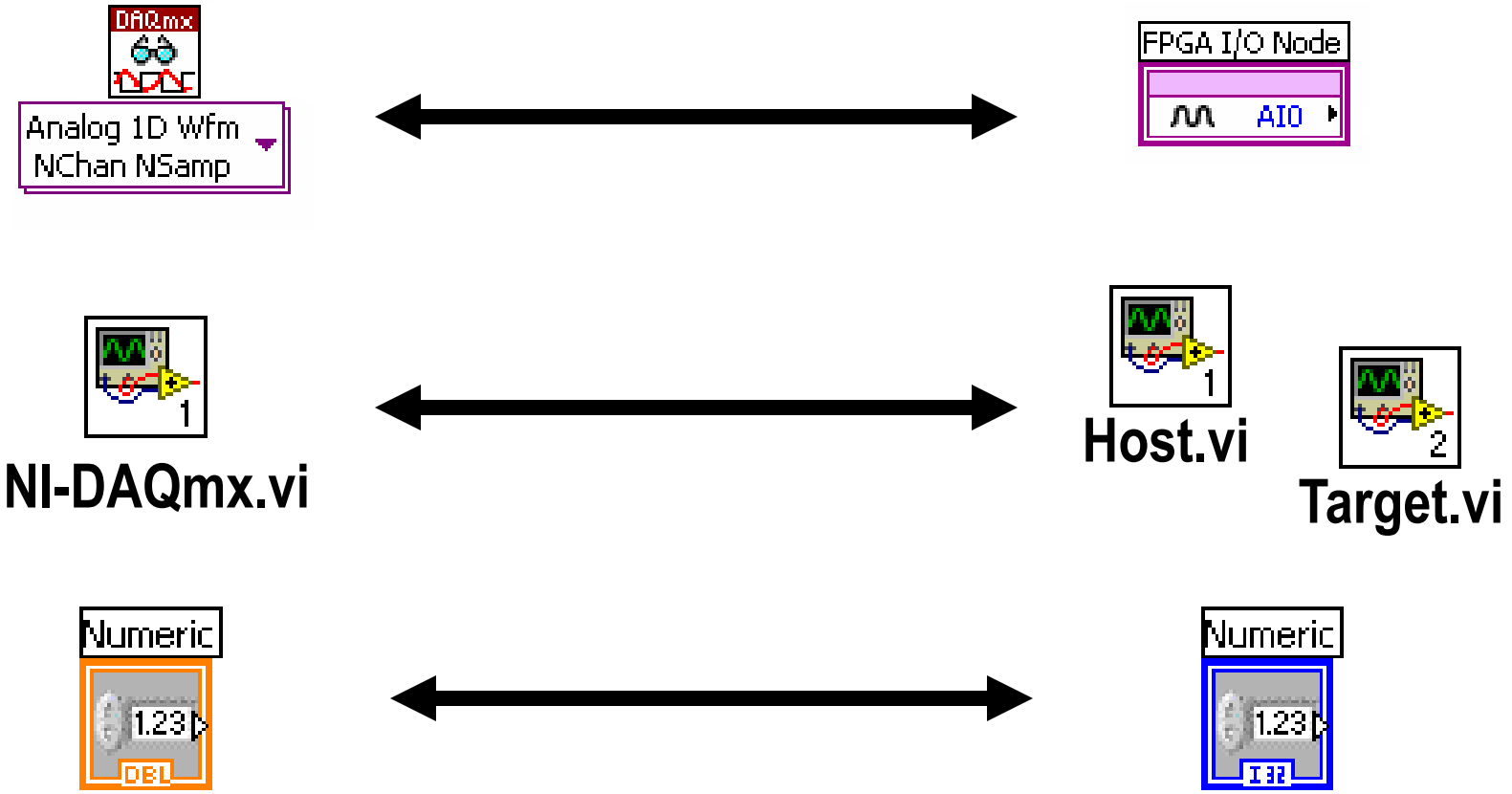


Development Computer

Demo

- Creating a Simple Event Counter in Hardware

LabVIEW FPGA Programming



No Floating Point

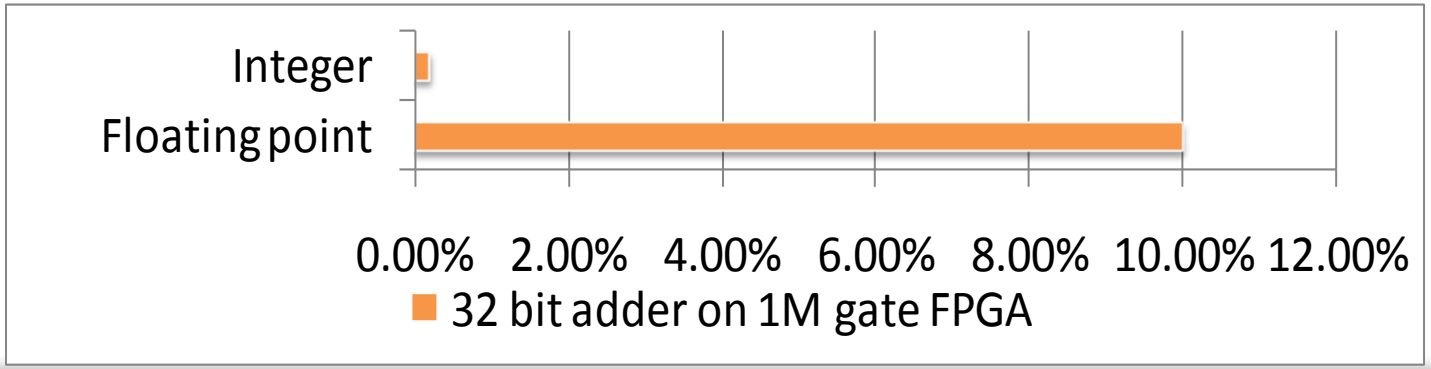
- Dynamic shifts are costly

$$\begin{array}{r} 9.99\text{x}10^{5} \\ +\ 2.0\text{x}10^{3} \end{array} \longrightarrow \begin{array}{r} 9.99\text{x}10^{5} \\ +\ 0.02\text{x}10^{5} \end{array} \longrightarrow 10.01\text{x}10^{5} \longrightarrow 1.001\text{x}10^{6}$$

Dynamic Shift

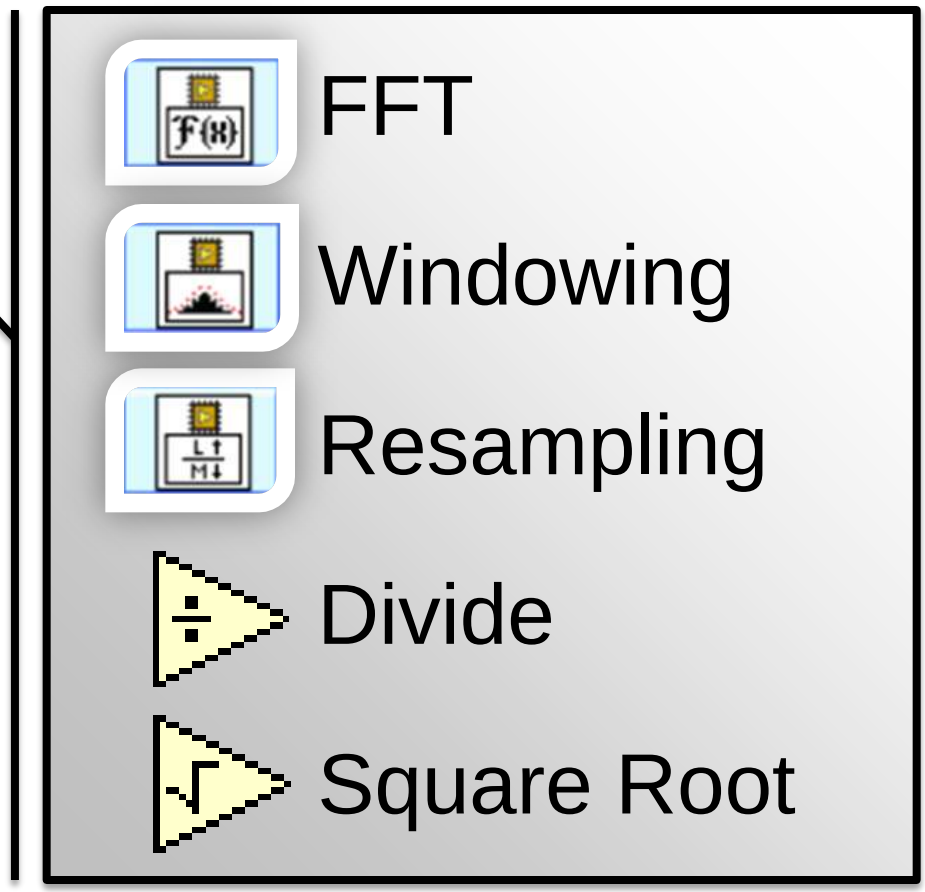
Dynamic Shift

- Fixed-point operations avoid dynamic shift



LabVIEW FPGA IP Options

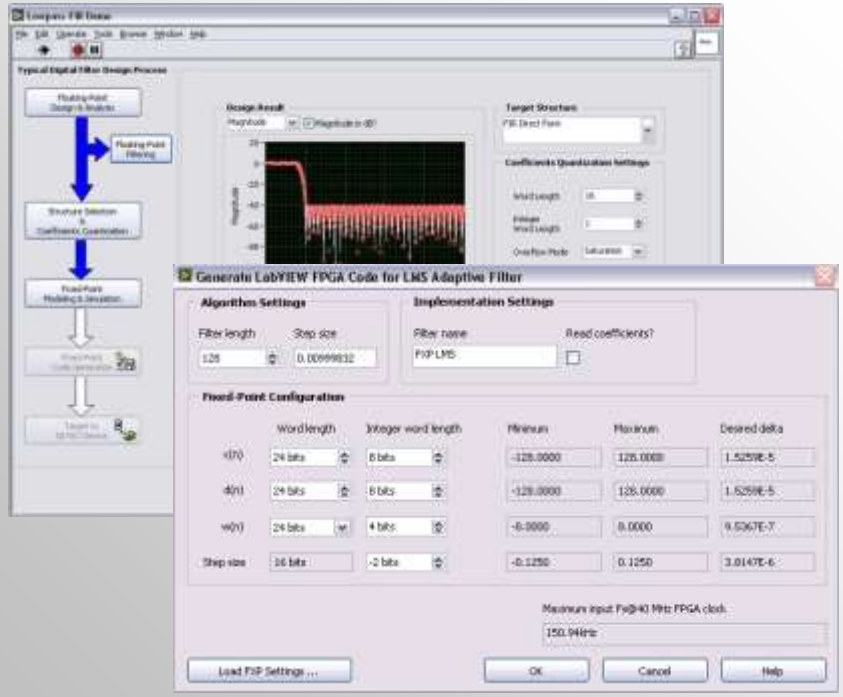
- LabVIEW IP
- IP generators
- FPGA IPNet
- HDL node
- CLIP node



LabVIEW FPGA IP Options

- New LabVIEW IP
- IP generators
- FPGA IPNet
- HDL node
- CLIP node

NI Digital Filter Design Toolkit



NI Adaptive Filter Design Toolkit

LabVIEW FPGA IP Options

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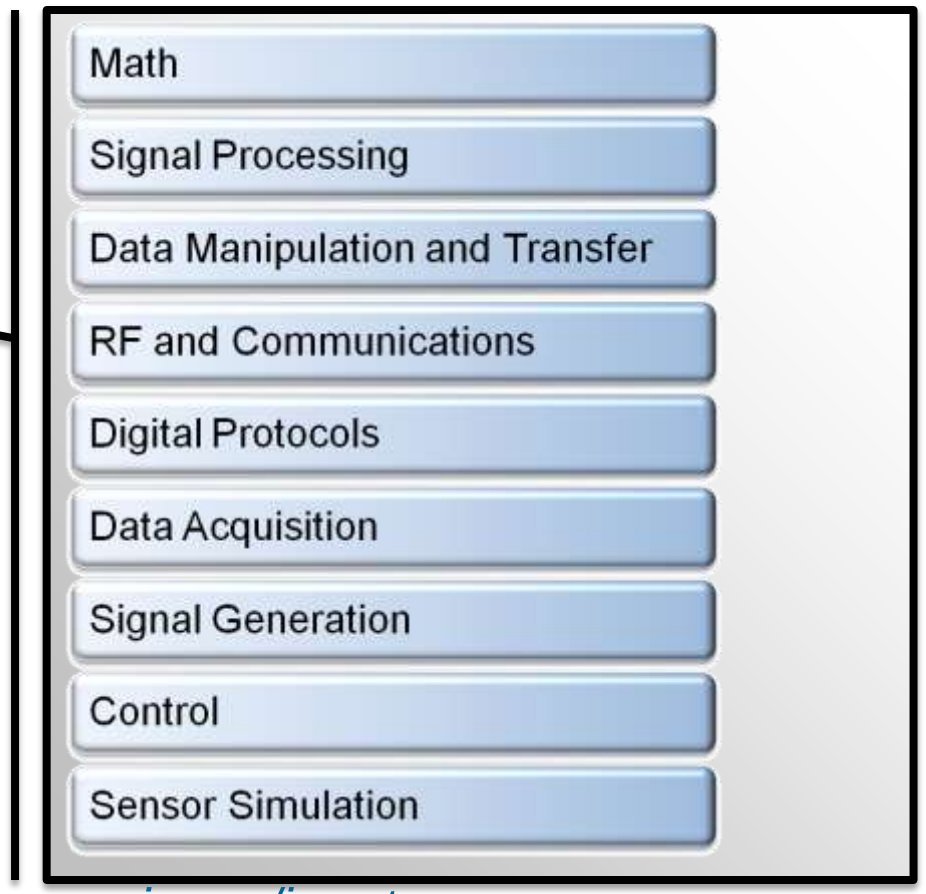

ni.com/ipnet

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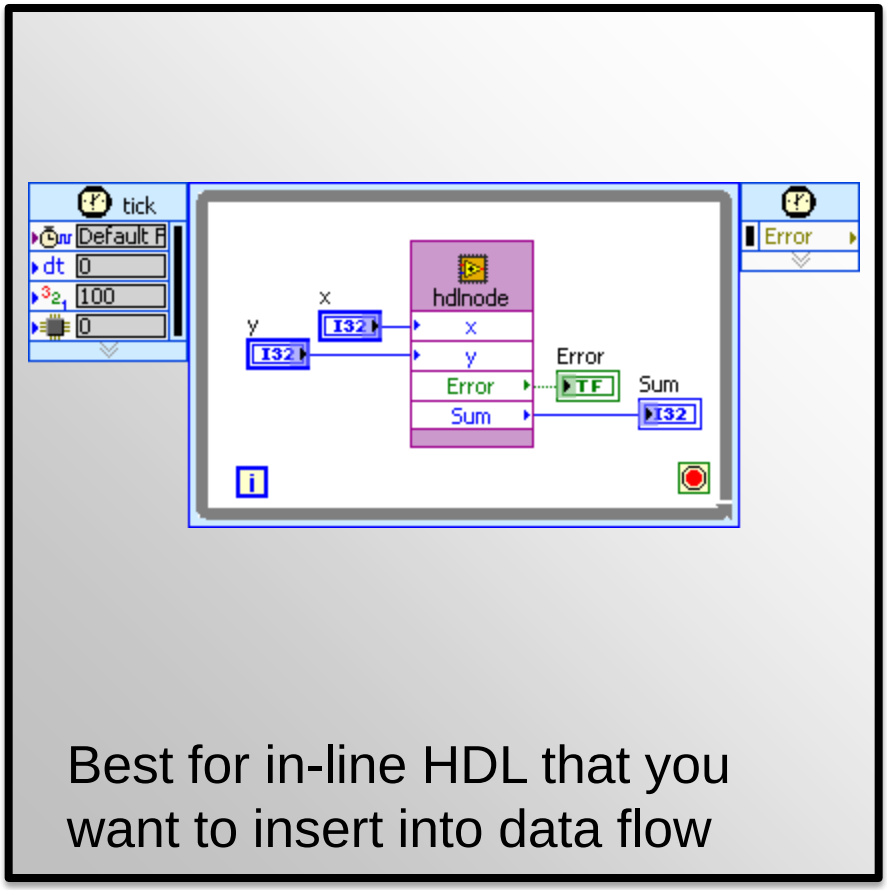

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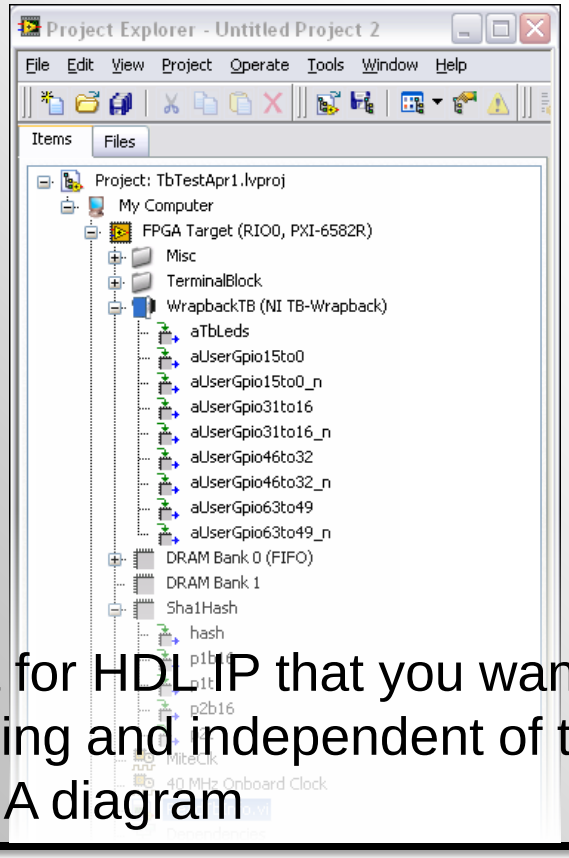


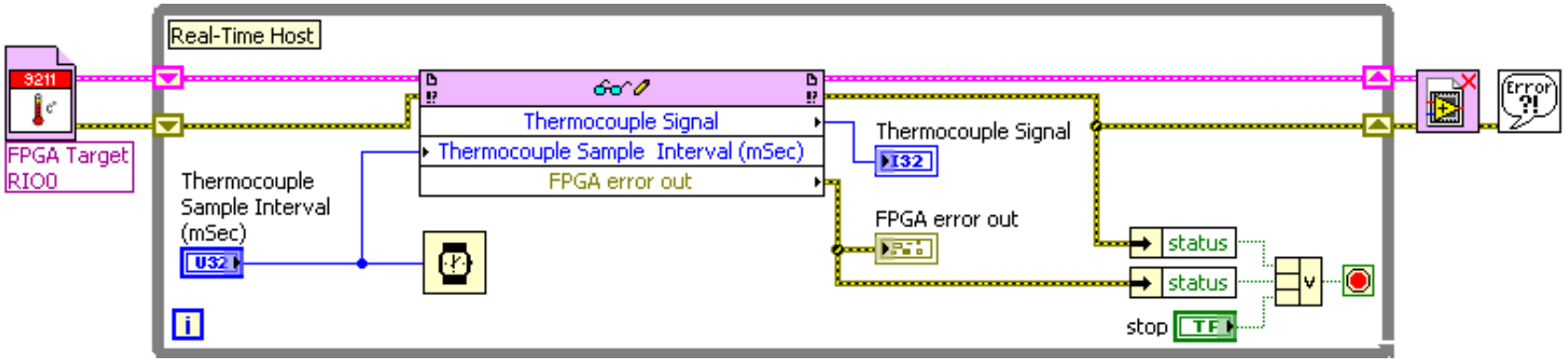
Best for HDL IP that you want free running and independent of the FPGA diagram

Controlling the FPGA VI

- Common host VI tasks:
  - Data processing
  - Perform operations not available on the FPGA target
  - Log data
  - Sequence multiple FPGA VIs
  - Control the timing and sequencing of data transfer

Typical FPGA host application

- Open FPGA VI Reference
- Read/Write Control
- Invoke Method
- Close FPGA VI Reference



Demo

- Communicate between FPGA and host

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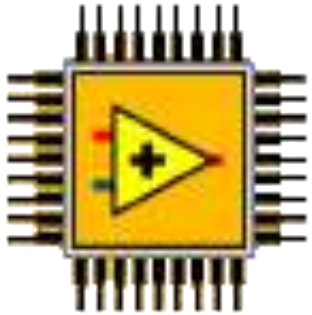
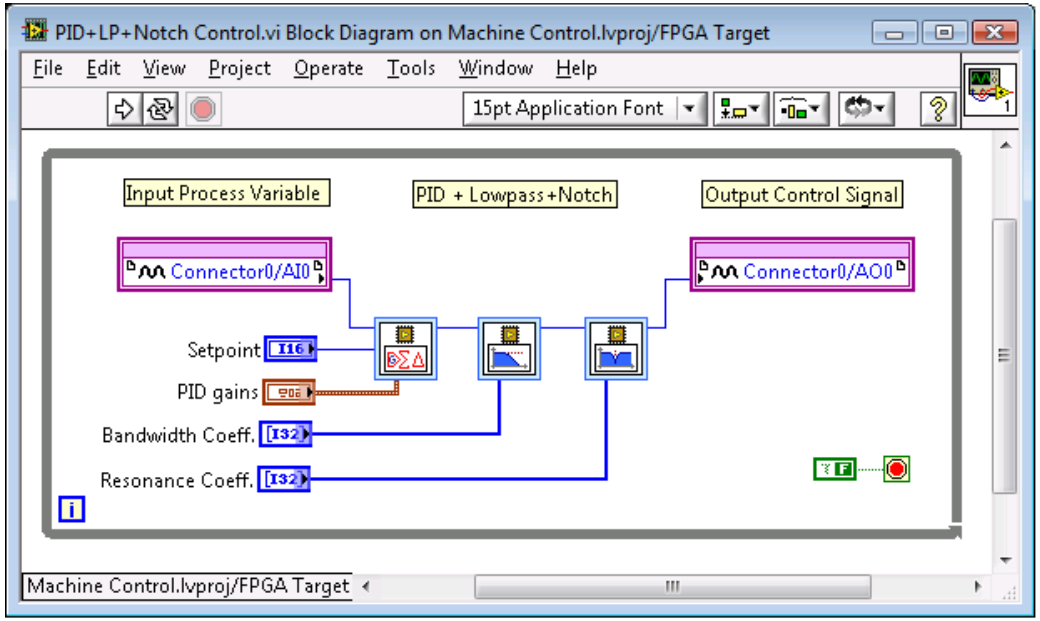
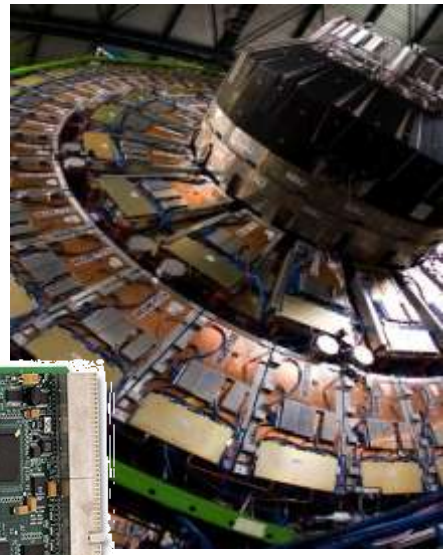
Common Applications

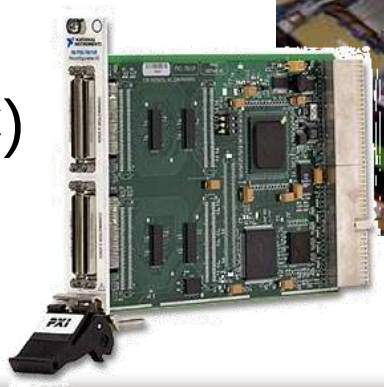


- High-speed control
- Intelligent DAQ
- Digital communication protocols
- Sensor simulation
- Onboard processing and data reduction
- Coprocessing

High-Speed Control



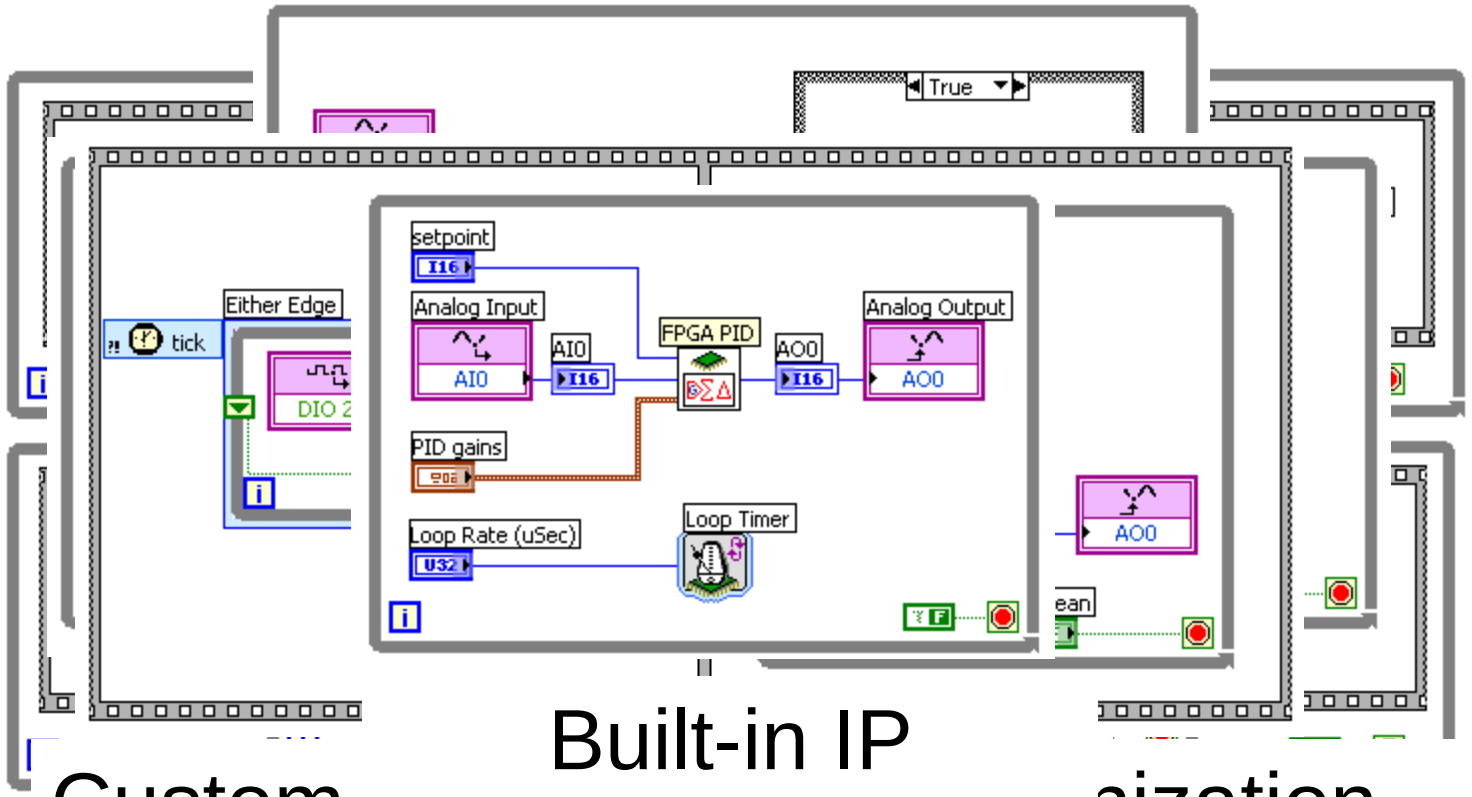




CERN – Large Hadron Collider (LHC)

- Control particle collision
- PXI “R-Series” module

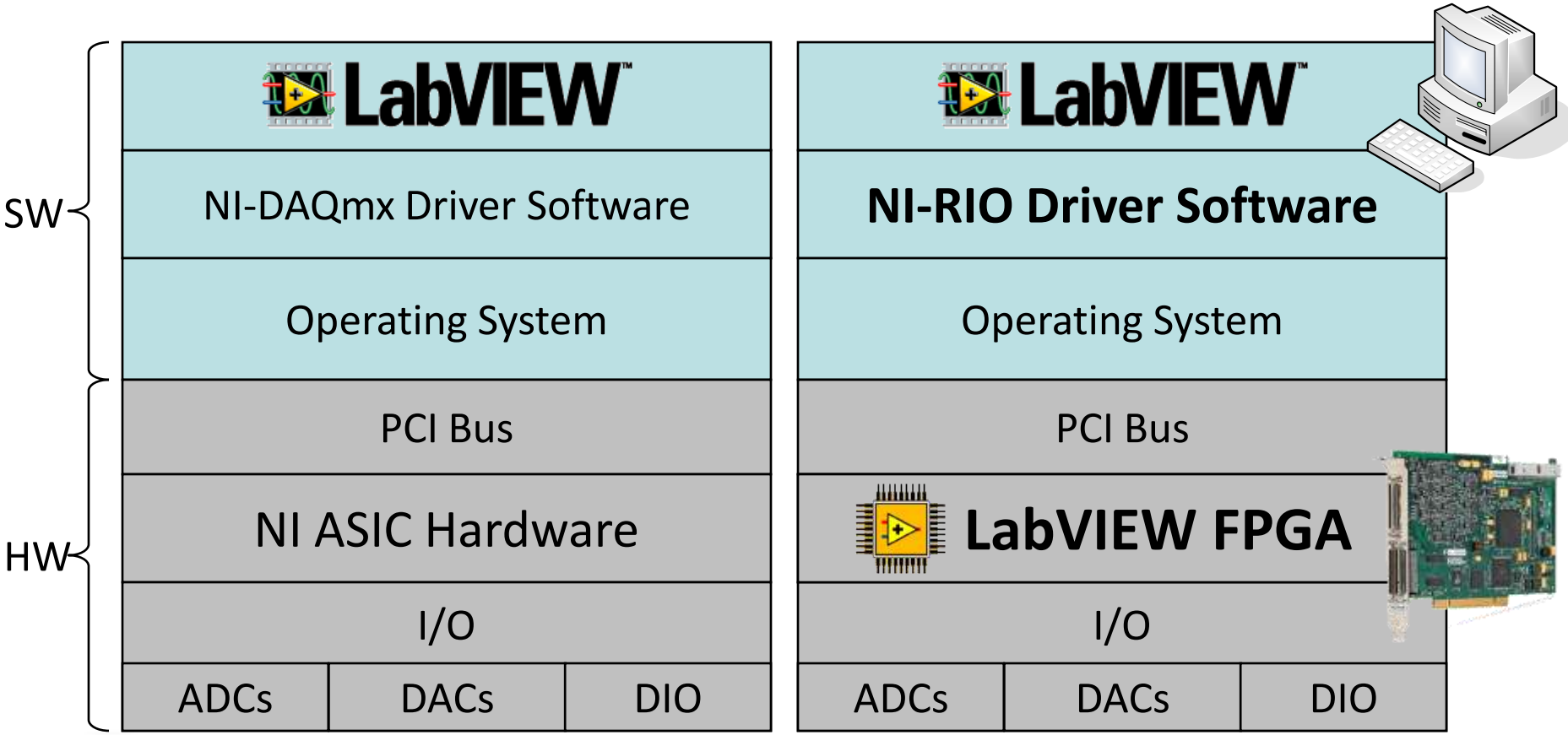
Intelligent DAQ



Custom … Built-in IP … nization

… processing blocks …

Data Acquistion and FPGA programming NI-DAQmx and NI-RIO

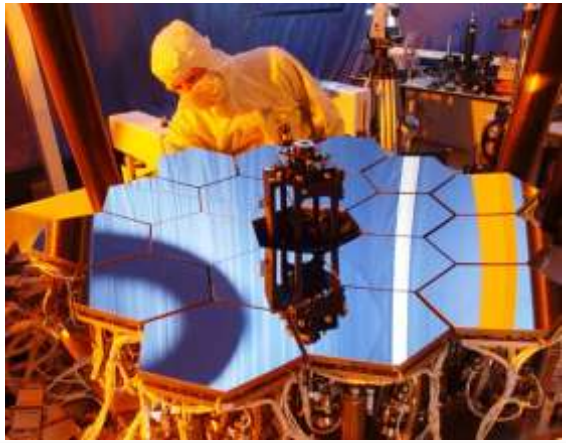


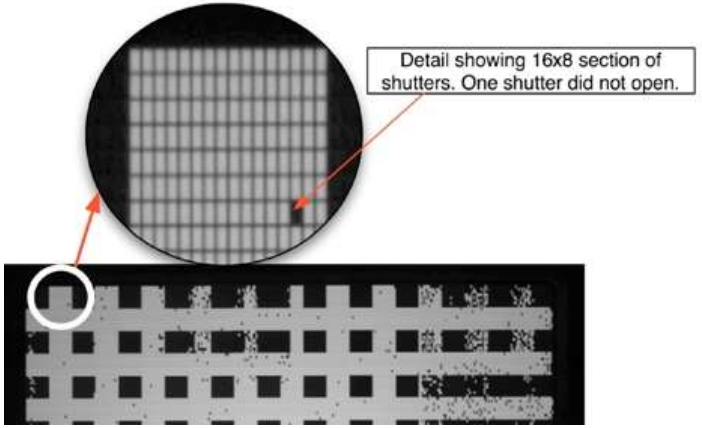
NI-DAQmx with DAQ HW

NI-RIO with R Series HW

Intelligent DAQ
NASA Microshutters Testing Application

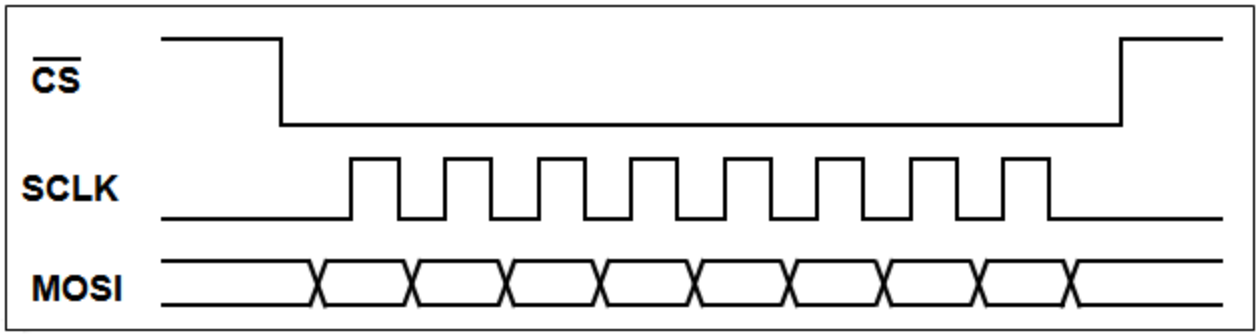
- Must function reliably for 10-year mission
- Expected to open and close over 100,000
- Complex timing requirements
- Motion and vision synchronization

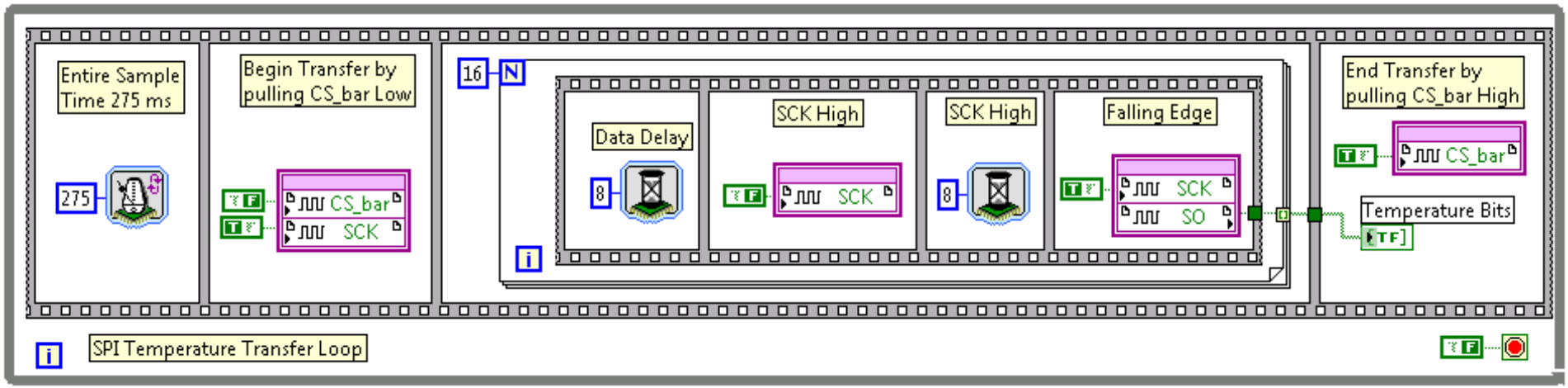




Digital Communication

Example – SPI





Sensor Simulation and FPGA

- Fully customizable hardware – Many types of sensors
- Parallelism – Many sensors on chip with no interference
- Strict timing requirements – Deterministic or highly realistic
- Onboard processing – Engineering units to sensor signals

Sensor Signals

Onboard Processing and Data Reduction

Built-In I/O

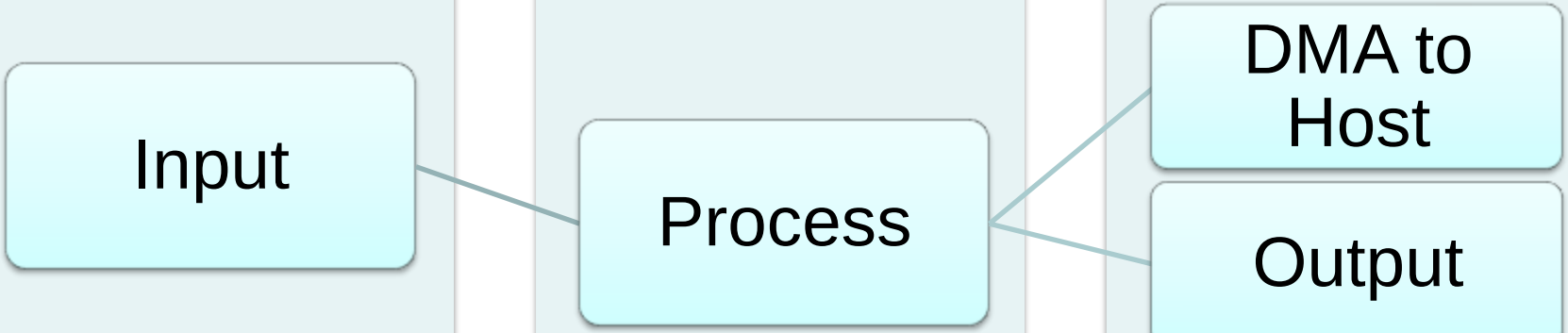
- Analog voltages
- Digital communications
- Sensor signals

Processing

- Encoding/decoding
- Filtering/averaging
- Modulation/ demodulation
- Decimation
- Stream processing

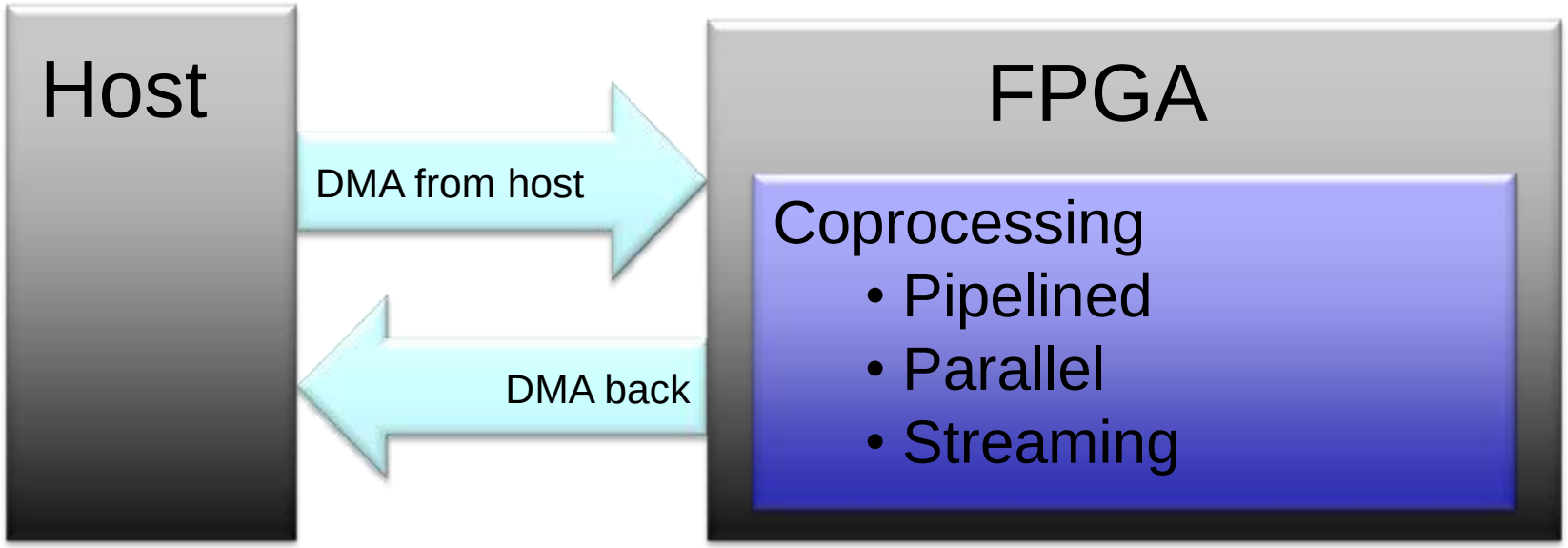
Output

- DMA preprocessed data
- Streaming from input to output without host involvement



FPGA Coprocessing

A method to supplement the primary processor functions is offloading processor-intensive tasks. FPGA coprocessing is especially useful for tasks that can take advantage of FPGA parallelism and pipelining tactics.



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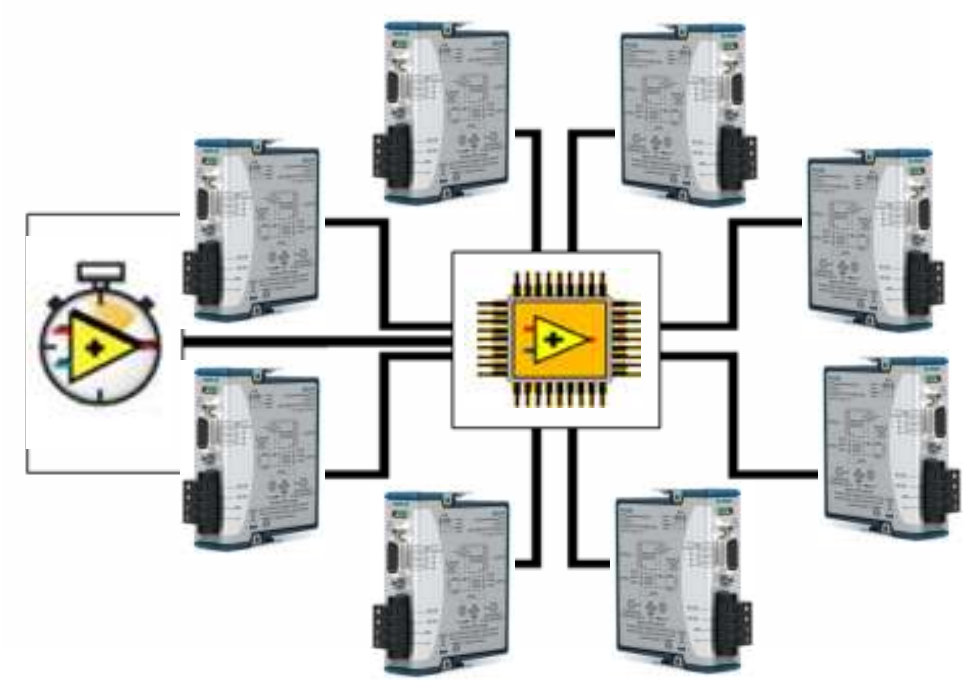
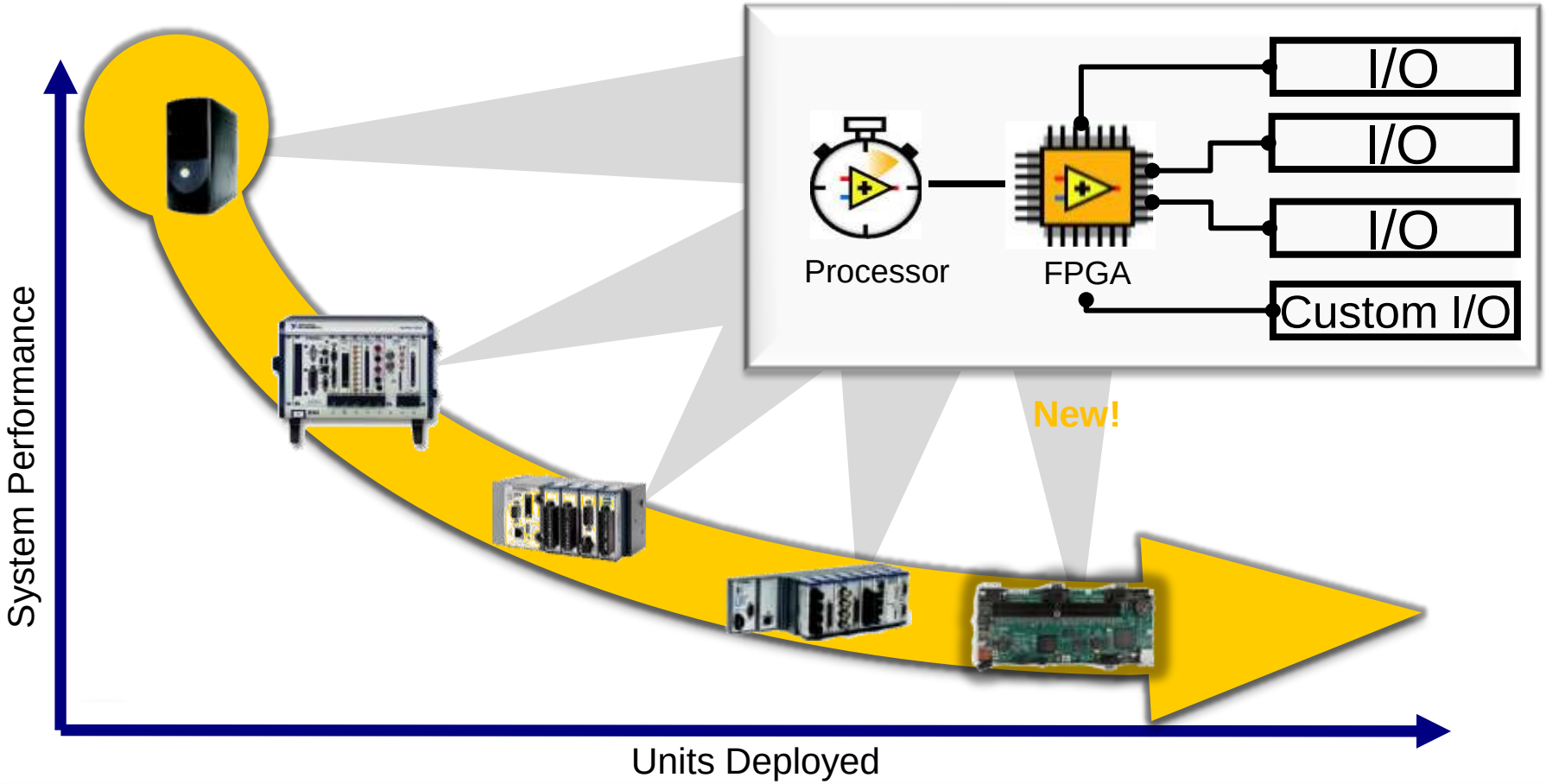
FPGA hardware platforms



RIO Deployment Curve
Standard Embedded Architecture, Standard Design Software



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How to Learn More

Attend:

- How to get a jump start using CompactRIO
- From rapid prototyping to low-cost deployment with LabVIEW embedded tools
- Seeding the future of test with reconfigurable instruments
- How to test embedded control systems with dynamic test methods

Online:

- ni.com/fpga
- ni.com/embeddedeval
- ni.com/ipnet