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T&M Solutions BV

Building a Complete Data Monitoring and Storage System with NI CompactRIO

Speaker: Arnoud de Kuijper, CTO T&M Solutions BV

Agenda

- Case Description
- Demonstration
- Key Challenges
- Concluding remarks
- Questions

Case Description

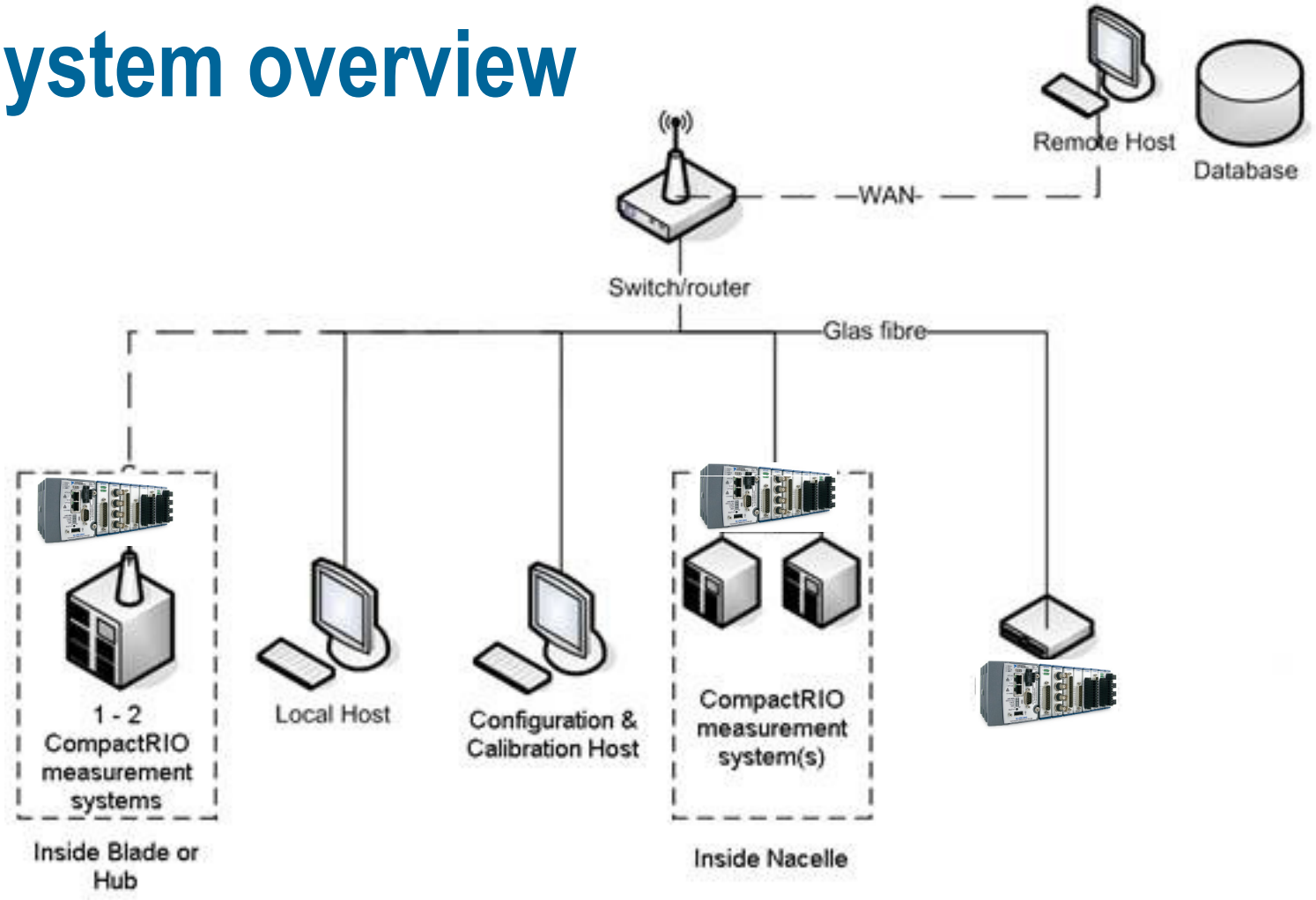
- Replacing existing remote monitoring systems by new monitoring systems.
  - All signals are time synchronized
  - supports a higher sample rate and higher accuracy.

Windmill

Requirements for data monitoring and storage system

- Reliability (harsh environment)
- Flexibility (different measurement types)
- Configurability (no programming!)
- Accuracy
- Channel count (multiple systems sync.)
- Customizable

System overview



Why NI CompactRIO & LabVIEW

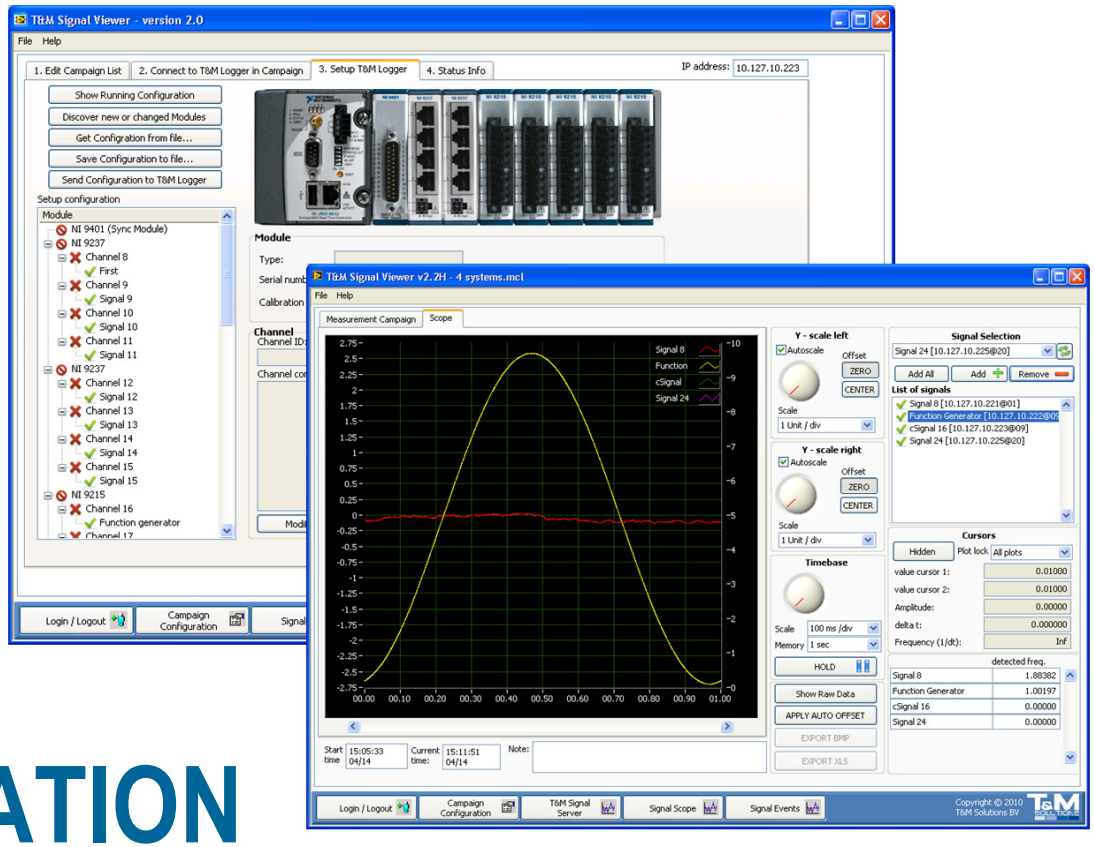
Pro's

- Quick time to market because of high HW+SW integration
- Wide range of availability for I/O modules
- Support for third-party instrument control
- Custom synchronization and filtering techniques

Why NI CompactRIO & LabVIEW

Con's

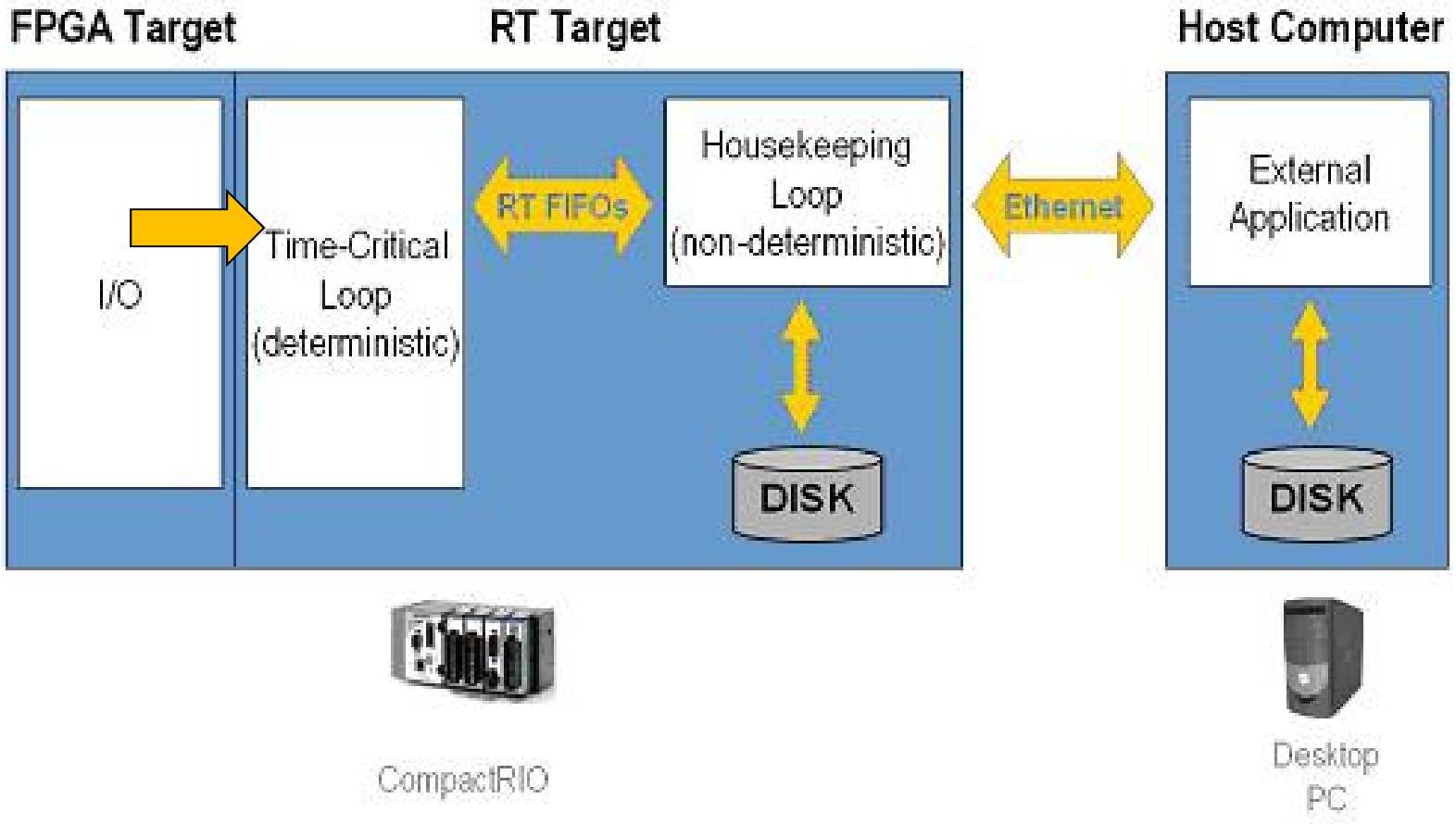
- No customer of the shelf (COTS) product
- Requires experienced software engineering effort
- Requires in-depth knowledge of NI products
- Custom synchronization and filtering techniques



T&M Signal Logger Studio

DEMONSTRATION

Stream from FPGA to Windows



Key challenges in software design

- Acquisition and logging speed
- Synchronization
- Configurability
- Software architecture

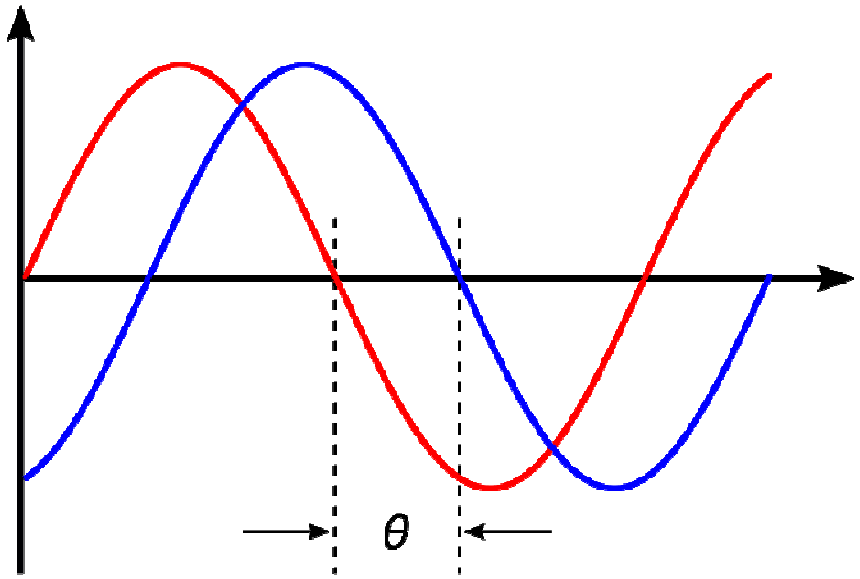
Acquisition and logging speed design considerations

- Log to file or in memory
  - 2 / 4 GB or 512MB
- Maximum storage size disk
  - 5 kHz, 28 channels will result in 45 minutes for 2 GB
- Stream to disk
  - (3/4 to 6 Mb for binary)
- Stream from FPGA to RT
  - (scan engine or custom?)

Acquisition and logging speed design considerations

- FPGA FIFO and file data types
  - SGL, DBL, FXP, INT
- Disk structure VxWorks Reliance
  - slow with file access if there are multiple files
- FPGA Type
  - Xilinx LX-30/50 or bigger? -> filtering and I/O modules / properties have big impact!
- Data transfer RT->HOST
  - Shared Variables, TCP/IP, UDP or FTP?

Synchronization: Why?



- 5 kHz signal-> T_{period}= 0.2 ms.
- Phase coherent at 1 degree -> 0.2 ms / 360 -> 0.5 microsecond.

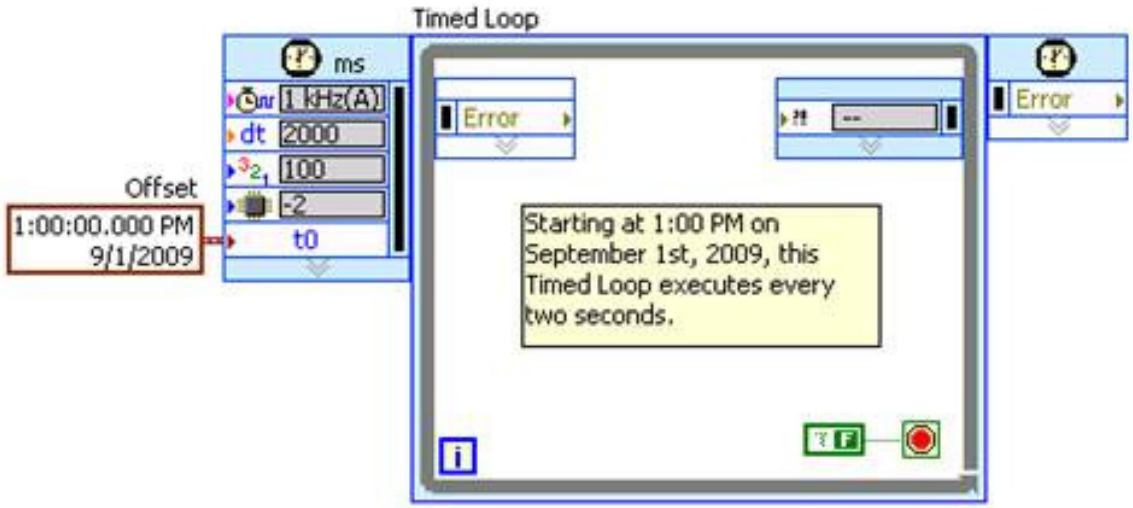
Synchronization: How?

- Internal clock sharing: NI DSA modules (9234, 9237,etc).

- External clock sharing:?

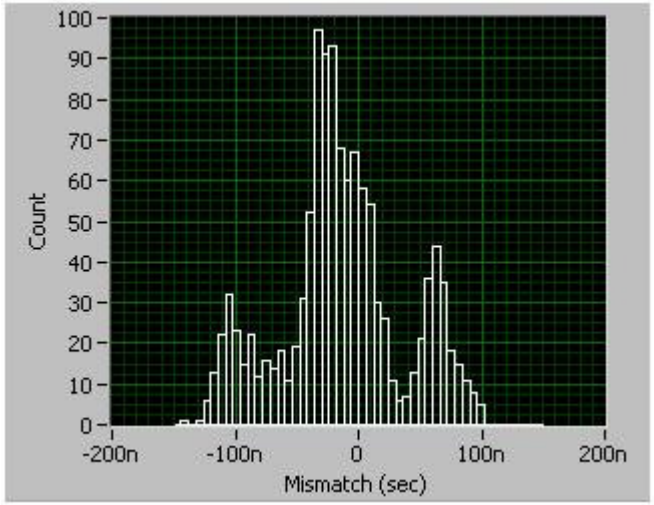
Synchronization options

- GPS RT-clock sync +/- 1 µs
- IEEE 1588 RT sync 1 MHz RT-loop sync



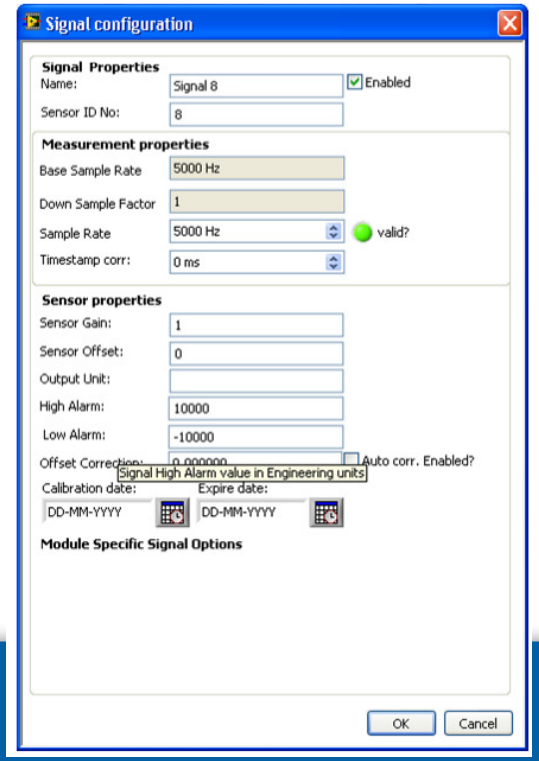
Synchronization Reference design

- DSA Module Synchronization Reference Design for Multiple cRIO Chassis



Configurability

- Storage of configuration on cRIO RT-Controller
- Configuration adjustable by host application
- Sampling rate
- Signal names
- Signal properties

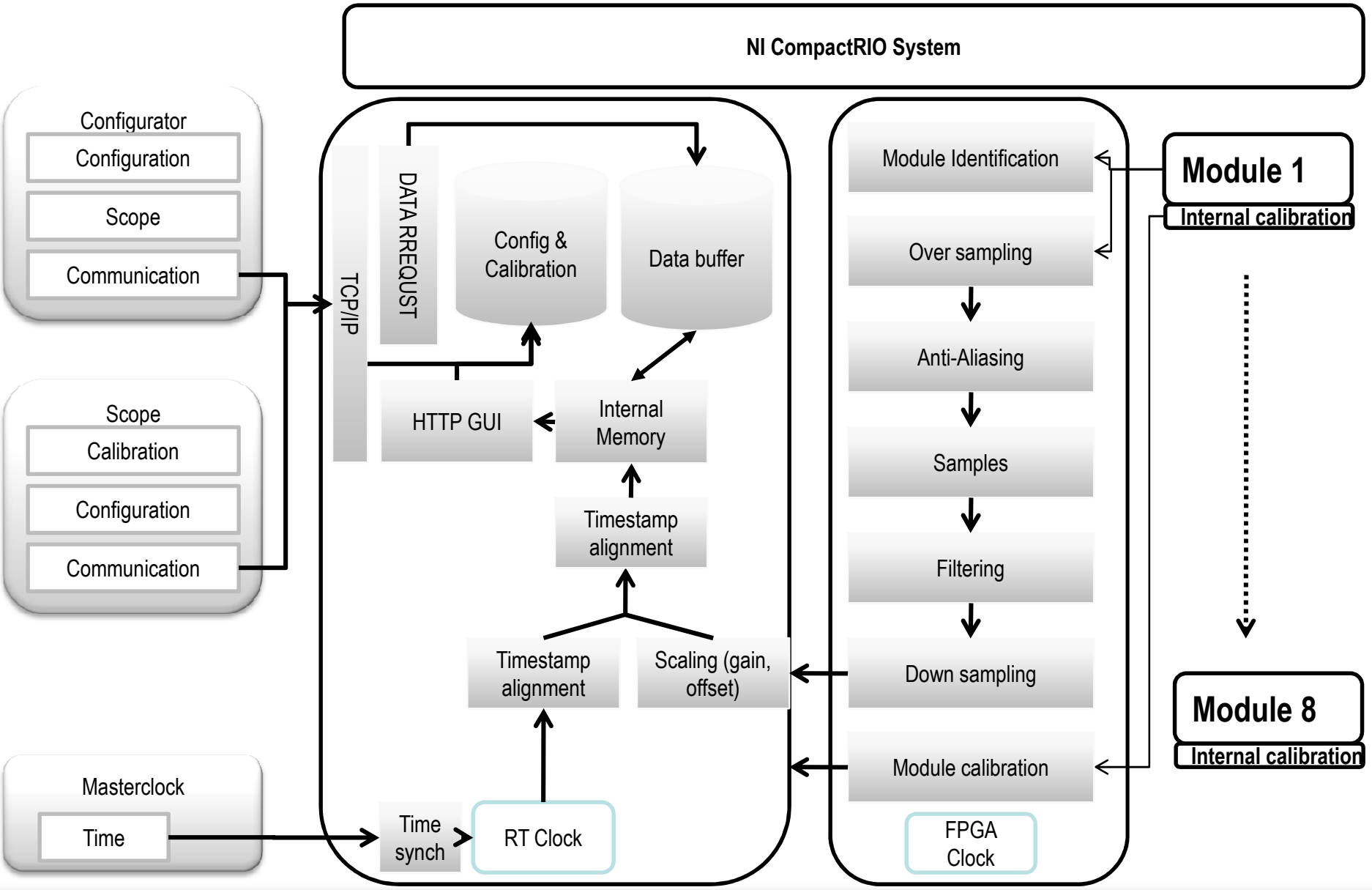


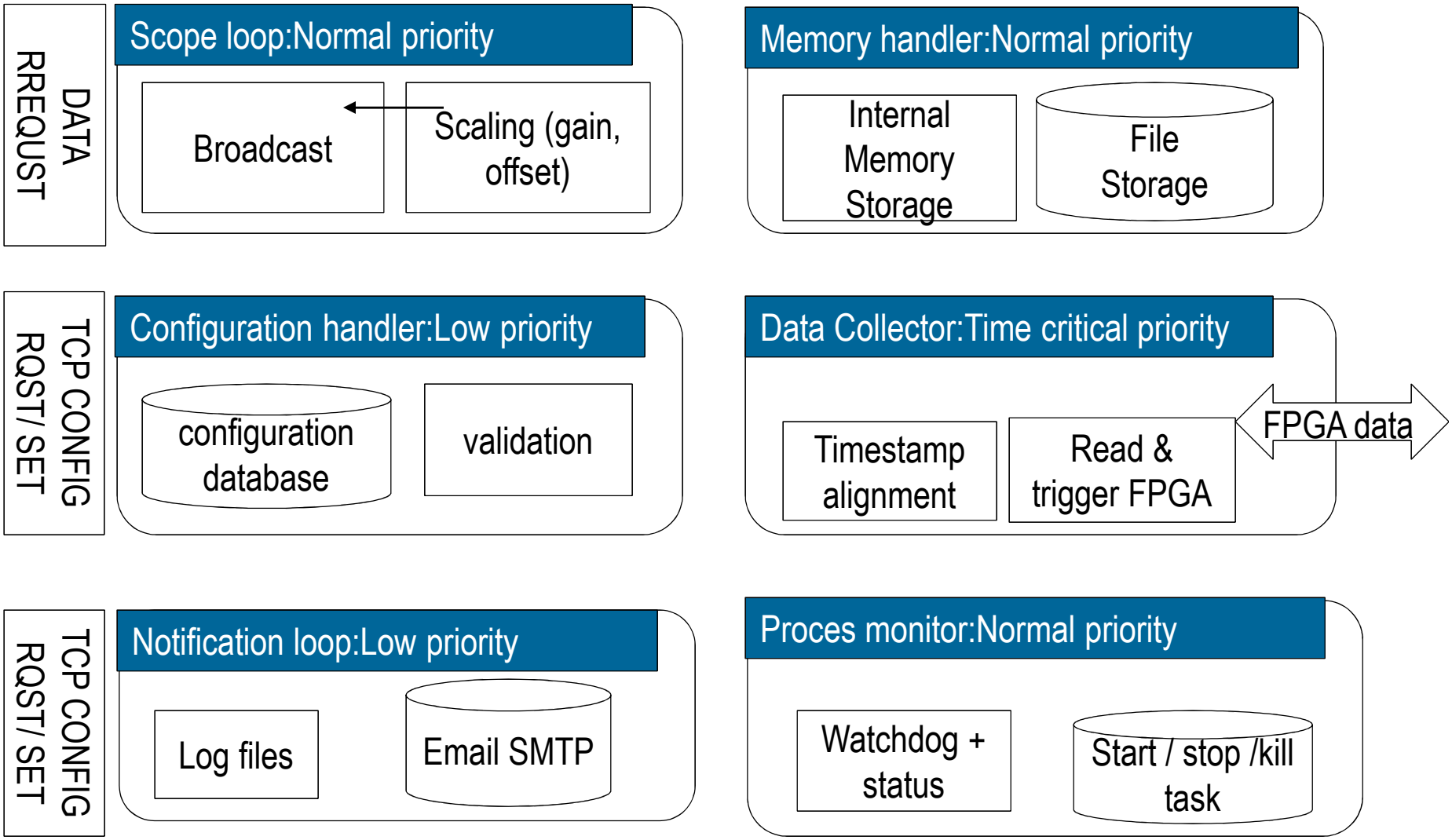
Configurability

- Support for different I/O module sets without scan engine support - > build own interface between FPGA – RT
- Dynamically load bitfile
- Not all module functions have full support for configuration in LV FGPA (NI 9219 Universal module)

Tasks, responsibilities and communication

SA can be defined as a **high-level system design** that '*describes the **sub-systems** and **components** of a software-system and the **relationships** between the components*'.


NI CompactRIO System
Configurator
Configuration
Scope
Communication
Scope
Calibration
Configuration
Communication
Masterclock
Time
TCP/IP
DATA RREQUST
Config & Calibration
Data buffer
HTTP GUI
Internal Memory
Timestamp alignment
Timestamp alignment
Scaling (gain, offset)
Time synch
RT Clock
Module Identification
Over sampling
Anti-Aliasing
Samples
Filtering
Down sampling
Module calibration
FPGA Clock
Module 1
Internal calibration
Module 8
Internal calibration


DATA RREQUST
Scope loop:Normal priority
Broadcast
Scaling (gain, offset)
Memory handler:Normal priority
Internal Memory Storage
File Storage
TCP CONFIG RQST/ SET
Configuration handler:Low priority
configuration database
validation
Data Collector:Time critical priority
Timestamp alignment
Read & trigger FPGA
FPGA data
TCP CONFIG RQST/ SET
Notification loop:Low priority
Log files
Email SMTP
Proces monitor:Normal priority
Watchdog + status
Start / stop /kill task

Timing and Priorities

- DMA buffer size between FGPA and RT determines the timing. (Buffer is set to 10..20 sec.)
- FTP runs at normal priority and can obtain full CPU. So other tasks must have similar or higher priorities. (2Mb/s)

Conclusions

- The NI cRIO platform is very powerful and flexible with respect to software-engineering.
- Familiarize with the OS behavior and the functionality supported by LabVIEW Real-Time and LabVIEW FPGA.
- Programming a Real-Time system still requires a solid understanding of software engineering!

Recommendations

- Plan ahead
  - Memory locations for buffering
  - Timing and priorities
  - Storage strategy
  - Supported features on FPGA
  - Test performance impact of features on RT

Recommendations

Reference Example for Streaming Data from FPGA to cRIO to Windows

http://zone.ni.com/devzone/cda/epd/p/id/5919

DSA Module Synchronization Reference Design for Multiple cRIO Chassis

http://zone.ni.com/devzone/cda/epd/p/id/6146

Stream to disk

http://zone.ni.com/devzone/cda/tut/p/id/9272

Synchronizing Multiple CompactRIO Chassis' Using IEEE 1588

http://digital.ni.com/public.nsf/allkb/BE814CC28C8D87CA8625785E0045C799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