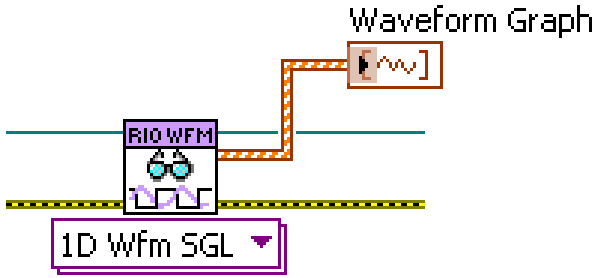
Understand High-Speed Data Acquisition with NI CompactRIO



Doug Farrell

Product Manager – Condition Monitoring Systems

National Instruments

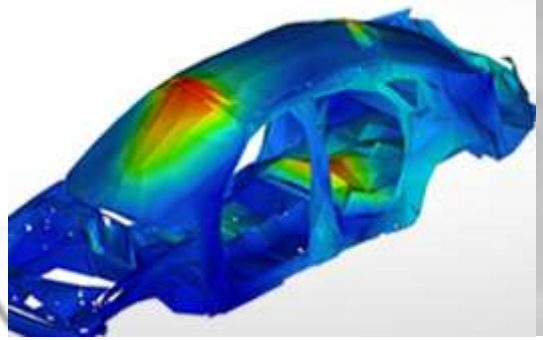
Agenda

1. CompactRIO Waveform Reference Library
2. Acquisition Modes and DMA Transfers
3. CompactRIO Streaming Benchmarks
4. Demo
5. Customizing the FPGA VI
6. Heterogeneous Acquisitions

Waveform Data

- Fundamental to DSA applications
- Waveform logging applications require cRIO

MCM



NVH

EPM

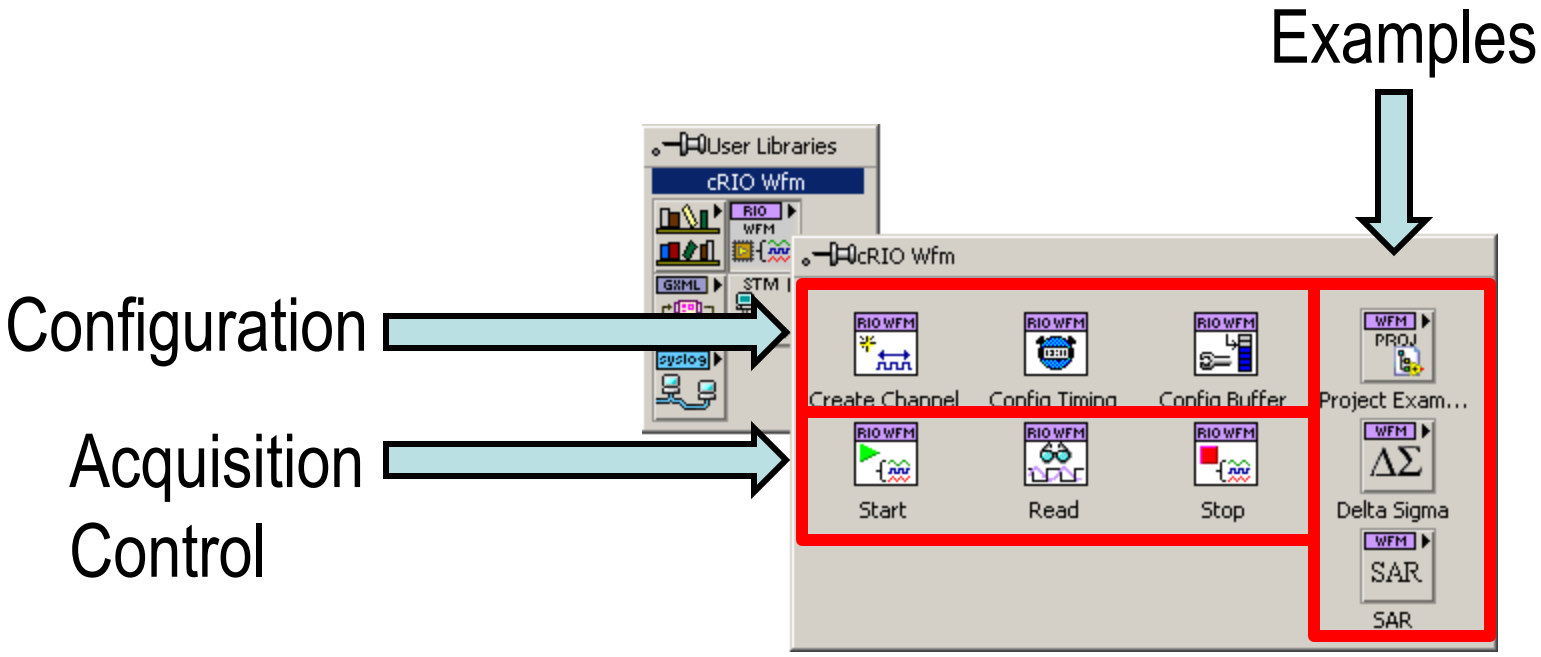
SHM

Key Concepts and Considerations

1. **CompactRIO resources are limited**
   - Memory and CPU must be managed on both FPGA and RT
2. **Mixed signal acquisitions**
   - Vibration, temperature, current, tachometer, pressure, strain
3. **Different acquisition modes**
   - Finite/continuous
4. **Adequate error checking is crucial**
   - Buffer overflow, buffer underflow, timeouts, etc.

CompactRIO Waveform Library for 2011

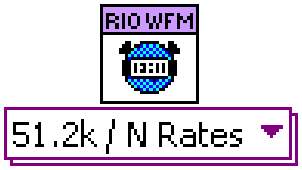
- Found on the LabVIEW Functions Palette



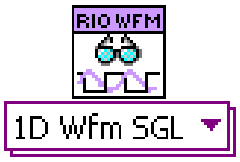
CompactRIO Waveform Reference Library

Channel Configuration

Start Acquisition



Timing Configuration

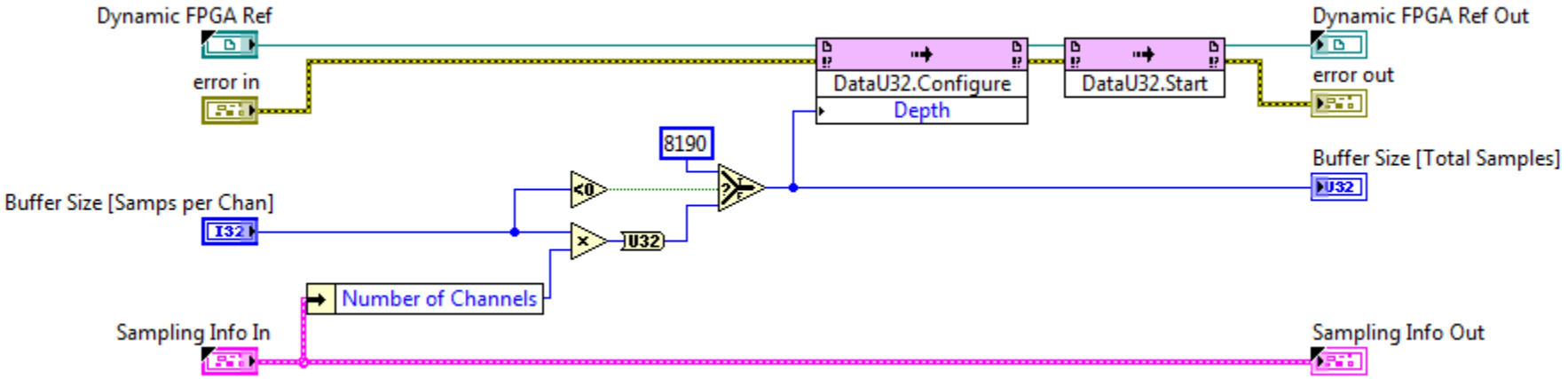


Read Data

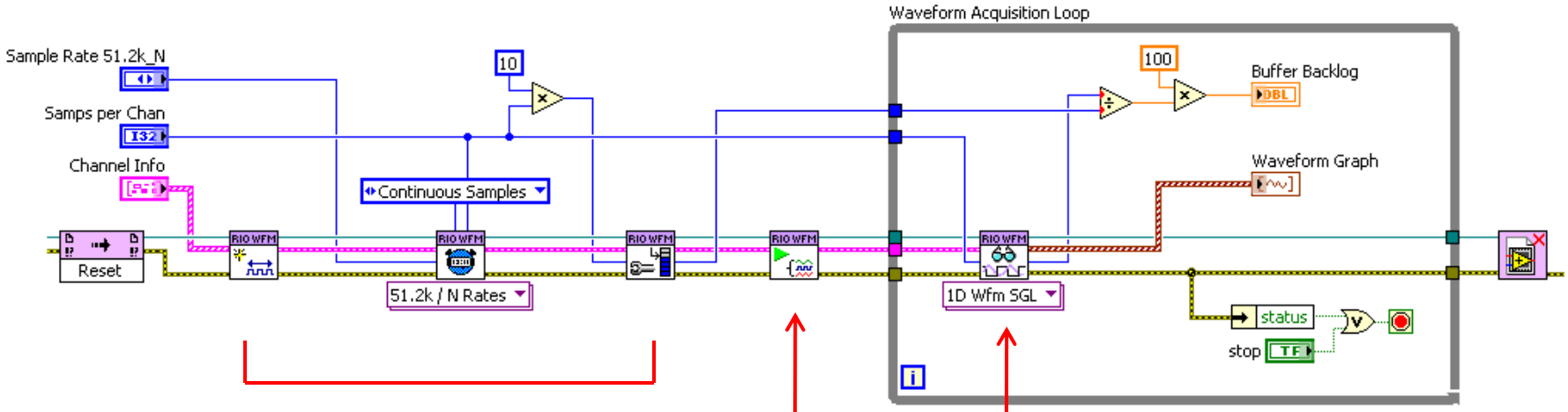
Buffer Configuration

Stop Acquisition

Buffer Configuration



CompactRIO Waveform Example



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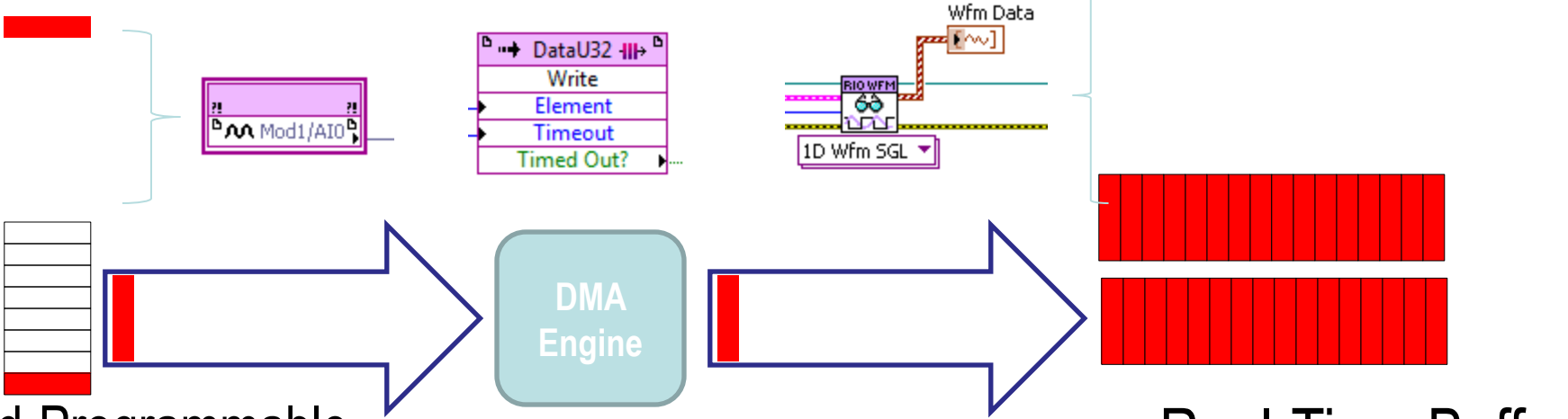
Target-to-Host Transfer – Finite

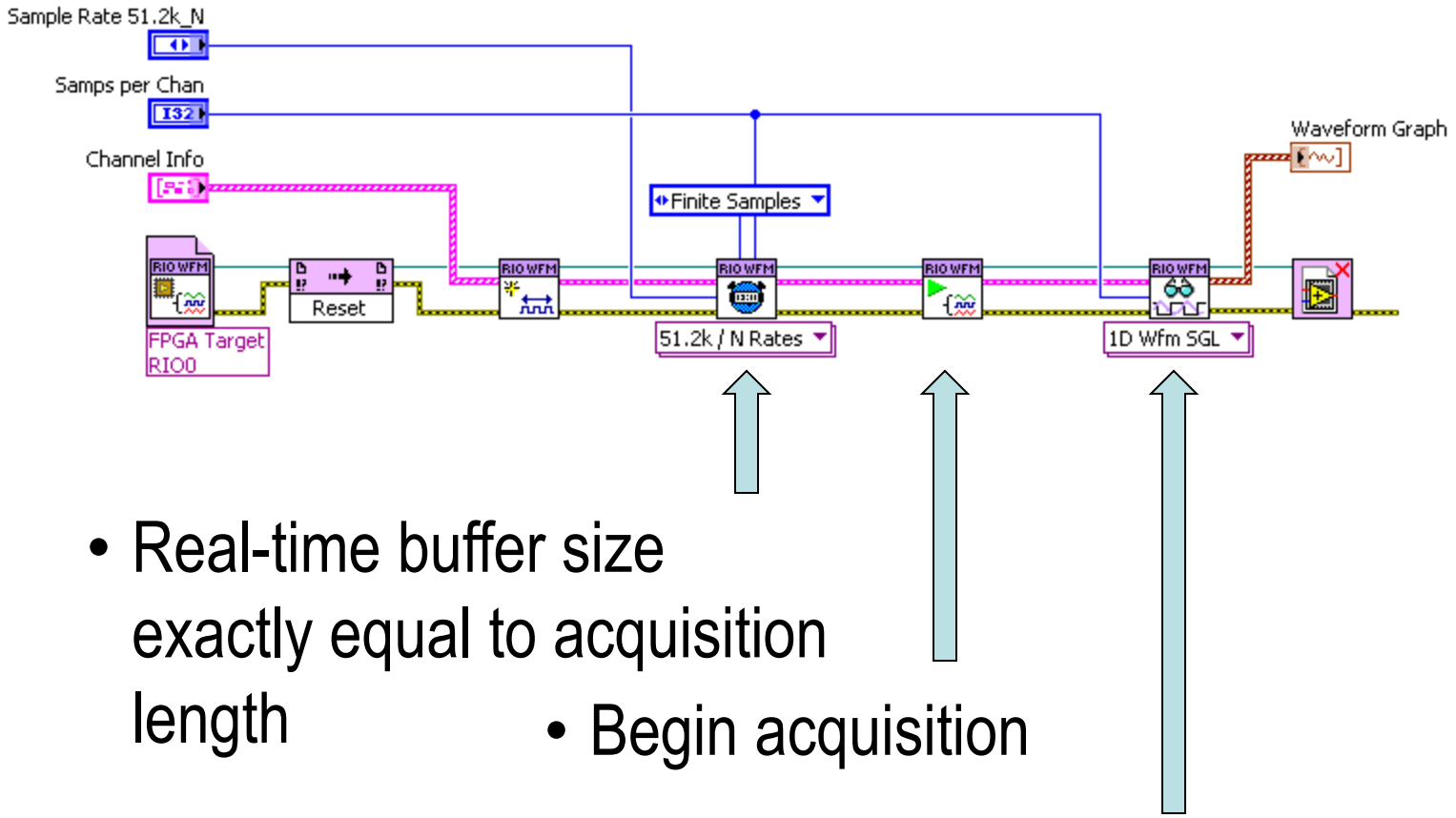
Data Element



Field-Programmable Gate Array (FPGA) FIFO

Real-Time Buffer

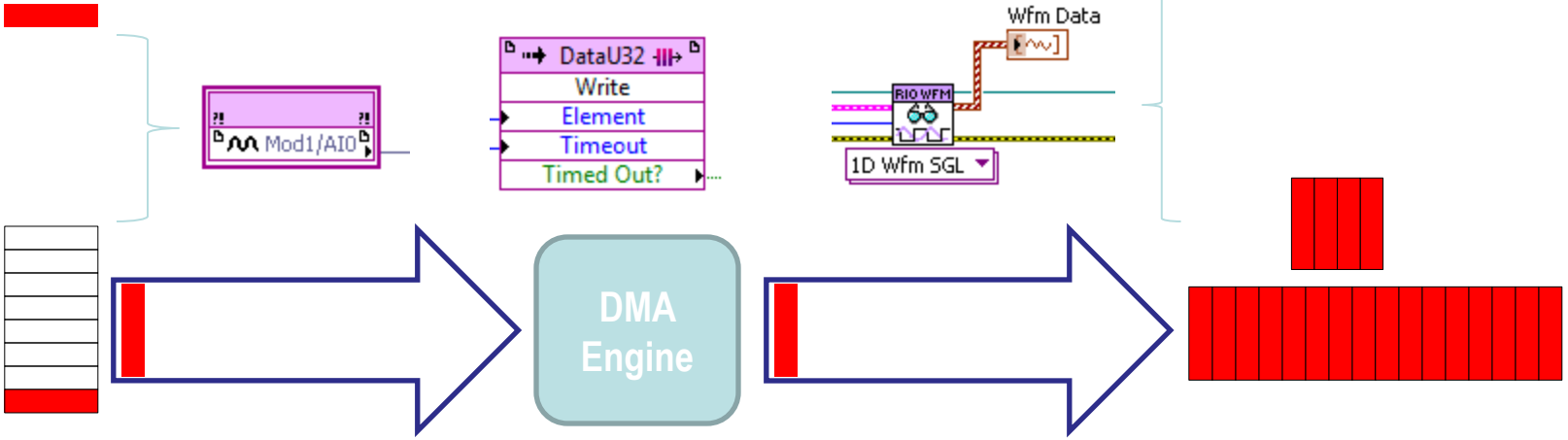
Finite Acquisition



- Real-time buffer size exactly equal to acquisition length
- Begin acquisition
- Read one (and only) data block

Target-to-Host Transfer – Continuous

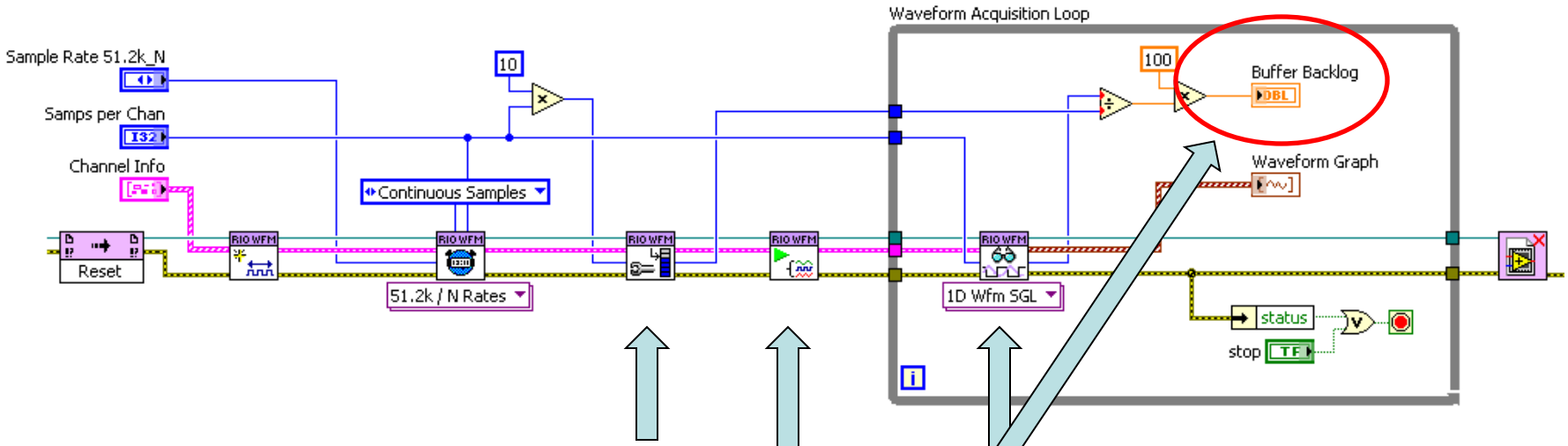
Data Element



FPGA FIFO

Real-Time Buffer

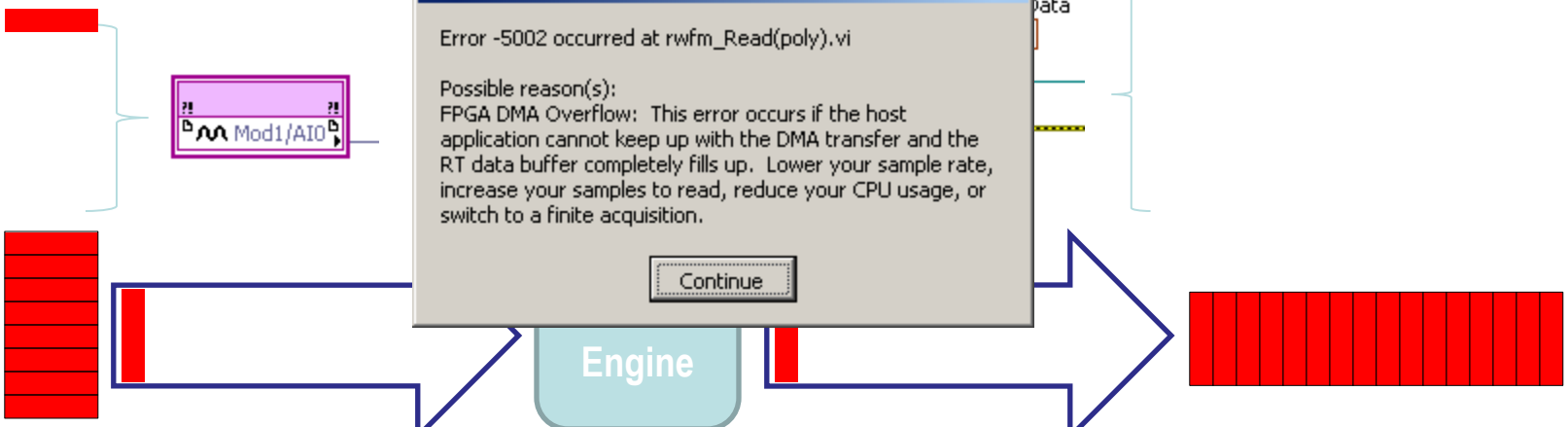
Continuous Acquisition



- Real-time buffer size ~5 -10 times larger than acquisition length
- Beware of overflows
- Begin acquisition
- Read one data block

Continuous Acquisition – Buffer Overflow

Data Element



FPGA FIFO

Real-Time Data Buffer

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1. CompactRIO Waveform Reference Library
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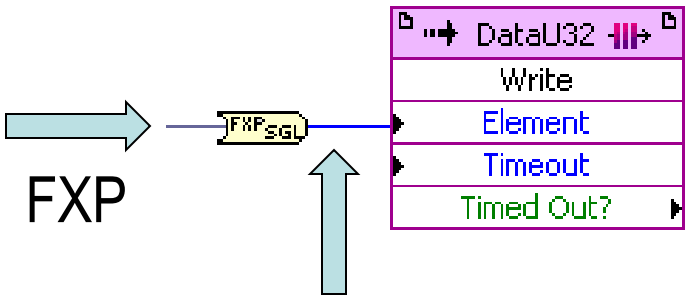
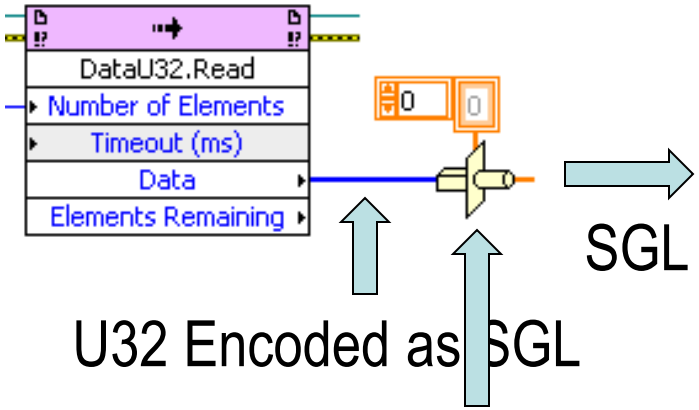
Performance

FXP to Floating Point Conversion:

On FPGA



In Read VI

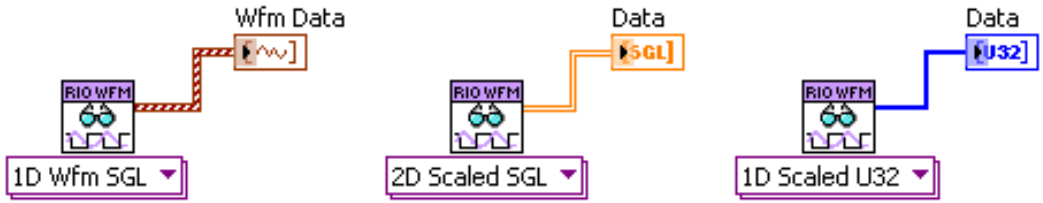


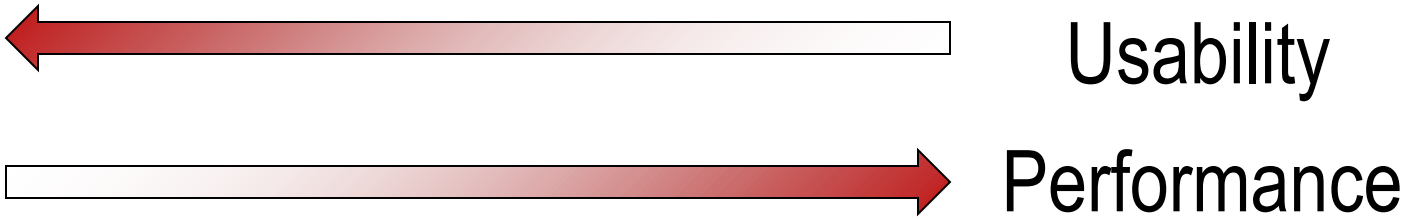
A typecast from U32 to SGL is 40% faster in real-time than a conversion from FXP to SGL

Performance

The “Read” VI Is Polymorphic

1D Wfm SGL 2D SGL Array 1D U32 Array





Benchmarks at fs = 51.2 kS/s

400 MHz

NI cRIO-9014	Old Channels	New Channels
Cont Wfm to TDMS	8	1.64
Cont 1D U32 to Binary	17	3.48
Cont Wfm over TCP/IP	11	2.25

533 MHz

NI cRIO-9022	Channels	Throughput (MB/s)
Cont Wfm to TDMS	10	2.05
Cont 1D U32 to Binary	25	5.12
Cont Wfm over TCP/IP	16	3.28

800 MHz

NI cRIO-9024	Channels	Throughput (MB/s)
Cont Wfm to TDMS	15	3.07
Cont 1D U32 to Binary	36	7.37
Cont Wfm over TCP/IP	29	5.94

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4. **Demo**
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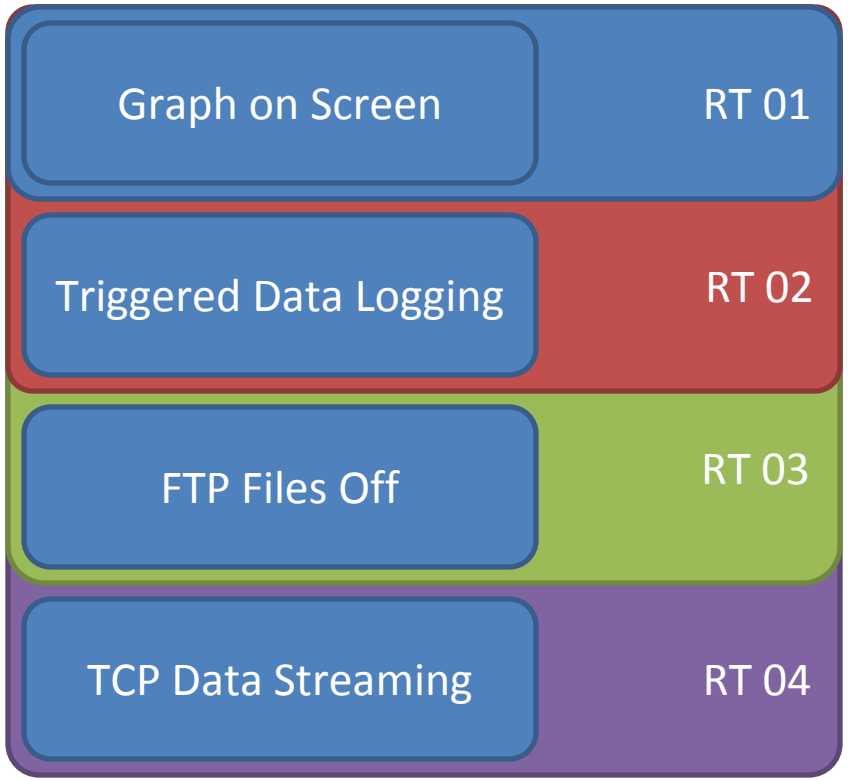
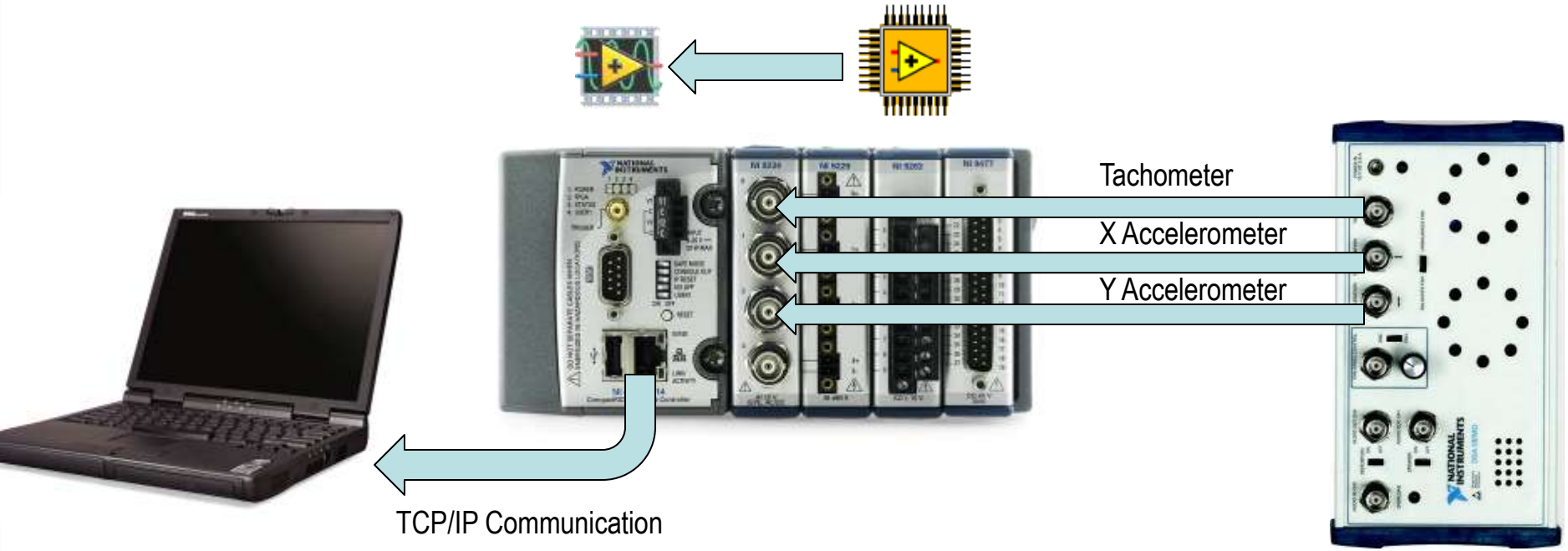
Vibration Data Logger



DEMO

- FPGA Acquisition Streamed to Real-Time Host



Agenda

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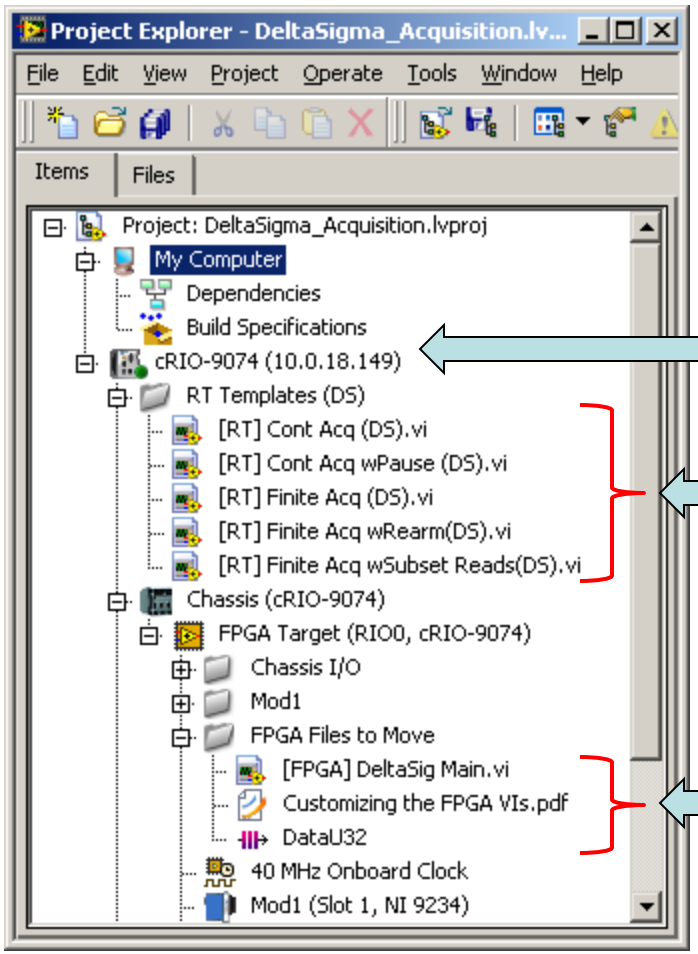
FPGA VI: Some Assembly Required



CompactRIO Target

Real-Time Examples

FPGA VI "Template"

Customization PDF

DMA Channel

NI C Series Hardware

“SAR” Modules

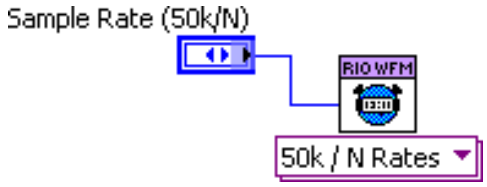
- Use “Successive Approximate Register” ADCs
- ADCs are lower latency, simpler to implement, and have less resolution

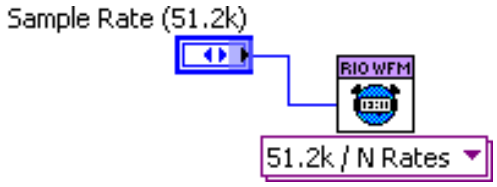
“Delta Sigma” Modules

- Use Delta Sigma ADCs
- ADCs have higher dynamic range and built-in antialiasing filters, but also group delays (high latency)

You Must Know Module Type

Delta Sigma

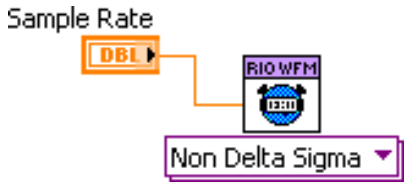




NI 9227
NI 9235
NI 9237

NI 9234

SAR



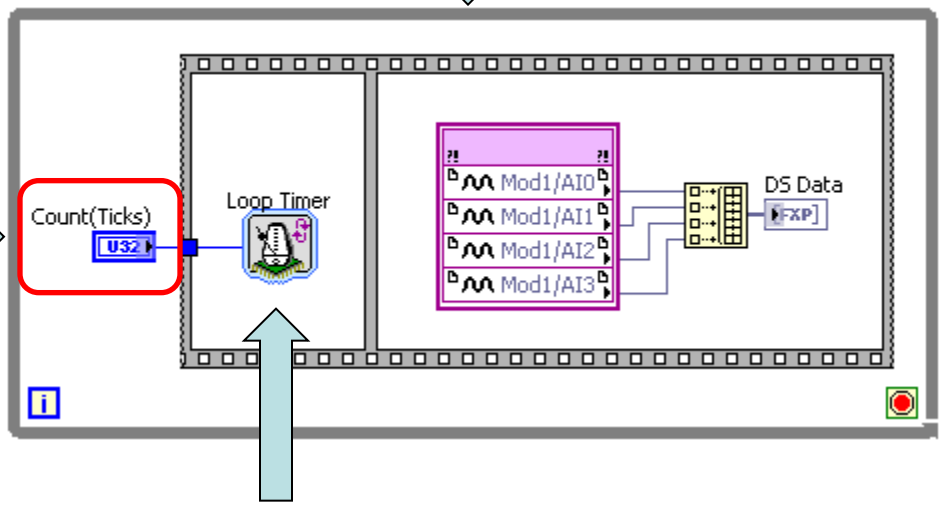
NI 9201
NI 9215
NI 9221

Timing the FPGA VI – SAR

- Externally Timed Modules

While Loop Rate = Sample Rate

Specify Sample Rate By Ticks



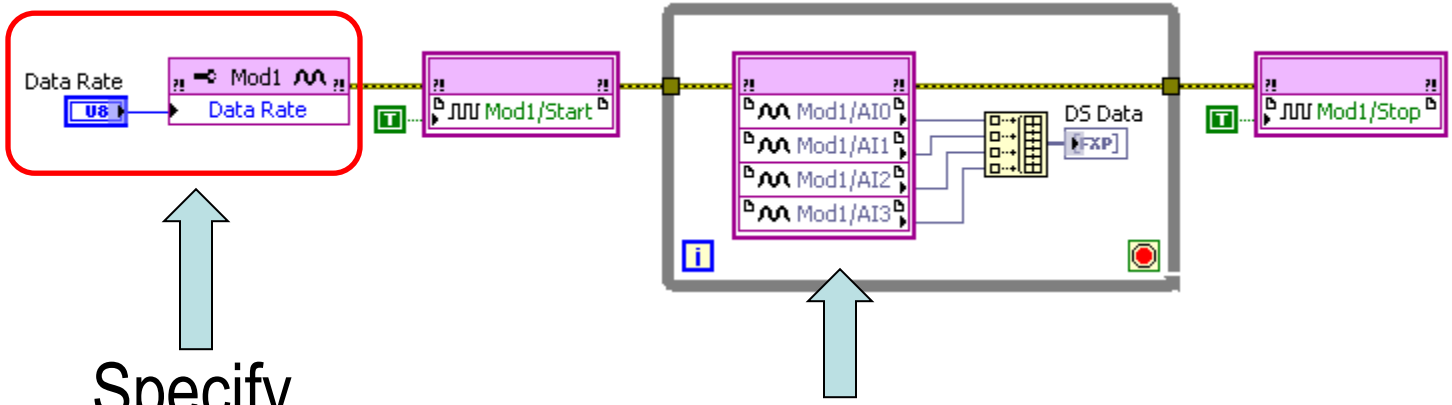
Loop Timer

Times the While Loop

Timing the FPGA VI – Delta Sigma

- Self Timed Modules

While Loop Rate = Sample Rate

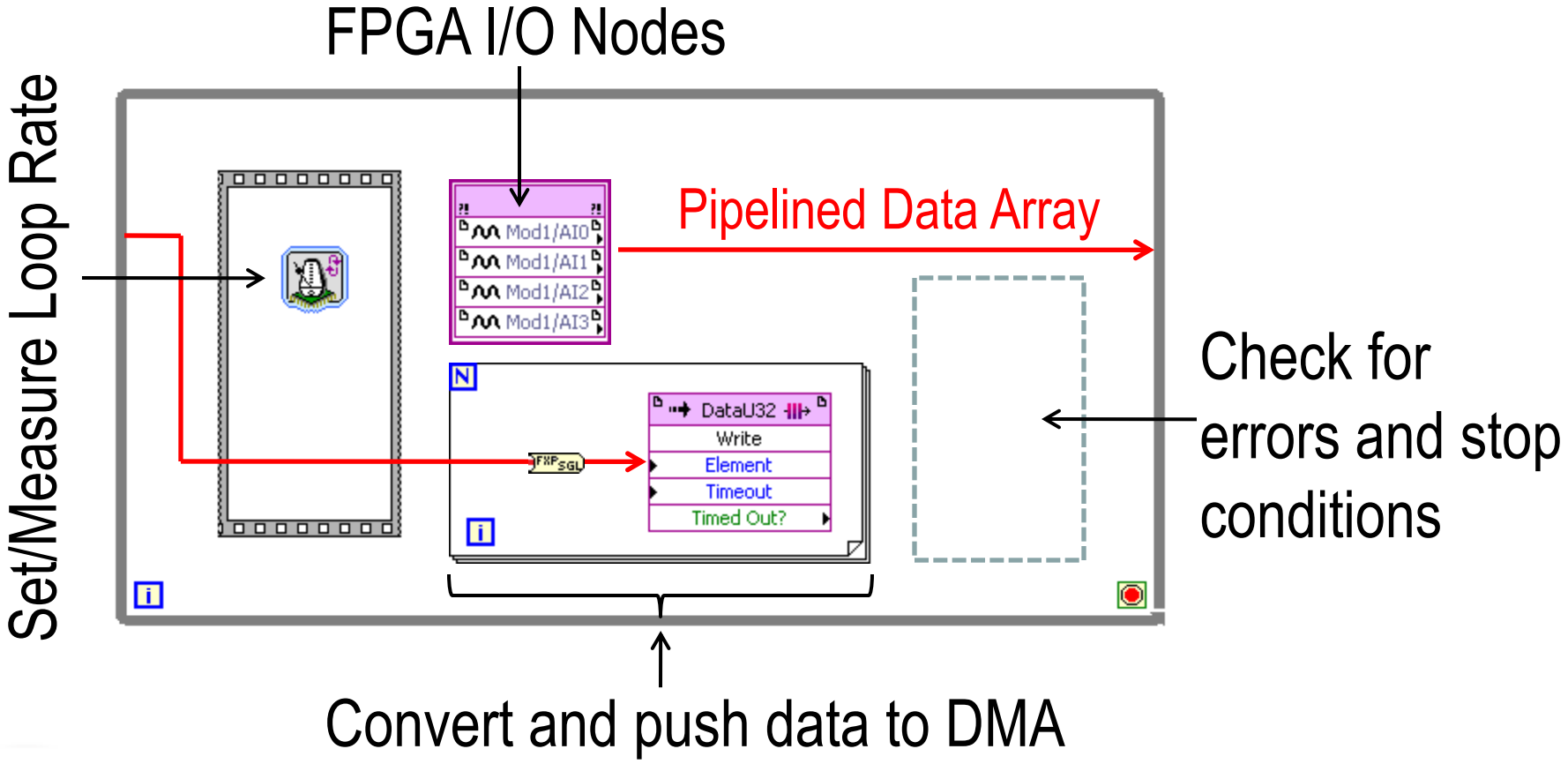


Specify Sample Rate By Enum

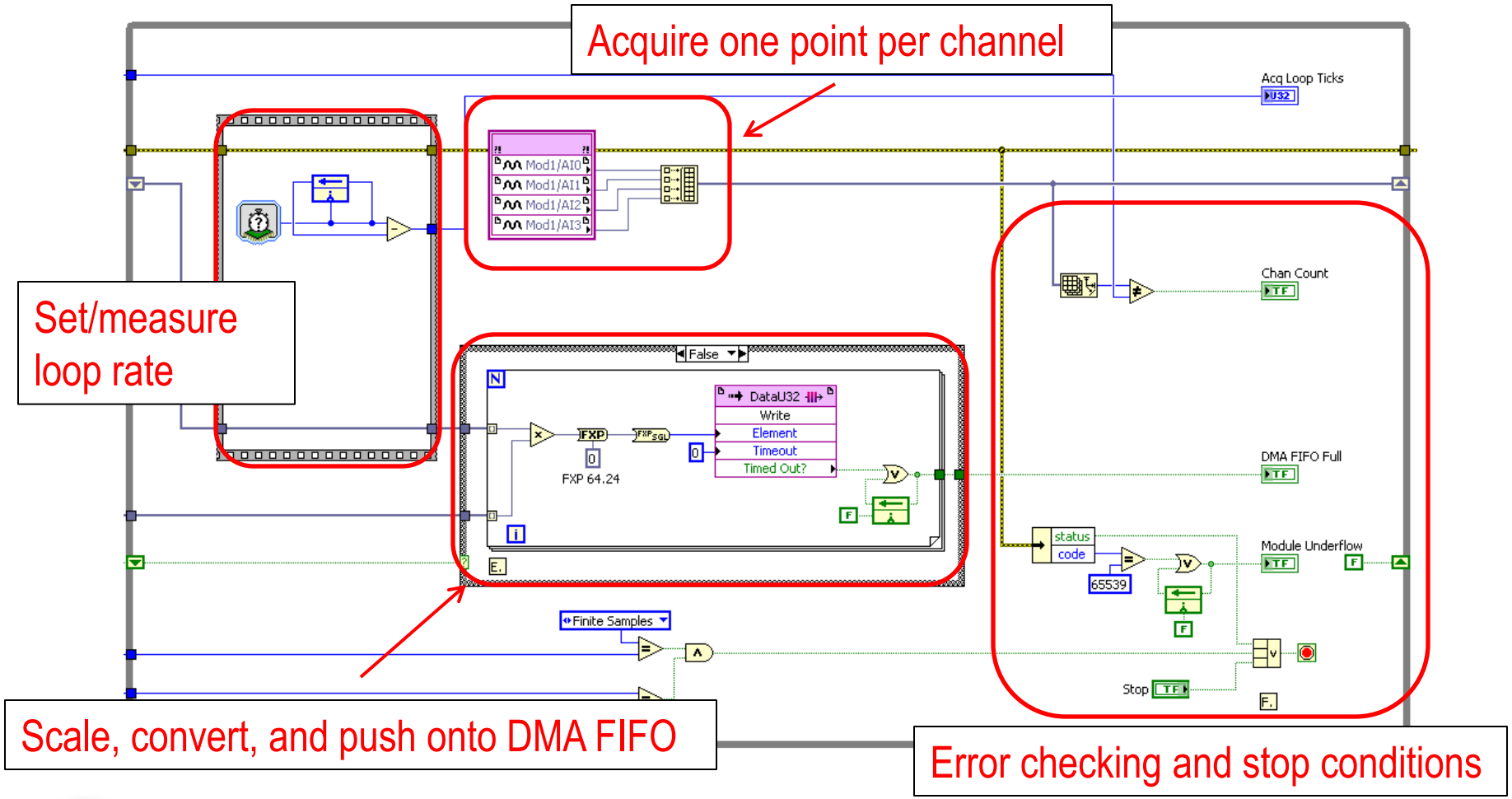
FPGA I/O Node Times the While Loop

Adding the DMA Channel

Delta Sigma FPGA VI and SAR FPGA VI have similarly structured

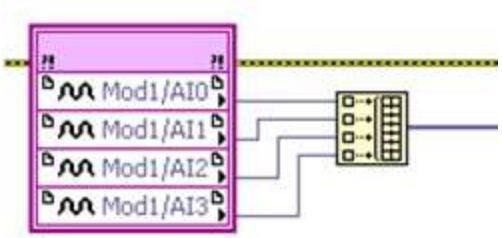


FPGA VI: Acquisition Loop

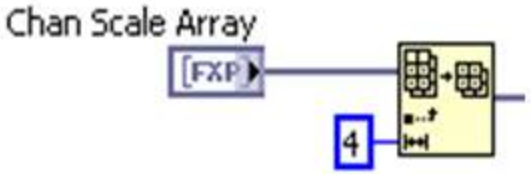


FPGA VI: What Do I Have to Change?

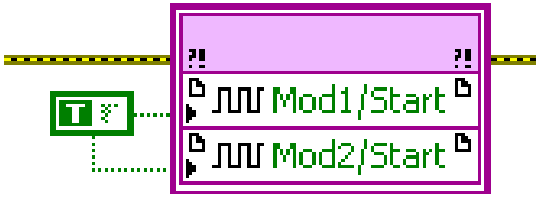
1. Expand Channels



2. Change this constant



3. Add data rate and start/top nodes (Delta-Sigma only)



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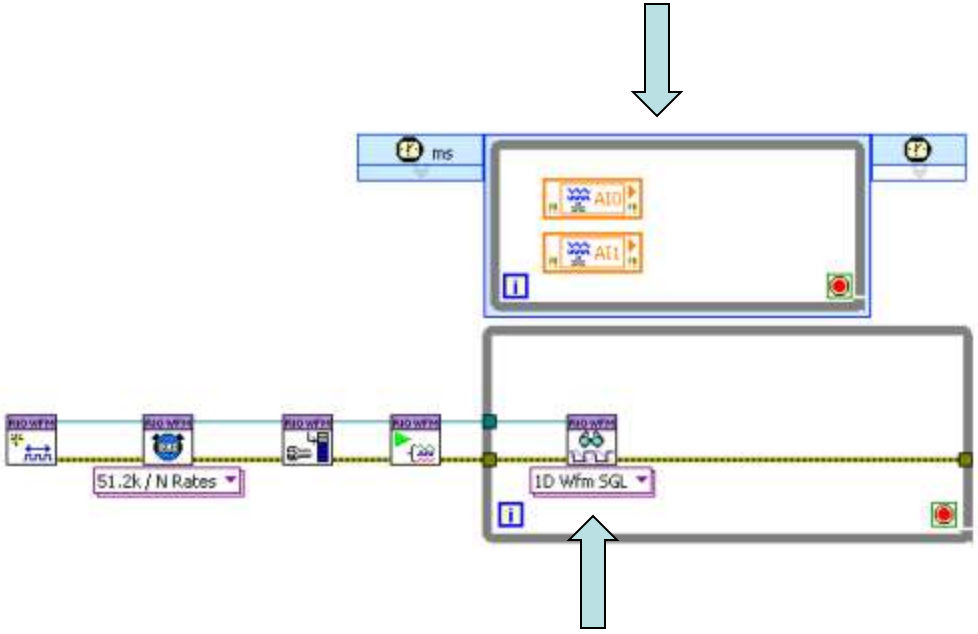
High-Speed and Low-Speed Acquisition

Two DMA Channels

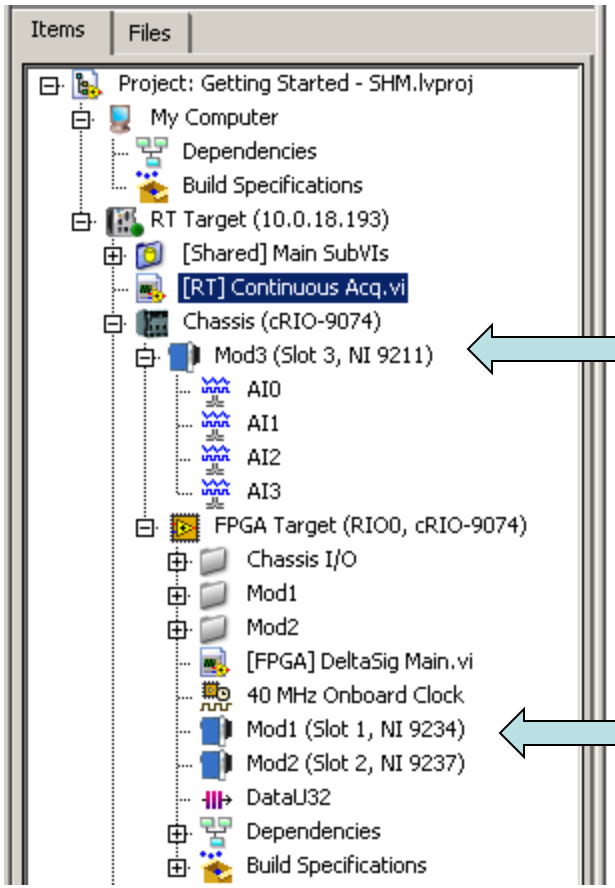


One DMA Channel

Low-Speed Analog Input via NI Scan Engine

High-Speed Analog Input via CompactRIO Waveform Reference Library

DMA With Scan Engine



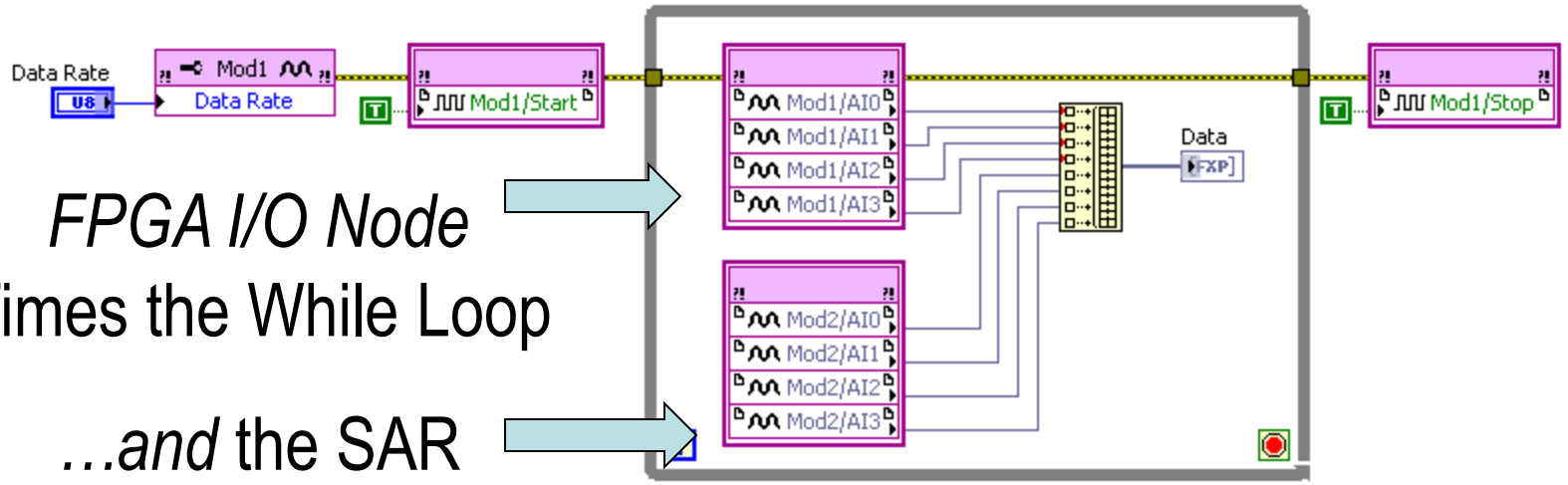
Module Location in Project Determines *FPGA* or *Scan* Operation

NI 9211 (thermocouple) is directly under “Chassis”

NI 9234 (vibration) and NI 9237 (strain) are under “FPGA Target”

What About DSA and SAR Together?

Recall the Delta Sigma Acquisition Method:



FPGA I/O Node Times the While Loop

…and the SAR Modules

Summary

- Abstracts FPGA
- Automatic Error Handling
- Reduced CPU Load
- Don’t Start From Scratch
- Common Architecture

Documentation

Developer Zone: CompactRIO Waveform Acquisition Reference Library

ni.com or Google search terms: **crio waveform**
http://zone.ni.com/devzone/cda/epd/p/id/6206

- Download CompactRIO Waveform Library
- Download includes examples for both Delta Sigma and SAR architectures
- Download includes documentation on each VI and instructions on how to modify the FPGA
- Dev Zone includes more detailed benchmarks on stream to disk and streaming over TCP/IP

Download