Design Customized Instruments with LabVIEW FPGA

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Hardware Overview

PXIe-5644R 6 GHz Vector Signal Transceiver

PXIe-5644R	
Configuration	VSA and VSG w/ independent LOs 24 DIO lines @ 250 Mbps
Frequency Range	65 MHz to 6 GHz
Bandwidth	80 MHz
Features	• Programmable FPGA w/ LabVIEW • Fast Tuning Mode: <400 µs

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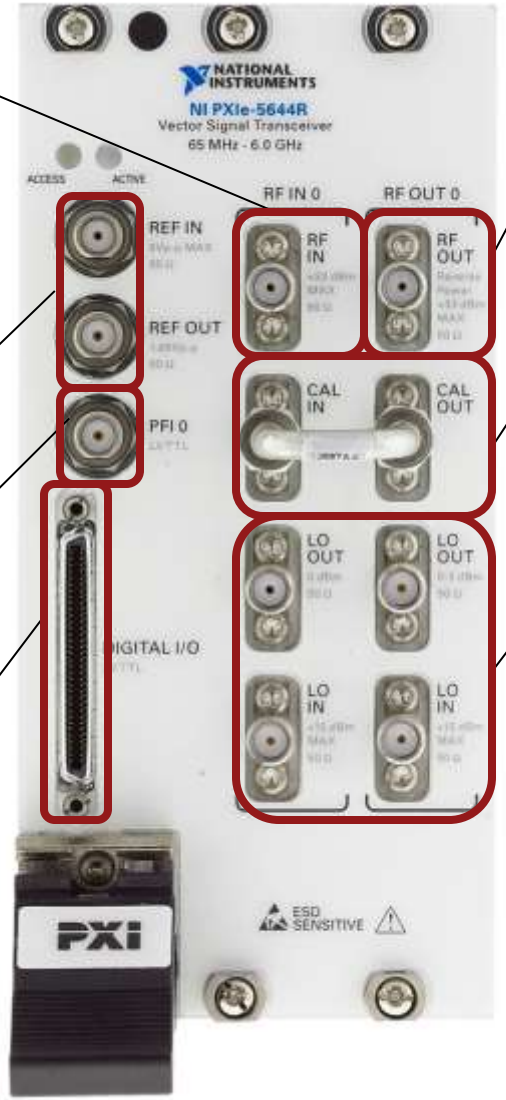
A Closer Look at the PXIe-5644R

RF Input
65 MHz – 6 GHz
80 MHz BW

Reference In/Out

Trigger

Digital I/O
24 channels
Up to 250 Mbps
Additional triggering



RF Output
65 MHz – 6 GHz
80 MHz BW

Calibration In/Out
Always keep the calibration cable connected

LOs In/Out
Independent
In & Out
MIMO Support

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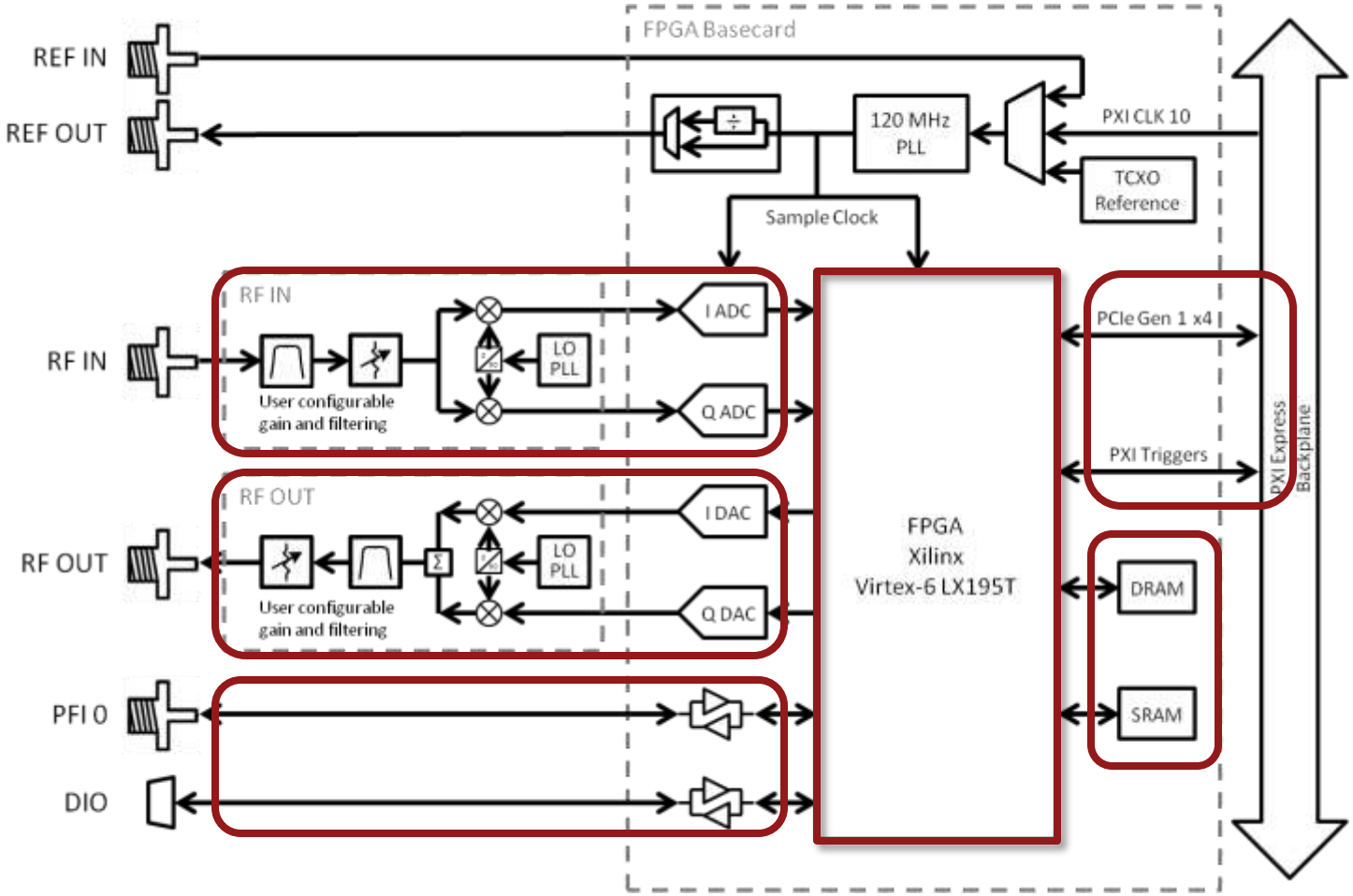
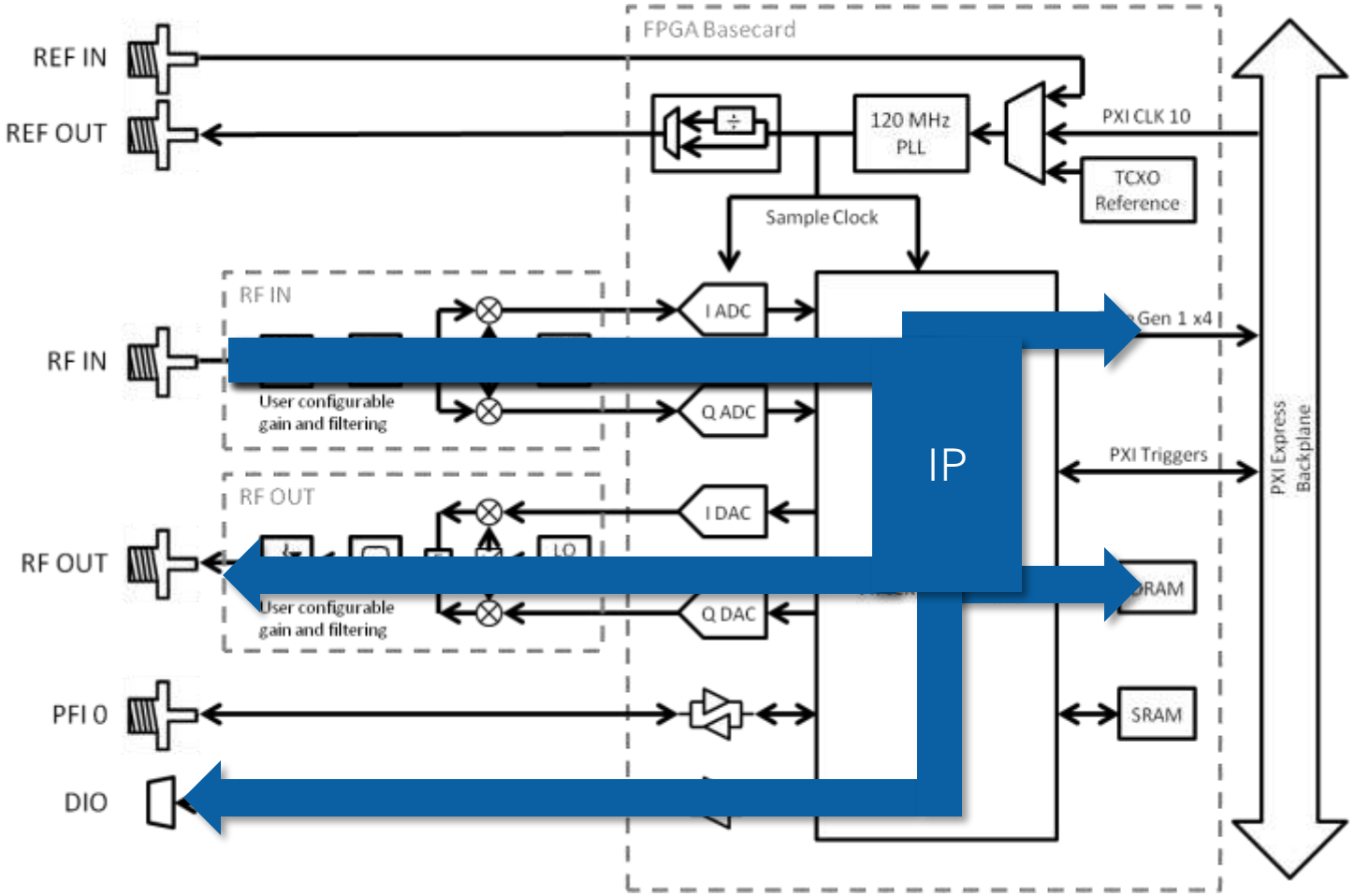
PXIe-5644R Block Diagram



PXIe-5644R Block Diagram

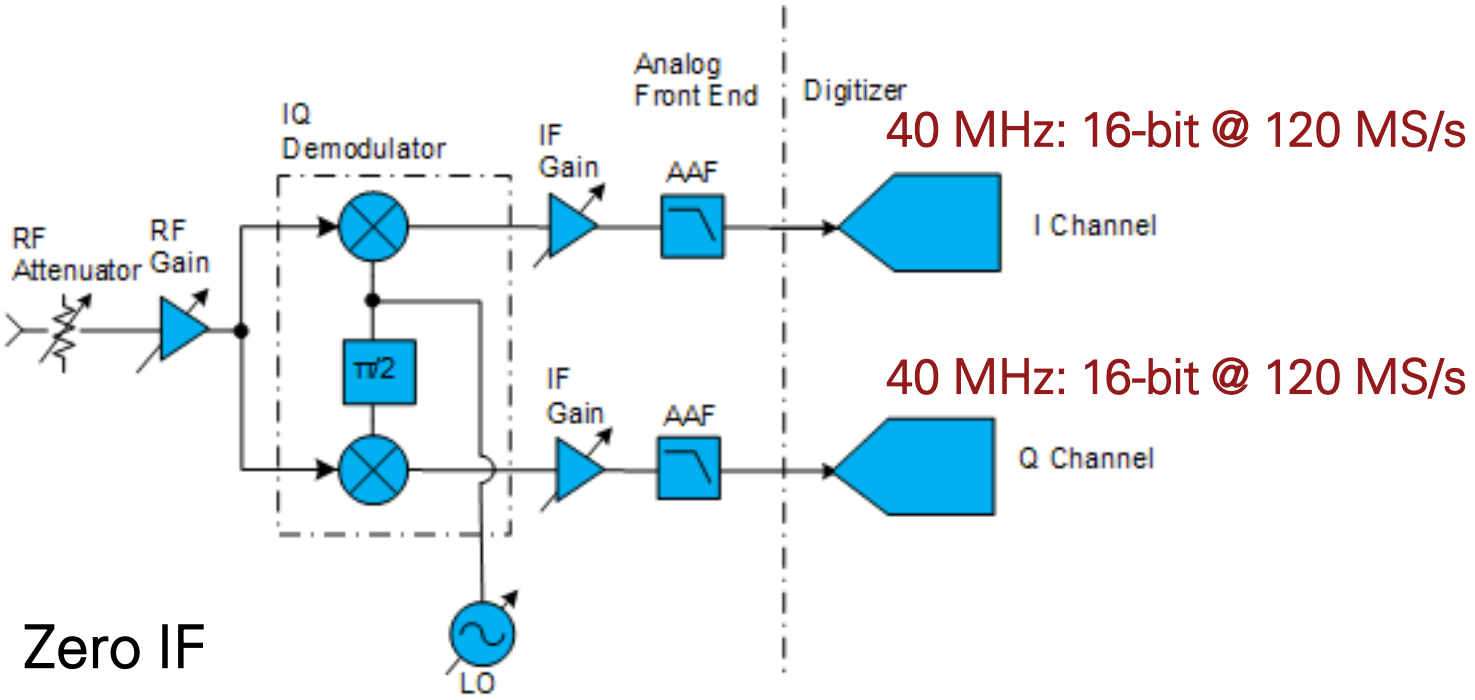


Up to 5 Signal Analyzers and Generators in a Single PXI Express Chassis

- MIMO Configurations
- Parallel Multi-DUT Test

Calibration

PXIe-5644R VST Receiver Architecture

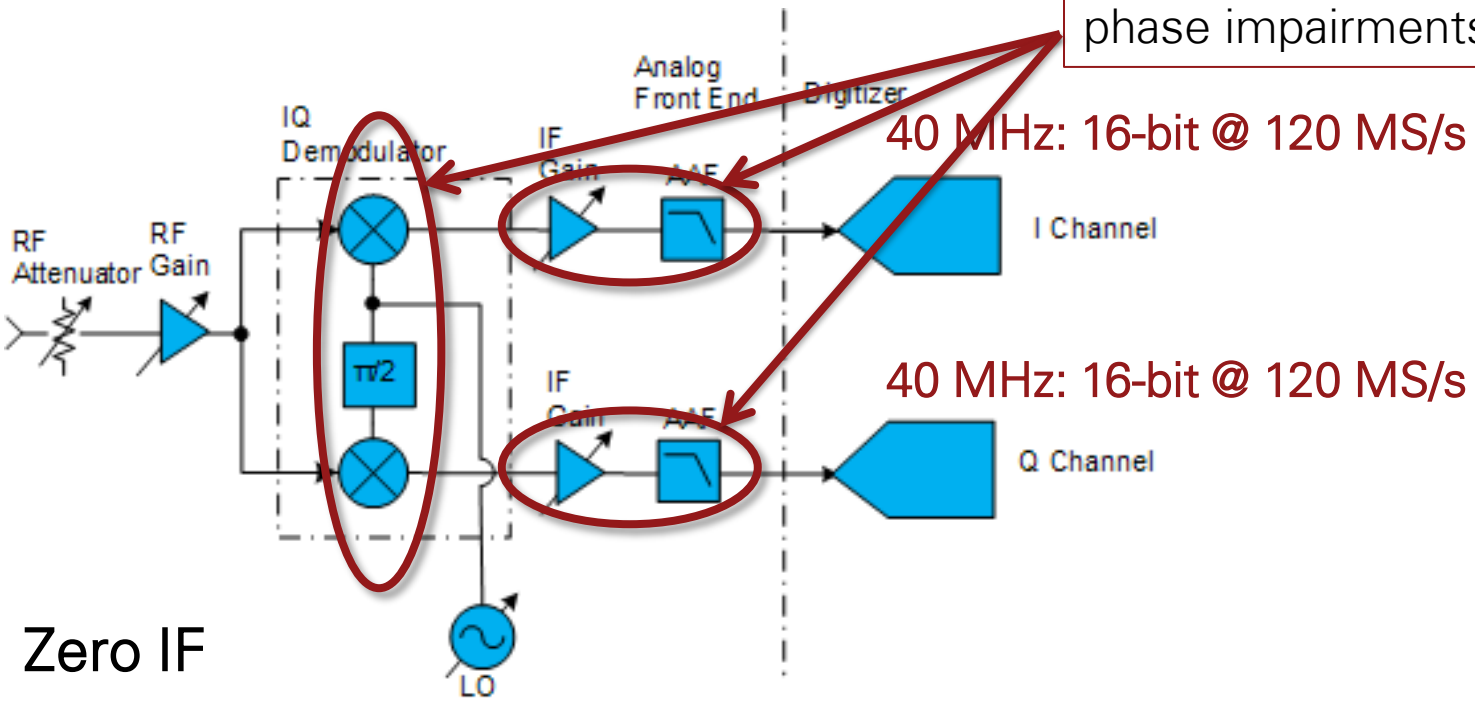


Zero IF

- ✓ Very small size, low cost, and low power
- ✓ Wide analysis bandwidth
- ✓ Ideal for modulated signal analysis
- ◆ Alias rejection and image suppression
- ◆ IQ Calibration/Equalization

PXIe-5644R VST Receiver Architecture

Calibration is needed to correct for I/Q gain and phase impairments

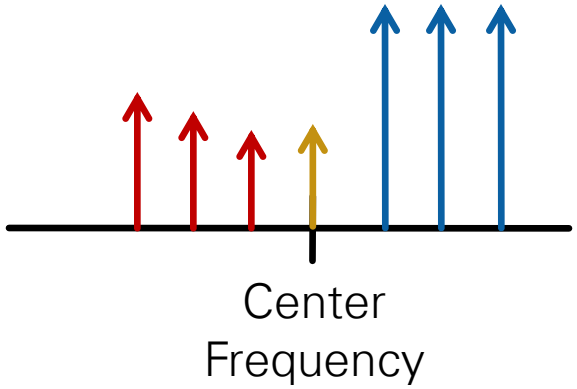


Zero IF

- ✓ Very small size, low cost, and low power
- ✓ Wide analysis bandwidth
- ✓ Ideal for modulated signal analysis
- ◆ Alias rejection and image suppression
- ◆ IQ Calibration/Equalization

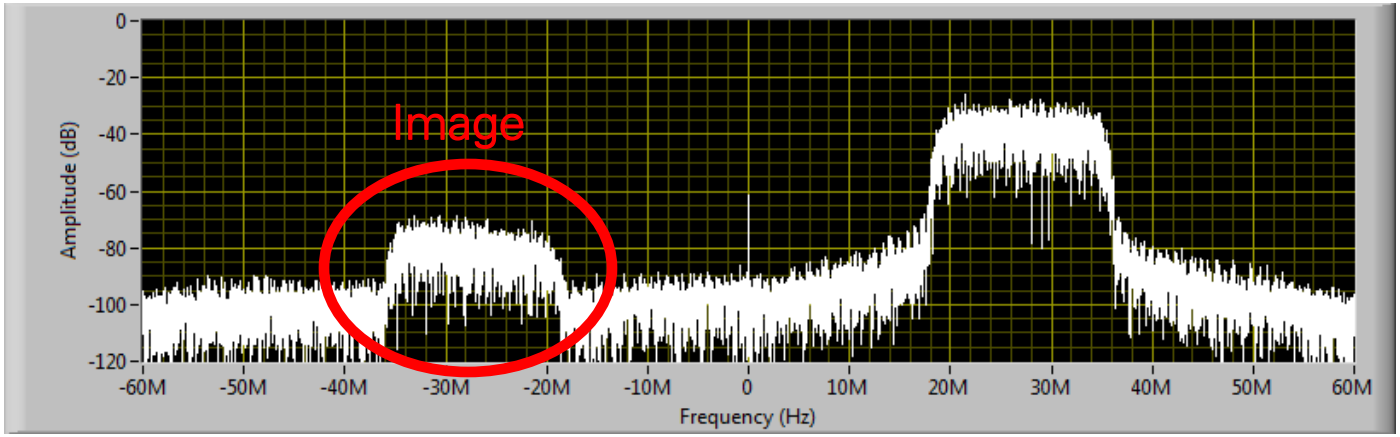
Traditional I/Q Calibration Approach

- Traditional approach only corrects for the impairments at a single frequency

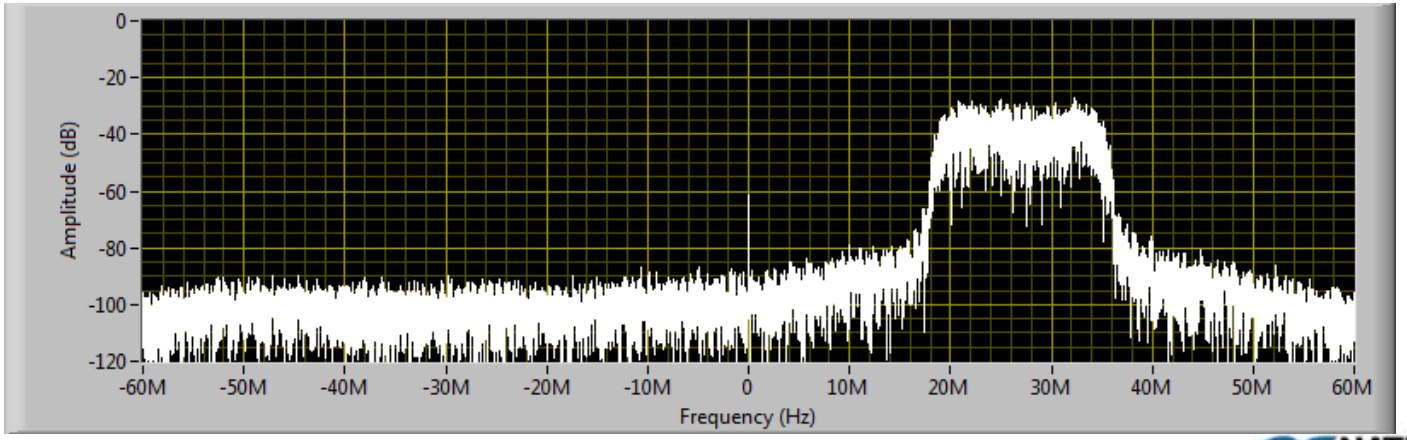


Effects of IQ Impairments on QAM

Traditional

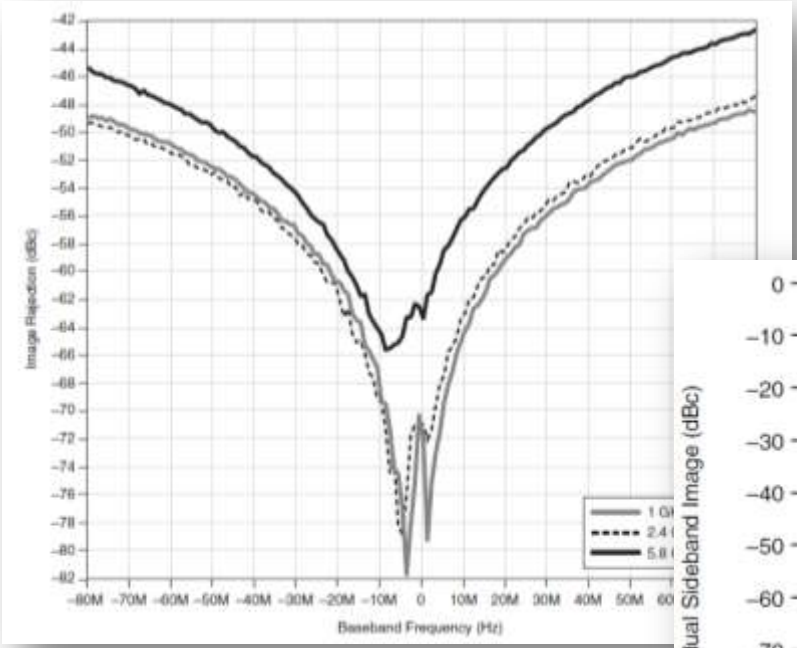


Wideband

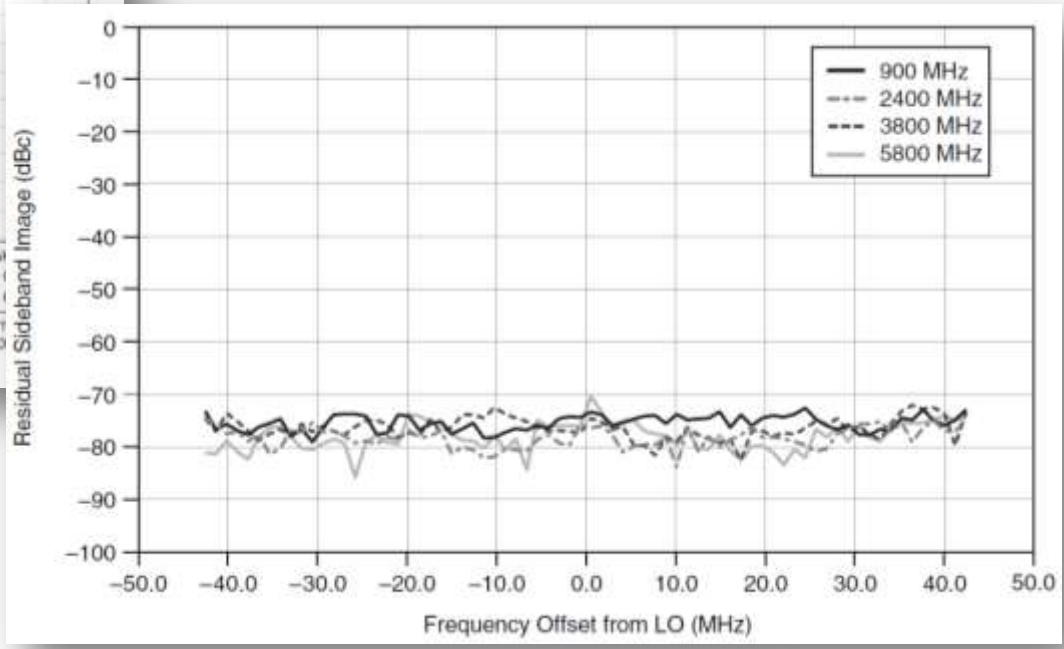


Specifications

NI PXIe-5673 VSG

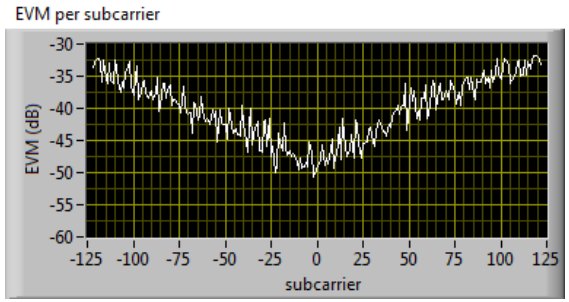


NI PXIe-5644R VST

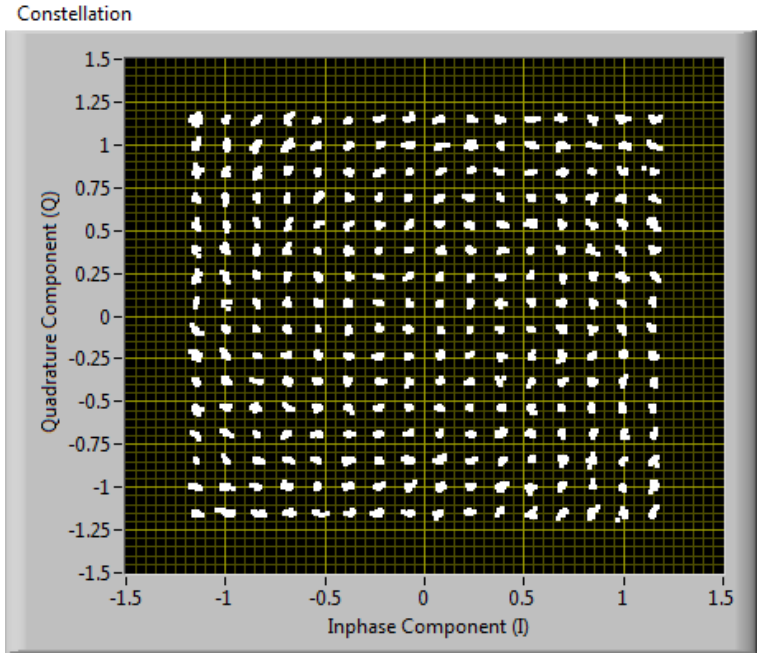


Effects on 802.11ac Signal (80MHz)

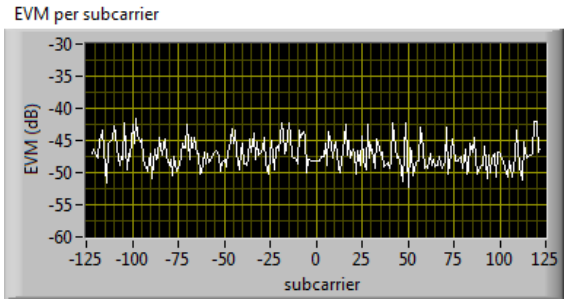
Traditional Correction



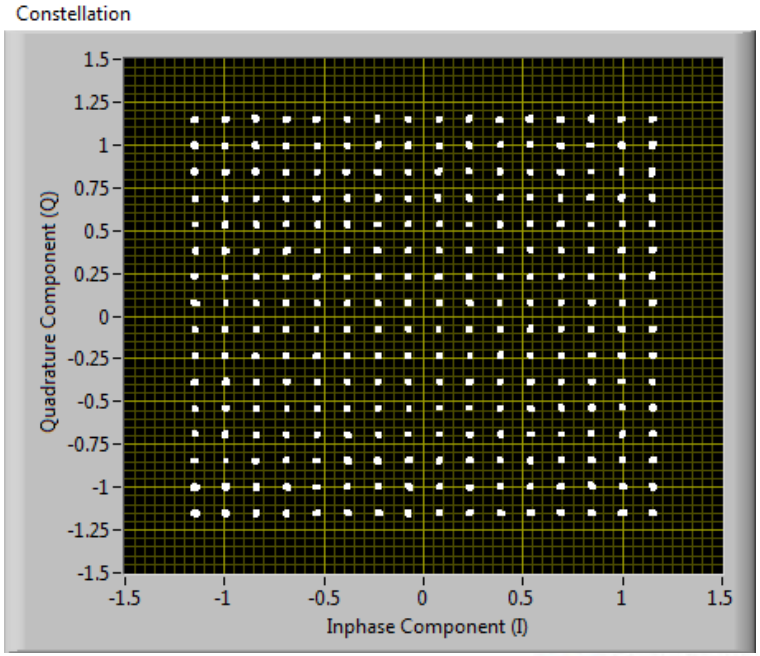
EVM
-37.6dB



Wideband Correction



EVM
-47.2dB



Software-Designed Instrument

NI PXIe-5644R Software

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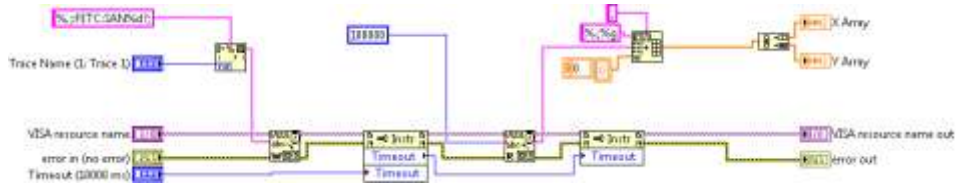
Open Source API

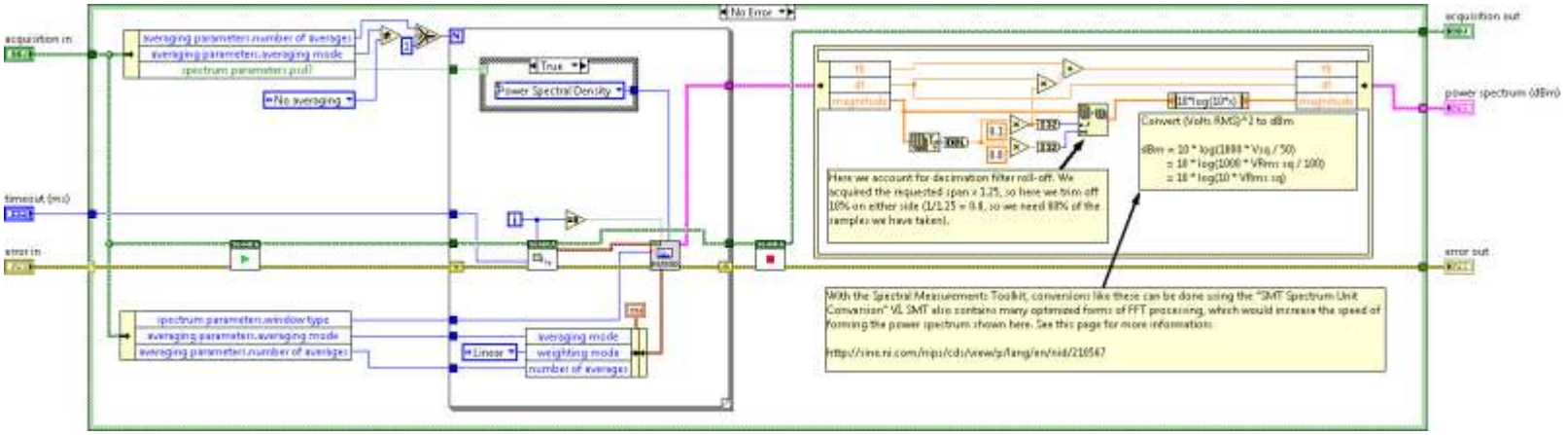
Read Trace.vi



Closed

Open

Read Spectrum.vi



Hardware Programmability through Software

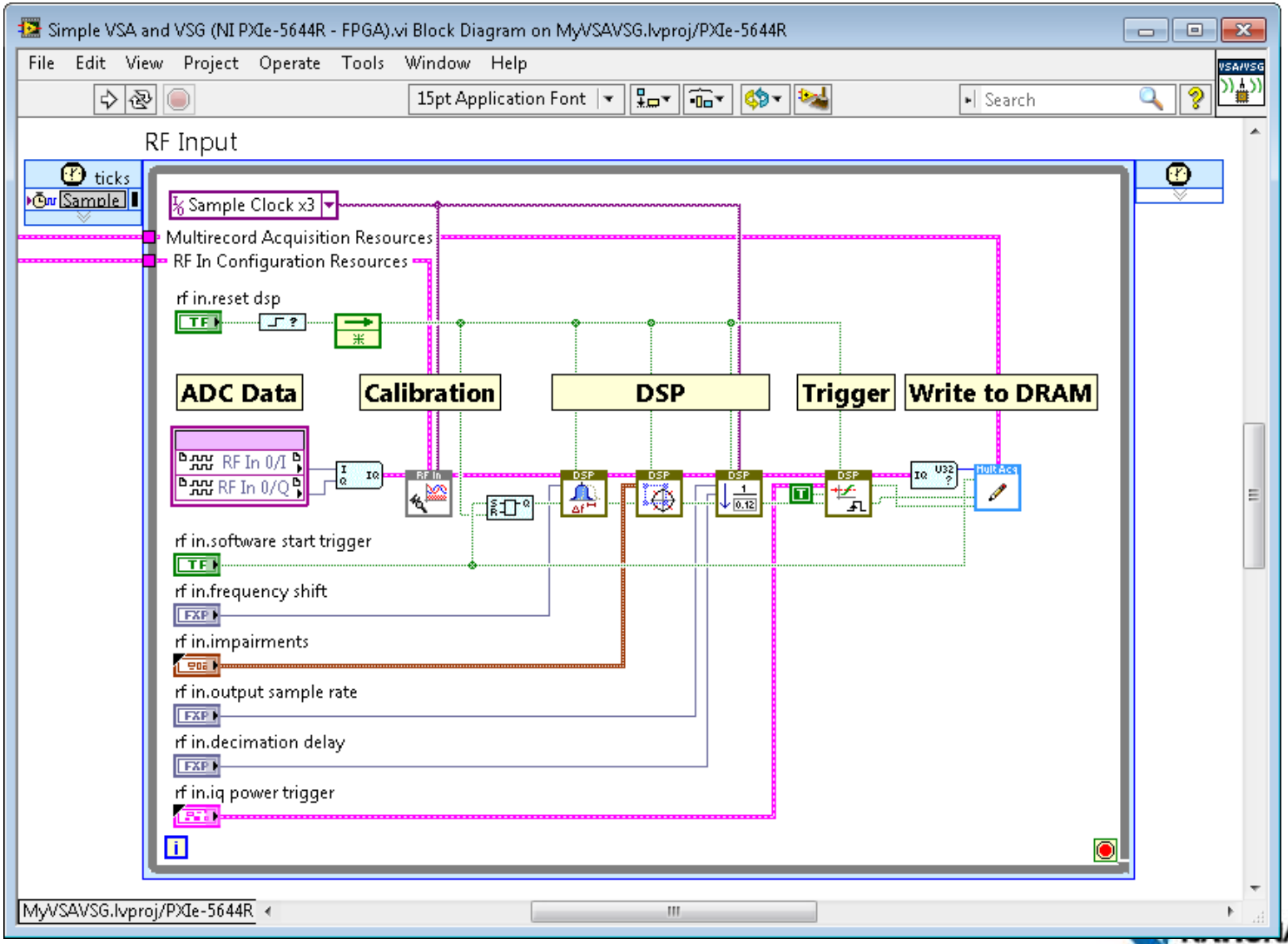
Configuration and Processes

RF Input

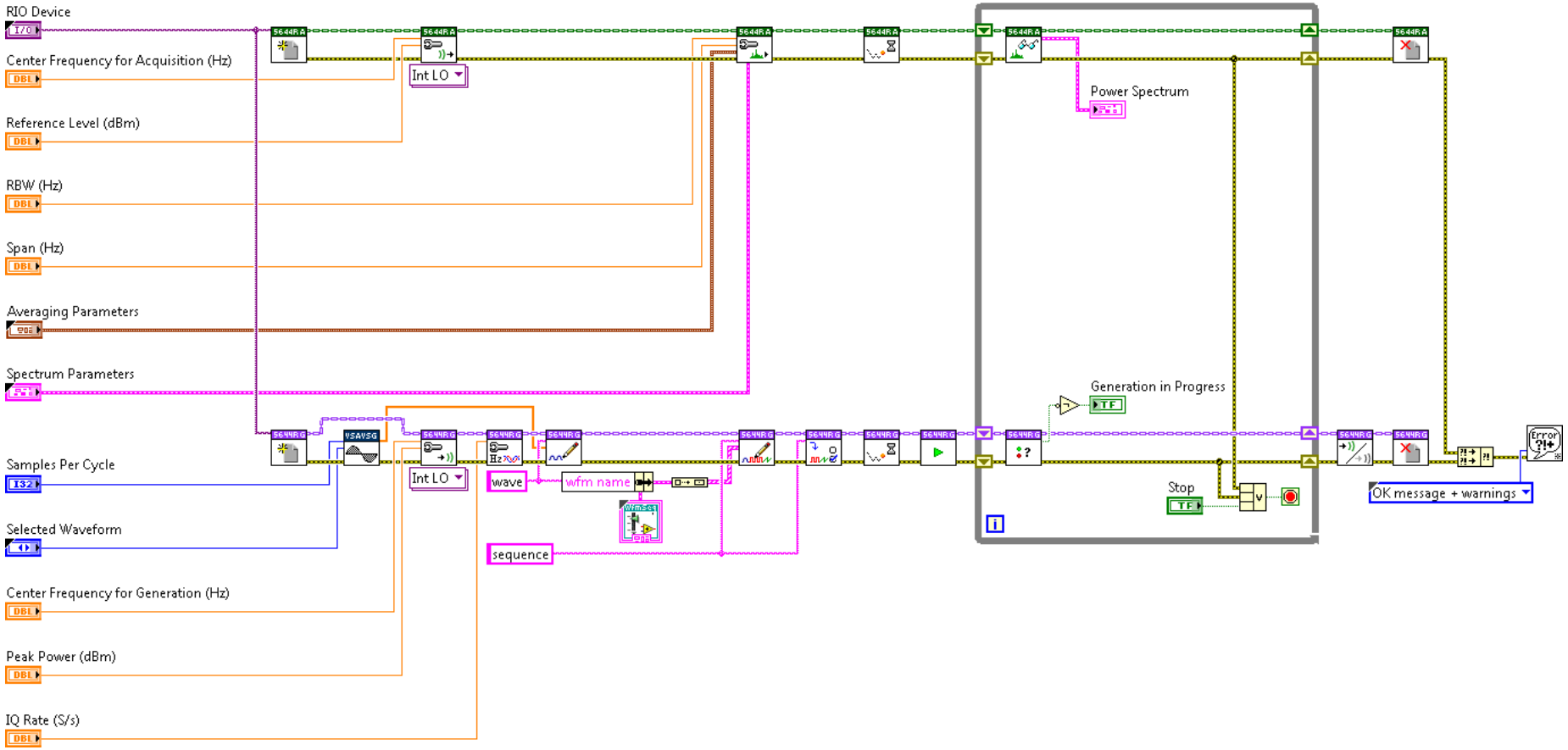
Equivalent to ~200,000 lines of VHDL.

RF Output

Component Disaggregation



Default Functionality



Multiple Processing Architectures

Algorithm Requirements	CPU	FPGA
Floating point math	X	
Integer and fixed point math	X	X
I/O		X
High parallelism		X
Complex conditional branching	X	
Low latency		X

Instrument Design Library

Host and FPGA Code From NI

DSP

- onboard signal processing

RF In

- RF input hardware configuration and calibration

RF Out

- RF output hardware configuration and calibration

Basecard

- ADC and DAC configuration

Multirecord Acquisition

- Multiple waveform acquisition DRAM abstraction

Waveform Sequencer

- Multiple waveform DRAM abstraction for waveform sequencing

Trigger Synchronization

- Multi-module sample clock synchronization, “T-Clk-like”

Embedded Configuration

- FPGA dynamic reconfiguration through register sequences, LabVIEW FPGA “list mode”

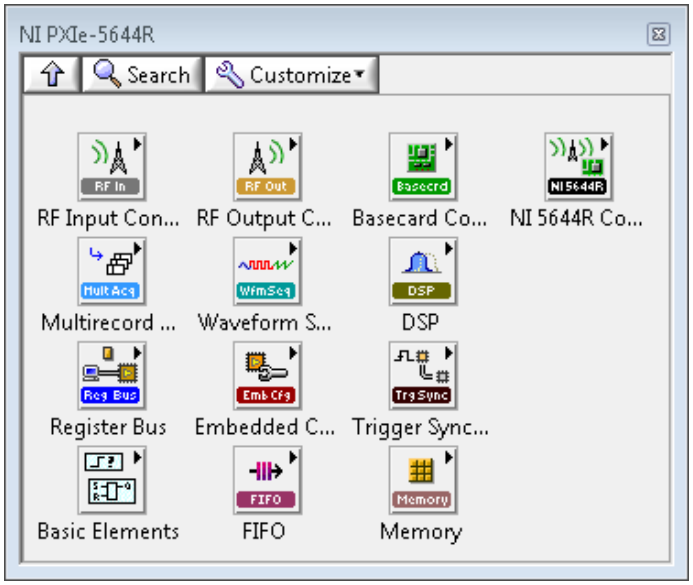
Instrument Design VIs

NI PXIe-5644R "APIs"

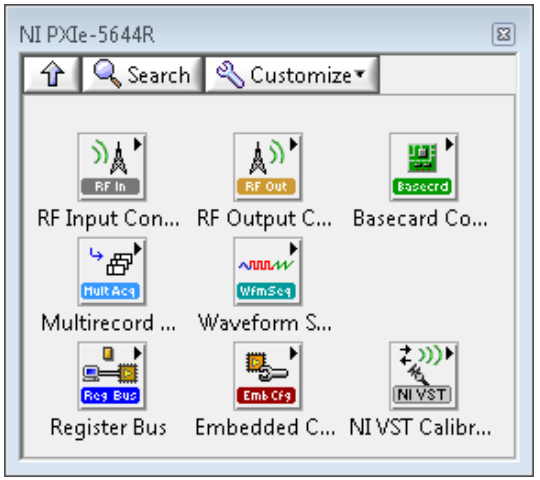
- Color-coded and thicker VI border
- Bundled into Host and FPGA *.lvlib
- Located in **c:\Program Files\National Instruments\LabVIEW 2012\instr.lib**
- Host and FPGA Palettes

Typical subVI

Instrument Design VI



FPGA



Host

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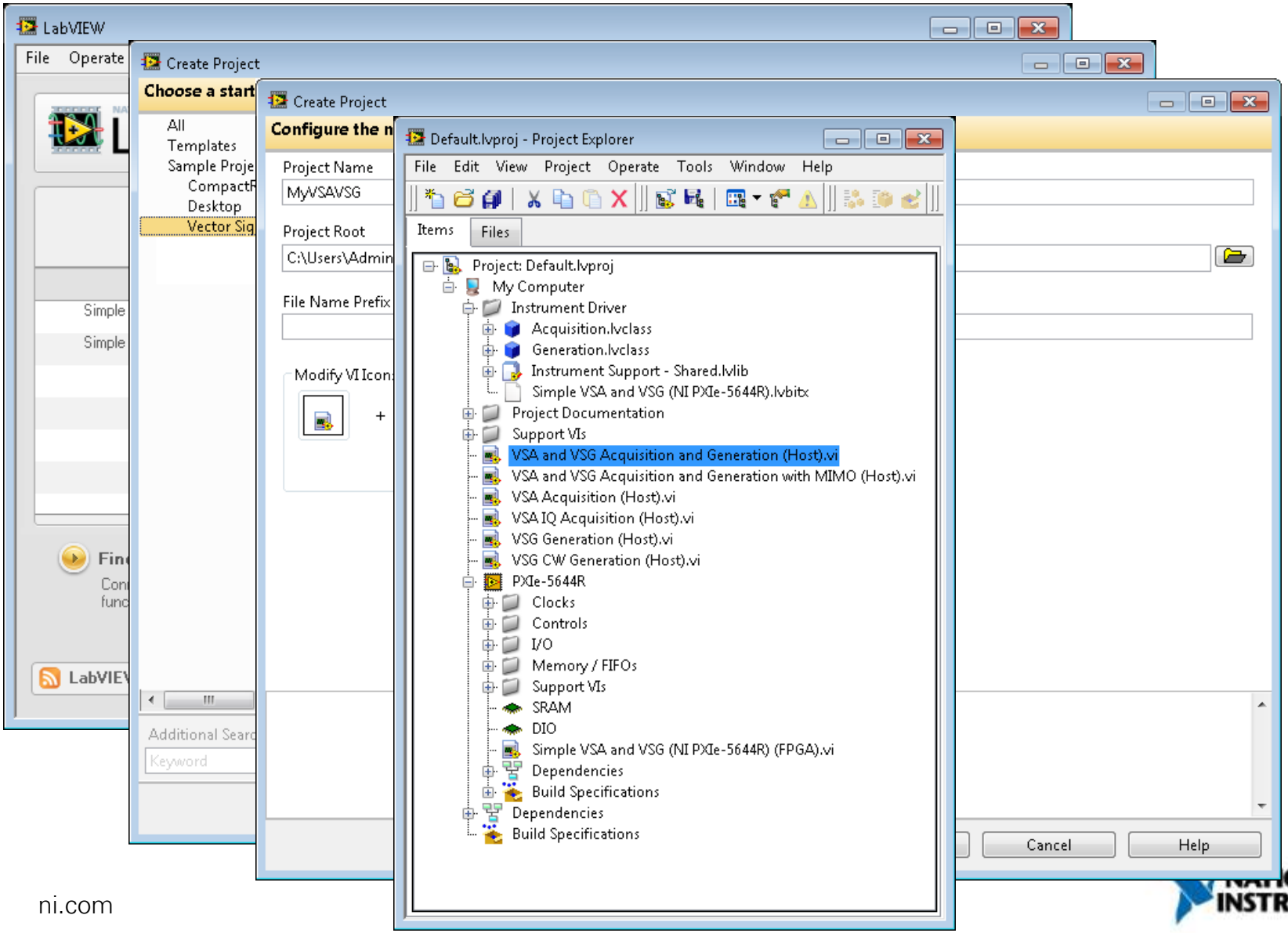
LabVIEW 2012 Sample Projects for the VST



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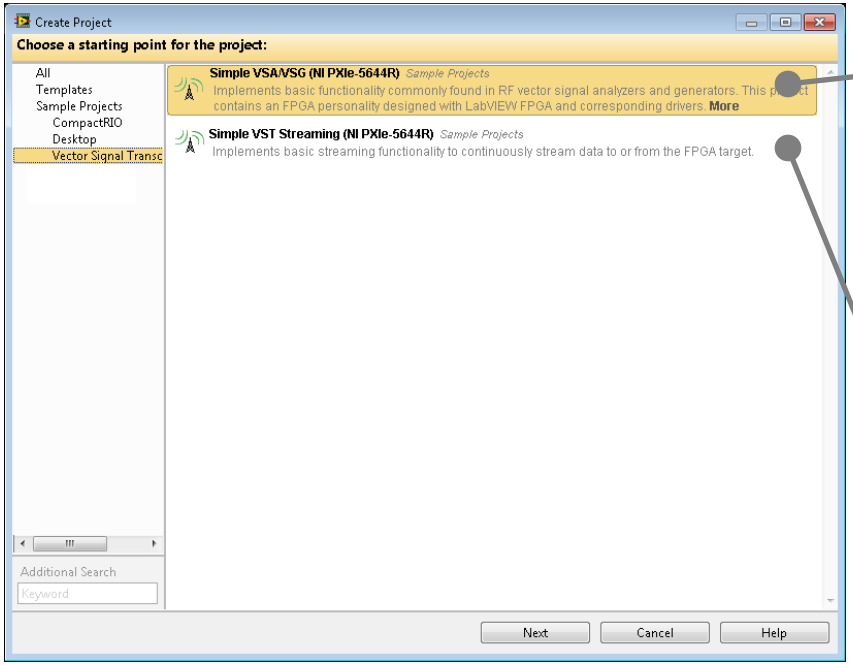
Multiple Design Patterns



Instrumentation

Implements triggering and multi-record acquisition and generation.

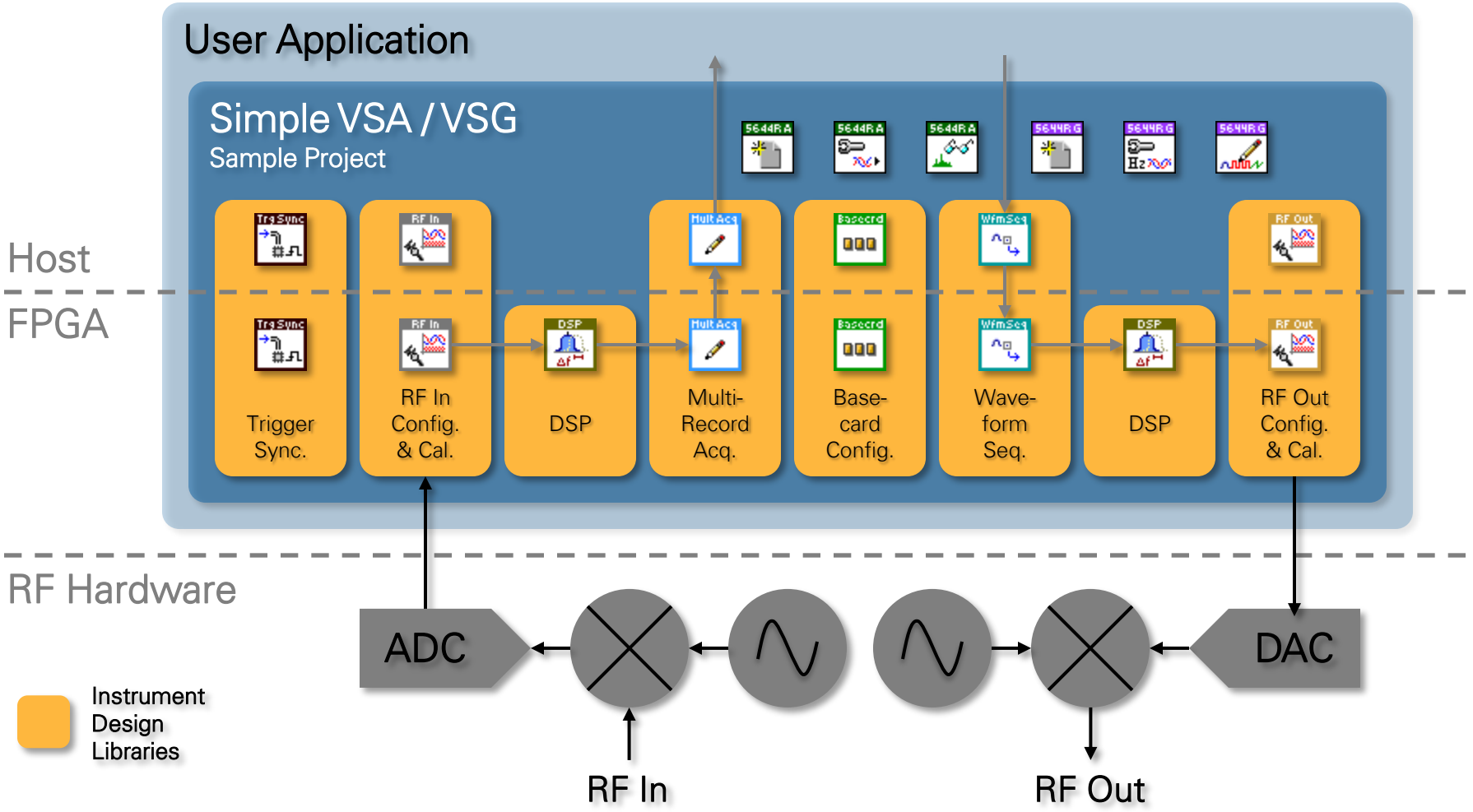
Provides a familiar look and feel to traditional instrument drivers on the host.

Streaming

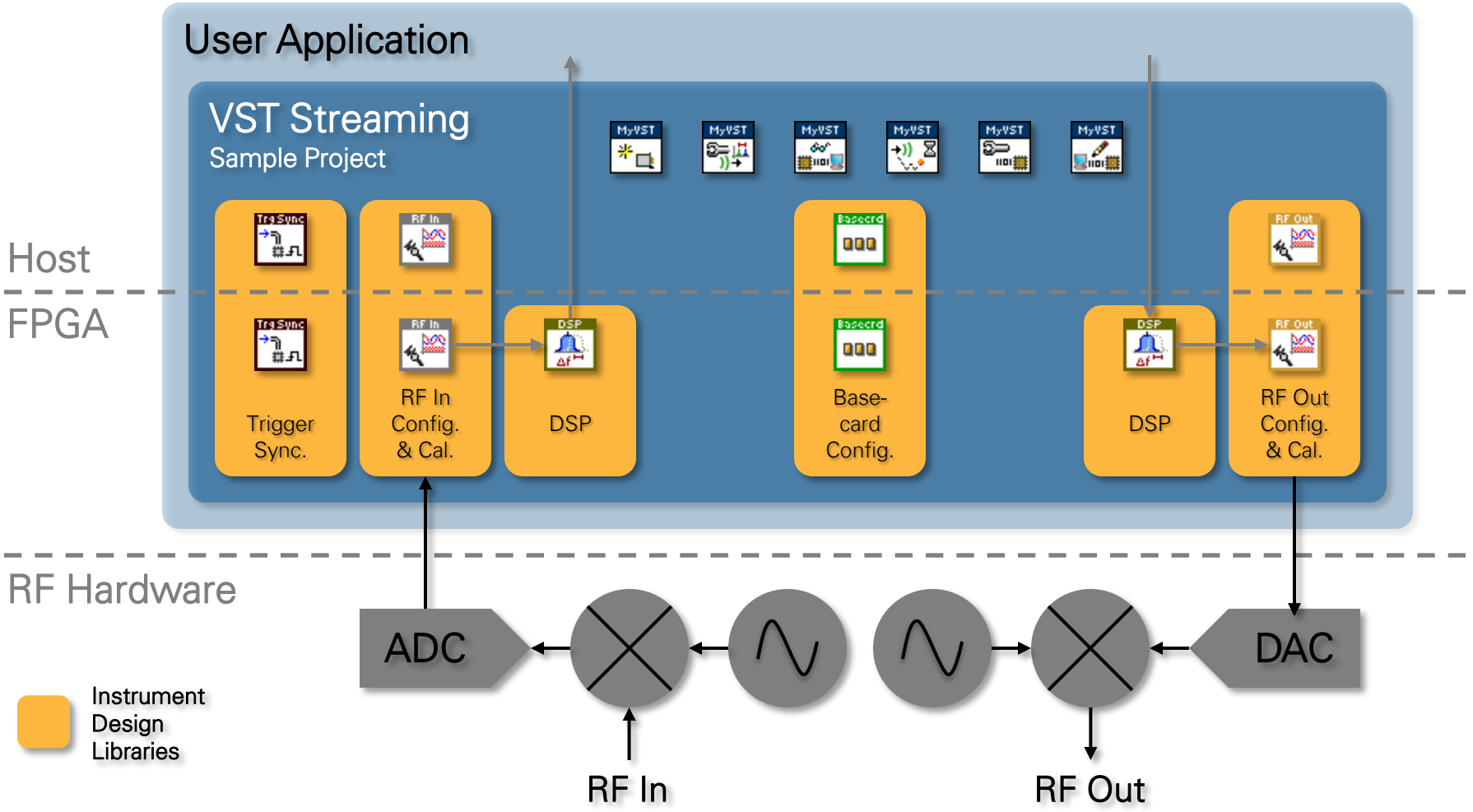
Implements basic real-time streams to and from the host

Serves as a starting point for implementing real-time DSP and re-routing data streams between loops, FPGAs, and host processing

Simple VSA / VSG Sample Project



VST Streaming Sample Project



Code Demonstration

Simple VSA / VSG Sample Project

VST Streaming Sample Project

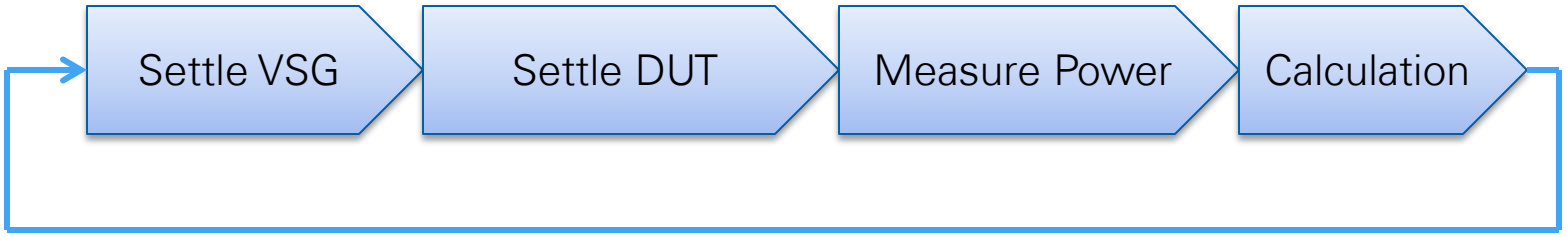
Example Modification

Power Level Servoing

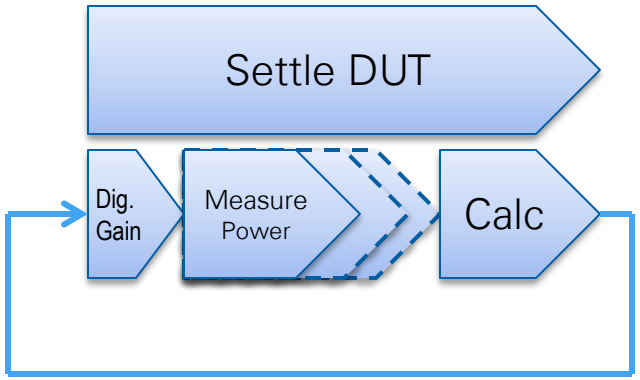
Streaming Loop-back

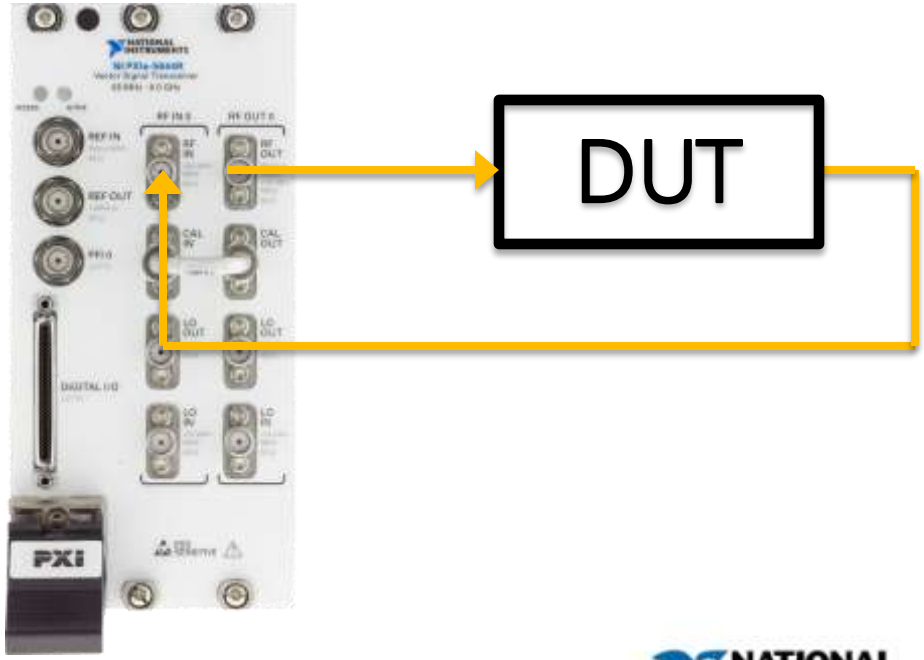
Power Level Servoing

The Traditional Approach

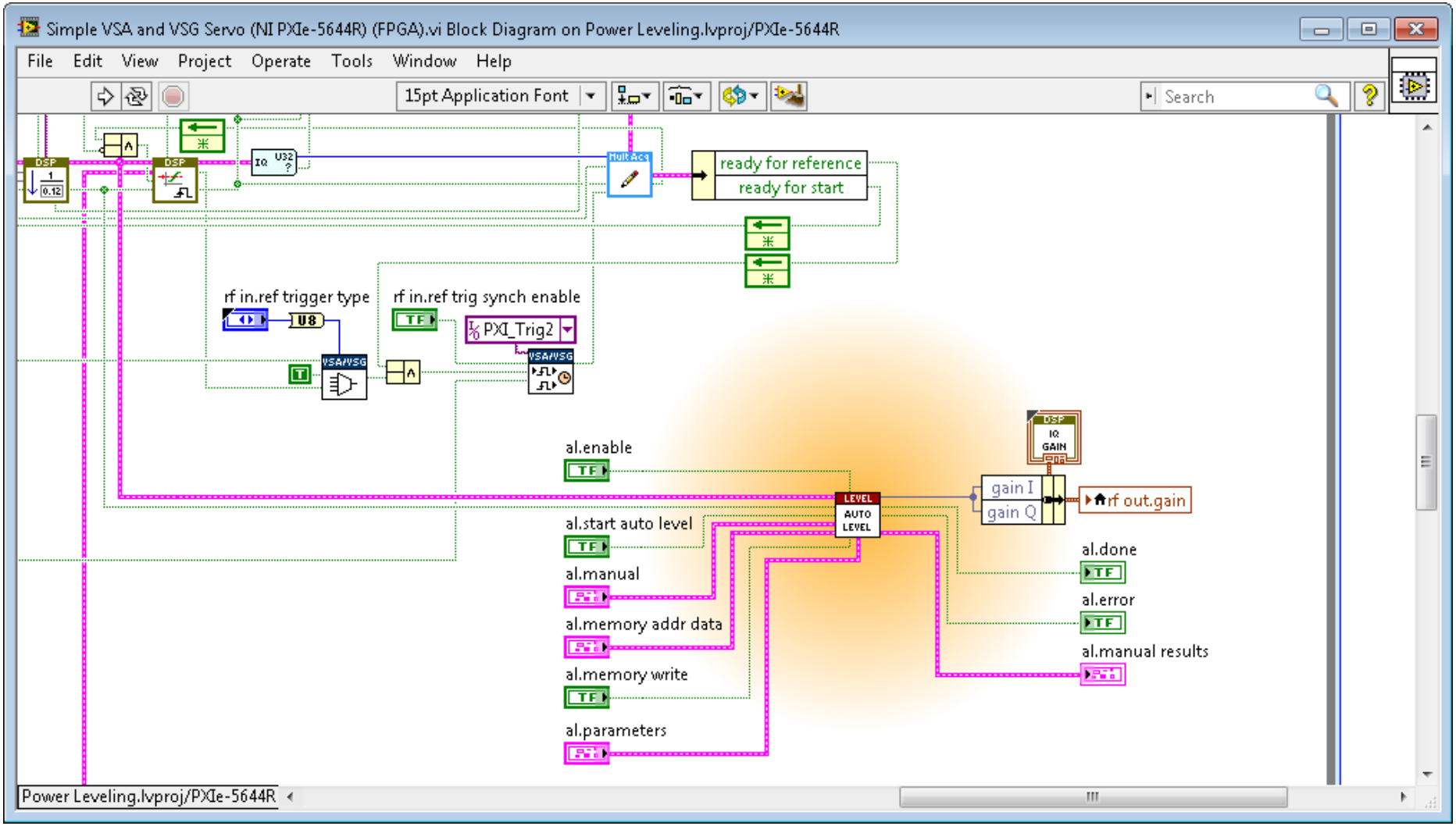


With FPGA





Power Level Servoing



Available IP and Examples

IP and Examples

ni.com/vstgettingstarted

Simple VSA / VSG

Hardware Power Leveling for PA Test

This example uses a control loop on the FPGA to quickly adjust the VST output power to reach a desired input power, when an RF power amplifier of an unknown gain is connected to each.

Download the example >>

FPGA-Based Spectral Mask

A real-time spectral mask trigger provides the frequency selectivity of a spectrum analyzer mask trigger, with the guaranteed detection of a VSA I/Q power edge trigger.

Download the example >>

Time-Gated Acquisition for ACP Measurements

Making ACP measurements of packet-based standards with a channel bandwidth approaching the real-time bandwidth of the instrument is challenging because it is not obvious when to trigger on the adjacent channels. This example auto-synchronizes adjacent channel triggers based on the packet frequency and phase.

Download the example >>

Digital DUT Control

Integrating digital DUT control and RF measurements reduces test equipment requirements and can accelerate test system throughput. This example implements basic I2C and SPI DUT control on the VST DIO port.

Download the example >>

802.11ac Measurements

NI cellular and wireless toolkits provide examples for use with NI RFSA and NI RFSG, though they also support hardware-agnostic measurements. This example shows how to integrate the Simple VSA / VSG sample project with the NI WLAN Measurement Suite for 802.11ac measurements.

Download the example >>

VST Streaming

Real-Time Channel Emulation

With a DSP-focused FPGA coupled to both RF input and RF output, the NI PXIe-5644R makes an ideal hardware platform for an RF channel emulator. This example implements inline, real-time DSP to apply arbitrary channel models to the RF data.

Download the example >>

Streaming to and from Disk

To record and play back the full RF bandwidth of the NI PXIe-5644R, this example uses NI high-speed data storage products and continuous data streaming to log up to 80 MHz of bandwidth to disk for hours, then play it back.

Download the example >>

Streaming GPS Waveform Generation

While GPS waveforms are low bandwidth and may be synthesized on the host CPU, they must be streamed in real time to hardware for generation. This example couples the NI GPS Simulation Toolkit with the NI PXIe-5644R for extended GPS signal generation.

Download the example >>

I/Q Data Streaming

The DIO port on the NI PXIe-5644R may be used to stream high-rate data to other hardware. This example streams RF input I/Q samples out the DIO port, or accepts I/Q samples through the DIO port and generates them on the RF output.

Download the example >>

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