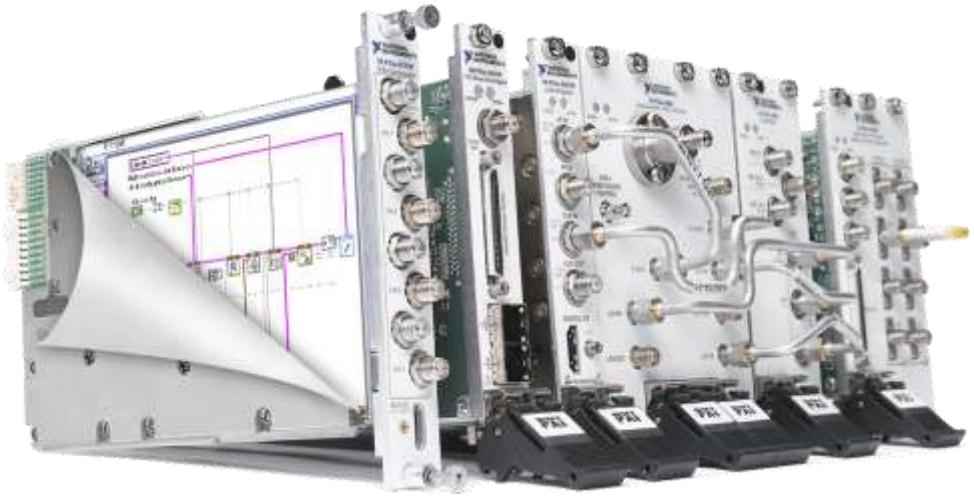


Create Without Limits: Add the Power of User-Programmable FPGAs to Your Test Applications

NATIONAL INSTRUMENTS

Agenda

- What Is a Software-Designed Instrument?
- Why Software-Designed Instrumentation?
- New Software-Designed Instruments
- Software-Designed Instrument… Software
- Next Steps

What Is a Software-Designed Instrument?

What Is a Software-Designed Instrument?

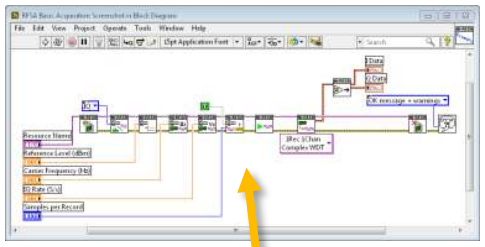
Typical Modular Instrument

Software-Designed Instrument

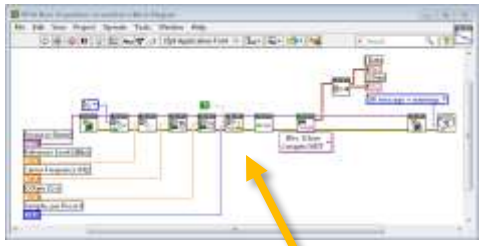
Software

Hardware

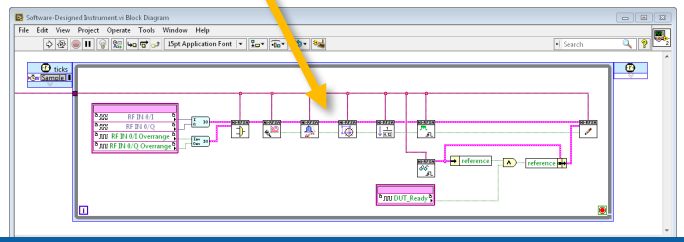
Processor

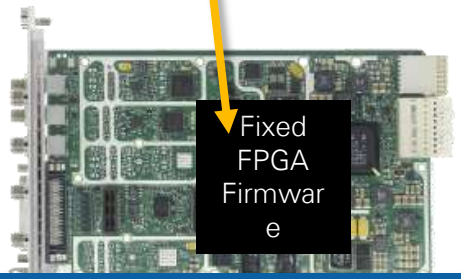


Processor



FPGA





Fixed FPGA Firmware

Out-of-the-box functionality with FPGA enhancements

Identical hardware architecture and measurement quality

NATIONAL INSTRUMENTS

Out-of-the-Box Functionality +
FPGA Enhancements

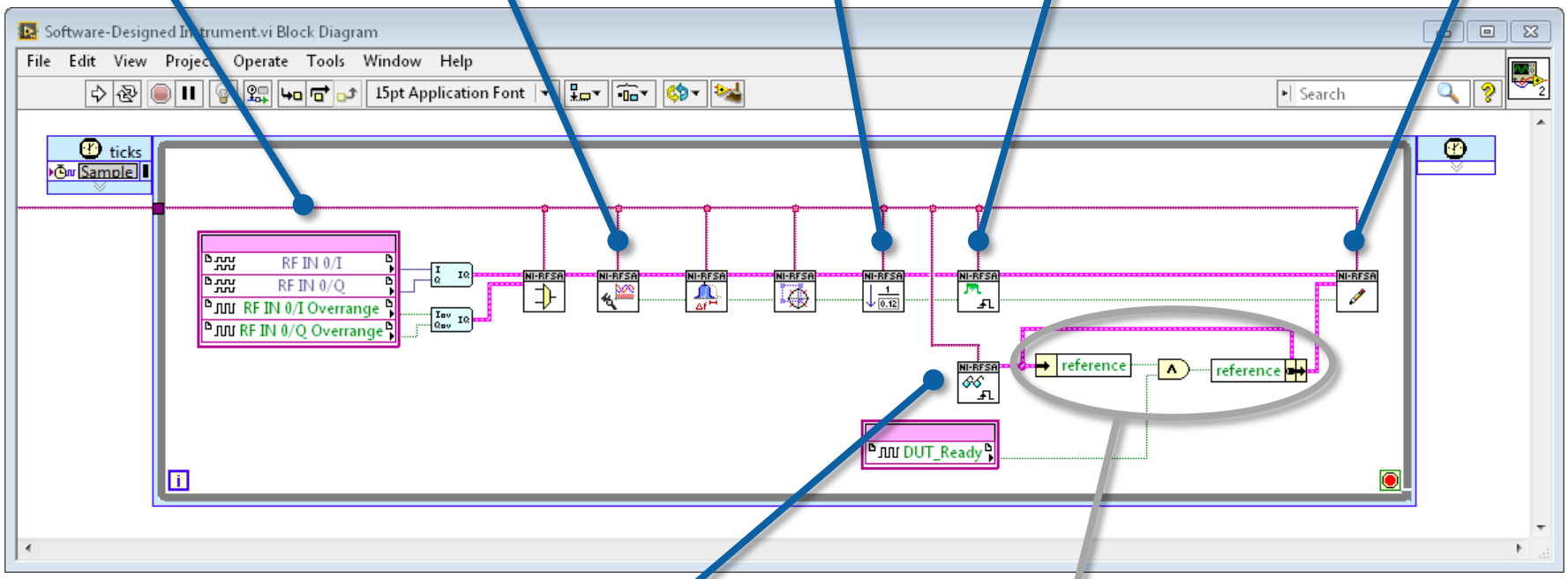
I/O

Calibration

DSP

Triggering

Acquisition



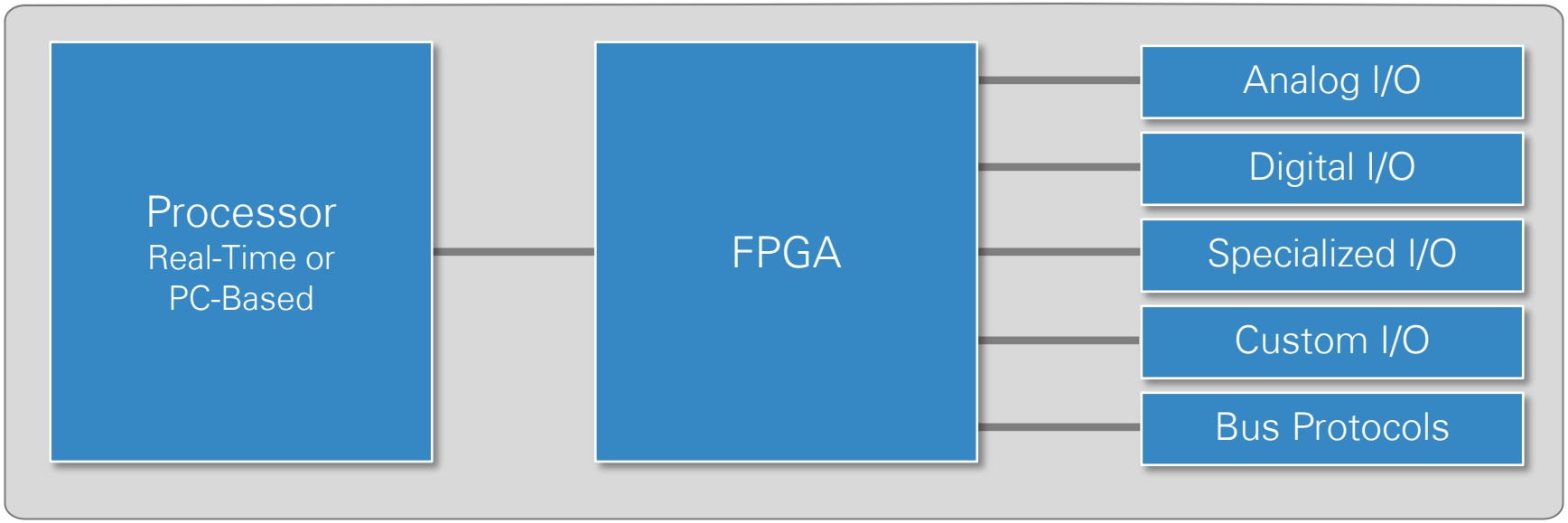
Synchronization

Application-Specific Enhancement

NATIONAL INSTRUMENTS

The NI Approach

We call this the LabVIEW Reconfigurable I/O (RIO) architecture.



Highly Productive **LabVIEW** Graphical Programming Environment for Programming Host, FPGA, I/O, and Bus Interfaces

FPGA Technology

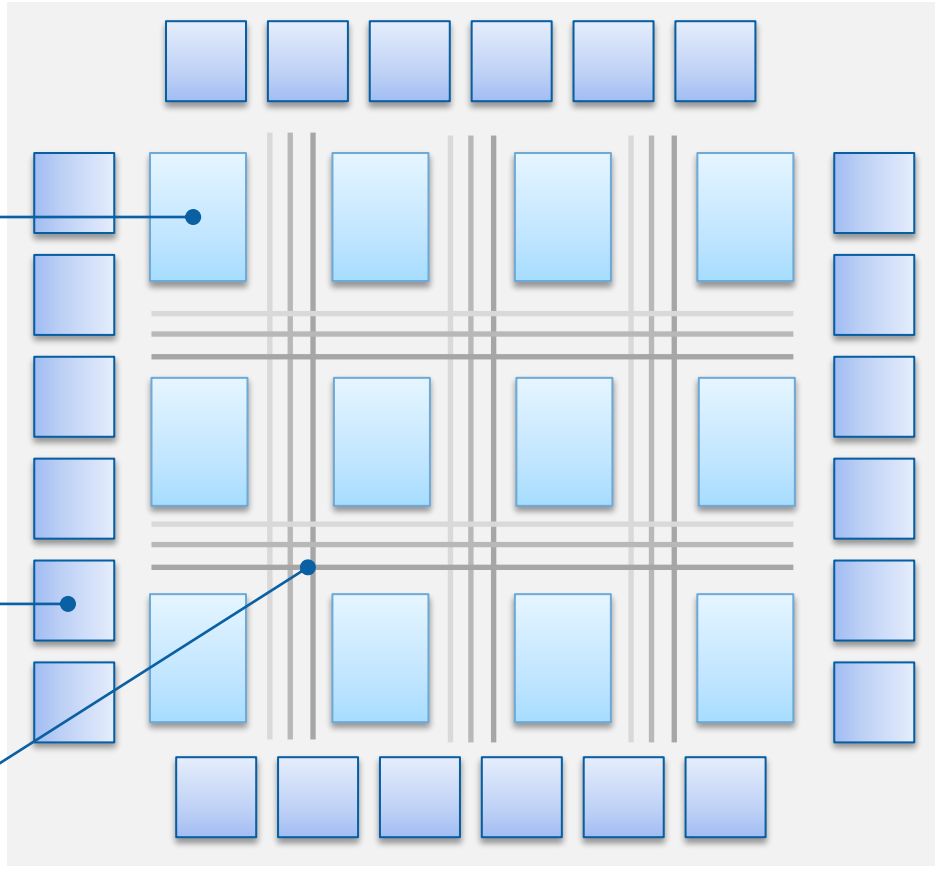
Memory Blocks
Store data sets or values in user defined RAM

Configurable Logic Blocks (CLBs)
Implement logic using flip-flops and LUTs

Multipliers and DSPs
Implement signal processing using multiplier and multiplier-accumulate circuitry

I/O Blocks
Directly access digital and analog I/O

Programmable Interconnects
Route signals through the FPGA matrix

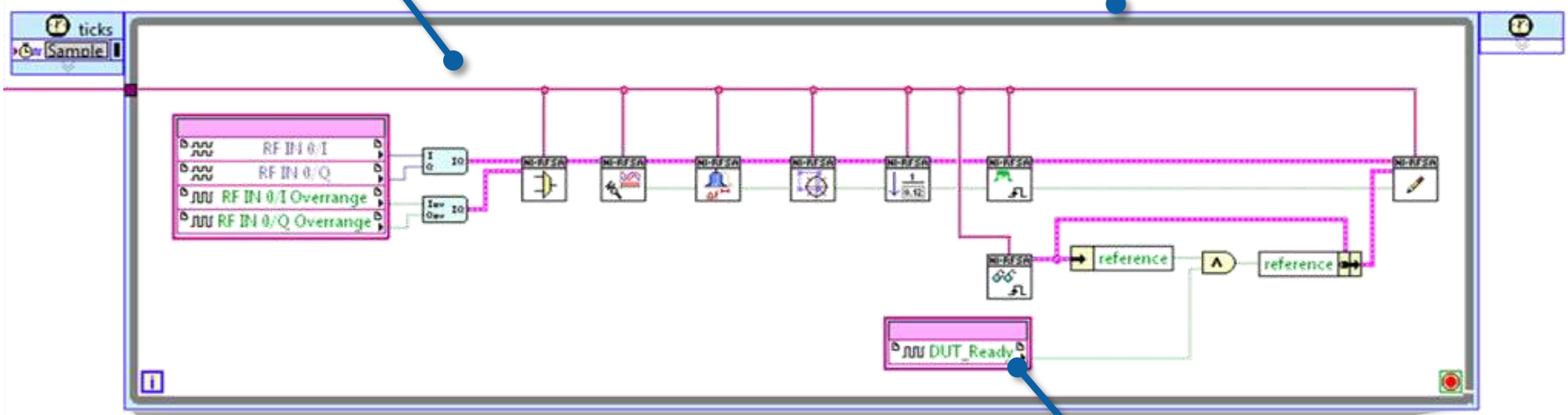


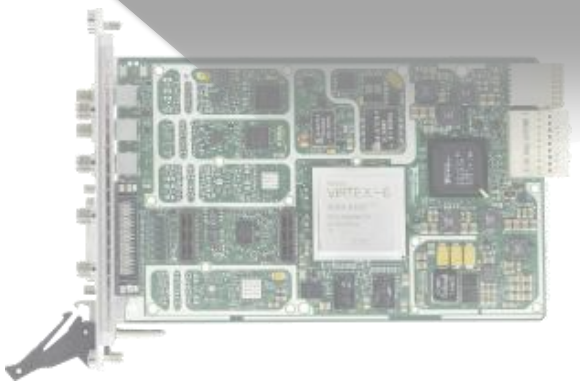
Program with LabVIEW FPGA

- Familiar LabVIEW programming elements
- Develop, simulate, debug, compile and deploy through LabVIEW
- Integrate external FPGA IP

High-Performance Features

- High-throughput math functions
- Advanced timing control with Single Cycle Timed-Loops
- Access to optimized DSP Cores





Access to IO and Peripherals

- Simple API for front-panel IO
- High bandwidth streaming over PCI Express to Host or other PXI devices
- Random access read/write to DRAM

Why Software-Designed Instrumentation?

– and –

New Software-Designed Instruments

Why FPGAs for Instruments?

High-Throughput Processing

- Inherently parallel
- High clock rate
- Algorithm-specific pipelining

Low-Latency Decision Making

- Custom logic in a single clock cycle

Complete Determinism

- Design implemented in a custom circuit

Reprogrammable Logic

- Design can be updated while system is running

User-Programmable FPGAs on Software-Designed Instruments Enable:

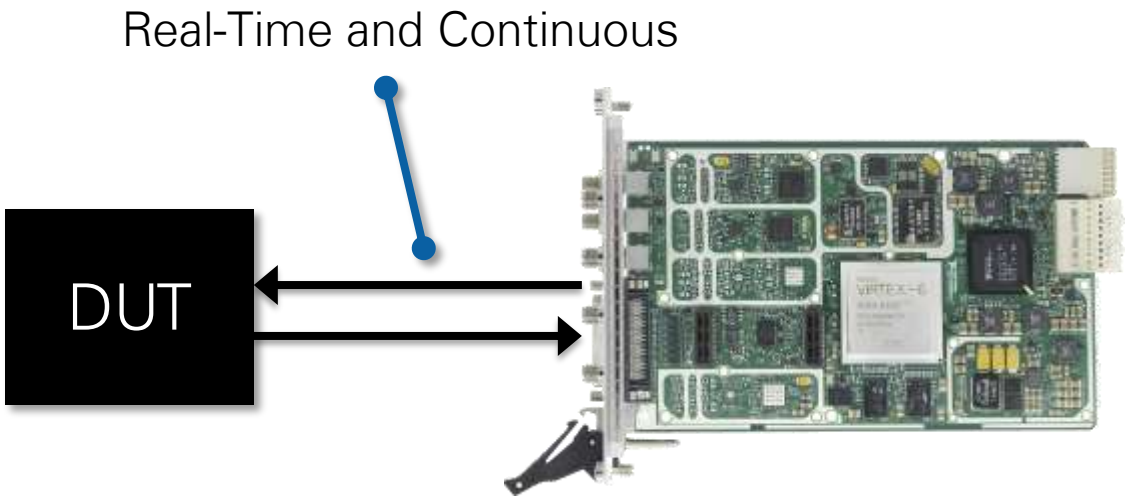
1. On-FPGA Measurements and Stimulus Generation
2. Closed-Loop or Protocol-Aware Test
3. Custom Triggering and Data Reduction
4. Deterministic Test Execution and DUT Control
5. DUT or Application-Specific Personalities

Higher Test Throughput

Hardware Re-Use and Future-Proofing

New, Innovative Tests

Lower Total Cost of Test



1. On-FPGA Measurements and Stimulus Generation

Higher Test Throughput

Hardware Re-Use and Future-Proofing

New, Innovative Tests

Lower Total Cost of Test

26.5 GHz Vector Signal Analyzer

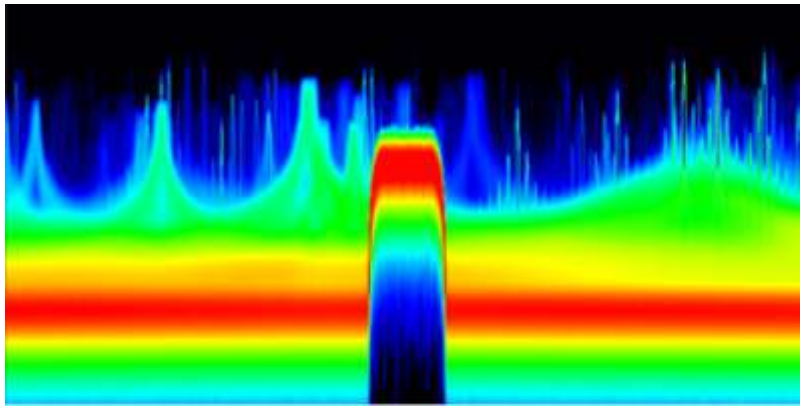
PXIe-5668 Specifications	
Frequency Range	20 Hz to **26.5 GHz**
Analysis BW	**320 MHz below 3.6 GHz** **765 MHz above 3.6 GHz**
Phase Noise (Typ, @10kHz offset)	-129 dBc/Hz at 1 GHz
Noise Floor	<-145 dBm/Hz (26 GHz)
TOI	>+20 dBm (26 GHz)
New Features	**Kintex-7 410T FPGA** **Programmable with LabVIEW**
Slots	7

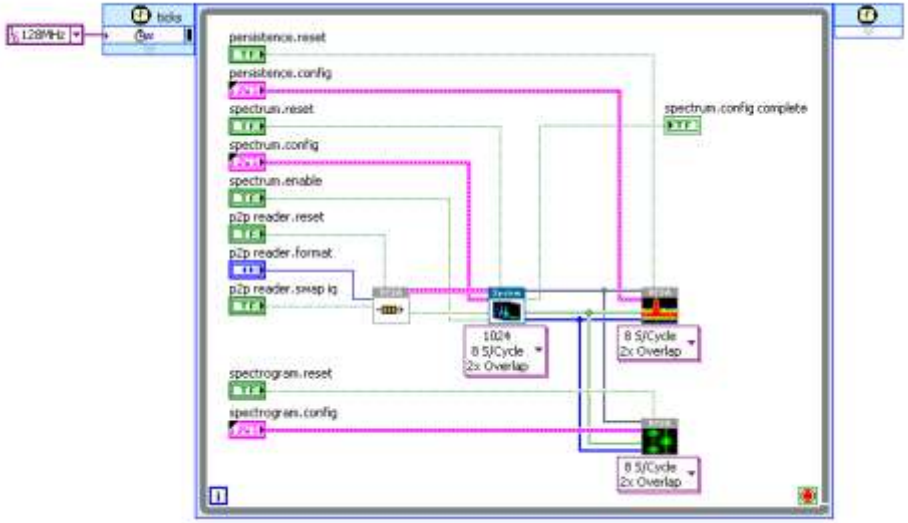
2 GHz Reconfigurable IF-Digitizer

PXIe-5624R Specifications	
Sample Rate	2 GS/s
ADC Resolution	12-bit
Analog Bandwidth	2 GHz
New Features	Kintex-7 410T FPGA Programmable with LabVIEW PCI Express x8 Gen 2 bus interface (> 3 GB/s)
Slots	1

Real-Time Spectrum Analysis
Features

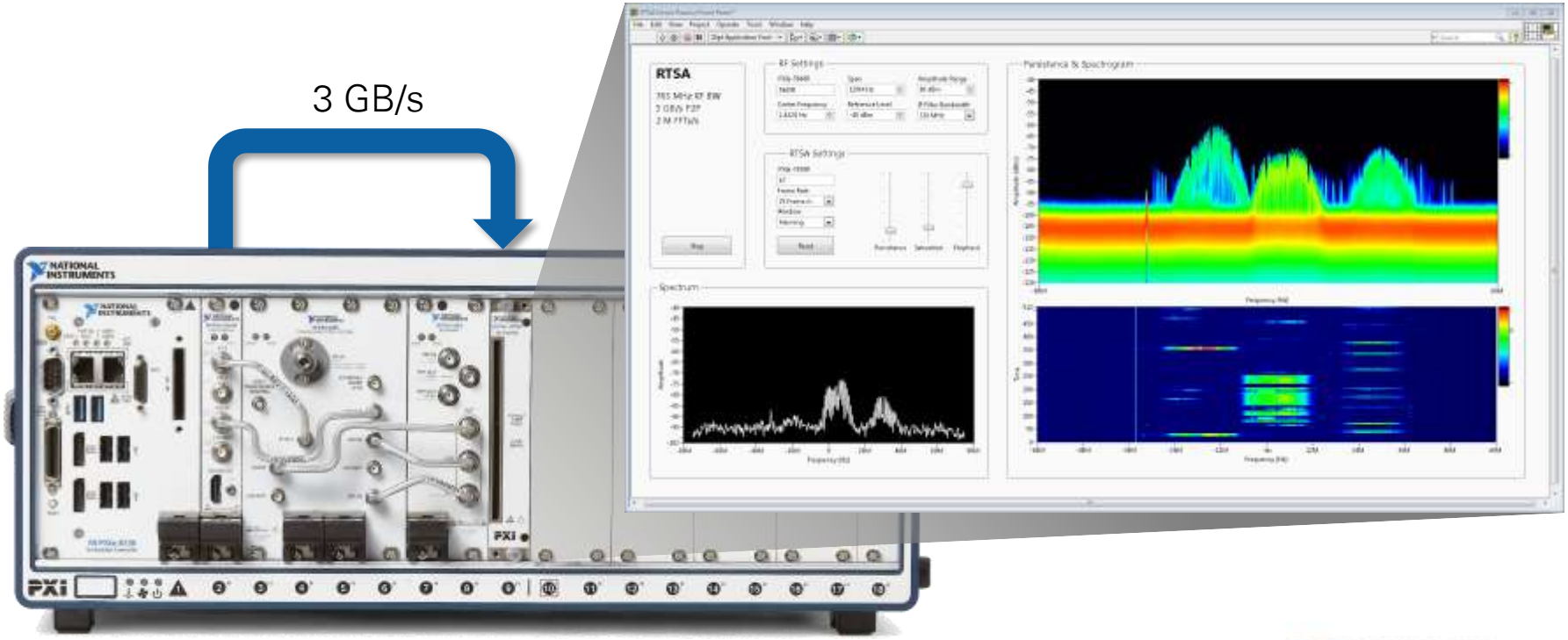
- Gapless persistence, spectrogram, and trace statistics (max hold, min hold, average) calculated on FPGA
- Ability to process up to 2 M FFTs/s using overlapped, windowed FFTs
- Real-time frequency mask triggering
- 100% probability of intercept (POI) minimum duration options:
  - 1 µs or >15 µs
- Source available upon request

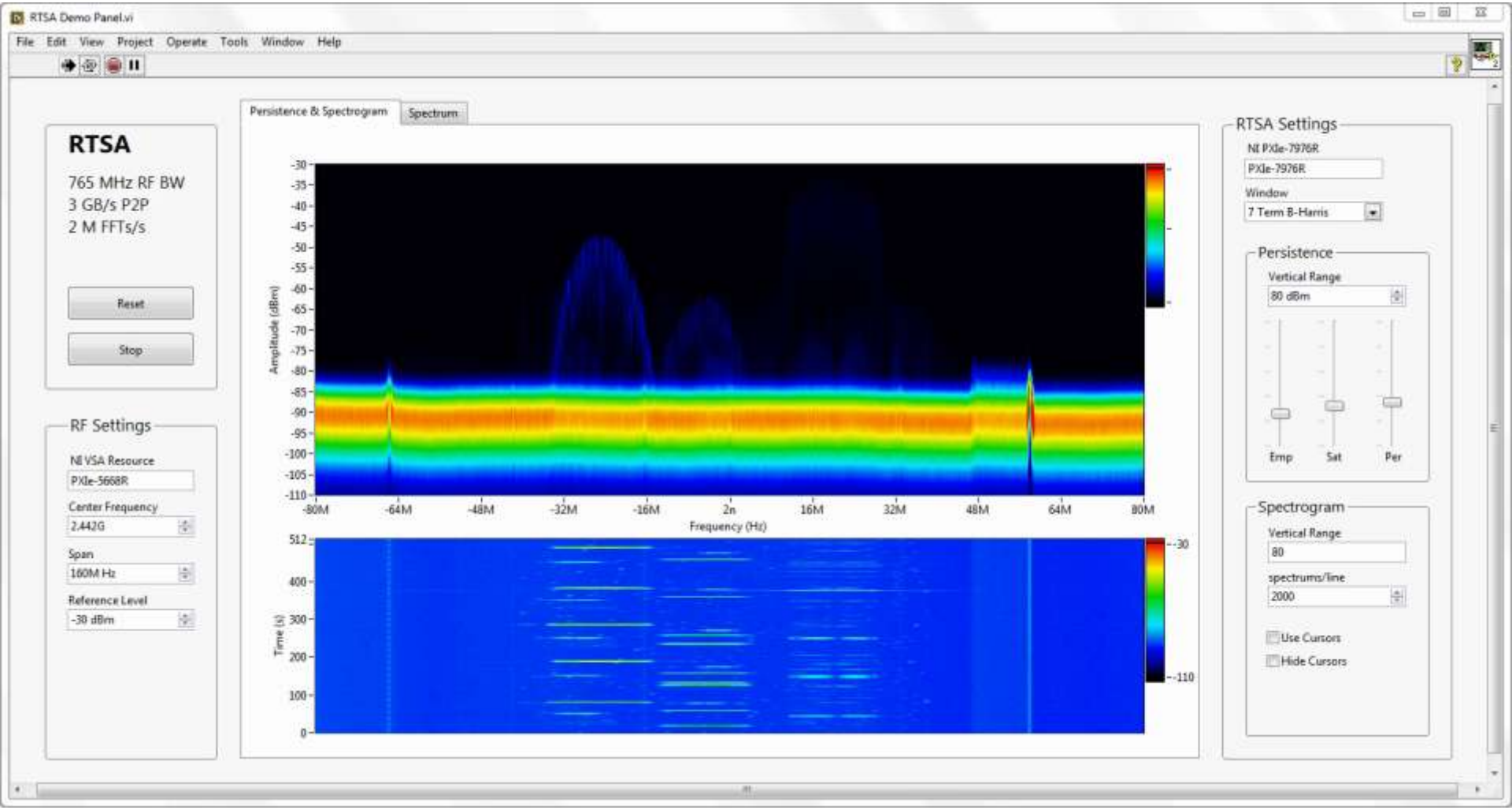




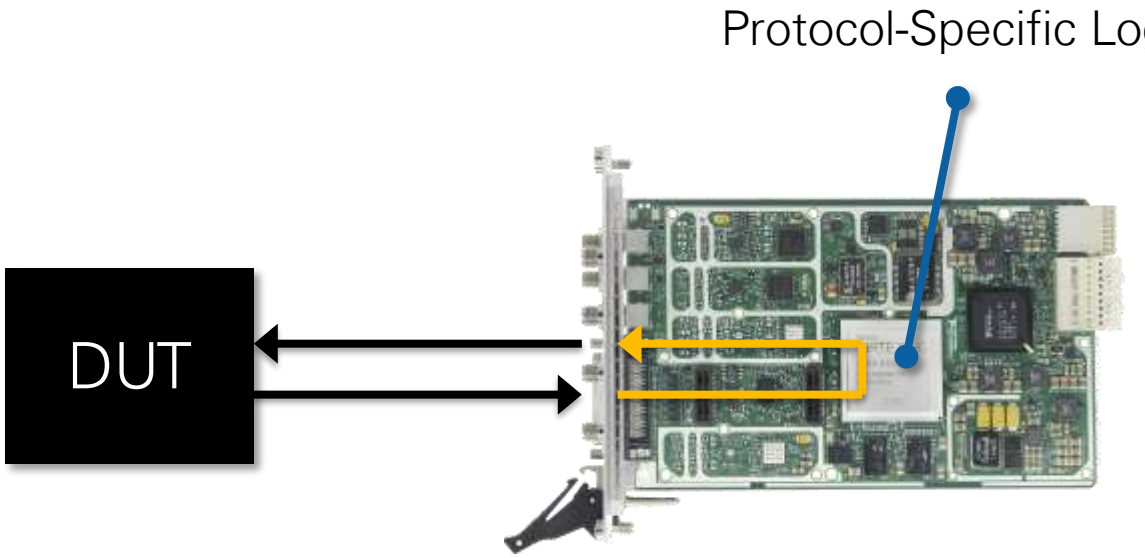
Demo: Real-Time Spectrum Analysis

- PXIe-5668R VSA + PXIe-7976R FlexRIO in PXIe-1085
  - May use other P2P-capable RF analyzers
- Up to 800 MHz RF bandwidth (3 GB/s)





NATIONAL INSTRUMENTS



2. Closed-Loop or Protocol-Aware Test

Higher Test Throughput

Hardware Re-Use and Future-Proofing

New, Innovative Tests

Lower Total Cost of Test

High-Speed Serial Instruments

PXIe-6591R & PXIe-6592R Specifications	
High-speed serial interface	Up to 12.5 Gbps Up to 8 TX and RX lanes
Connector	SFP+ or Mini-SAS HD
RAM	2 GB / 10.6 GB/s bandwidth
FPGA	Kintex-7 410T FPGA Programmable w/ LabVIEW PXI Express x8 Gen 2 bus interface (> 3 GB/s)

Available end of 2014

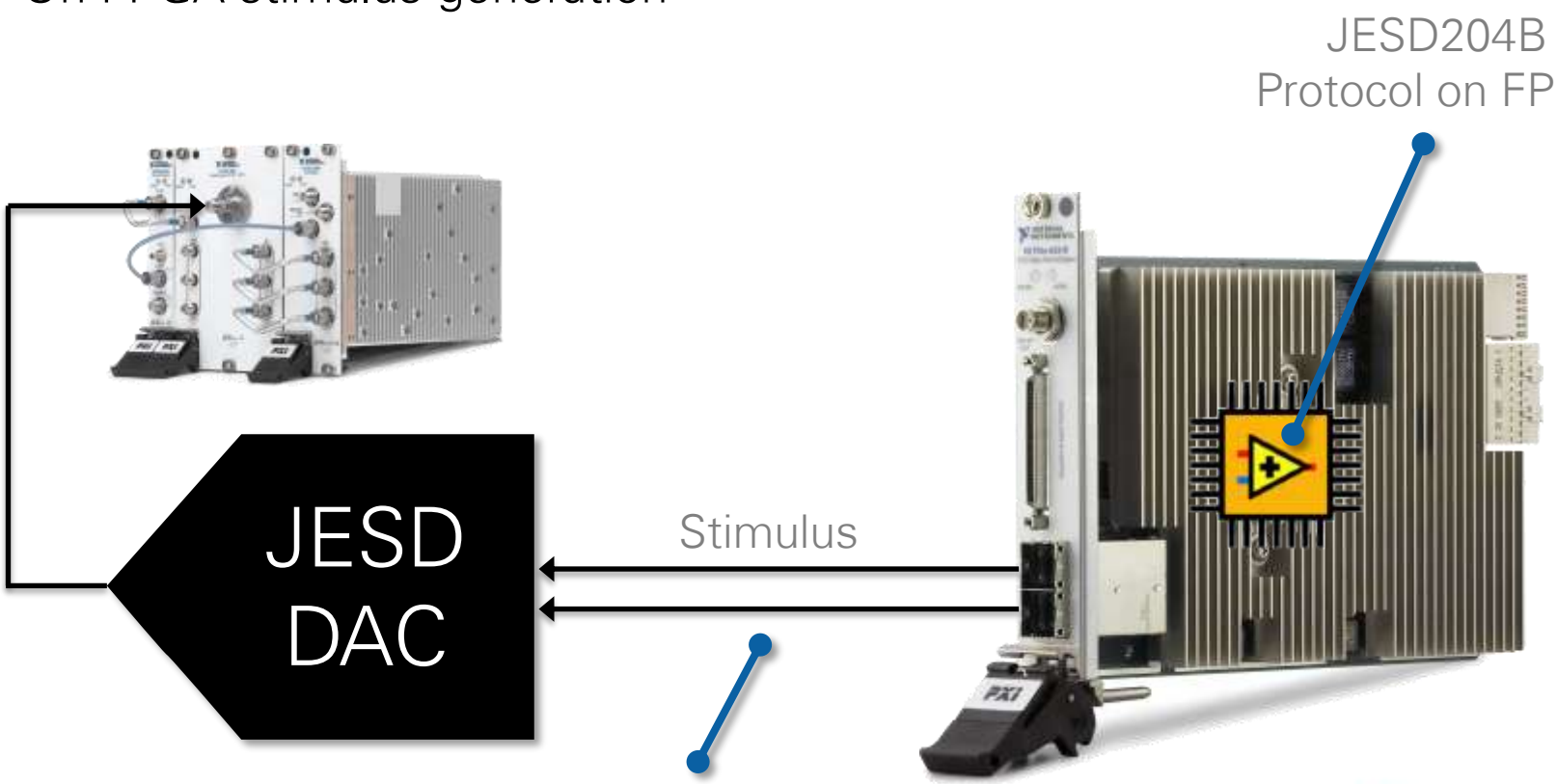
Examples for:

- JESD204B
- Xilinx Aurora
- Serial RapidIO
- 10 Gigabit Ethernet
- CPRI

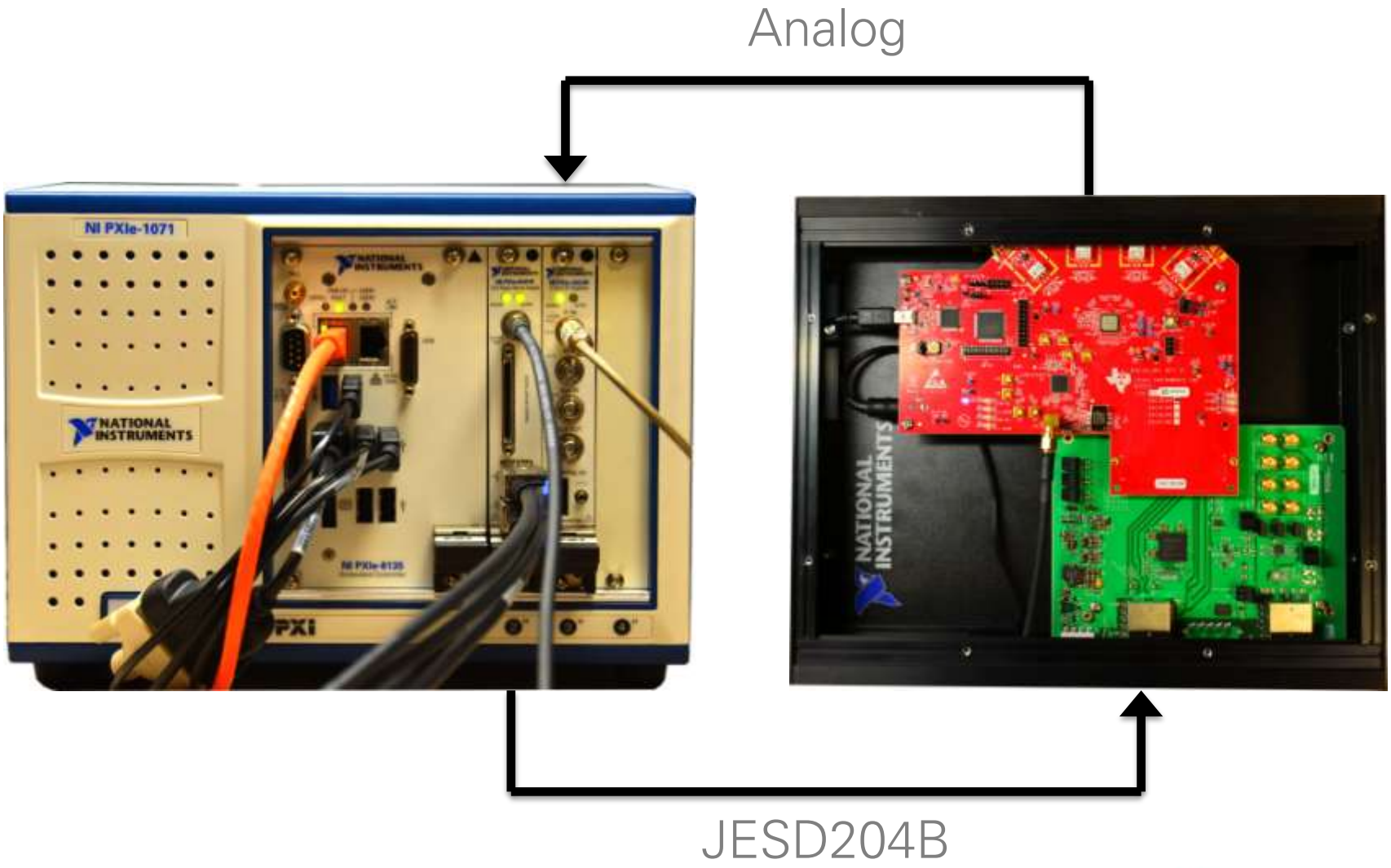
"FlexRIO-like" VHDL control of Xilinx MGTs

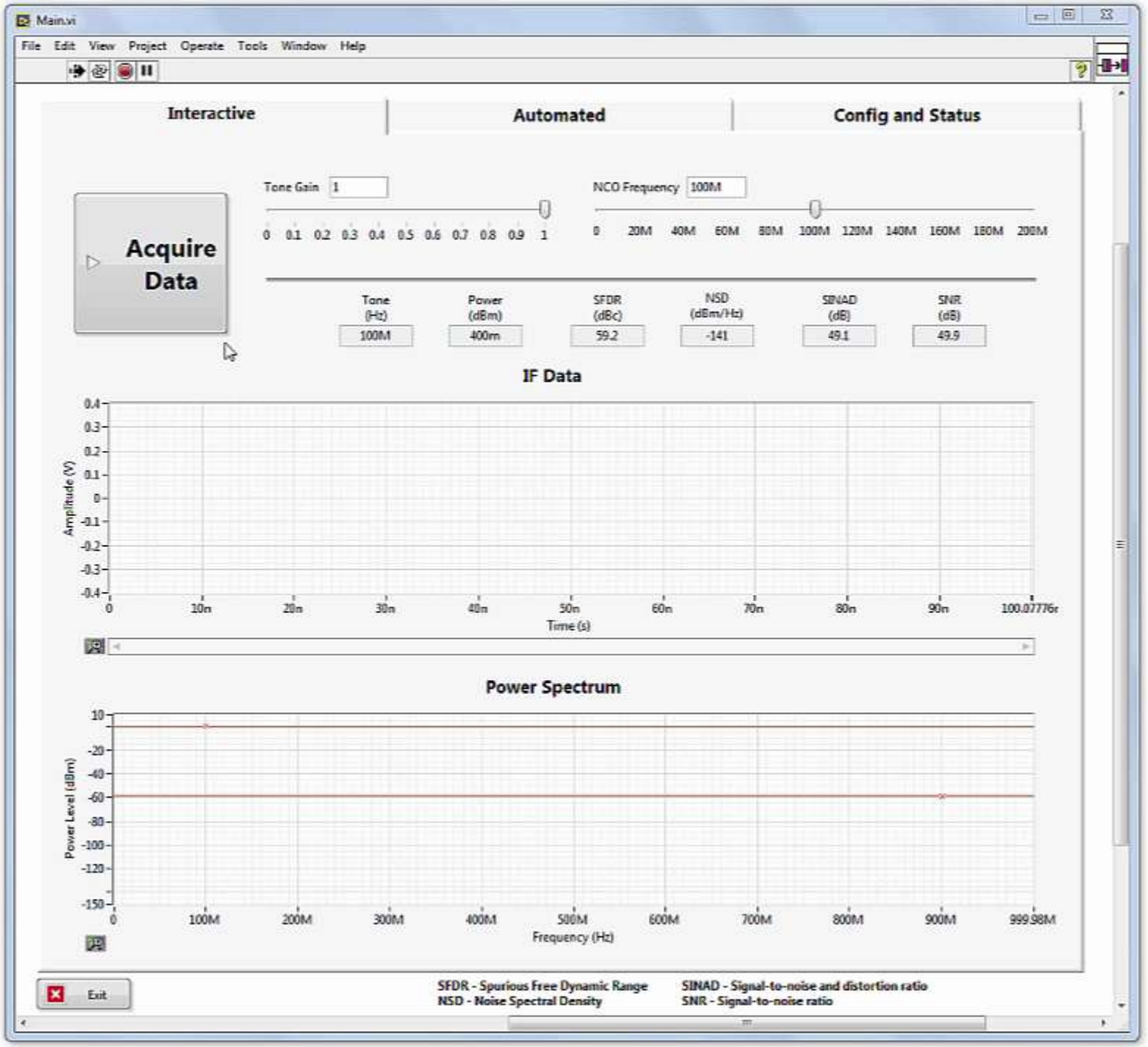
Demo: Protocol-Aware Test

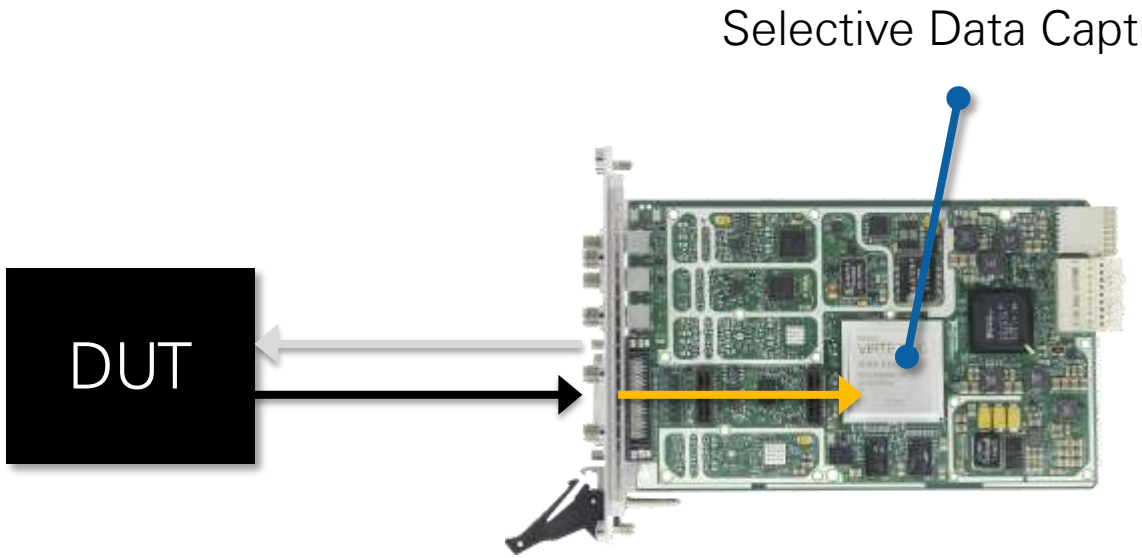
- High-speed serial protocol implemented on FPGA
- Ability to adapt to custom protocol implementations
- No need to synthesize protocol vectors on processor
- On-FPGA stimulus generation



Demo: DAC Test Hardware




Main.vi
File Edit View Project Operate Tools Window Help
Interactive
Automated
Config and Status
Acquire Data
Tone Gain 1
0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1
NCO Frequency 100M
0 20M 40M 60M 80M 100M 120M 140M 160M 180M 200M
Tone (Hz) 100M
Power (dBm) 400m
SFDR (dBc) 59.2
NSD (dBm/Hz) -141
SINAD (dB) 49.1
SNR (dB) 49.9
IF Data
Amplitude (V)
Time (s)
Power Spectrum
Power Level (dBm)
Frequency (Hz)
Exit
SFDR - Spurious Free Dynamic Range
NSD - Noise Spectral Density
SINAD - Signal-to-noise and distortion ratio
SNR - Signal-to-noise ratio



3. Custom Triggering and Data Reduction

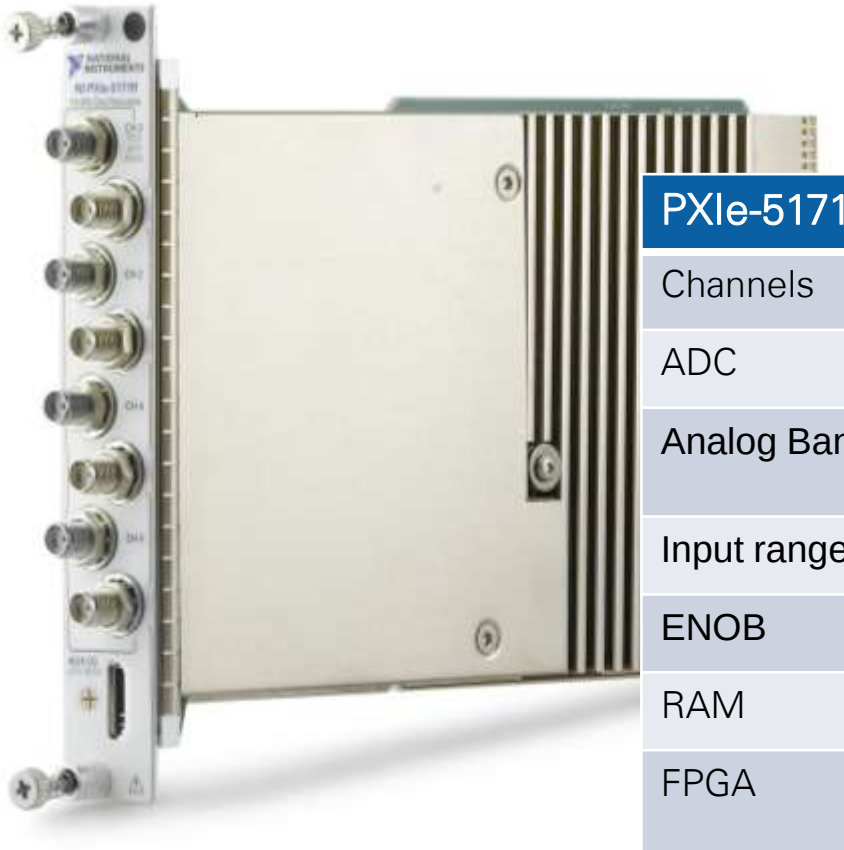
Higher Test Throughput

Hardware Re-Use and Future-Proofing

New, Innovative Tests

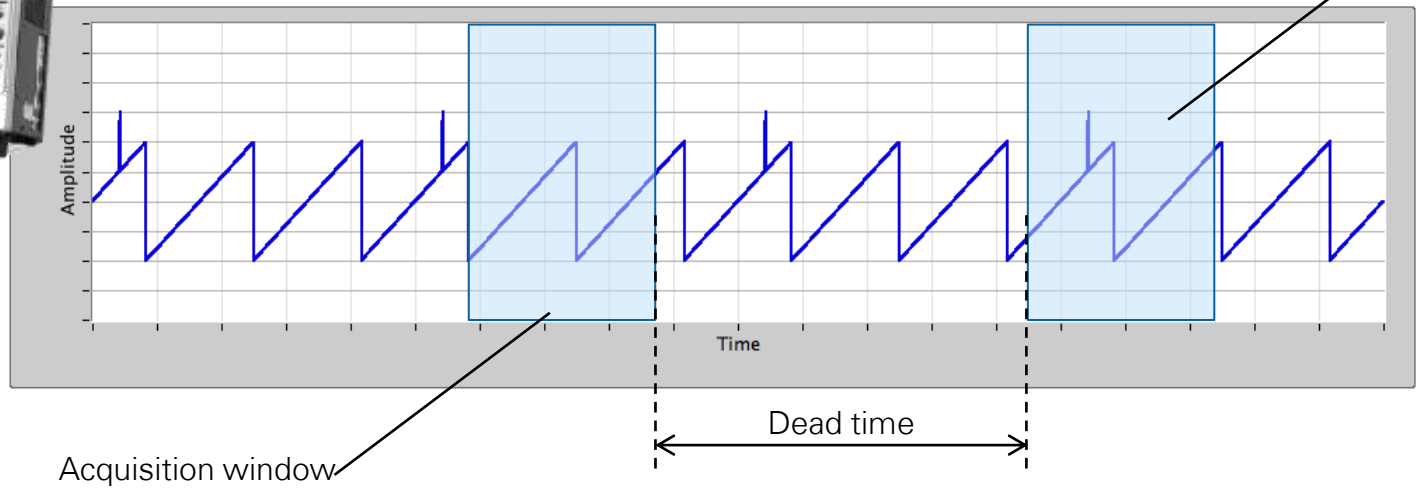
Lower Total Cost of Test

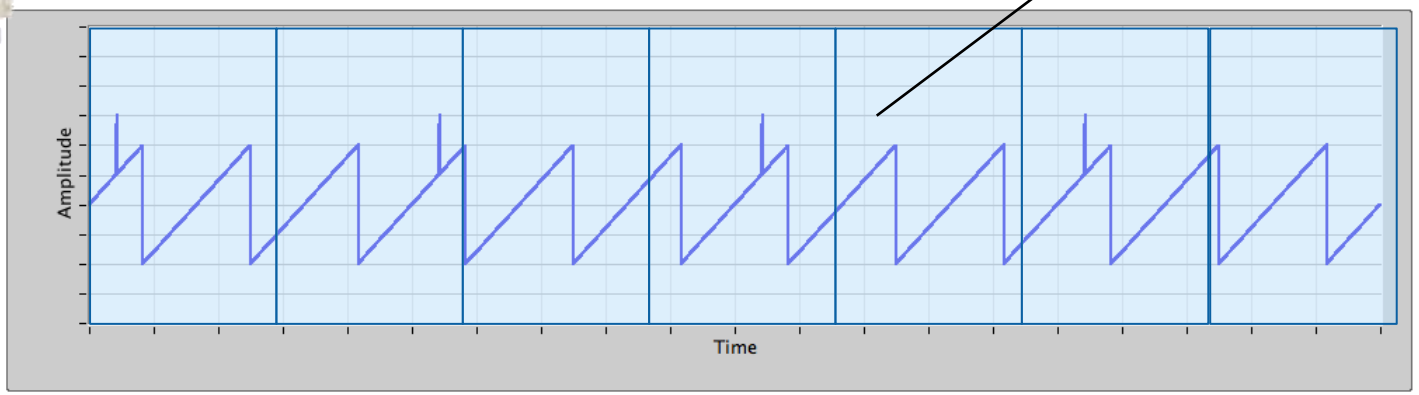
8 ch., 250 MHz Reconfigurable Oscilloscope



PXIe-5171R Specifications	
Channels	8 (simultaneously sampled)
ADC	250 MS/s, 14-bit
Analog Bandwidth	250 MHz Selectable 100 MHz filter
Input ranges	0.2 V_{pp} to 5 V_{pp}
ENOB	> 11 (preliminary)
RAM	1.5 GBit
FPGA	Kintex-7 410T FPGA Programmable with LabVIEW PXI Express x8 Gen 2 bus interface (> 3 GB/s)
No. of Slots	1

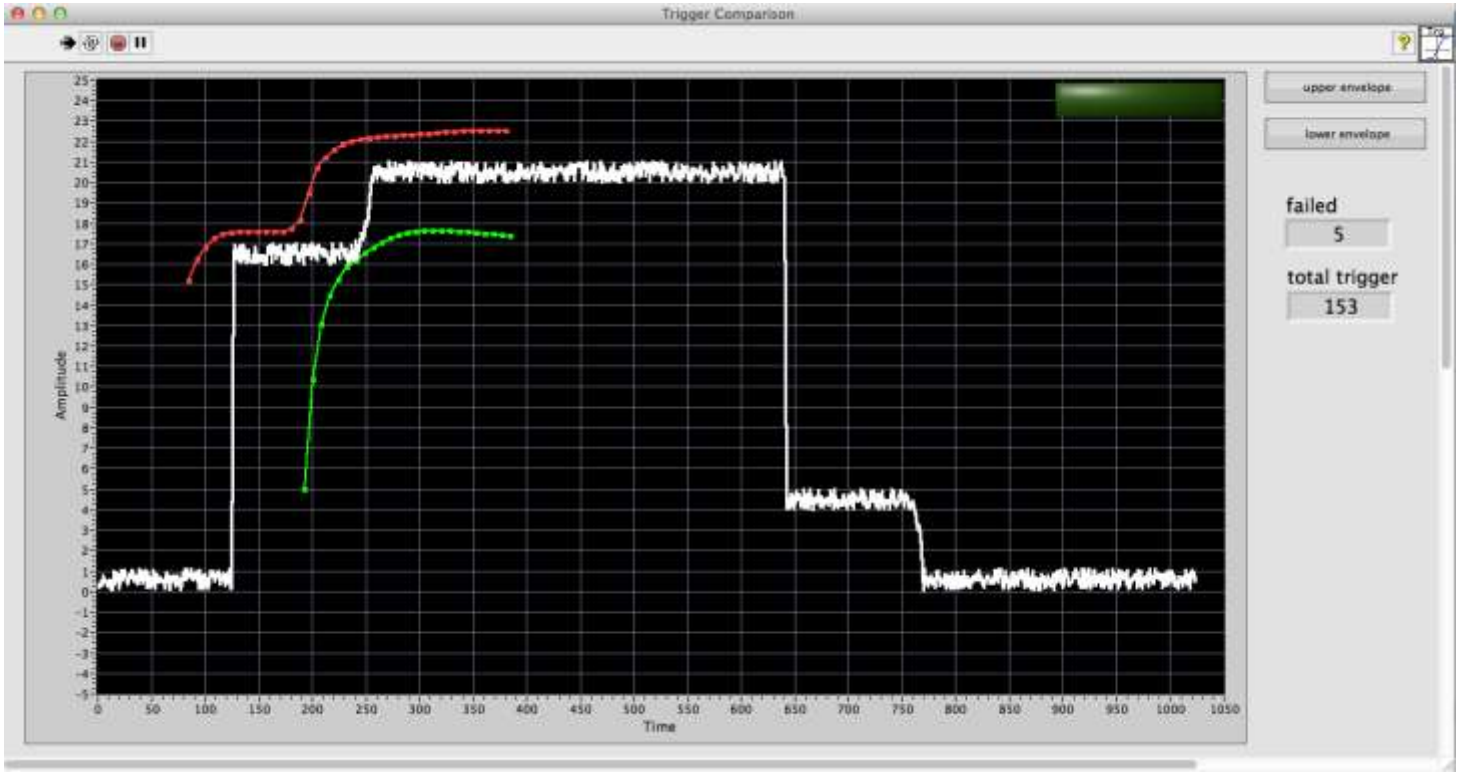
Detect Events Faster and Deterministically





Demo: Time Domain Mask Trigger

- Acquire signals (glitch) that are within a given envelope



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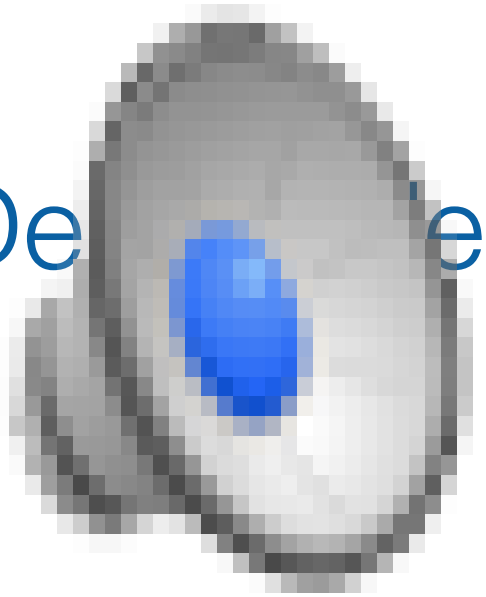

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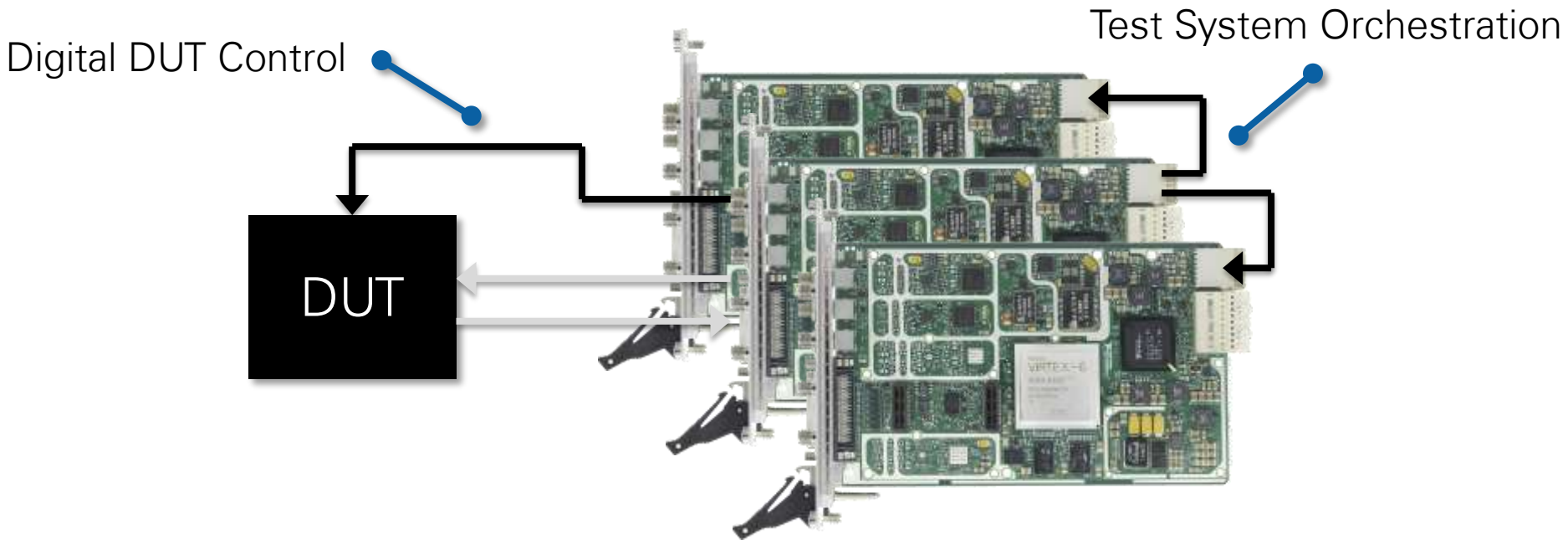


4. Deterministic Test Execution and DUT Control

Higher Test Throughput

Hardware Re-Use and Future-Proofing

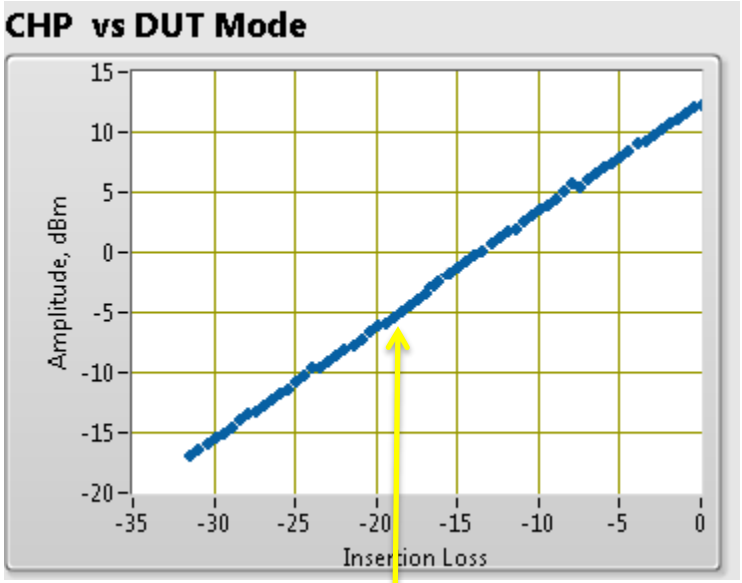
New, Innovative Tests

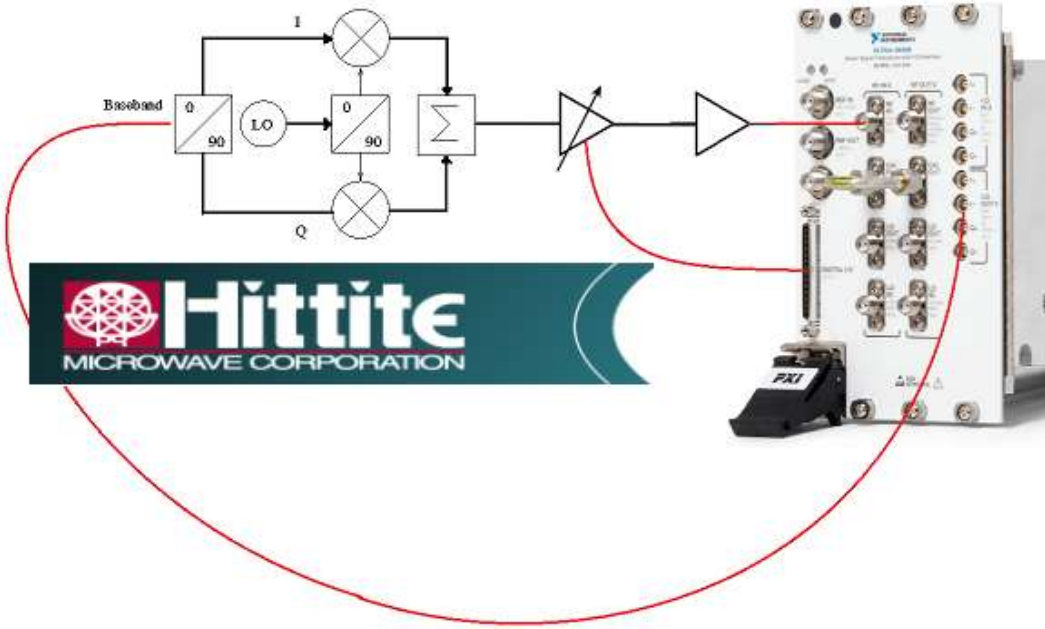
Lower Total Cost of Test

6 GHz, 200 MHz Bandwidth Vector Signal Transceiver

PXIe-5646R Specifications	
Configuration	VSA and VSG with independent LOs 24 DIO lines
Frequency Range	65 MHz to 6 GHz
Sample Rate	**250 MS/s**
Bandwidth	**200 MHz**
Features	• Virtex-6 **LX240T** programmable FPGA w/ LabVIEW • Fast Tuning Mode: <400 µs
New Features	• Support for 802.11ac 160 MHz • Support for LTE-Advanced

Demo: VST DUT Control and Hardware Test Sequencing





64 DUT Modes

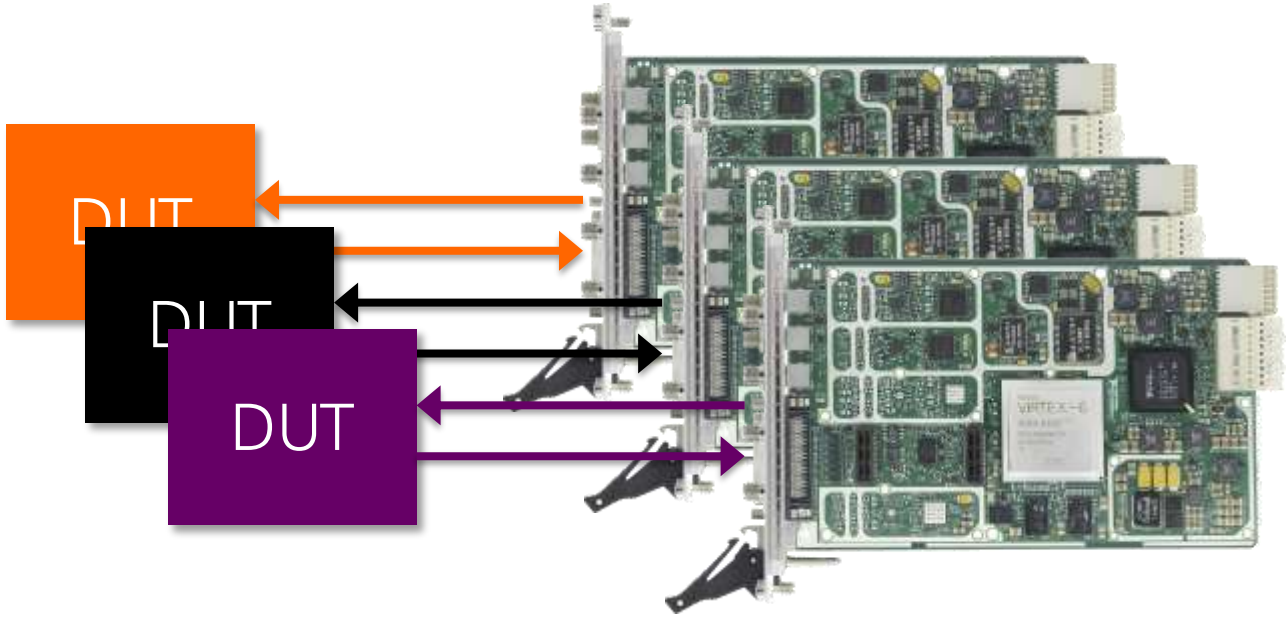
ACPR, CHP, EVM at Each Point

Test Sequencing

Software-Bas

Hardware-Ba

Hardware-Based Test Sequencing with additional CPU



5. DUT or Application-Specific Personalities

Higher Test Throughput

Hardware Re-Use and Future-Proofing

New, Innovative Tests

Lower Total Cost of Test

Multiple Personalities

DUT A
- Serial RapidIO
- 1 Lane
- 3.125 Gbps

DUT B
- Serial RapidIO
- 4 Lanes
- 6.25 Gbps

User-Programmable FPGAs on Software-Designed Instruments Enable:

1. On-FPGA Measurements and Stimulus Generation
2. Closed-Loop or Protocol-Aware Test
3. Custom Triggering and Data Reduction
4. Deterministic Test Execution and DUT Control
5. DUT or Application-Specific Personalities

Higher Test Throughput

Hardware Re-Use and Future-Proofing

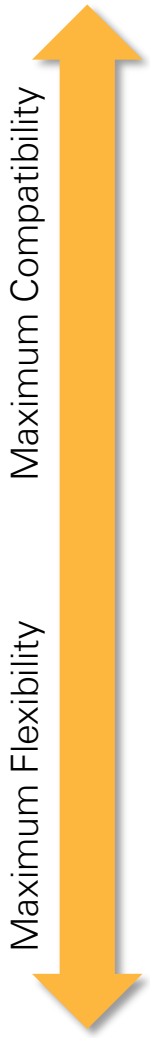
New, Innovative Tests

Lower Total Cost of Test

Software-Designed Instrument…. *Software*

NATIONAL INSTRUMENTS

Software-Designed Instrument Programming Options



Instrument Driver

- Industry-standard programming paradigm
- Out-of-the-box functionality

Instrument Driver FPGA Extensions

- Industry-standard programming paradigm
- Out-of-the-box functionality
- Application-specific FPGA enhancements

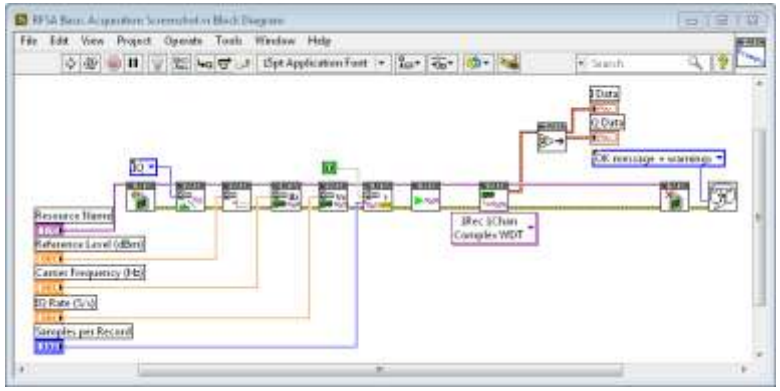
LabVIEW Sample Projects and Instrument Design Libraries

- Variety of architectural templates
- End-to-end customization of processor and FPGA capabilities

Instrument Drivers

- Primary Benefit: Hardware Abstraction
  - APIs for simplified instrument programming
    - LabVIEW API
    - C/C++ and .NET APIs
  - Code portability
    - Across driver versions
    - Across hardware devices
    - Across vendors (IviScope, IviDMM)

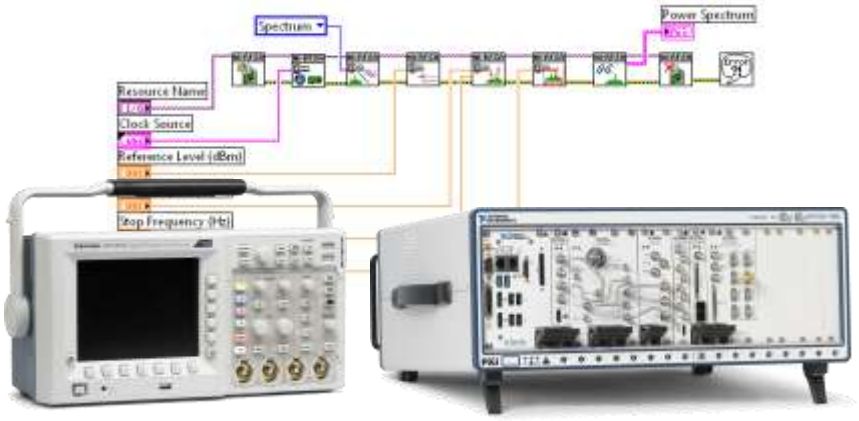
- *NI* Instrument Drivers Add:
  - Configuration in NI MAX
  - Soft front panels (SFPs) for interactive use
  - Example programs that exercise full functionality of the API
  - Integrated API help/documentation

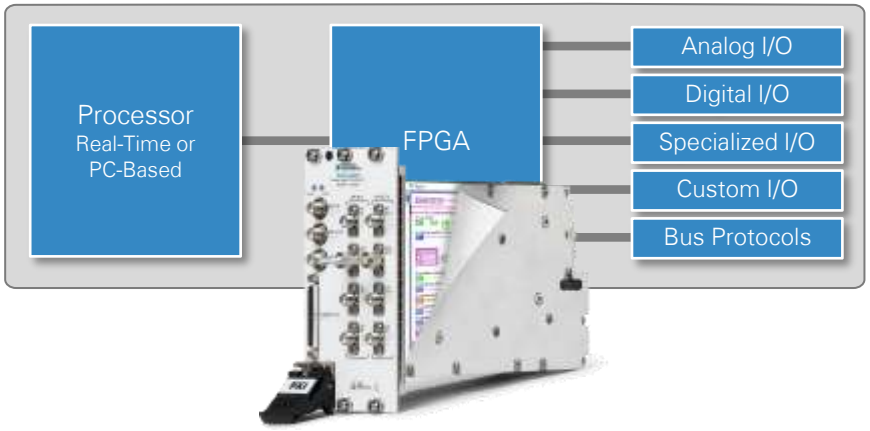


NI-RFSA LabVIEW API

NI-RFSA Soft Front Panel

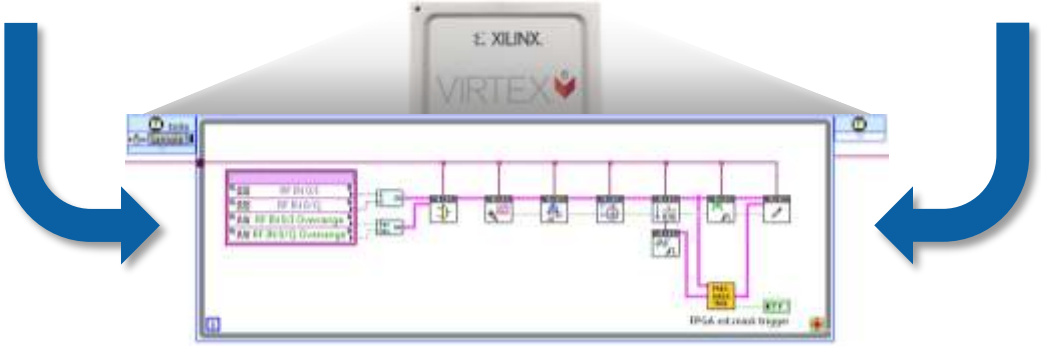
Instrument Driver *FPGA Extensions*





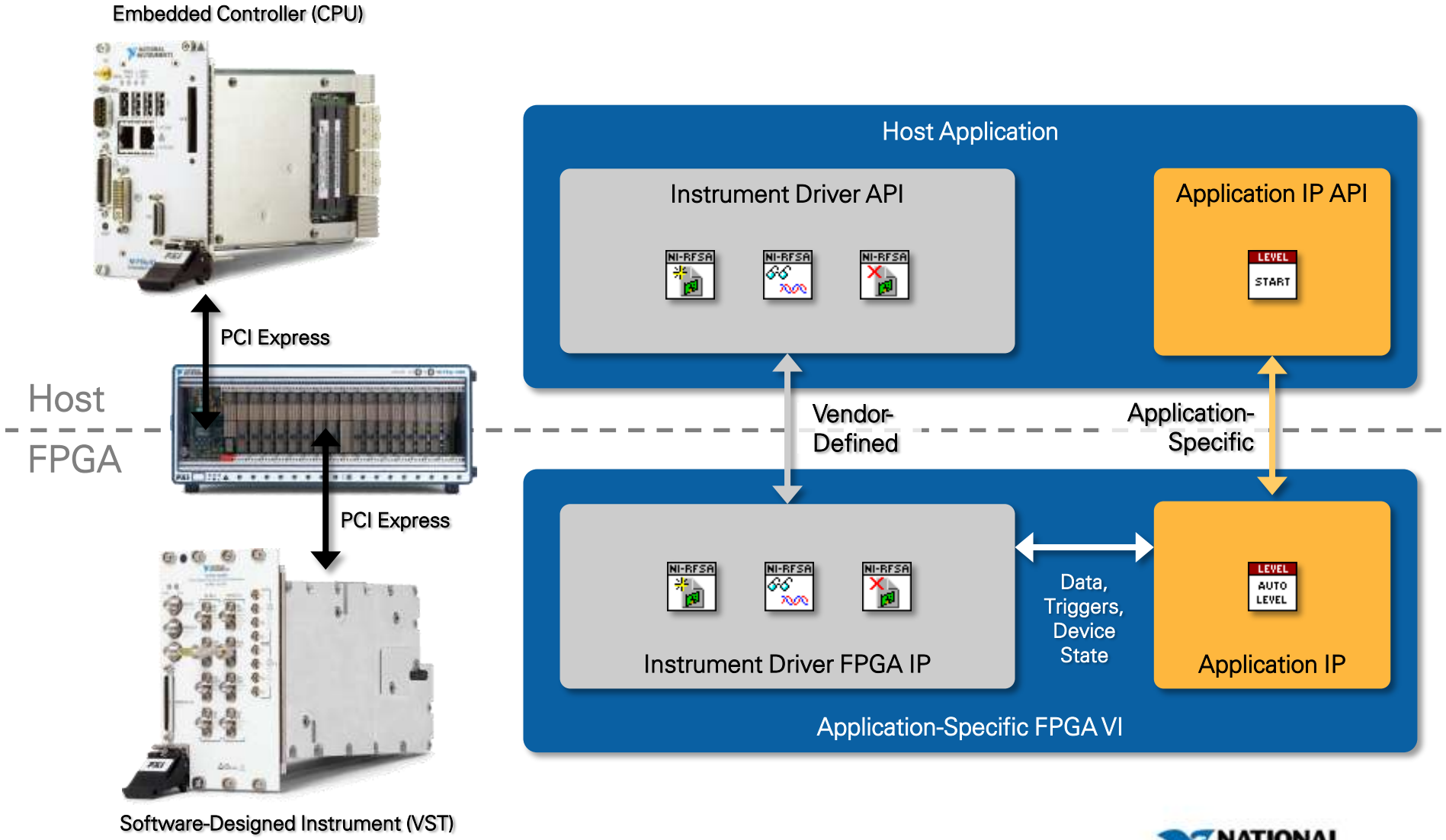
The *compatibility* of
industry-standard instrument drivers

The *flexibility* of
the LabVIEW RIO architecture



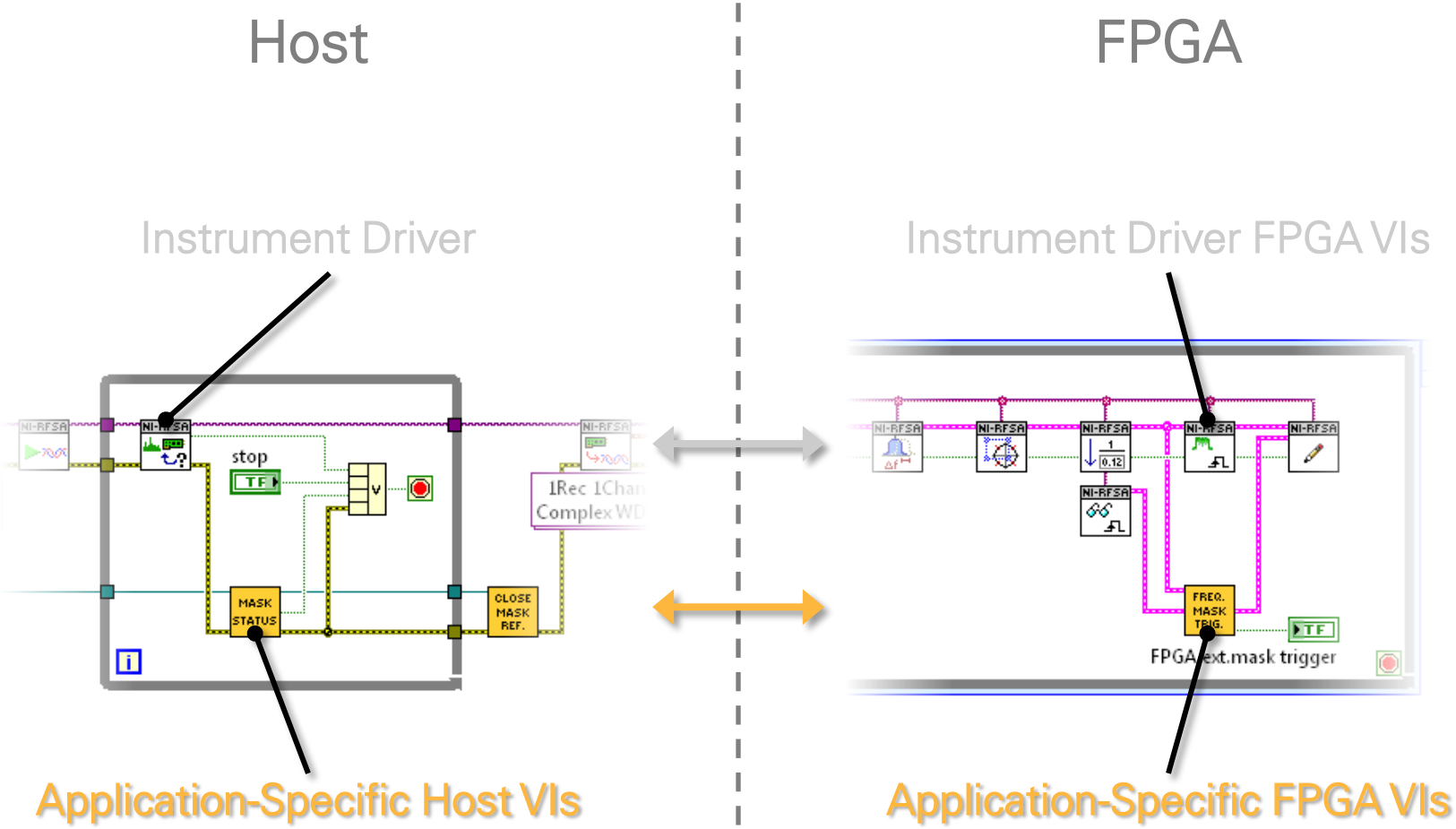
Instrument Driver *FPGA Extensions*

Instrument Driver *FPGA Extensions*

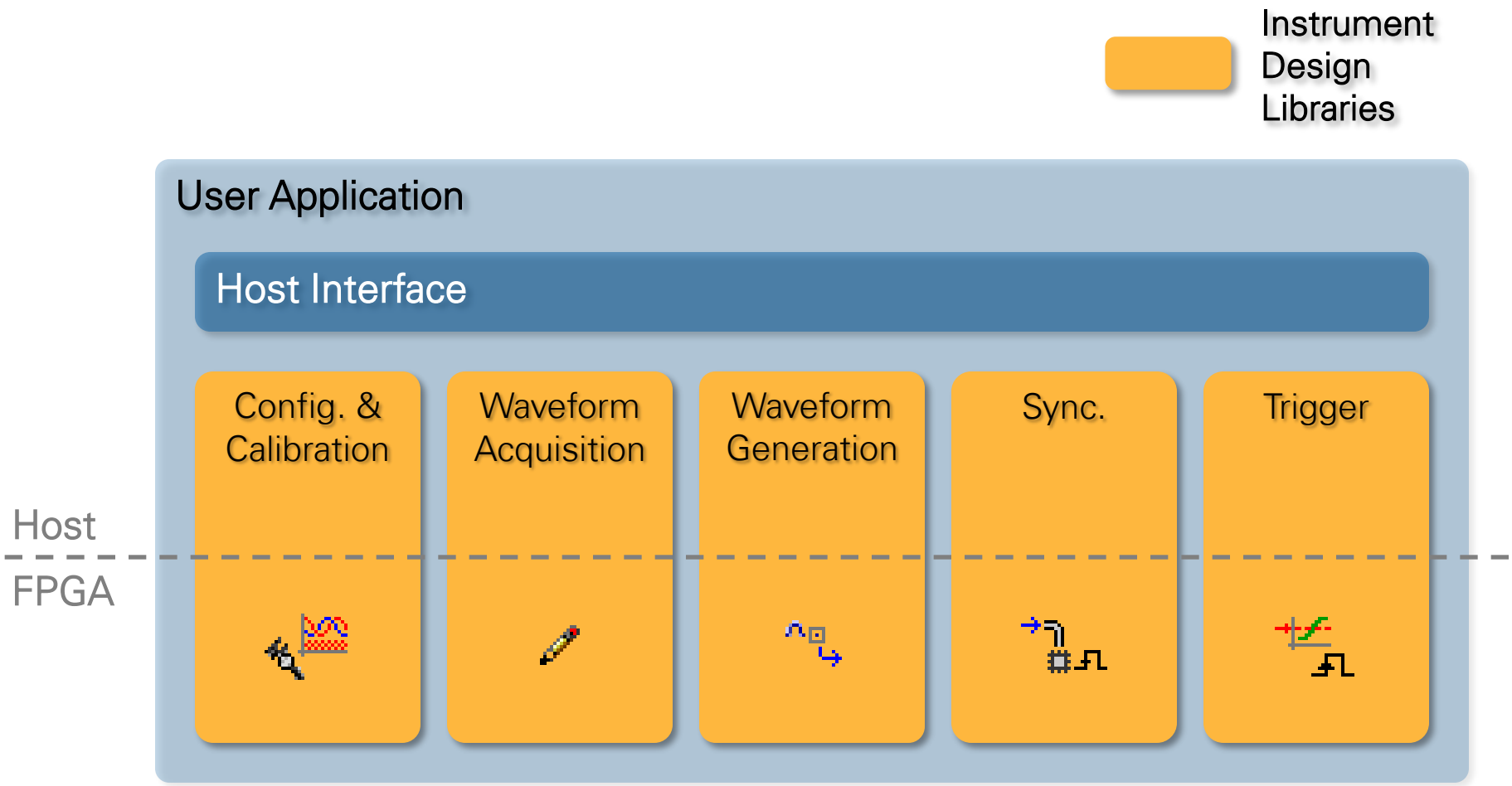


NATIONAL INSTRUMENTS

Instrument Driver *FPGA Extensions*



Software-Designed Instrument Architecture

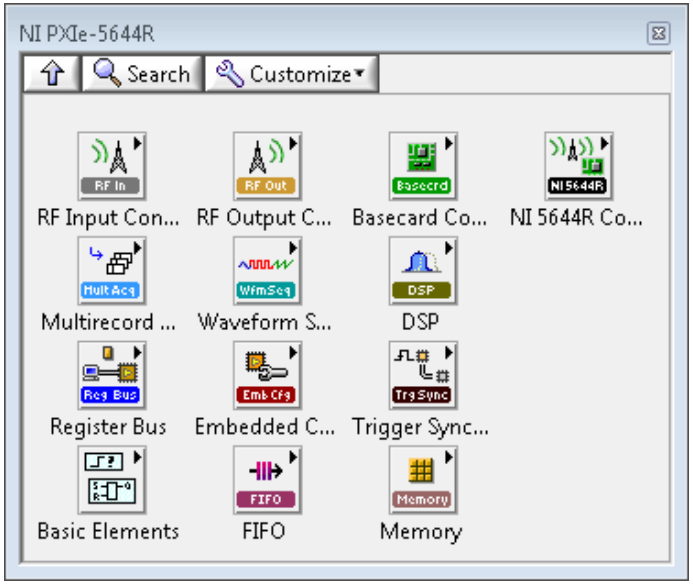


Instrument Design Libraries

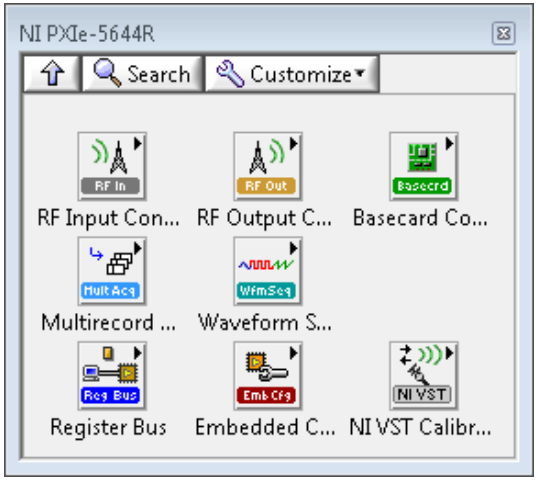
- Color-coded and thicker VI border
- Bundled into Host and FPGA *.lvlib
- Located in **[LabVIEW Dir]\instr.lib**
  - NI "owned," but primarily open source
  - VIs are locked to avoid accidental editing
- Host and FPGA Palettes

Typical subVI

Instrument Design Library VI



FPGA

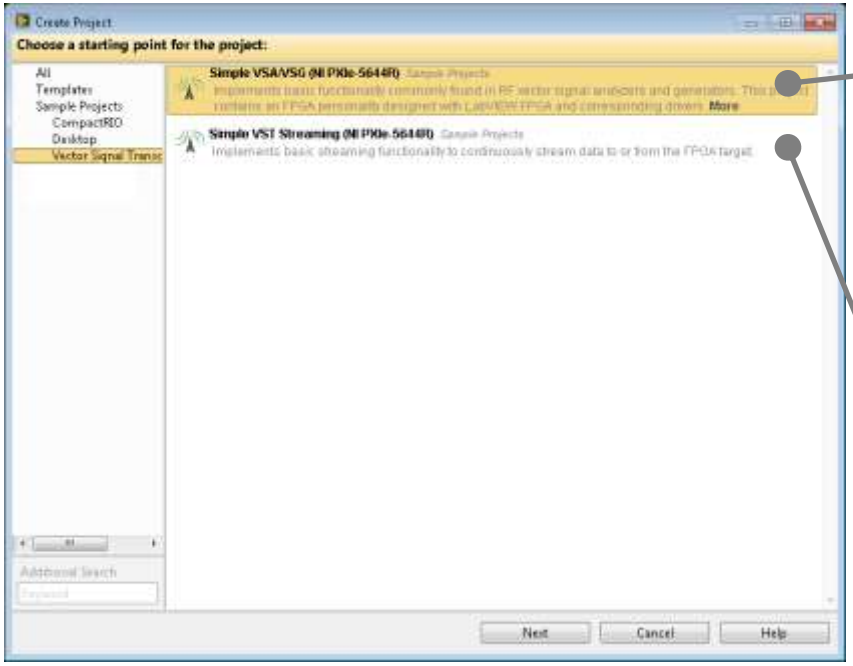


Host

NATIONAL INSTRUMENTS

LabVIEW Sample Projects for Software-Designed Instruments

Completely flexible, built on instrument design libraries



Instrumentation

Implements triggering and multirecord acquisition and generation.

Provides a familiar look and feel to traditional instrument drivers on the host.

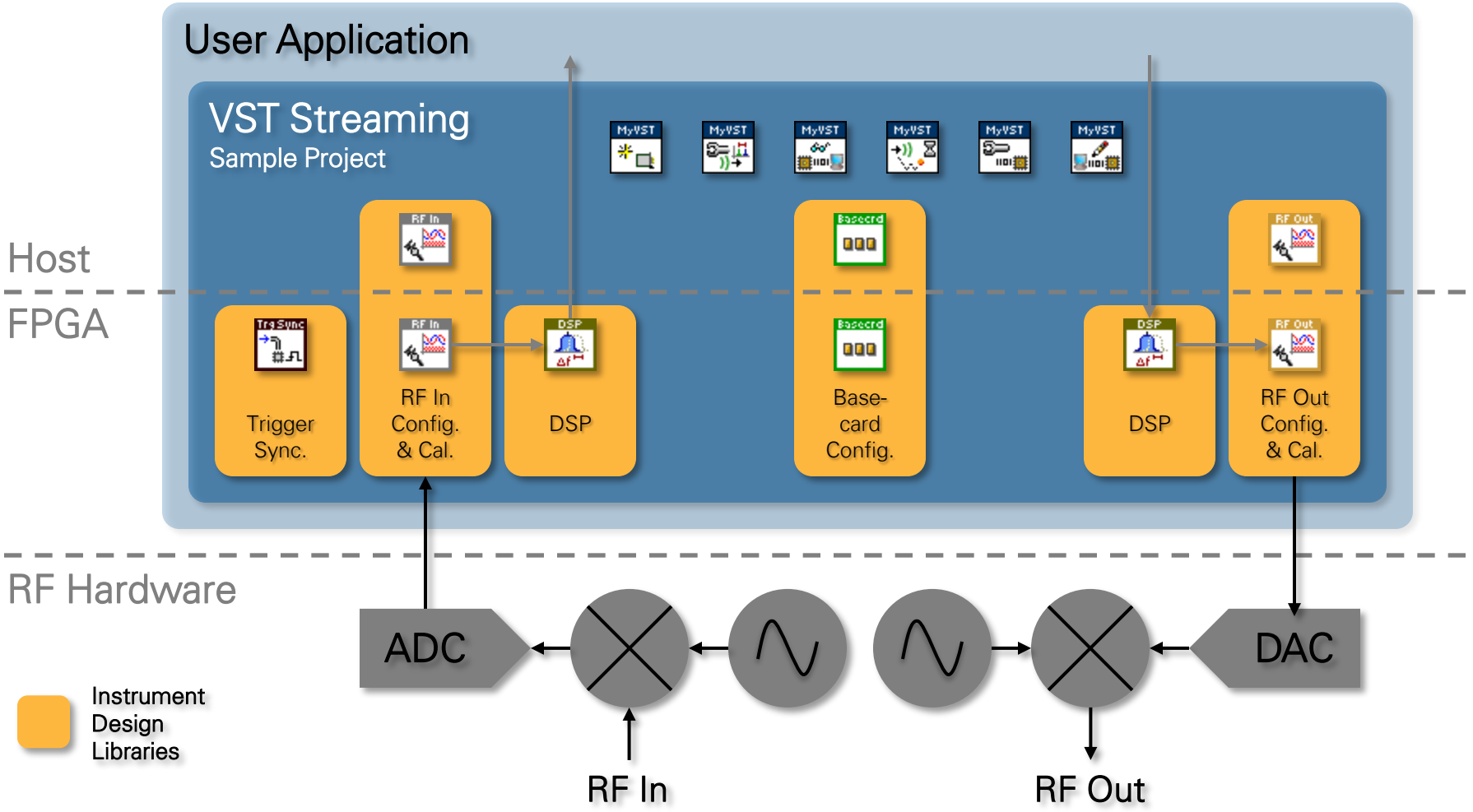
Streaming

Implements basic real-time streams to and from the host

Serves as a starting point for implementing real-time DSP and rerouting data streams between loops, FPGAs, and host processing.

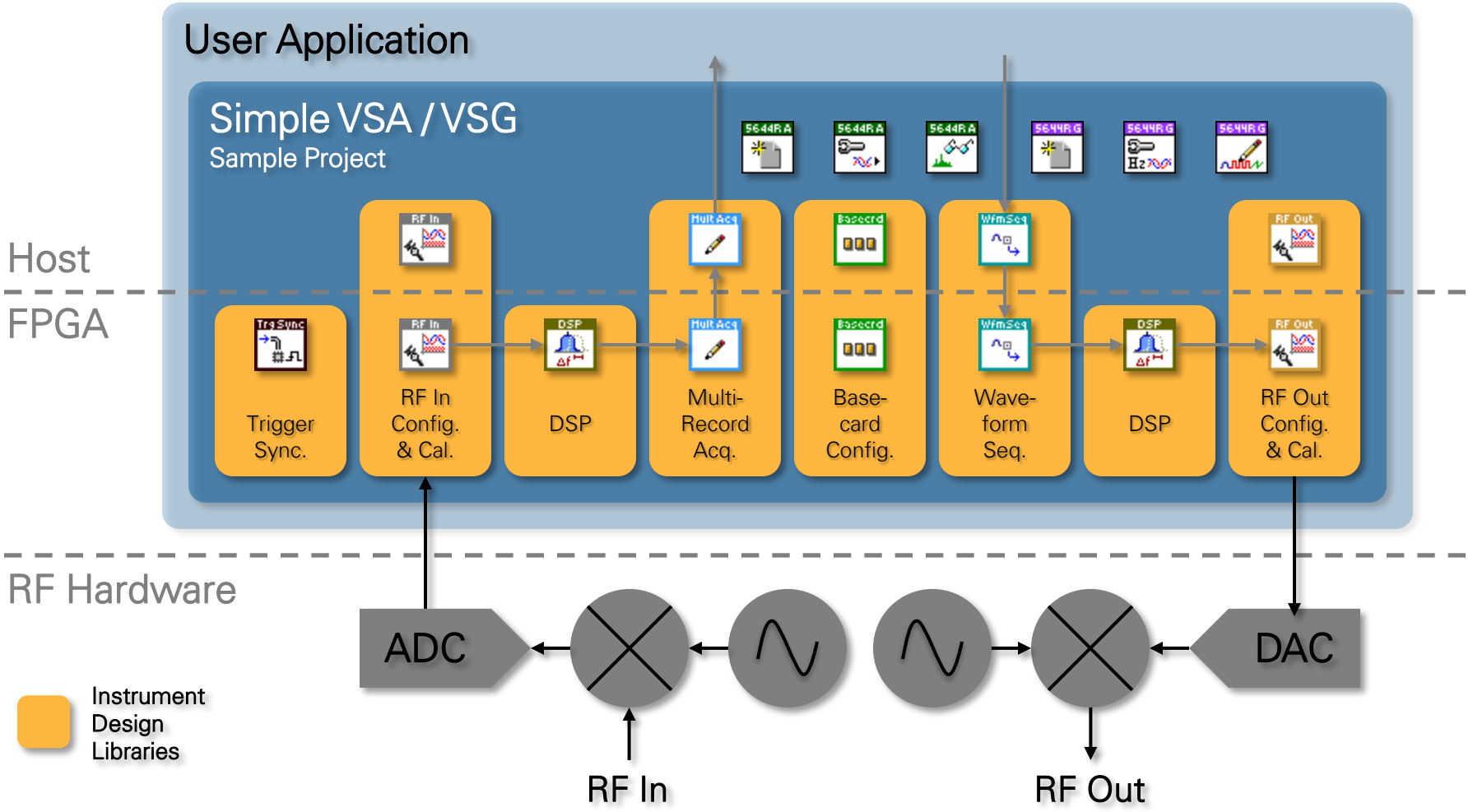
Streaming Sample Project

VST Example



Record-Based Sample Project

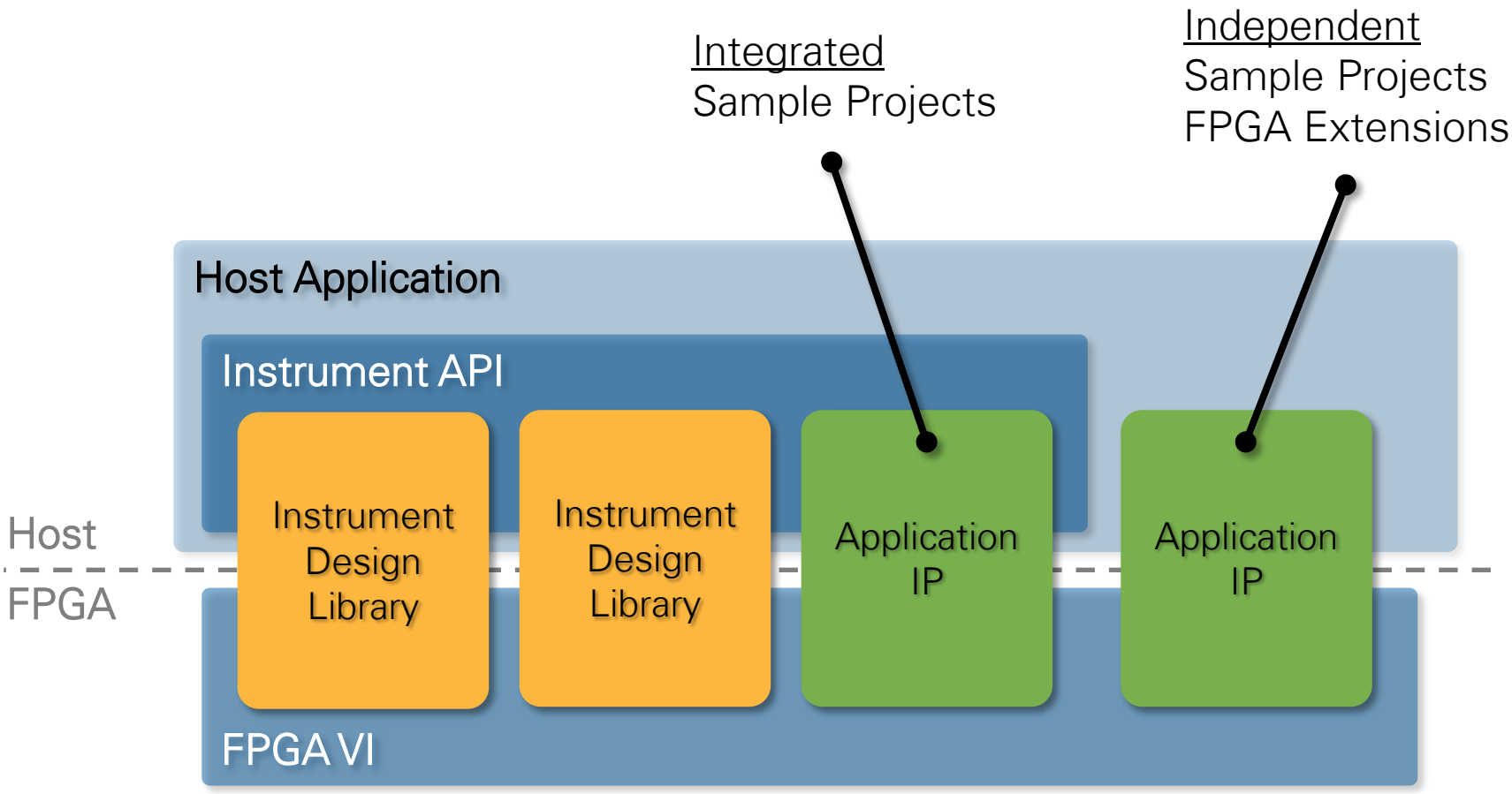
VST Example



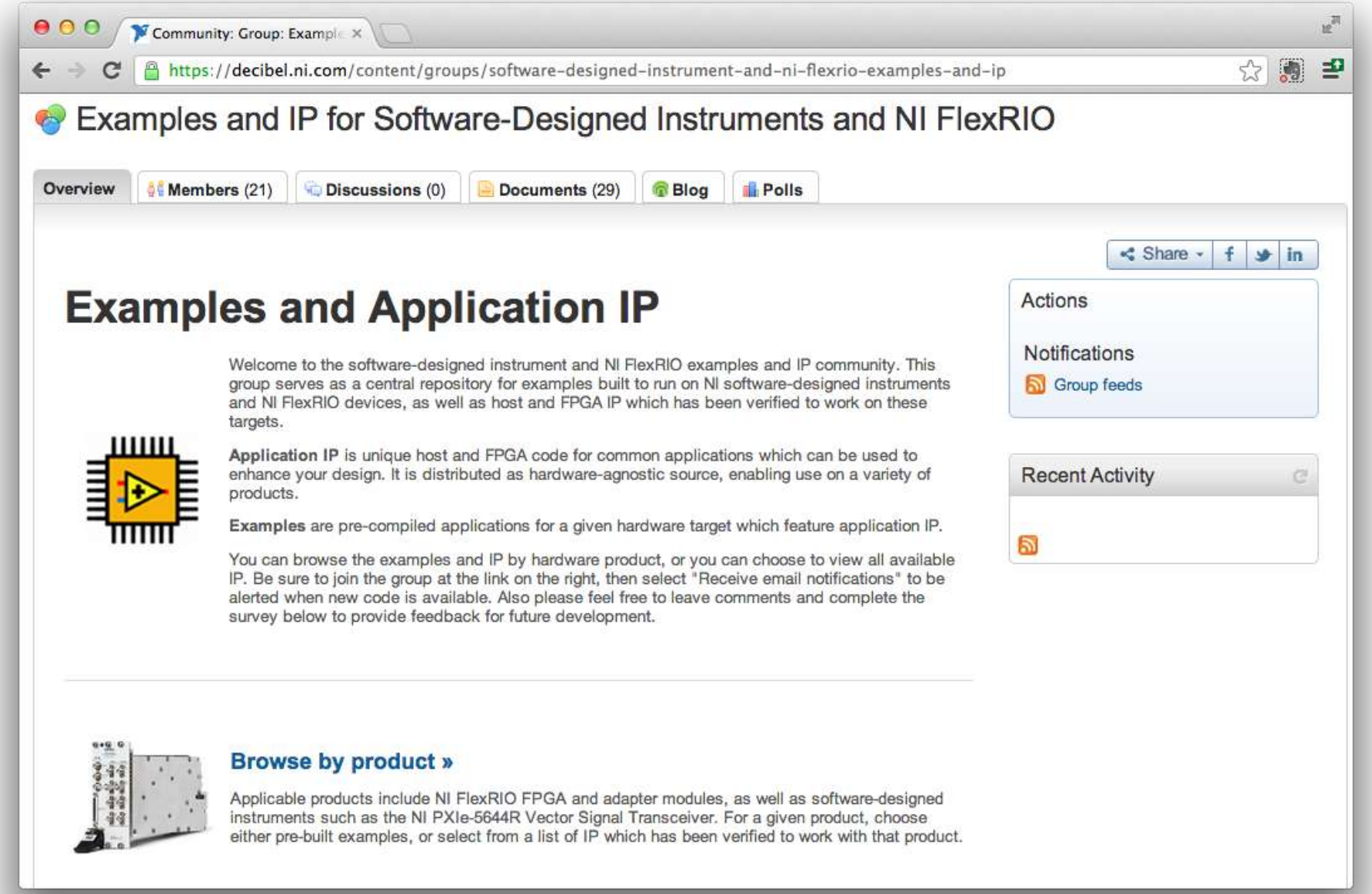
Instrument Model	Instrument Driver	Instrument Driver FPGA Extensions	LabVIEW Sample Projects and Instrument Design Libraries
Vector Signal Transceivers			
PXIe-5644R	NI-RFSA / NI-RFSG / NI-RFmx	Use bitfiles from ni.com or custom development through early access program	NI LabVIEW 2014 Instrument Design Libraries for Vector Signal Transceivers 14.0
PXIe-5645R			
PXIe-5646R			
Oscilloscopes			
PXIe-5170R	NI-SCOPE Planned	Planned	NI LabVIEW 2014 Instrument Design Libraries for Oscilloscopes 14.0
PXIe-5171R			
IF Digitizers			
PXIe-5624R	X	X	NI LabVIEW 2014 Instrument Design Libraries for IF Digitizers 14.0
Vector Signal Analyzer			
PXIe-5668R	NI-RFSA / NI-RFmx	Use bitfiles from ni.com or custom development through early access program	NI LabVIEW 2014 Instrument Design Libraries for Vector Signal Analyzers 14.0
High-Speed Serial Instruments			
PXIe-6591R	X	X	NI LabVIEW 2014 Instrument Design Libraries for High Speed Serial Instruments 14.0
PXIe-6592R			

IP and Examples

Componentized IP Use Model

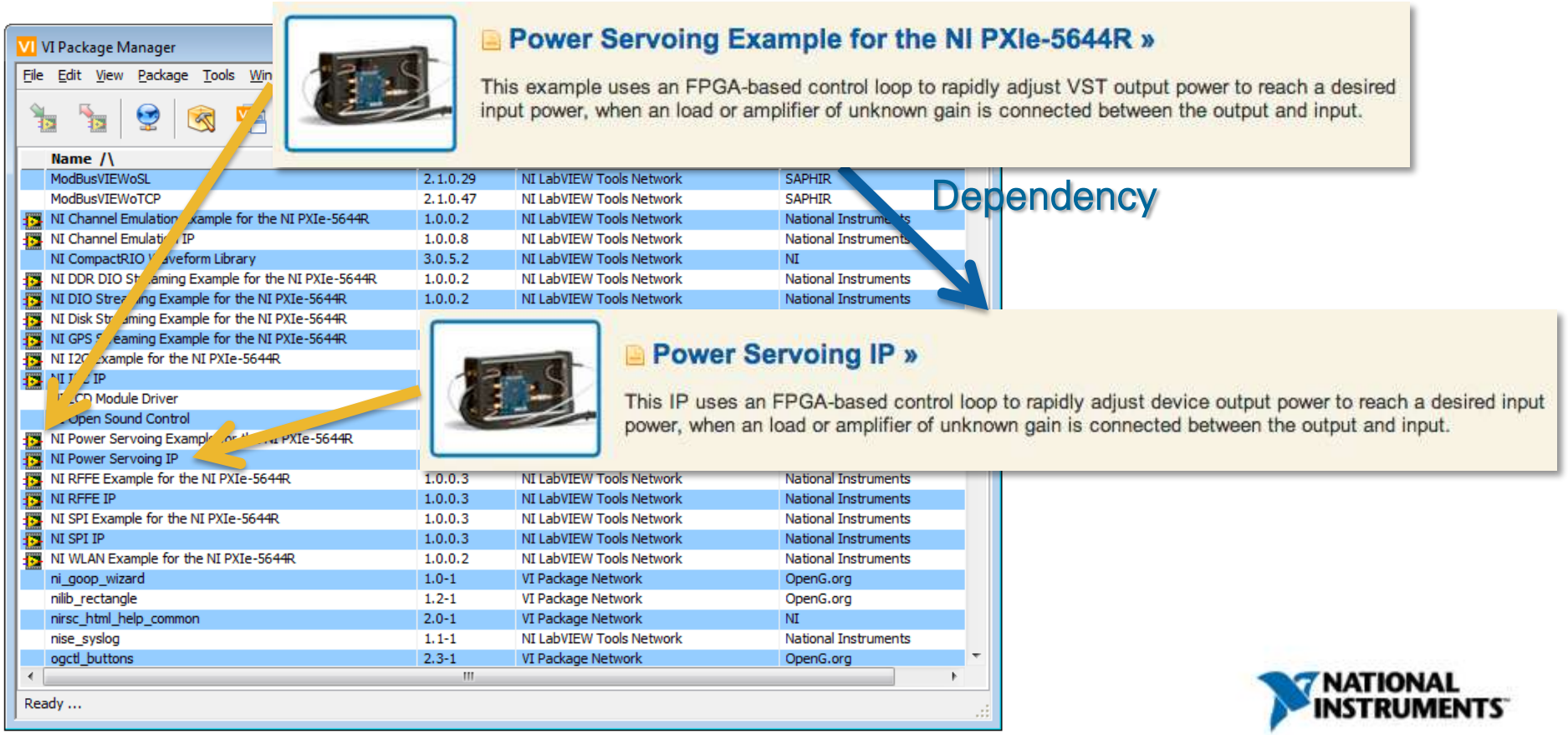


Application-Specific Instrument Design Libraries


Community: Group: Example
https://decibel.ni.com/content/groups/software-designed-instrument-and-ni-flexrio-examples-and-ip
Examples and IP for Software-Designed Instruments and NI FlexRIO
Overview
Members (21)
Discussions (0)
Documents (29)
Blog
Polls
Share
Examples and Application IP
Welcome to the software-designed instrument and NI FlexRIO examples and IP community. This group serves as a central repository for examples built to run on NI software-designed instruments and NI FlexRIO devices, as well as host and FPGA IP which has been verified to work on these targets.
Application IP is unique host and FPGA code for common applications which can be used to enhance your design. It is distributed as hardware-agnostic source, enabling use on a variety of products.
Examples are pre-compiled applications for a given hardware target which feature application IP.
You can browse the examples and IP by hardware product, or you can choose to view all available IP. Be sure to join the group at the link on the right, then select "Receive email notifications" to be alerted when new code is available. Also please feel free to leave comments and complete the survey below to provide feedback for future development.
Actions
Notifications
Group feeds
Recent Activity
Browse by product »
Applicable products include NI FlexRIO FPGA and adapter modules, as well as software-designed instruments such as the NI PXIe-5644R Vector Signal Transceiver. For a given product, choose either pre-built examples, or select from a list of IP which has been verified to work with that product.

VI Package Manager

- Automatic dependency resolution
- Automatic updates
- Simplified installation experience



Next Steps

- ni.com/software-designed-instruments
  - Technical content
- ni.com/software-designed-instruments/getting-started
  - Examples and application IP
- High-Throughput LabVIEW FPGA Training
  - Link
- LabVIEW High-Performance FPGA Developer's Guide
  - Link
- Alliance Partners
  - ni.com/alliance – LabVIEW FPGA specialty