NIDays

THE LabVIEW CONFERENCE

PXI Synchronization

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Agenda

- Why synchronization?
- Clock/Trigger Synchronization
- PXI(e) architecture
- Timing Cards and Routing triggers
- Time-Based Synchronization
- Triggering and Synchronization code examples

What is Synchronization

- The Synchronization of two or more Instruments involves getting them to perform actions with a fixed and known relationship.

Requires the coordination of

- The instruments clocks
- The Trigger event

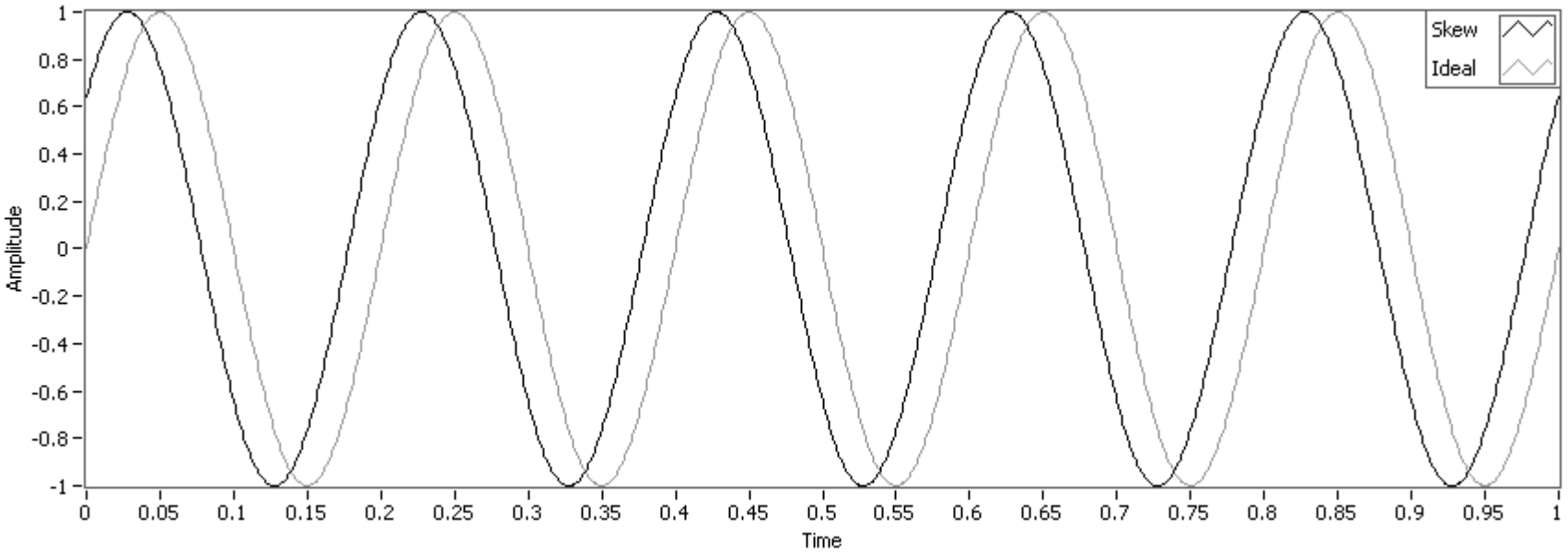
Synchronization Errors

- Common types of synchronization errors between Instruments
  - Skew
  - Drift
  - Jitter

- Synchronization Techniques aim to reduce these error significantly

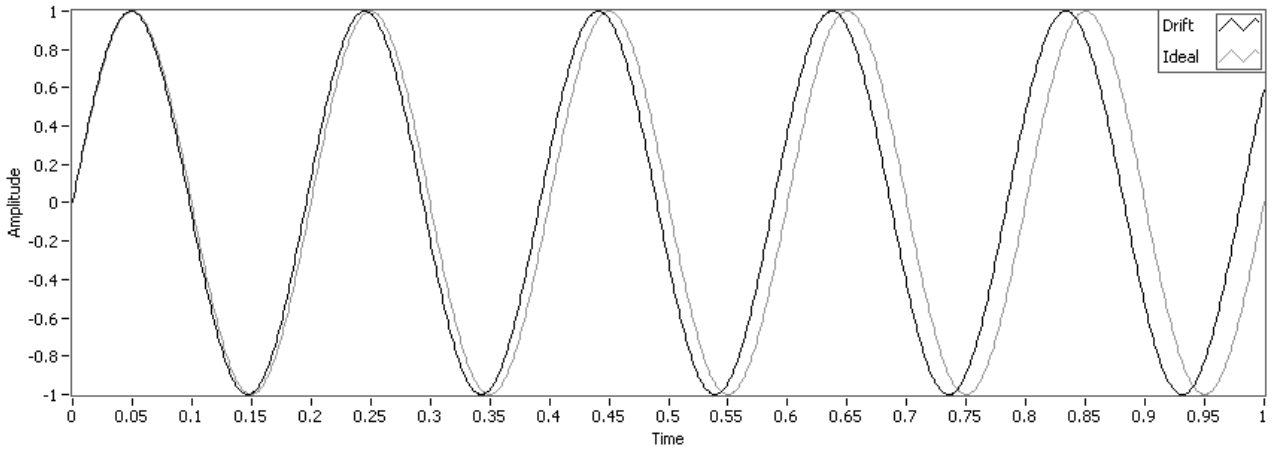
Skew

- Difference in trigger event times
- Many causes
- Propagation Delay
  - Common cause of skew in synchronized systems



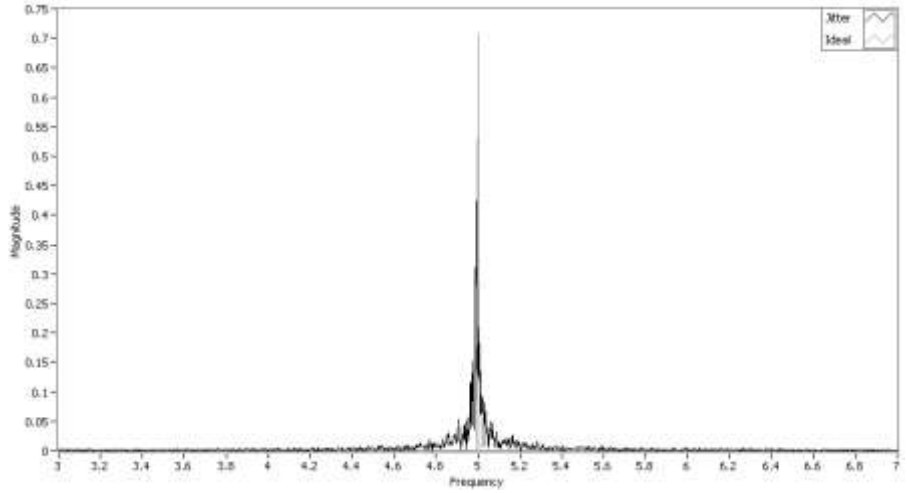
Drift

- Caused by differences between ideal and actual clock rates
- Causes synchronized instruments to loose synchronization over time.



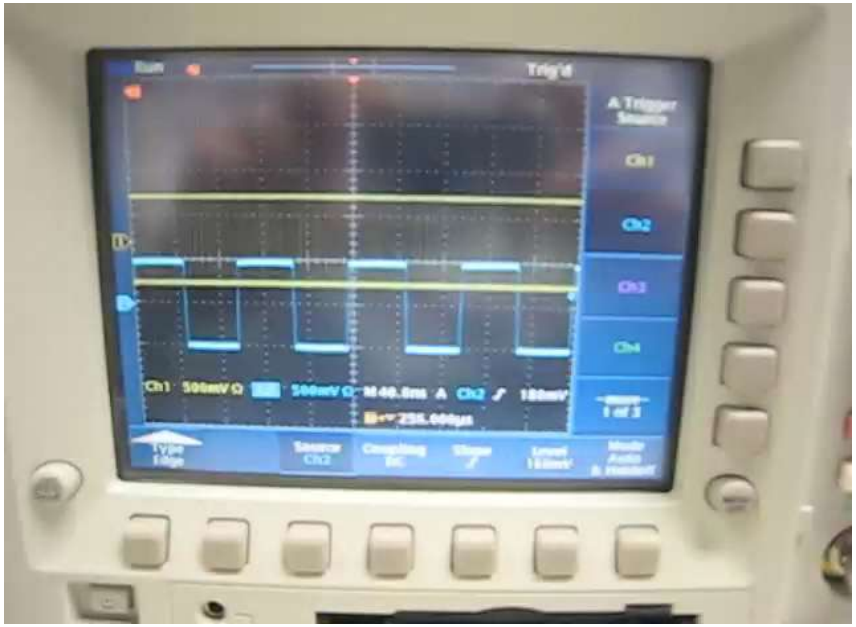
Jitter

- Random fluctuations in timing signals
- Common causes are noise or ringing on clock lines
- Causes phase noise in the frequency spectrum



Example

- Comparing PXI_CLK10 from two different Chassis



- Comparing two different 6653 OCXO

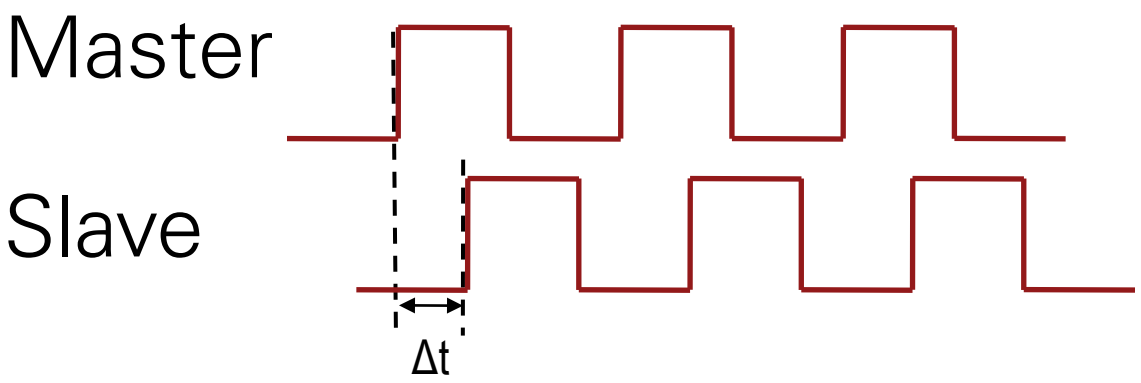
Clock Synchronization

There are two generic Clock Synchronization Methods

1. Shared Clock
2. Reference Clock

Shared Clock Synchronization

- The master instruments exports one of it's clocks
  - Timebase, Sample Clock, Update Clock, etc.
- All Slaves replace there own clock with this shared clock.



Reference Clock Synchronization

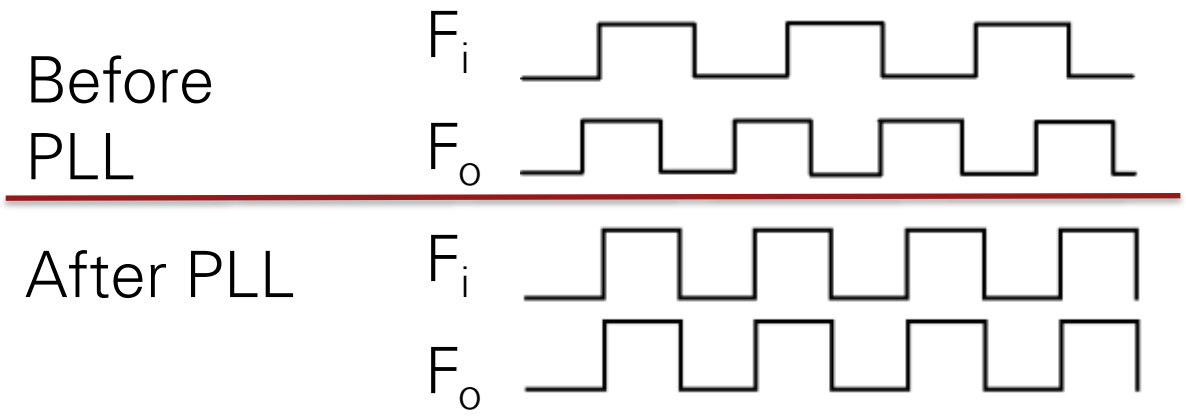
- Common Reference Clock is distributed to all instruments
  - Can be an external clock or Timebase from one of the Instruments
  - Typically 10MHz
- All instruments Phase-Lock there own internal Timebase to this reference Clock.

Phase-locking

Phase-Locked Loop (PLL)

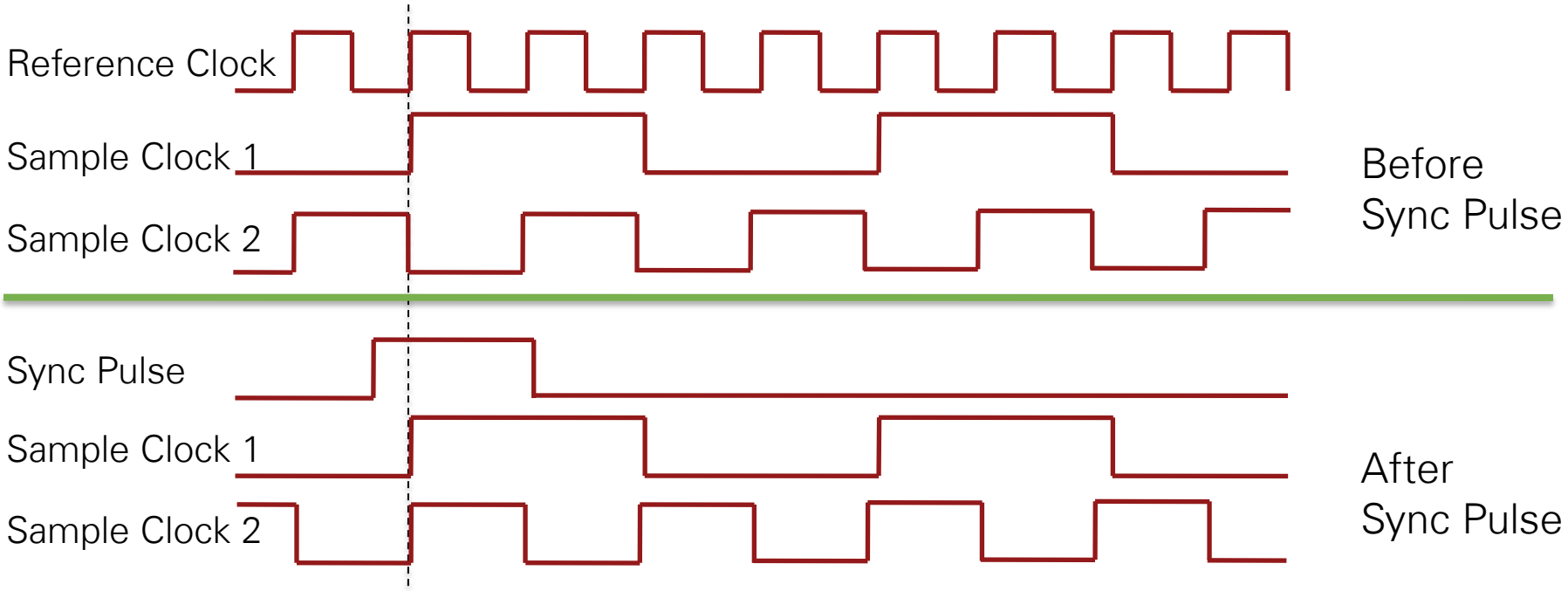
Control circuit that fixes Phase and Frequency relationship

- \+ F_o has same frequency accuracy and phase relation as F_i
- \- Control circuit adds additional Jitter and Phase noise.



Reference Clock Synchronization

Sync Pulse - Used to align Sample Clocks on all Instruments to the reference clock



Comparison Clock Synchronization

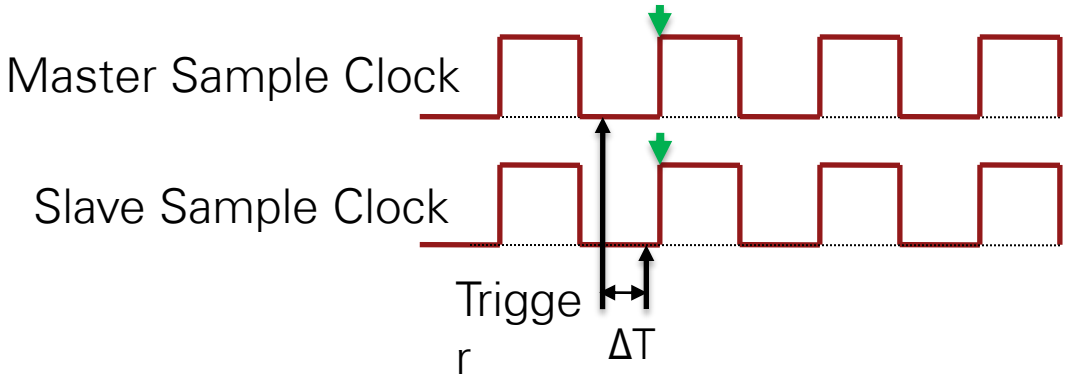
Shared Clock Method

+ Simple
+ Low Sample rates
- Clock Skew
  - Propagation delay of clock signal
- Single Clock Rate
- Similar Instrument Architectures

Reference Clock Method

+ High Sample Rates
+ Different Clock Rates
+ Dissimilar Instrument Architectures
- Adds Jitter (PLL)
- More Complex
  - Requires Sync Pulse

Trigger Synchronization



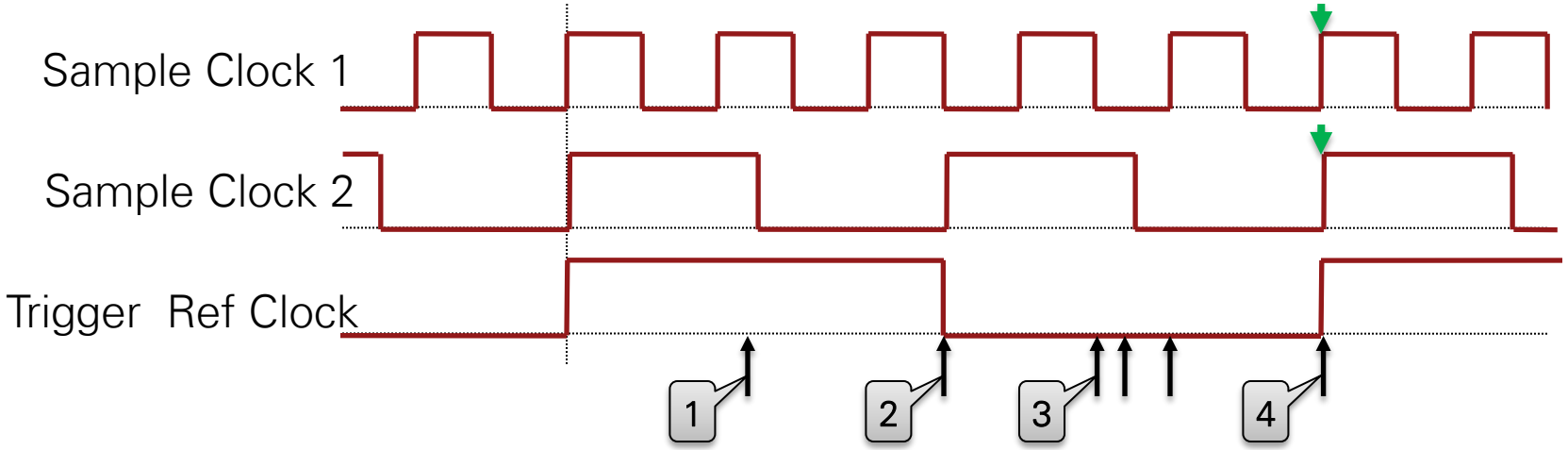
- Propagation Delay between master and slave can cause slaves to start on different sample clock edge.
- Depends on the moment the Master is triggered.
- More likely with High sample rates and/or long propagation delays

Trigger Synchronization

- Synchronize trigger on the master with Sample Clock edges using a common reference clock.

- Use a Trigger Reference Clock
  - Typically used with Reference Clock Synchronization.
  - Trigger clock rate must be a common divider of all Sample Clocks.
  - Aligned with all Sample Clocks.

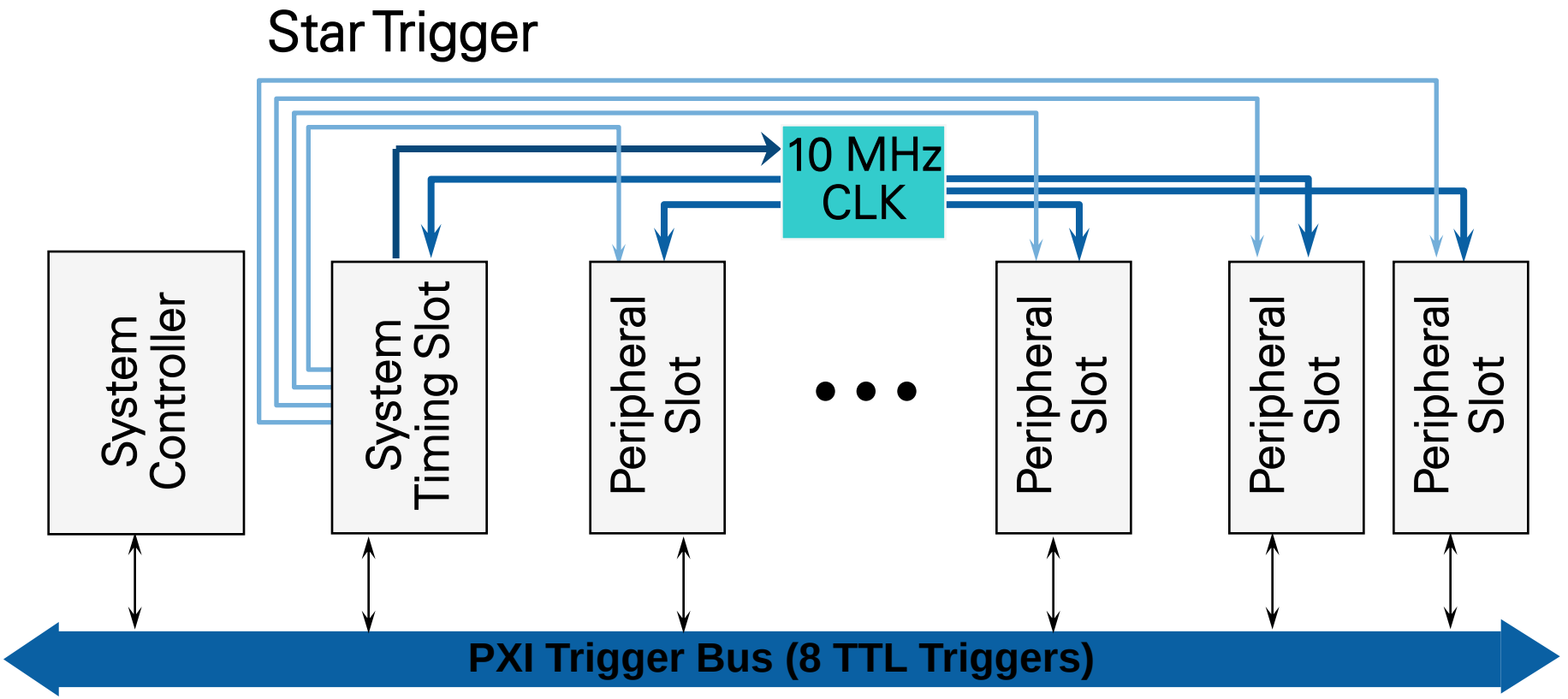
Trigger Synchronization



1. Master is triggered
2. Master transmits trigger to slaves
3. Triggers arrive at Slaves
4. All devices start on this Sample clock edge

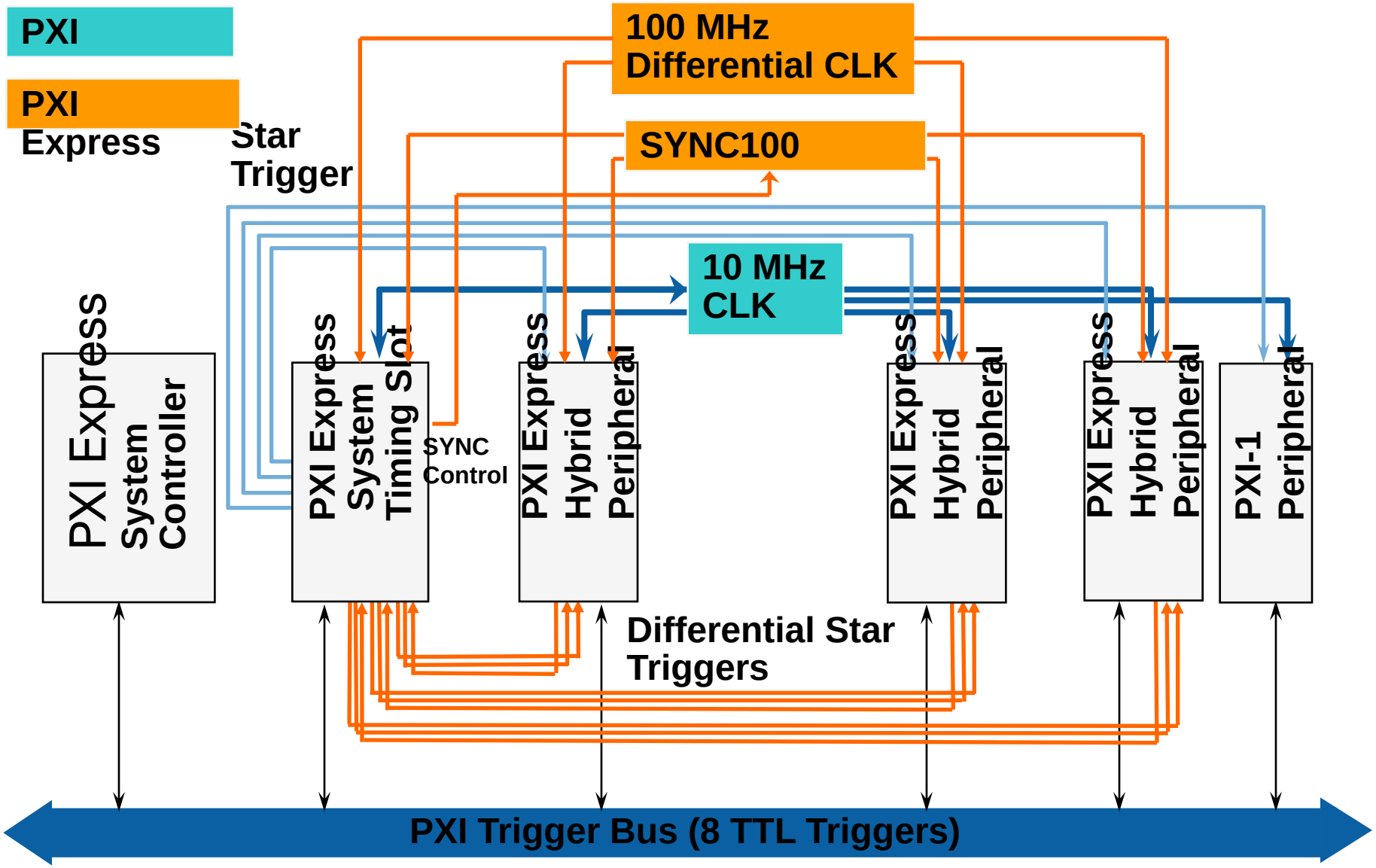
This is how NI-TClk does it but different schemes are also possible.

PXI Signal Routing



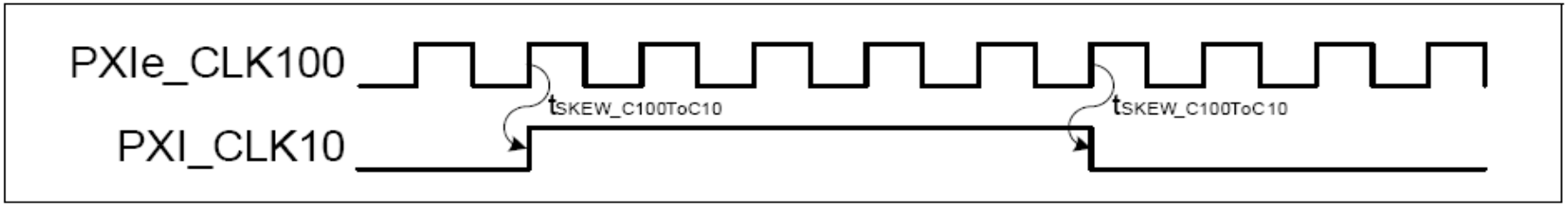
PXI Signal Routing

- PXI_CLK10
  - 100 ppm Accuracy
  - <1 ns slot to slot skew
  - Overwritten by BNC or timing card
- PXI Triggers (RTSI)
  - 8 line trigger bus between PXI slots
  - Used to share clocks, triggers, i.e.
  - Max Frequency 20MHz
- PXI Star Triggers
  - Direct one-way connection from Timing slot (2) to first 13 slots.
  - Trace length matched within 1 ns


PXI
PXI Express
Star Trigger
100 MHz Differential CLK
SYNC100
10 MHz CLK
PXI Express System Controller
PXI Express System Timing Slot
SYNC Control
PXI Express Hybrid Peripheral
PXI Express Hybrid Peripheral
PXI Express Hybrid Peripheral
PXI-1 Peripheral
Differential Star Triggers
PXI Trigger Bus (8 TTL Triggers)

Comparing PXIe_CLK100 and PXI_CLK10

- PXI_CLK10 preserves compatibility with PXI modules
- PXI_CLK10 is synchronous to PXIe_CLK100



- Specifications comparison:

	PXIe_CLK100	PXI_CLK10
Frequency	100 MHz	10 MHz
Logic Family	LVPECL, Diff	TTL, SE
Freq. Accuracy	±100 ppm or better	±100 ppm or better
Skew	≤ 200 ps	≤ 1 ns

Clock and trigger routing

- Some chassis have built in BNC connections to route external 10 MHz clock to/from backplane
  - Cannot route triggers
- Use PXI Timing and Sync Modules

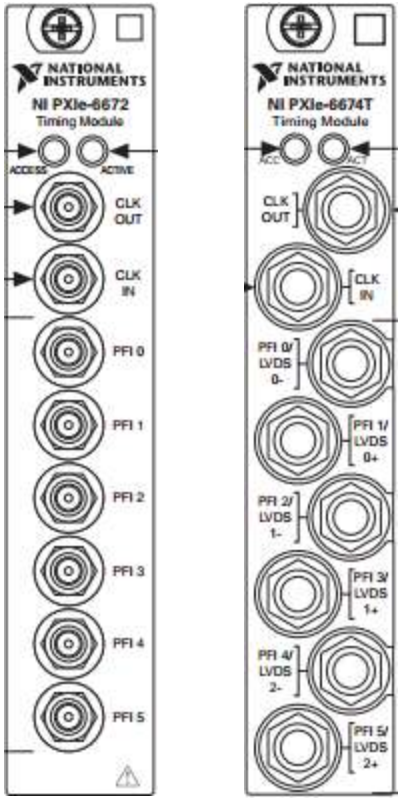
Timing Modules for Clocks

Each module adds a variety of high quality clock creation and routing, as well as trigger creation and routing.

- Useful for distributing clocks/triggers to multiple chassis/instruments
- DDS Clock generation
  - DC to 105MHz
  - Resolution <1.1uHz
- Provide high-quality, stable clock source
  - Better than PXI_CLK10/CLK100
    - VCXO – 100ppm
    - TCXO - 1ppm
    - OCXO – 50 ppb

PXIe-6672 and PXIe-6674T

- Function as master or slave
  - PXI_Clk10 in & out
  - 6 PFI lines for triggers
- 6672 has TCXO and DC to 105 MHz DDS
- 6674T has OCXO and DC to 1 GHz DDS



PXIe-6683 and PXI-6683H

- Time-based synchronization
- Supports disciplining the onboard TCXO (1 ppm) to any sync source
- Onboard high-stability TCXO (1 ppm)
- Can be used as a PXI slot 2 star trigger controller (not available on PXI-6683H)

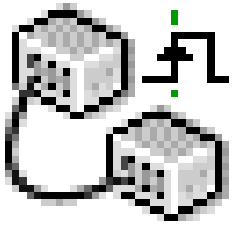
PXI-6682 and PXIe-6682H

- Cannot override the PXI_CLK10 backplane reference
- 6682H common complement with other timing modules for additional features

NI-Sync Software Driver

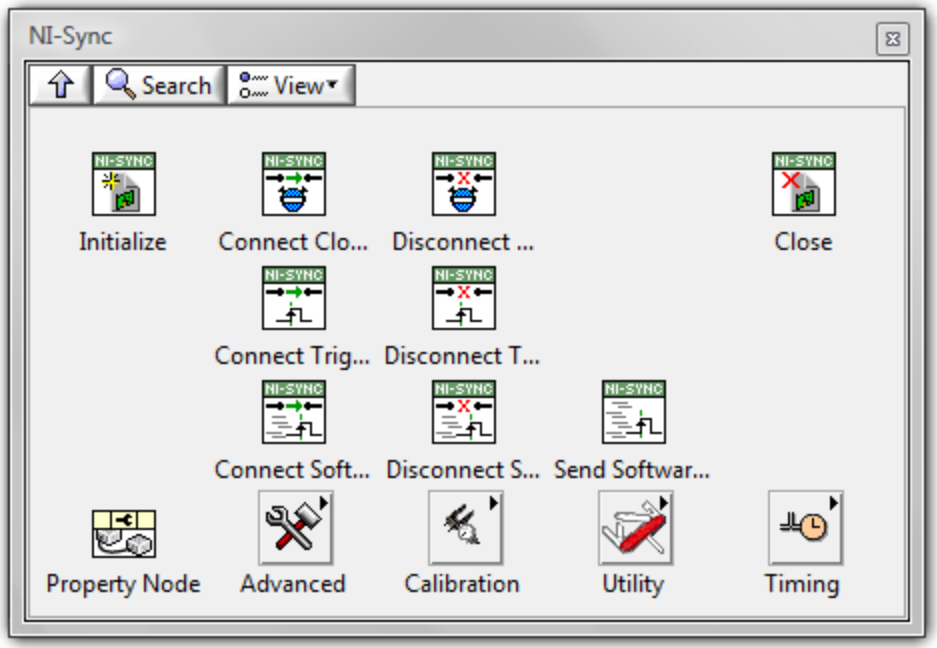
Two part API

- Signal Based Synchronization
  - Clock and Trigger routing
  - DDS Configuration
- Time Based Synchronization (PXI-6682)
  - GPS, IRIG-B & IEEE-1588
  - Time stamping

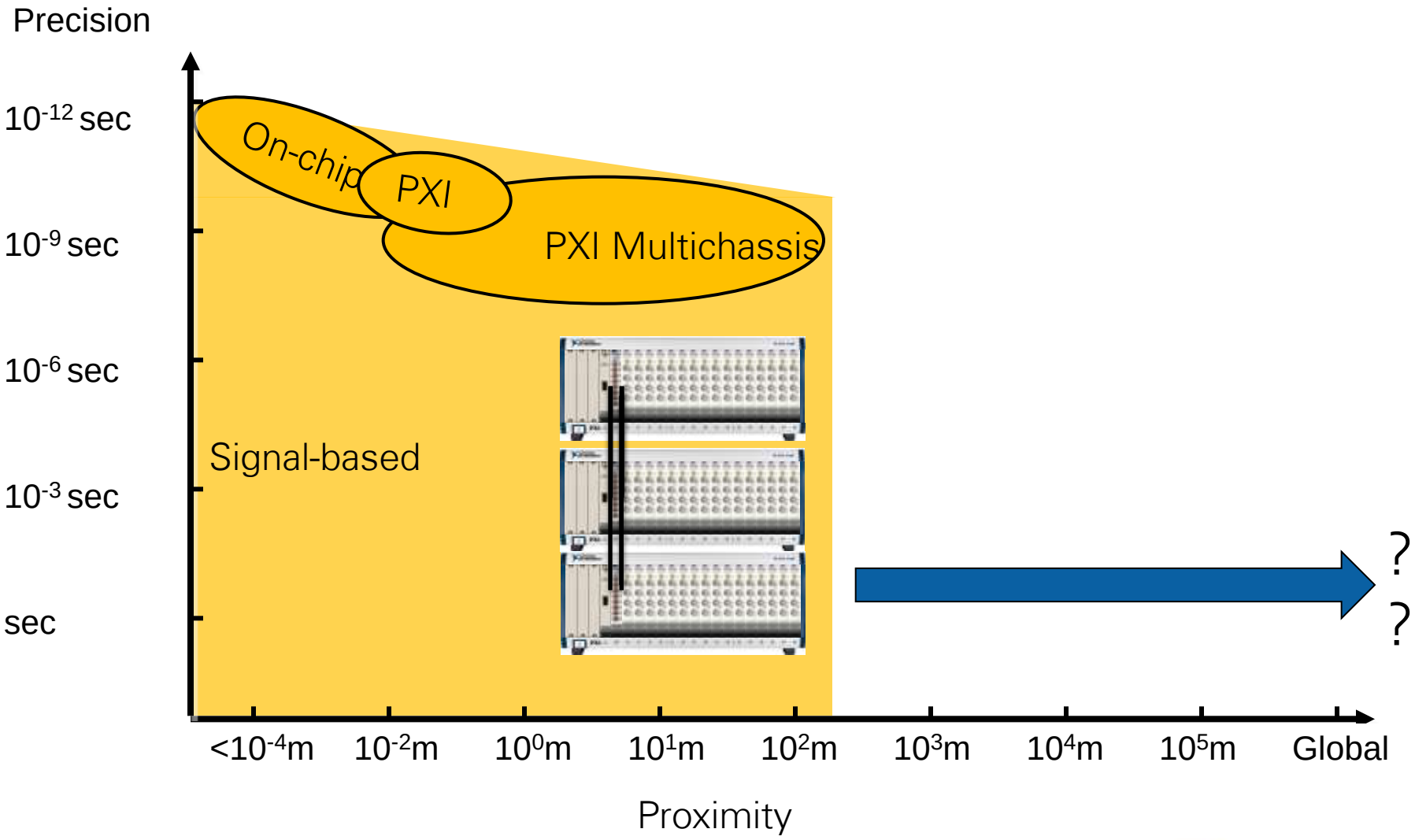


NI-Sync Software Driver

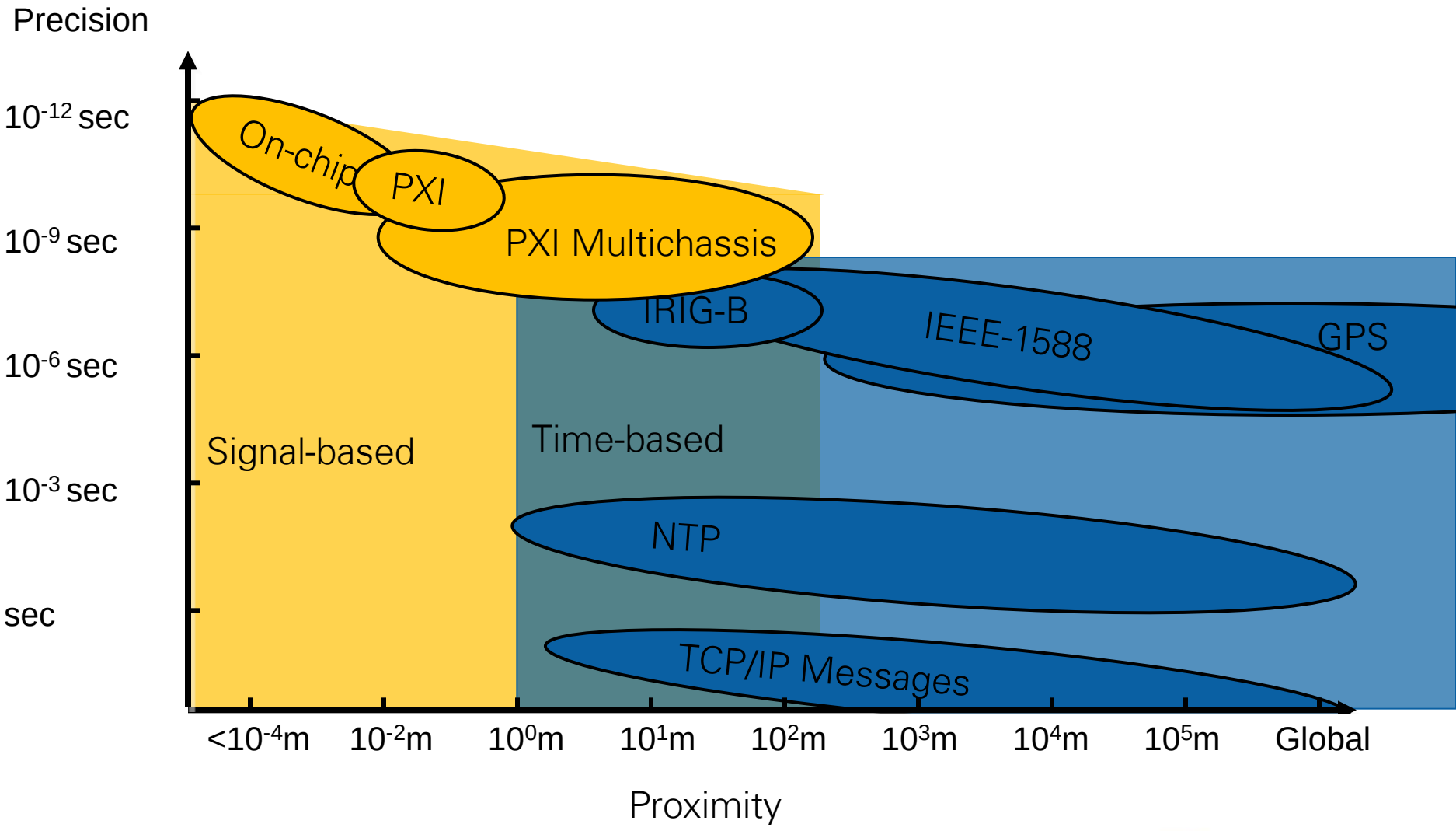
- Session Based
- Connect / Disconnect Signals
- Property node
- Advanced



Previous Synchronization Technologies



Current Synchronization Technologies



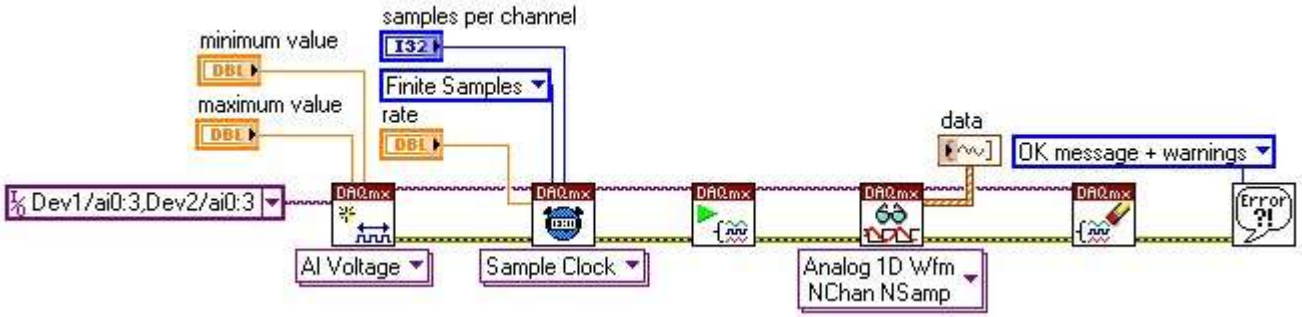
Signal-Based vs Time-Based Synchronization

- Signal-Based
  - Clocks and Triggers physically connected between systems
  - Highest-precision synchronization
- Time-Based
  - System components have a common reference of what time it is
  - Events, Triggers and Clocks can be generated based on this time
  - Signals can be timestamped and correlated in post-processing
  - Eg. Multiple Analog inputs start acquisition at 12:00 p.m. and every µs thereafter

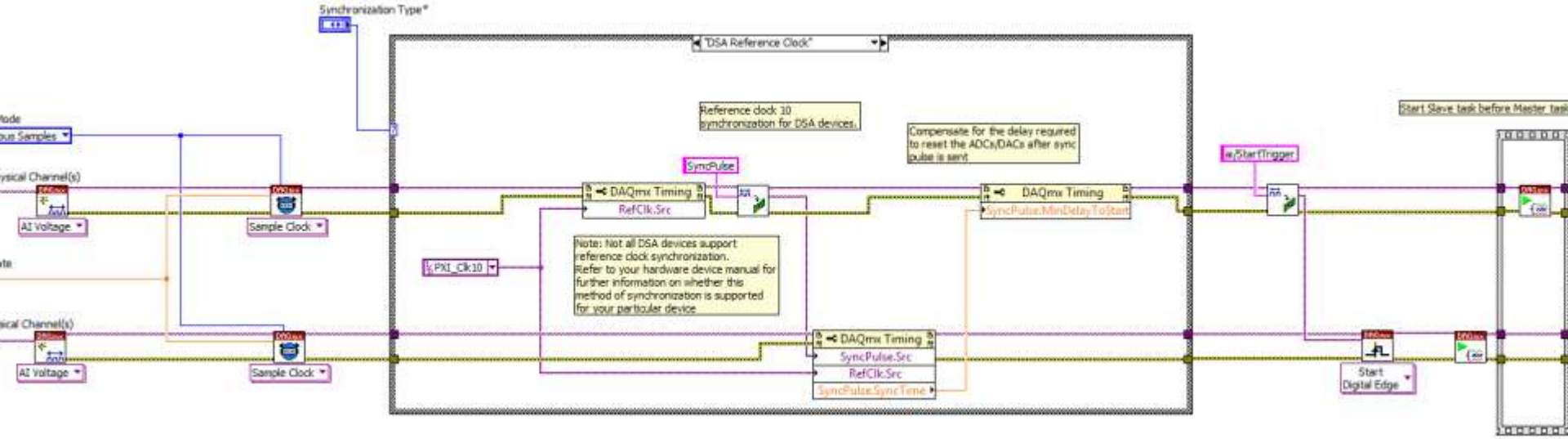
DSA Synchronization

DSA AI Synchronization in NI-DAQmx

- Can have multiple DSA devices in one DAQmx task
- NI-DAQmx automatically synchronizes the devices
  - Share or Lock Sample Clock Timebase
  - Sent Sync Pulse
  - Sent start Trigger

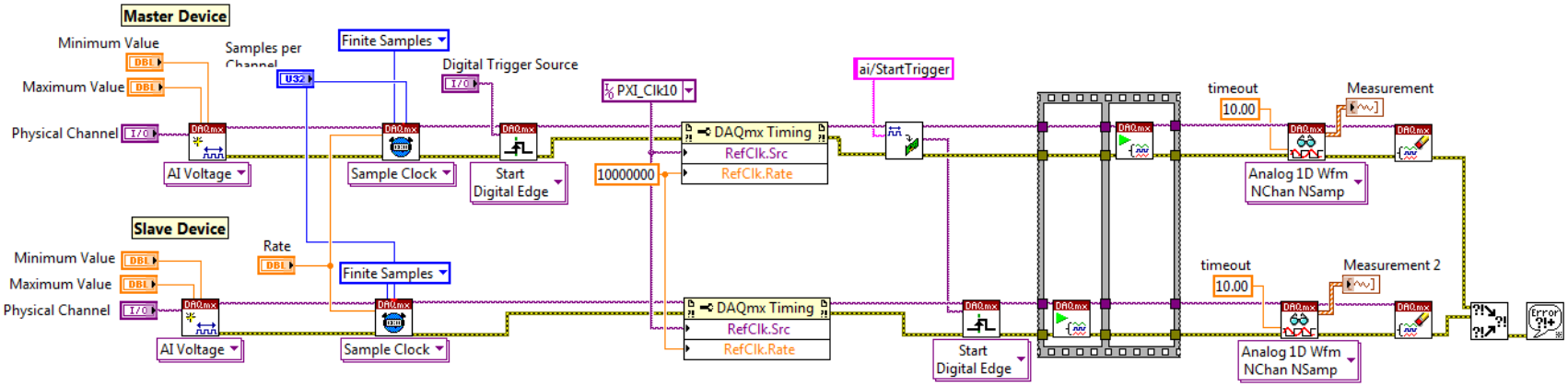


DSA Synchronization manually



NATIONAL INSTRUMENTS

DAQ Synchronization



Example of PXI M Series Synchronization

More examples in the Example Finder DAQmx -> Synchronization -> Multi De

NI Modular Instruments Synchronization

NI-TClk

- Synchronization and Memory Core (SMC)
  - High Speed Memory Transfer Core
  - Synchronization Core
  - Shared architecture among all High speed Instruments
    - Generators, Digitizers and High Speed Digital I/O

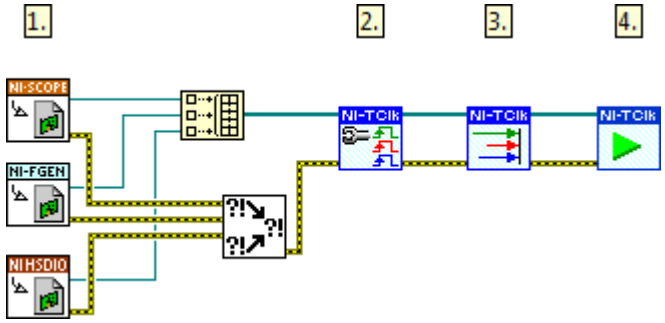
NI Modular Instruments Synchronization

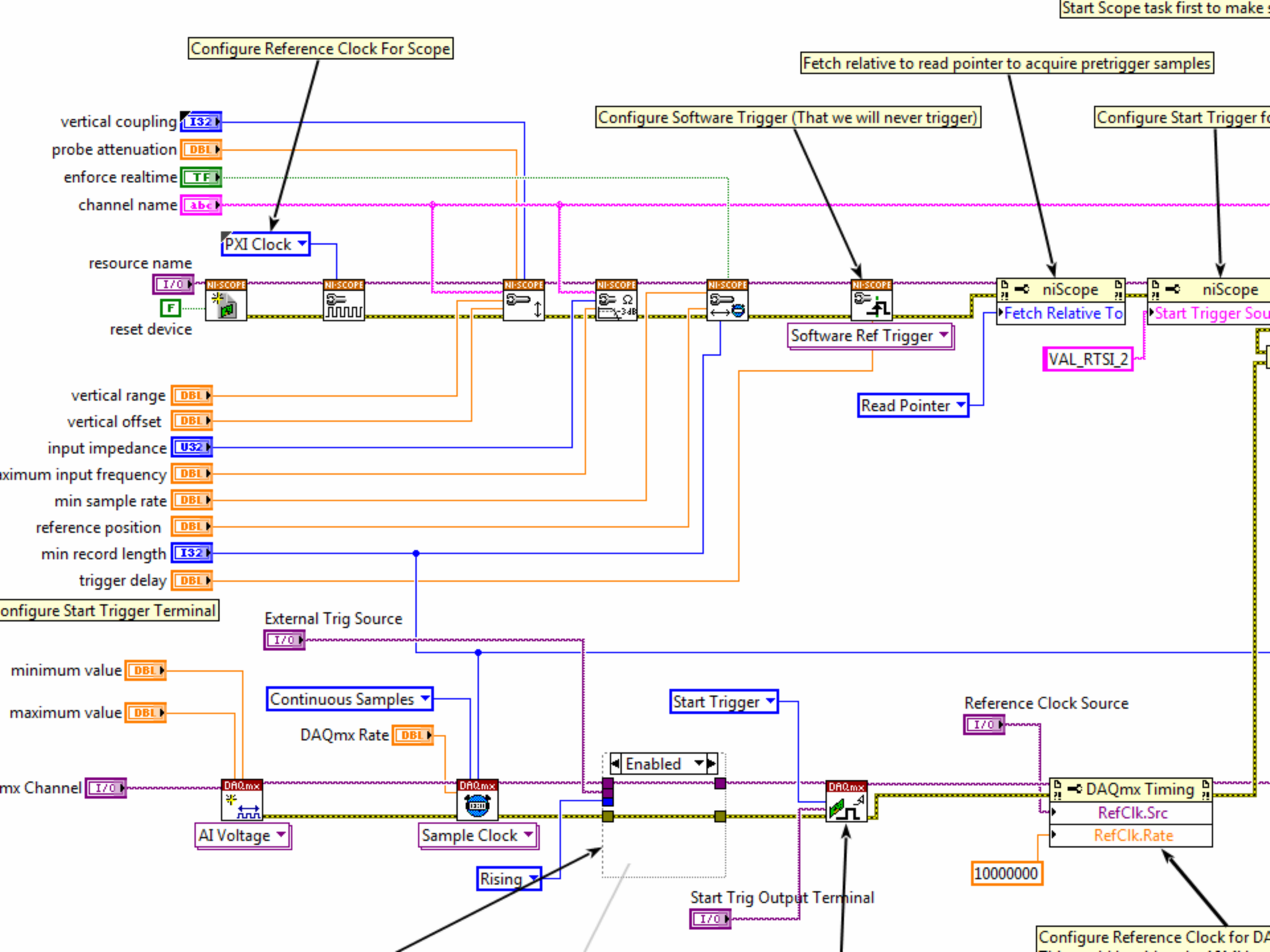
- NI-TClk (Trigger Clock)
  - Reference Clock Synchronization with Start Trigger Synchronization.
  - Pico Second Level Synchronization
  - High Level API.
  - Supported Instrument Drivers
    - ✓ NI-SCOPE
    - ✓ NI-FGEN
    - ✓ NI-HSDIO

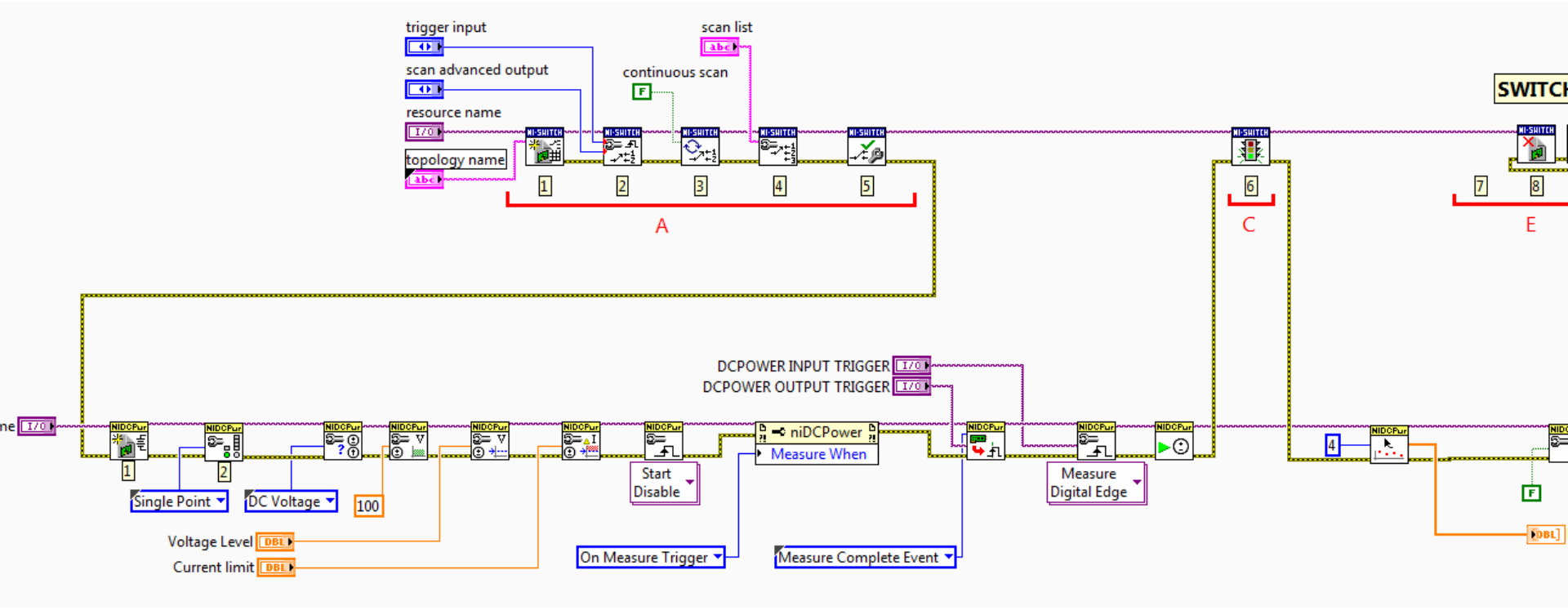
NI Modular Instruments Synchronization

NI-TClk Programming

1. Get Session References for all devices.
2. Route Signals
3. Synchronize
4. Initiate




Start Scope task first to make
Configure Reference Clock For Scope
Fetch relative to read pointer to acquire pretrigger samples
Configure Software Trigger (That we will never trigger)
Configure Start Trigger fo
vertical coupling
probe attenuation
enforce realtime
channel name
PXI Clock
resource name
reset device
niScope
Fetch Relative To
Start Trigger Sou
Software Ref Trigger
VAL_RTSI_2
Read Pointer
vertical range
vertical offset
input impedance
ximum input frequency
min sample rate
reference position
min record length
trigger delay
onfigure Start Trigger Terminal
External Trig Source
minimum value
maximum value
Continuous Samples
DAQmx Rate
Start Trigger
Reference Clock Source
mx Channel
Enabled
DAQmx Timing
RefClk.Src
RefClk.Rate
AI Voltage
Sample Clock
Rising
10000000
Start Trig Output Terminal
Configure Reference Clock for DA


trigger input
scan advanced output
resource name
topology name
scan list
continuous scan
SWITCH
A
C
E
DCPOWER INPUT TRIGGER
DCPOWER OUTPUT TRIGGER
niDCPower
Measure When
Start
Disable
Measure
Digital Edge
Single Point
DC Voltage
100
Voltage Level
Current limit
On Measure Trigger
Measure Complete Event