Hardware-in-the-loop Ultrasonic Flow sens Emulation for Siemens Flow Instrument

Prevas have used NI's FPGA technology in our test systems since it was released.

This presentation will contain information how Prevas solved a specific customer HIL problem using NI hardware and software related to FPGA

Tuesday

Nov 2015

17

Prevas

NI Days
Copenhagen
Stockholm

Per Finnstam / Henrik Thomsen

- Founded in 1985
- Nordic leader in Embedded Systems
- Nordic leader within MES, EMI and Automation
- 650+ employees – Sweden, Norway, Denmark and India.
- 1000+ freelancers across Scandinavia in catalogue
- Listed on NASDAQ OMX
- ISO 9001:2008 Certification

Our Value Proposition

We add value across the product life cycle by improving our customers

- Innovation pace
- Time to market
- Productivity
- Quality

We deliver Excellence in Technology through

- Consulting services
- System delivery
- Outsourcing
- Products and Platforms

Innovation | **Development** | **Manufacturing** | **Support & Sustaining**

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Prevas Test Systems

- **Production test systems**
  - Electronics production test
  - Product development test
- **Development (R&D) test systems**
  - Hardware in the loop (HIL)
  - Measurement systems
- **Laboratory Systems**
  - Pre-made data acquisition systems
  - Specialized instruments based on National Instruments products
- **TSD, Prevas Centre of Excellence**

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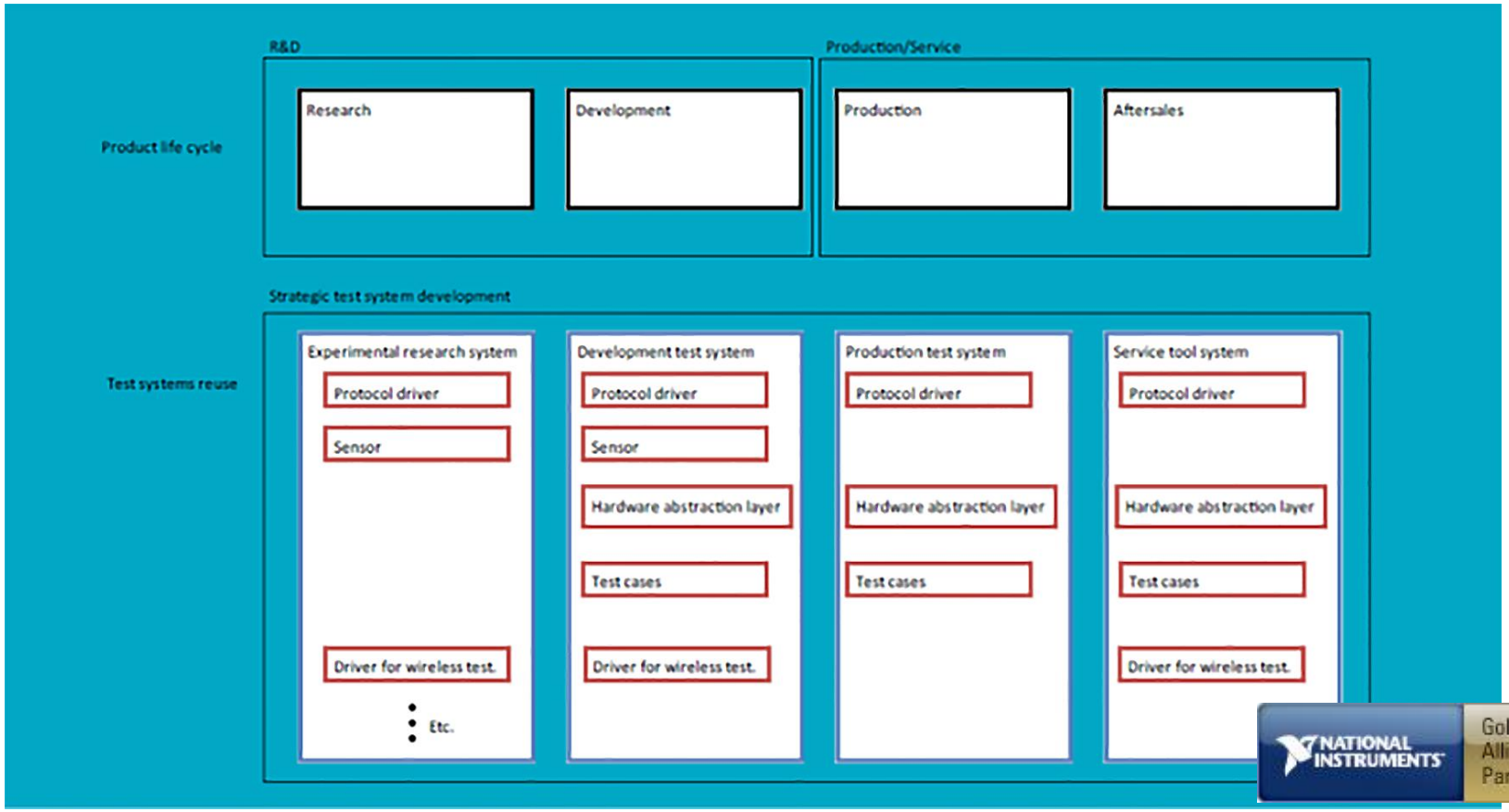
Prevas Test Systems

Working across the organisation



Technical agenda

Technical agenda

- What is a HIL?

Technical agenda

- What is a HIL?
- What is a FPGA?

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- What is a HIL?
- What is a FPGA?
- NI HW and LabVIEW FPGA
  - NI FPGA Targets
  - PXI and flexRIO
  - flexRIO adapters

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  - HIL Test System description and implementation
  - NI HW used in HIL
  - Challanges with sub-nanosecond time resolution
  - LabVIEW programming
  - Final implementation

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- Lesson learned

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What is HIL?

- HIL stands for “Hardware in the loop”

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- HIL system gives real world response to stimuli from DUT

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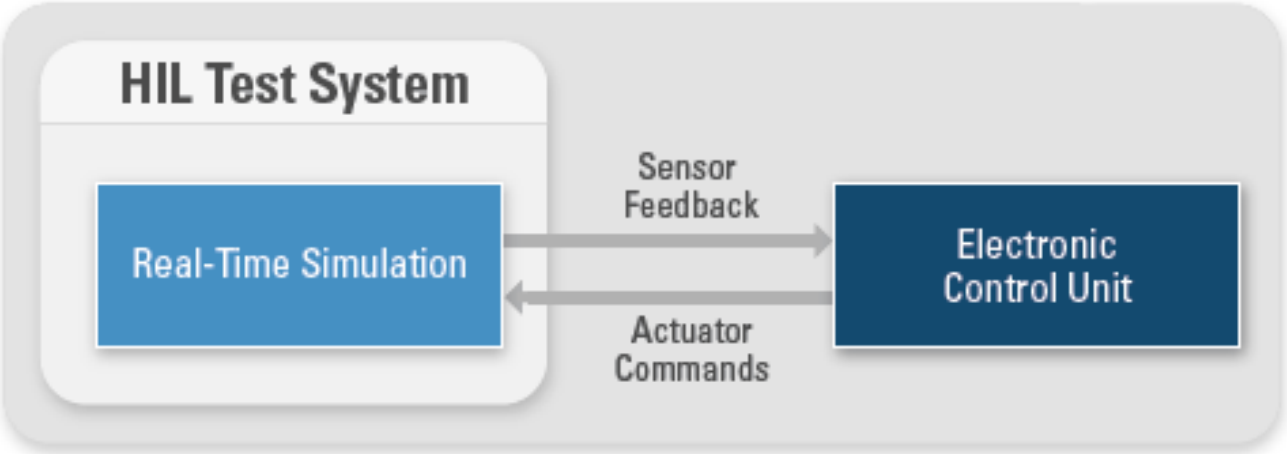
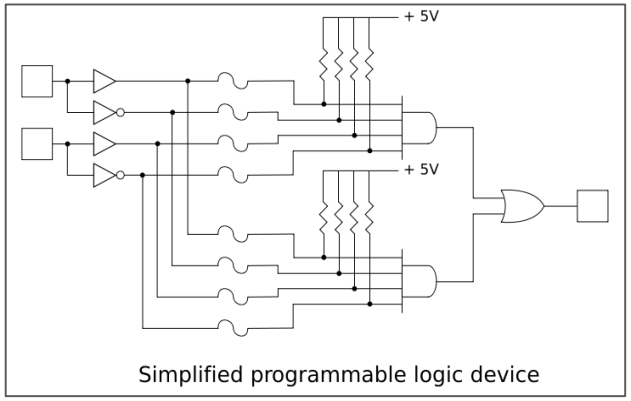
Example:

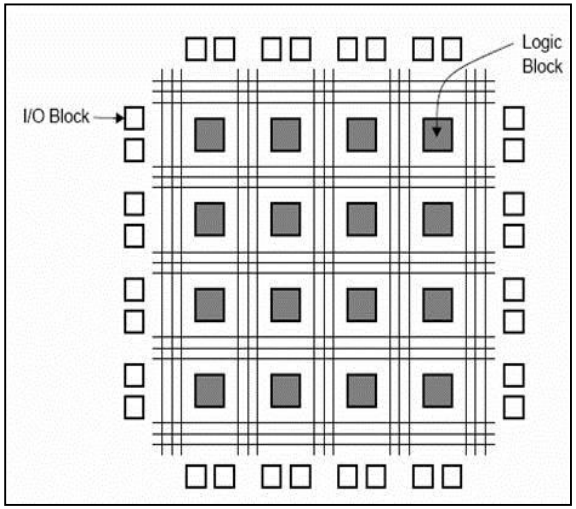


What is an FPGA ?

- Field-Programmable Gate Array
- Gate Array – Interconnect is done once with a specified function
- FPGA – Field-programmable gates and interconnects



Gate Array



FPGA

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Some National Instruments FPGA Targets

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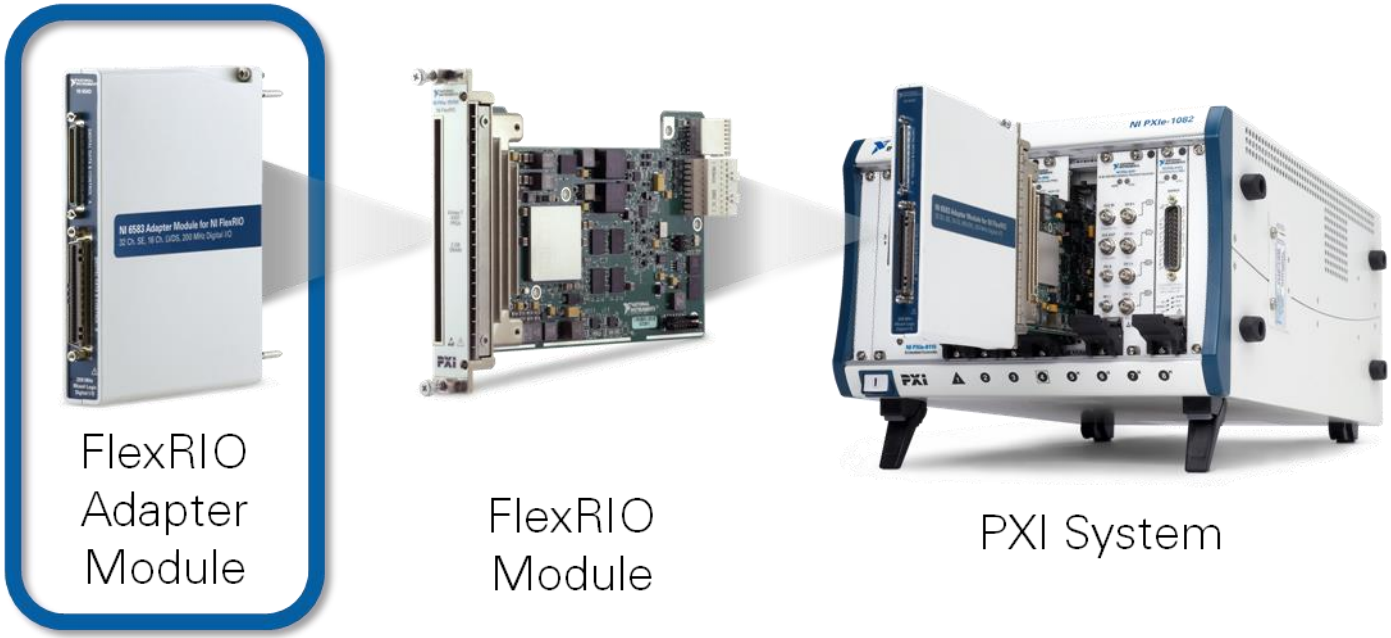
PXI and flexRIO systems



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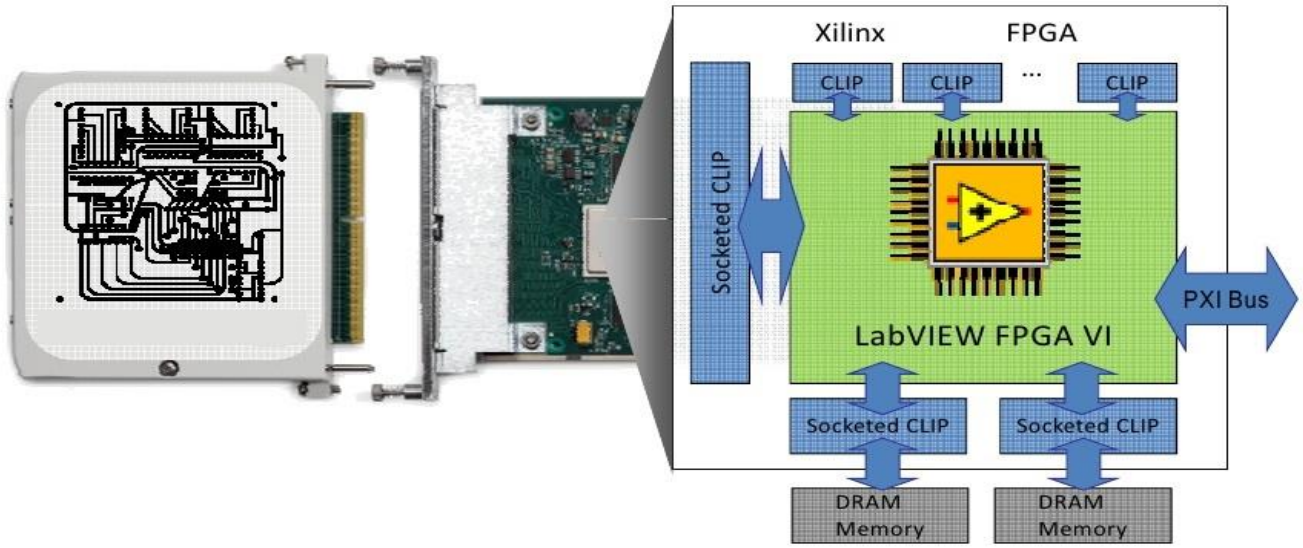
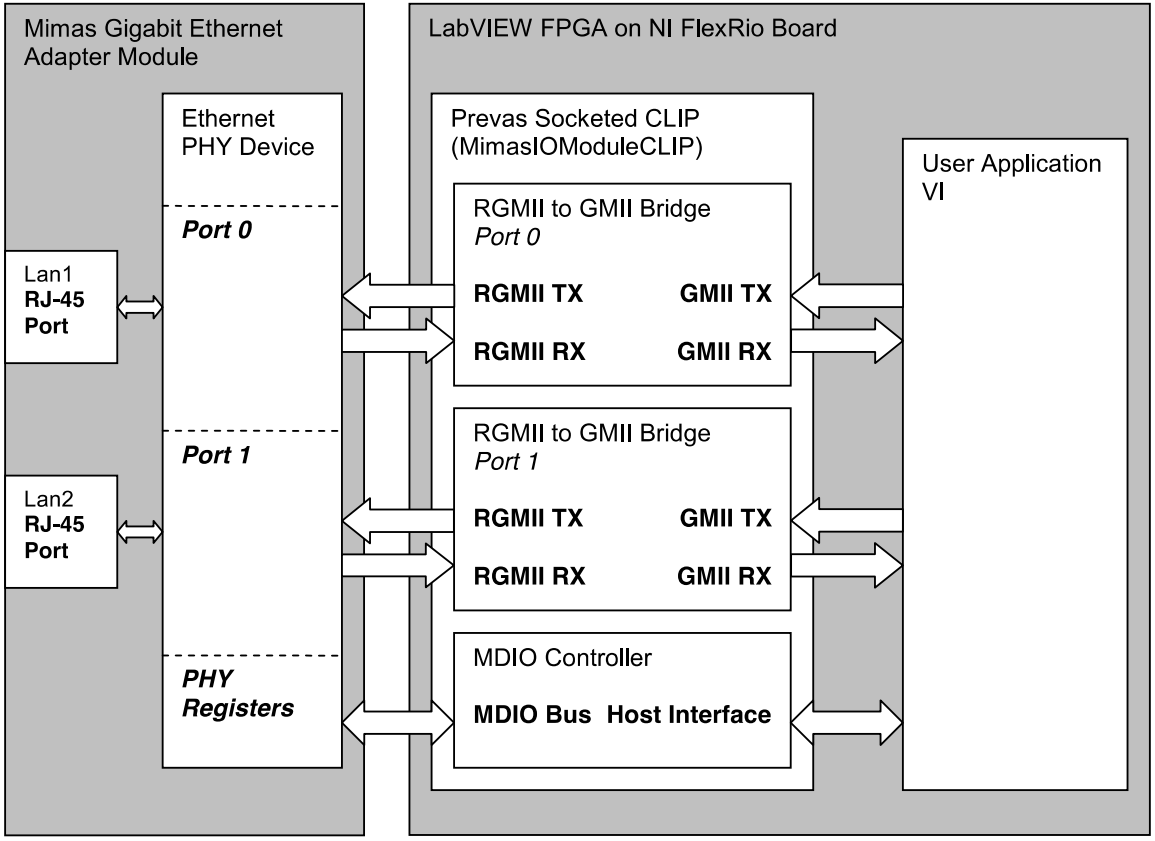
Adapters to flexRIO boards in general



Prevas FlexRIO Adapter

2 x 1GBit Ethernet ports



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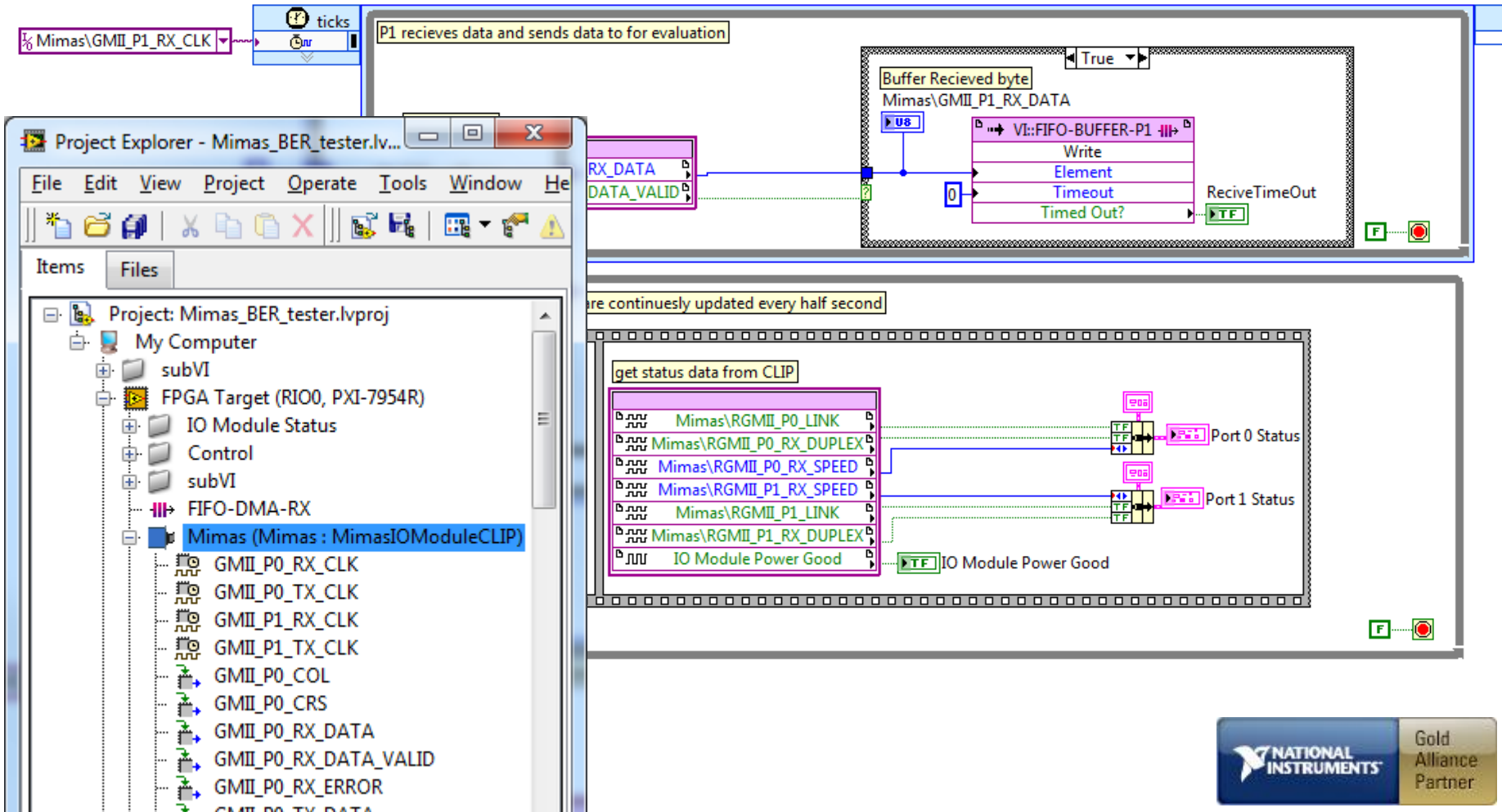
Application Example, Gigabit



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HIL Simulator for Siemens Flow Instruments

- Located in Sønderborg, Denmark
- Developing, producing and marketing flow measurement instruments and sensor infrastructure
- Different sensor principles: Electromagnetic, Coriolis, Ultrasonic and others

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- Used in all sorts of environments - Main applications include the measurement of volume flow within:
  - General industrial purpose
  - Petrochemical and chemical industries
  - Power engineering
  - Water and waste water.

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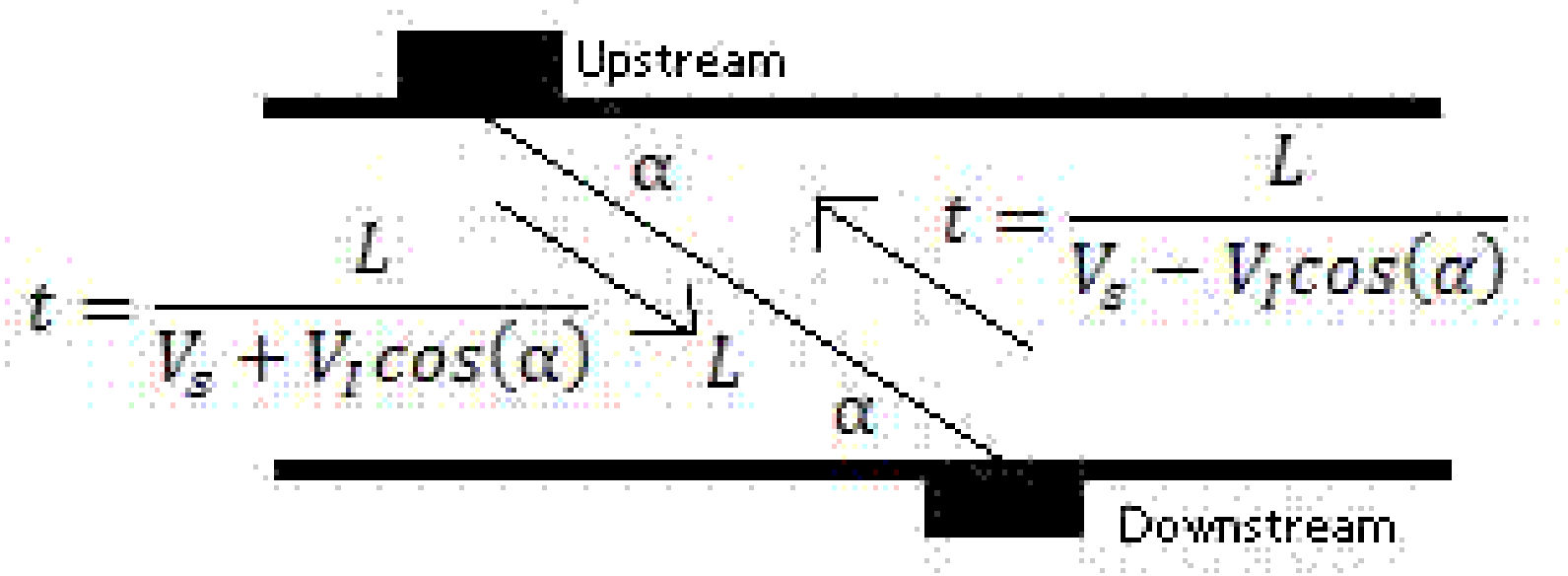
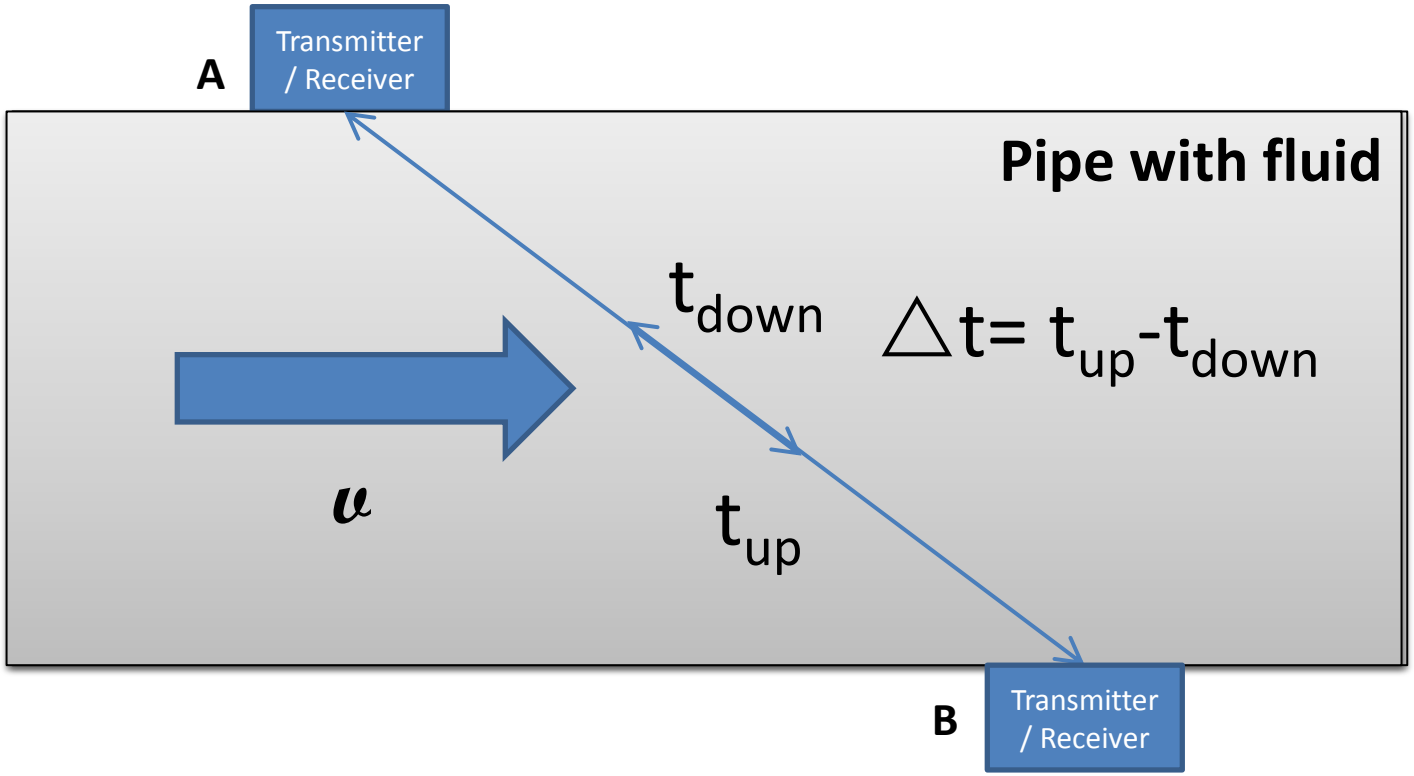
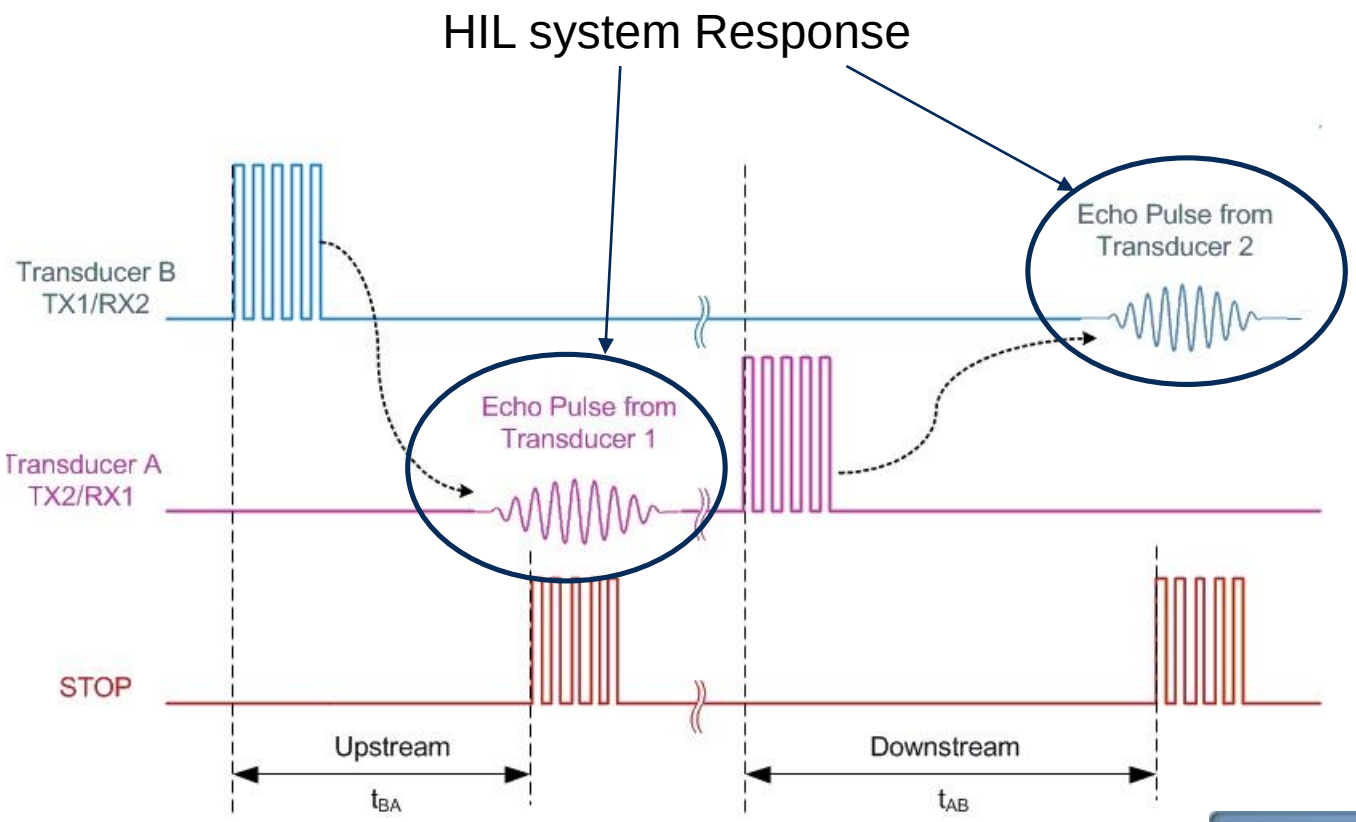
Transit time/time of flight method



Example: Ultrasonic flow sensor schematic picture



Schematic picture of functionality



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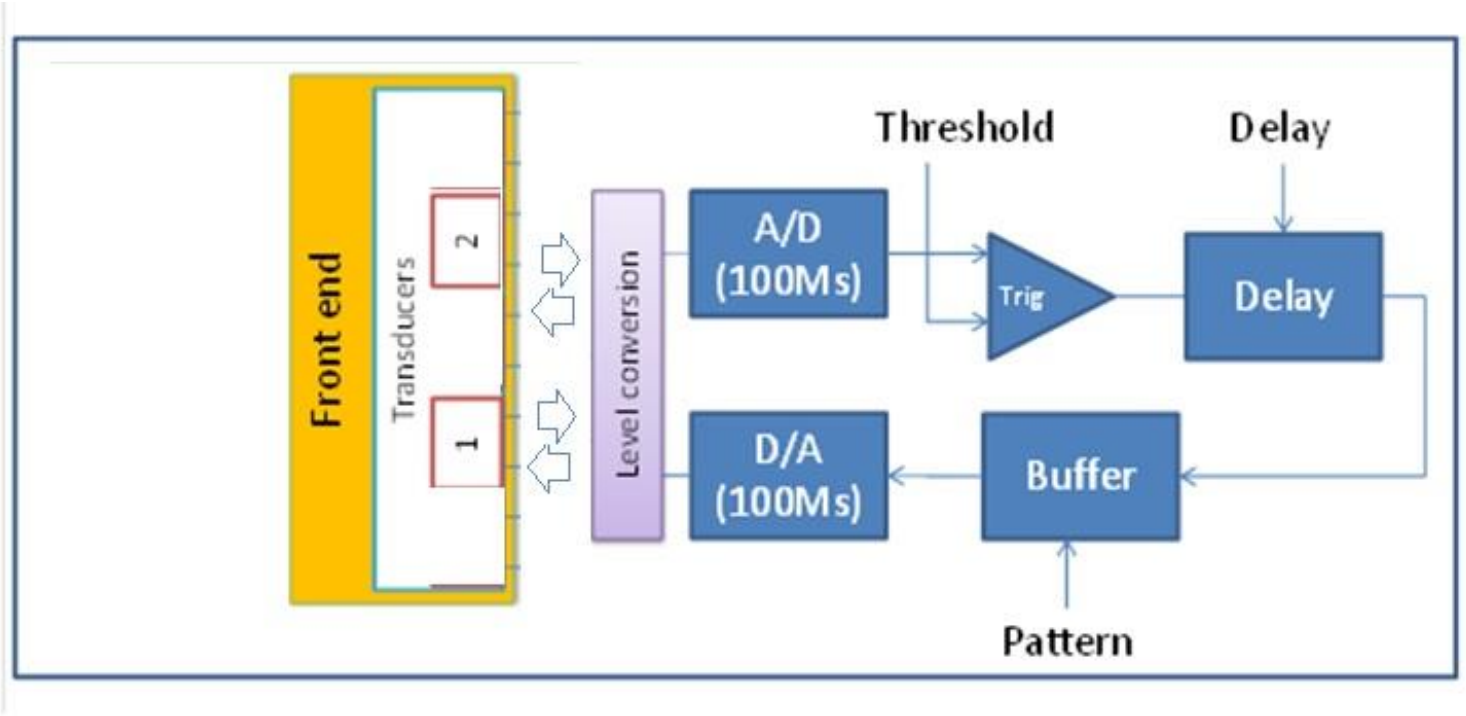
HIL system Block diagram



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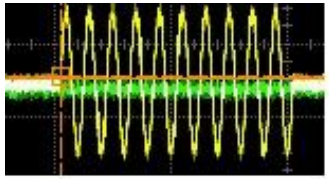

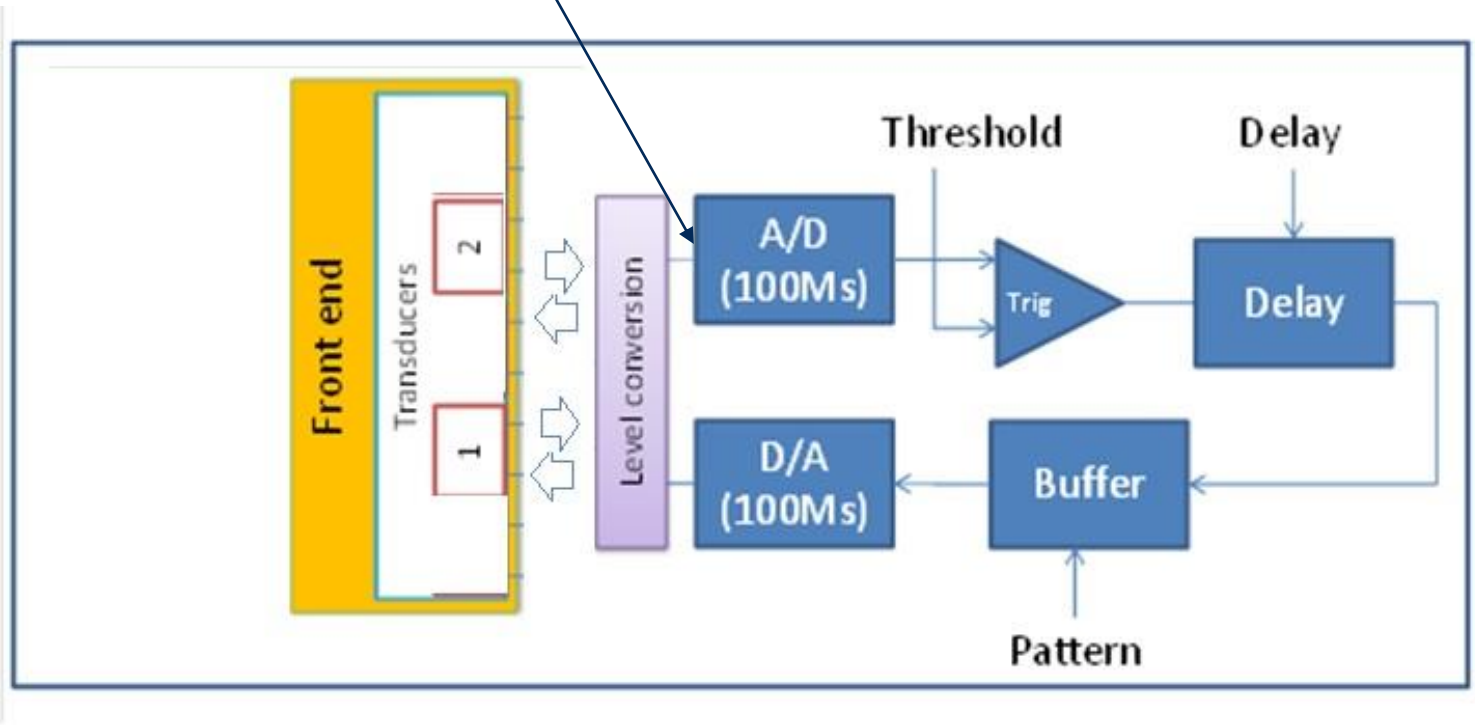

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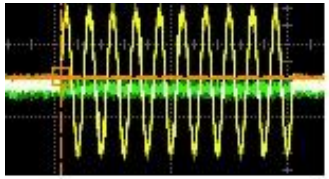
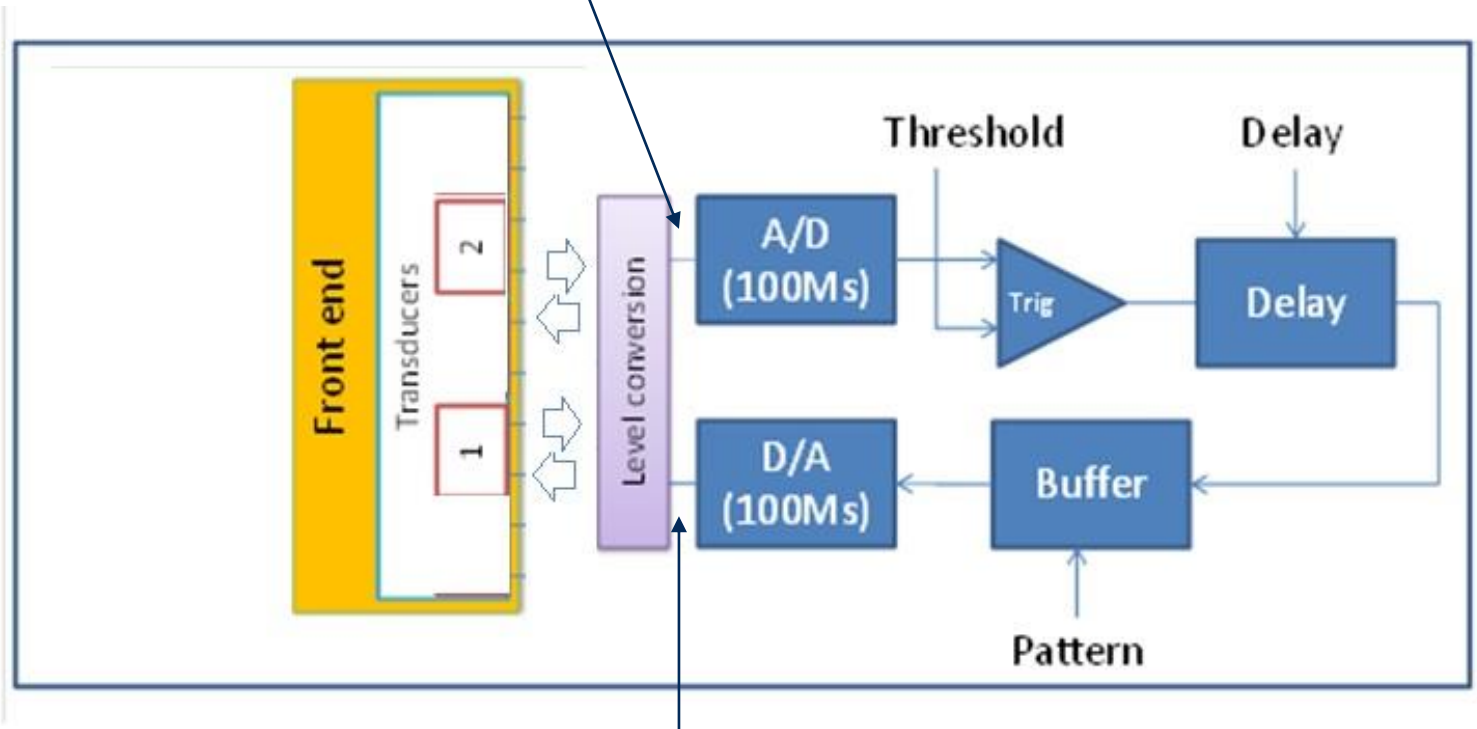
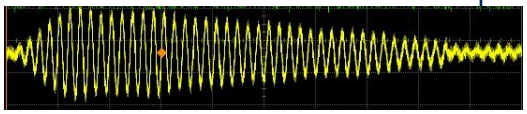
HIL system Block diagram







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Implmentation in NI HW

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Selected FPGA, FlexRIO

First generation Flex RIO

- Virtex-5
- Access to 132 FPGA pins
  - LVDS pairs up to 1 Gb/s
- 128 MB onboard memory
- 17,000 slices, 4kbit blockRAM

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Selected ADC flexRIO adapter NI 5781

- Dual 100 MS/s, 14-bit inputs
- Dual 100 MS/s, 16-bit outputs
- 2 Vpp differential I/O (1 Vpp single-ended capable)
- 40 MHz bandwidth (-3 dB)
- External clock input and output

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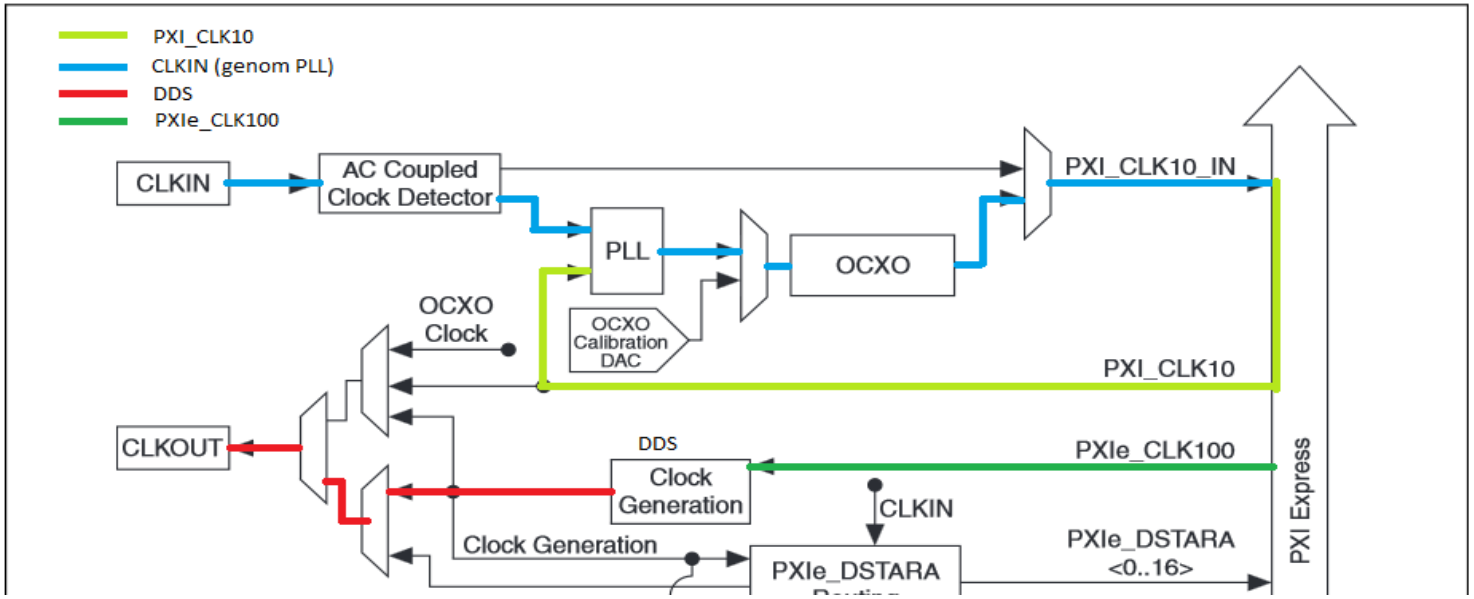
Clock module PXIe NI6674T

- Onboard routing of internal and external clock and trigger signals
- Onboard high-stability 10 MHz OCXO (50 ppb/year)
- High resolution DDS clock generation, 0.3 Hz to 1 GHz
- Advanced trigger and timing routing with PXIe-DStar differential star trigger lines
- Discipline 10 MHz to GPS, IEEE 1588, or IRIG, when coupled with the NI PXI-6683H



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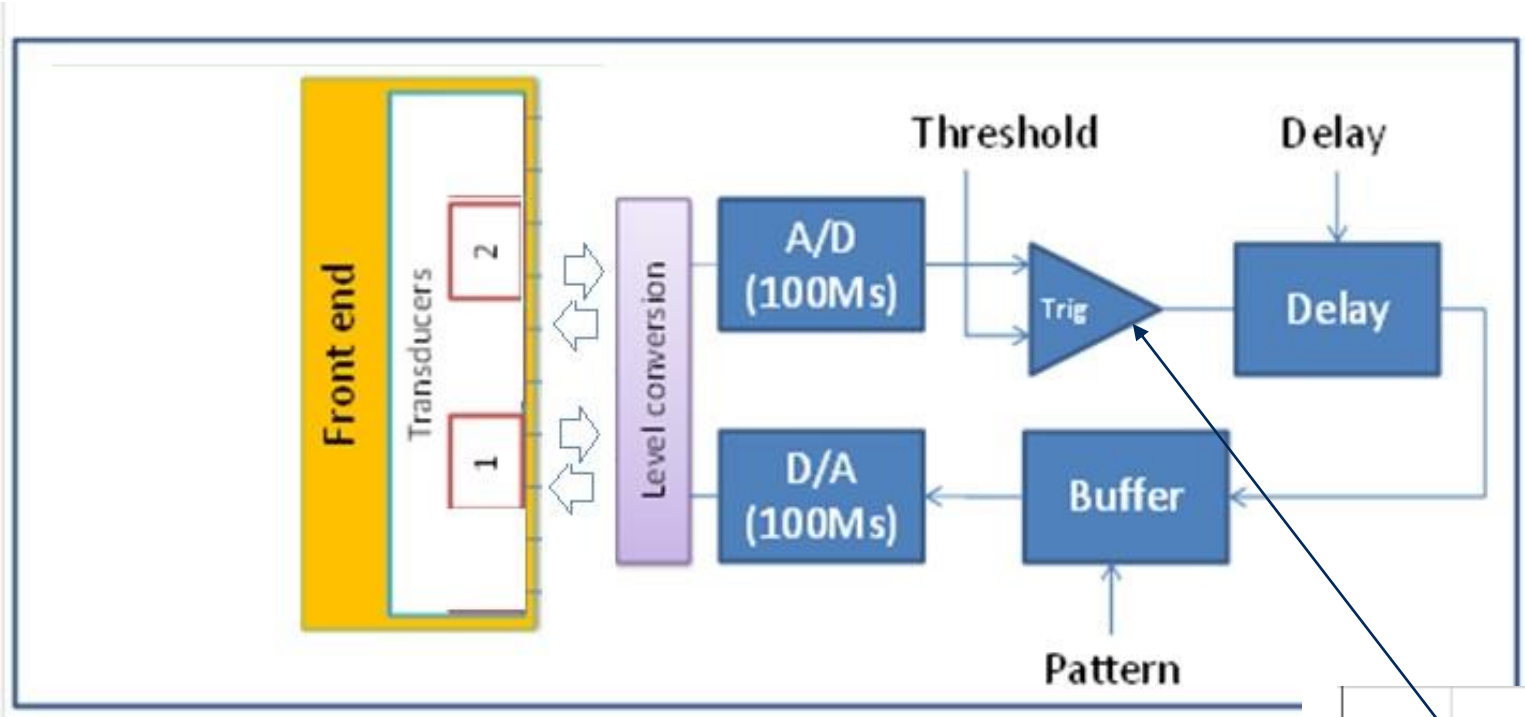
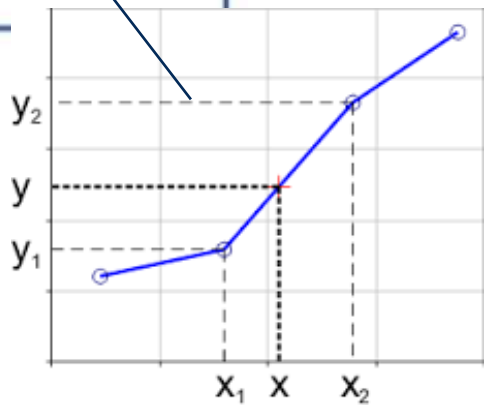
Challanges with sub-nanosecond time resolution

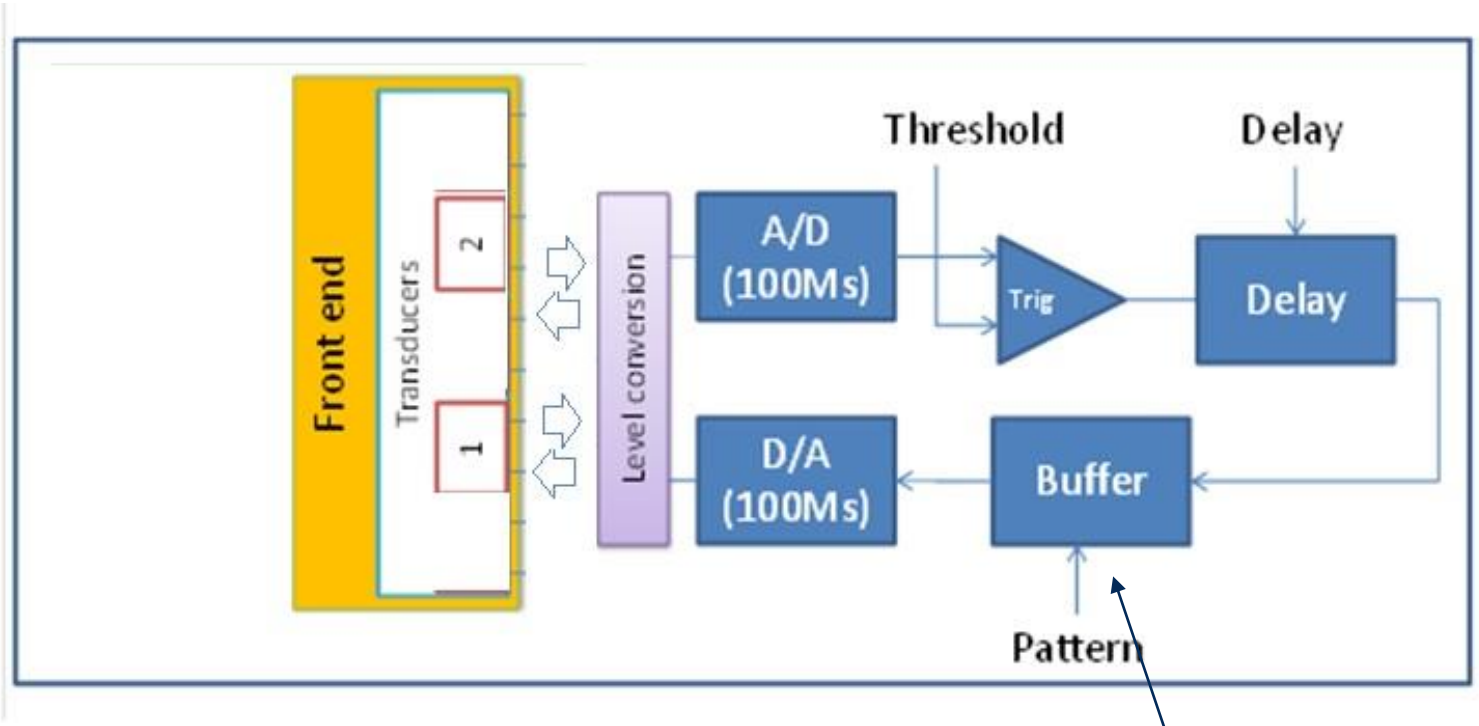
- Trigger
- Memmory considerations
- Measuring with sub nano accuracy

Challange One: TRIG Intepolation





Challenge Two :Memmory



Memmory considerations

$$(Typical)Mem_{size} = ca\ 1{,}2\ Mbyte$$

- 1.2 Mbyte too big for flexRIO 7954R to be implemented in FPGA in dedicated block RAM or in flipflops

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  - Size data correct and use optoimal clock
  - Pipeline DRAM read request
  - Sequential Access (One assumption DRAM designers make is that data will be accessed sequentially in ascending order, that is, you read the data in address 0x1 after you read the data in address 0x0) is not possible in our case

Solution to memory considerations

- Mem 1: Holds a sinus wave with contant amplitude(sub nano resolution)

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- Mem 2: Holds the envelope for the response (a scaling factor for each sample to output with 10ns resolution)

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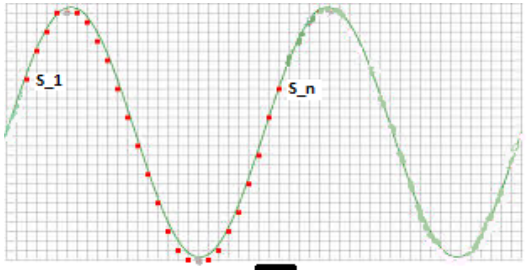
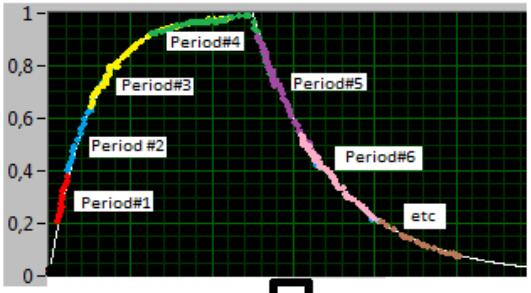
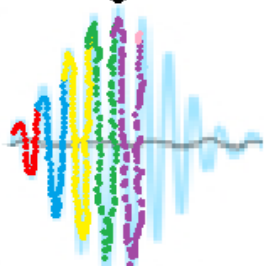


Mem 1: Period Data



Mem 2: Scaling points



OUTPUT = Mem 1 x Mem2

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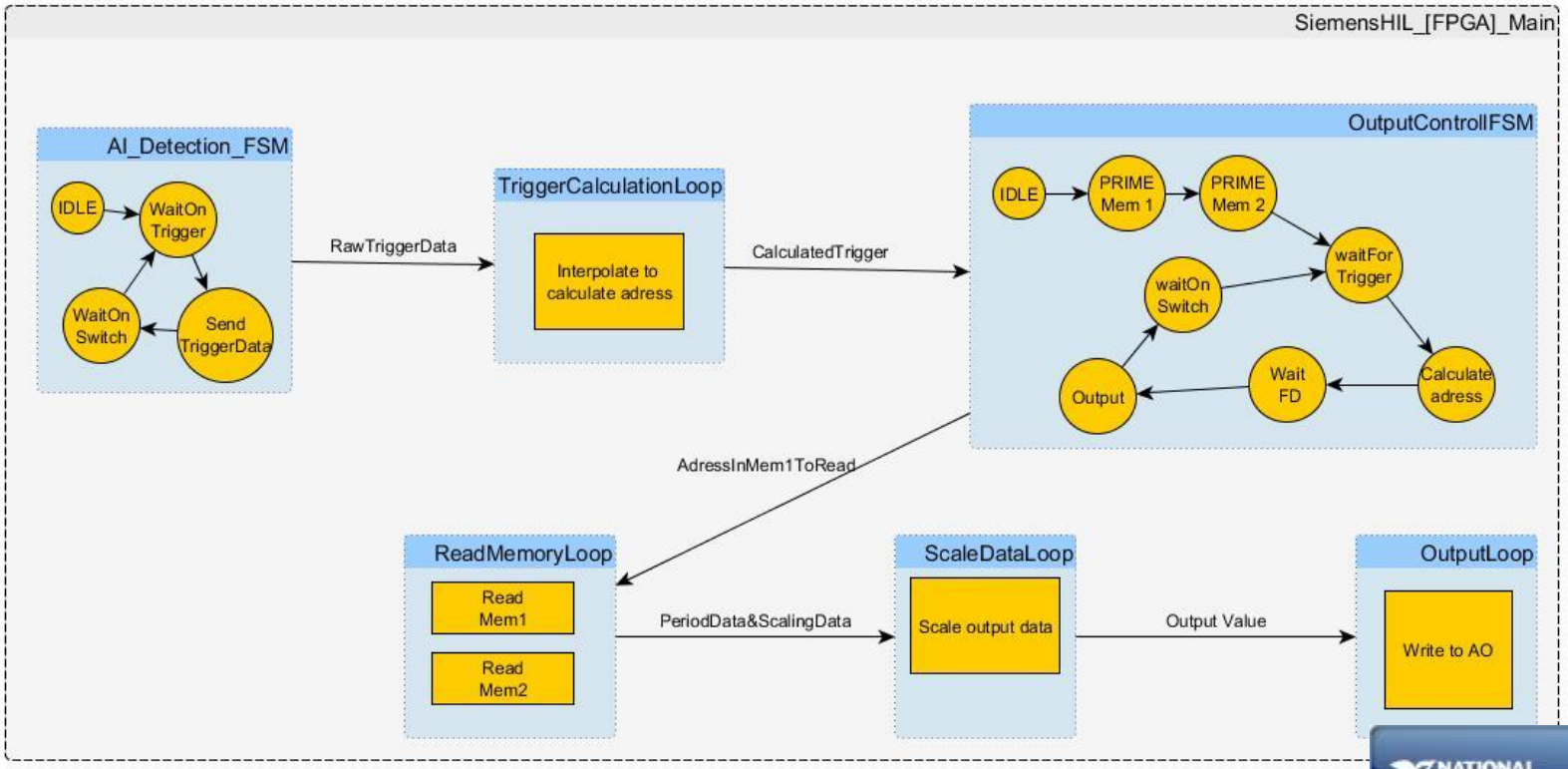
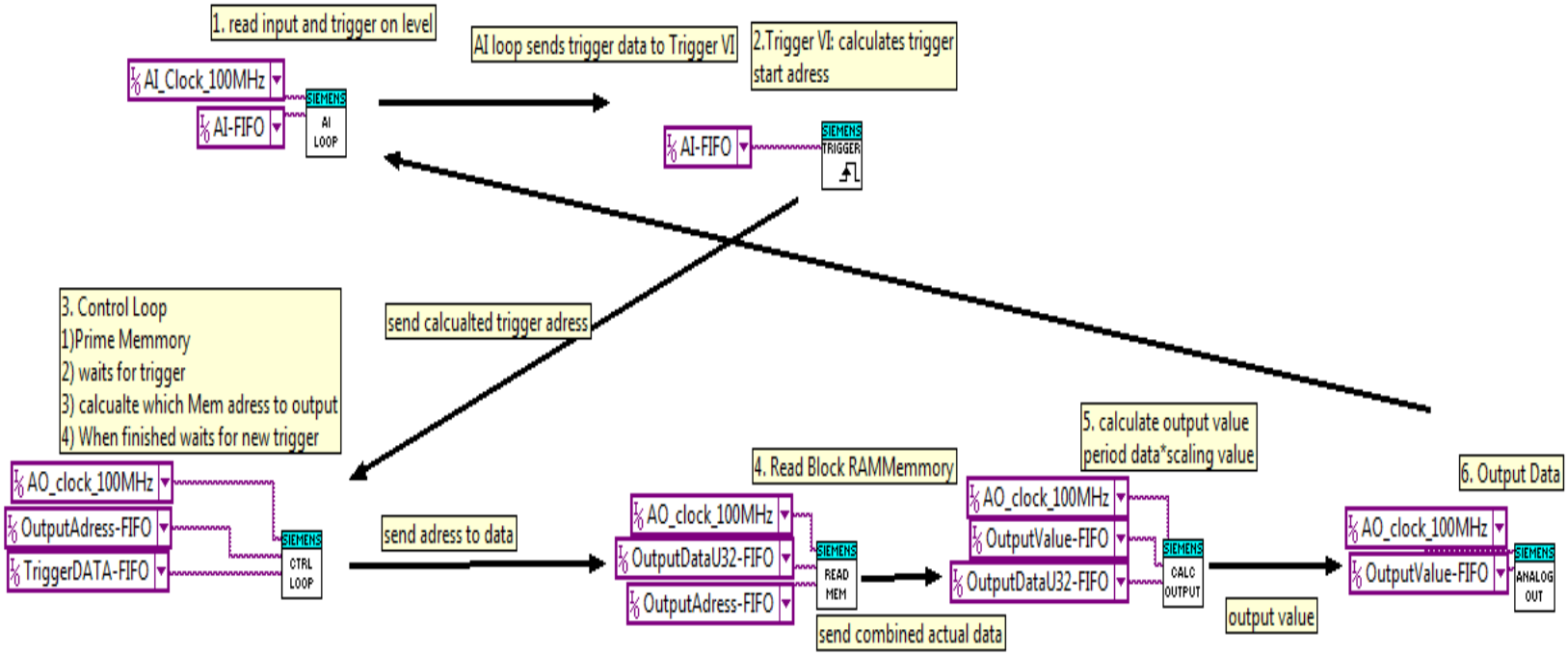
Example: Ultrasonic flow sensor simulator – LabView FPGA programming schematic picture



Example: Ultrasonic flow sensor simulator LabVIEW program main



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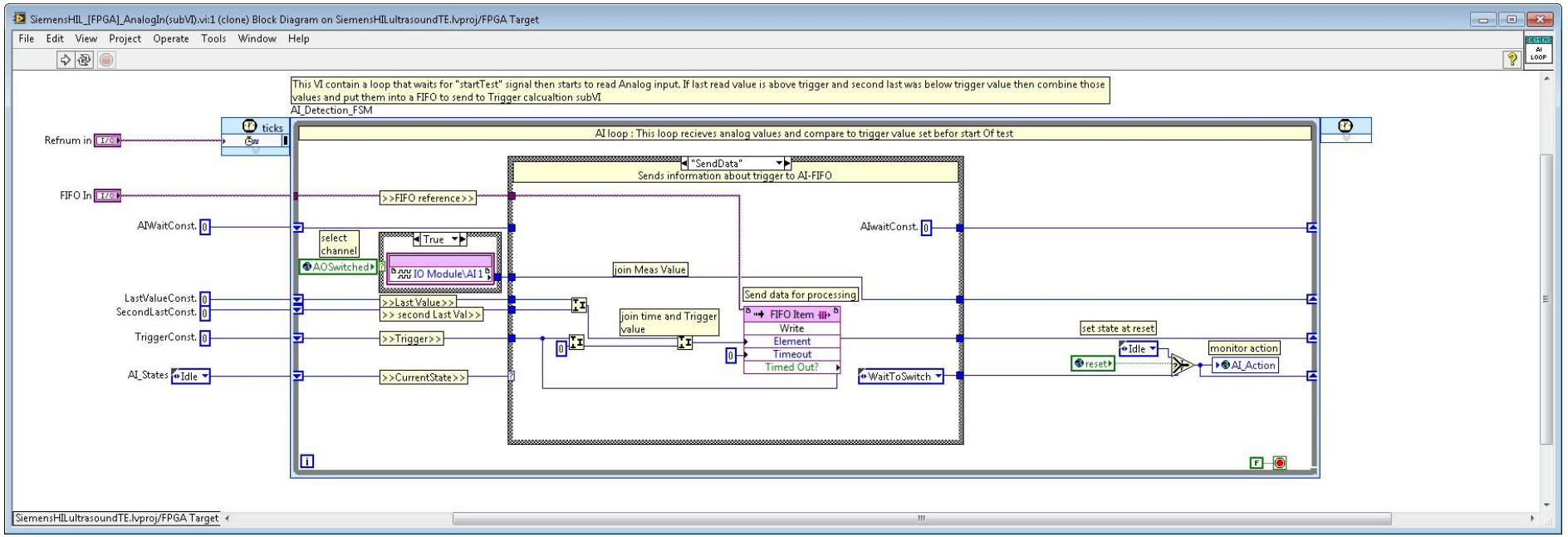
Example Code: Triggering



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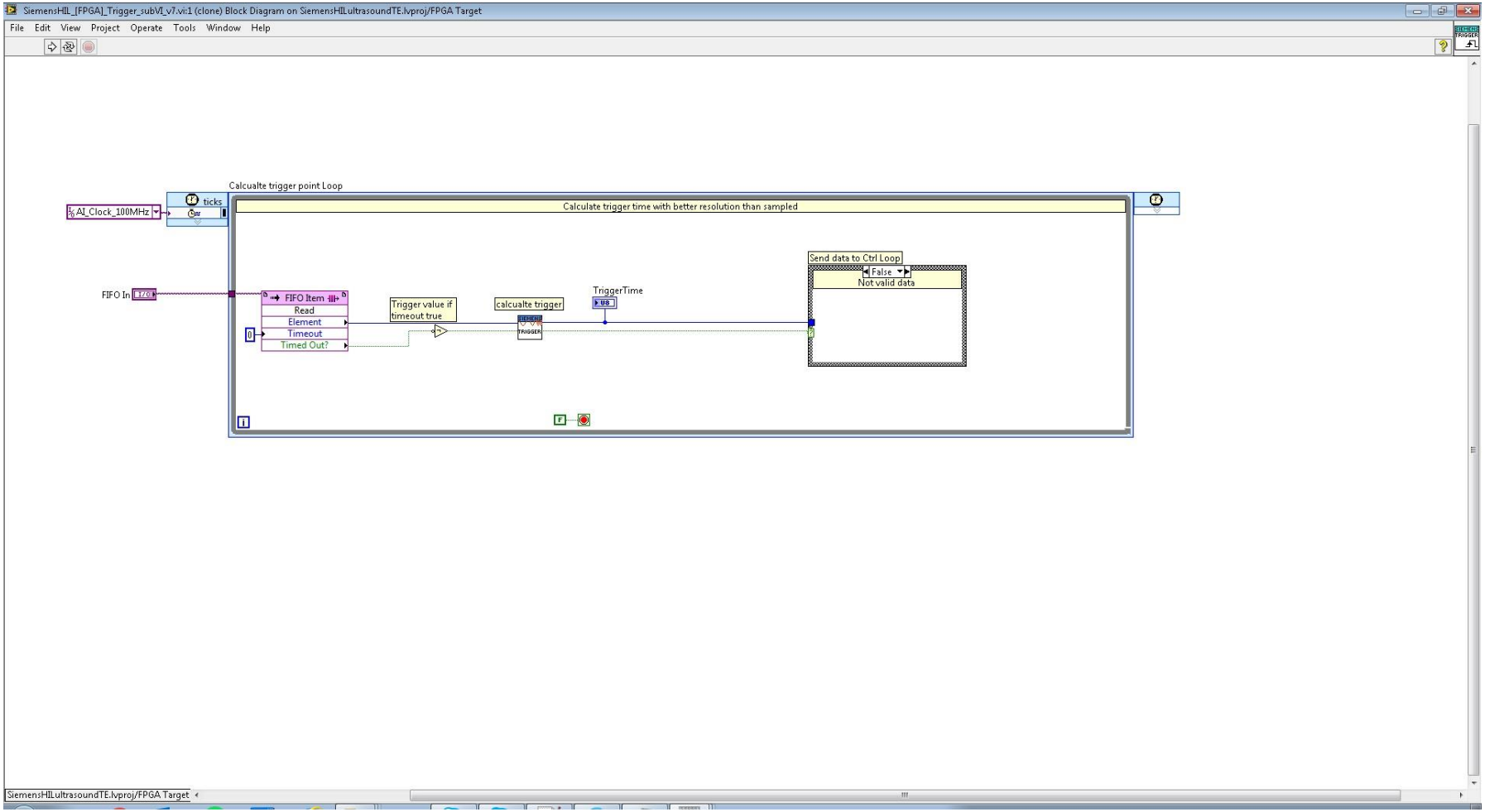
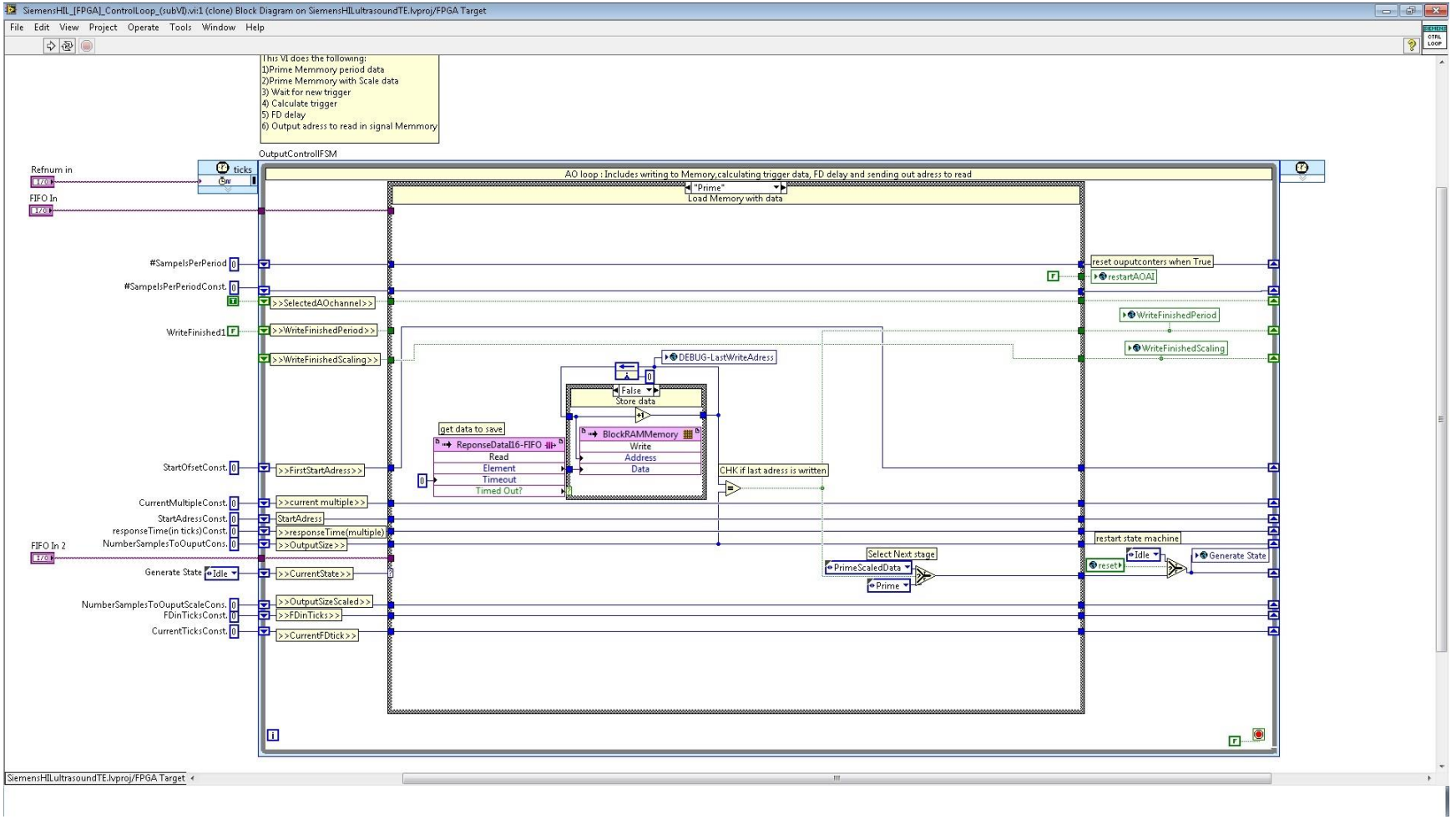
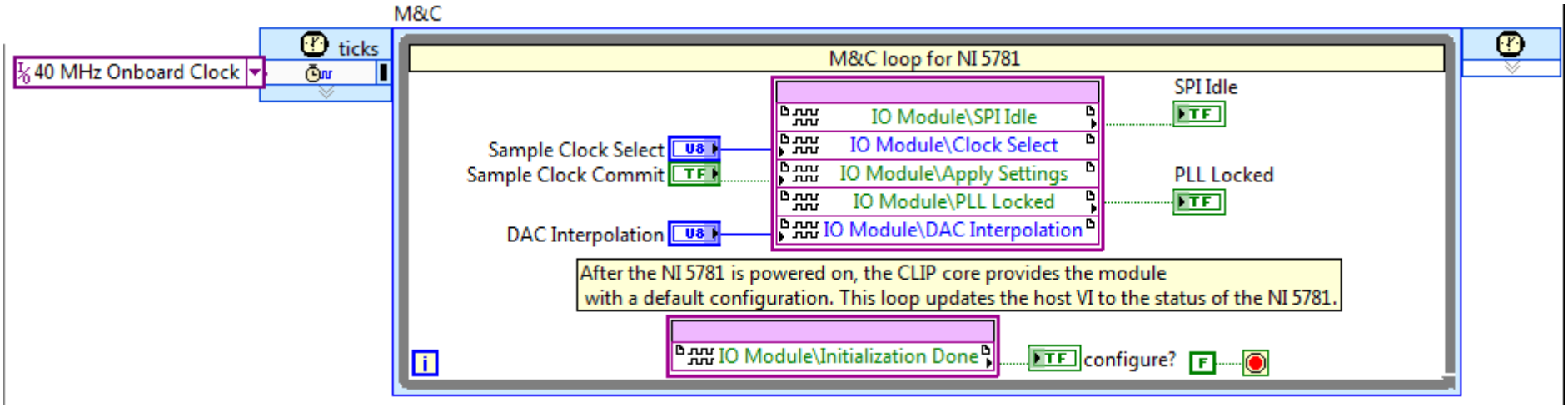
Example Code: Triggering: LabVIEW code Inpterpolation



Controll FSM to prime memory with response from the Controller



Setting up M&C on NI 5781



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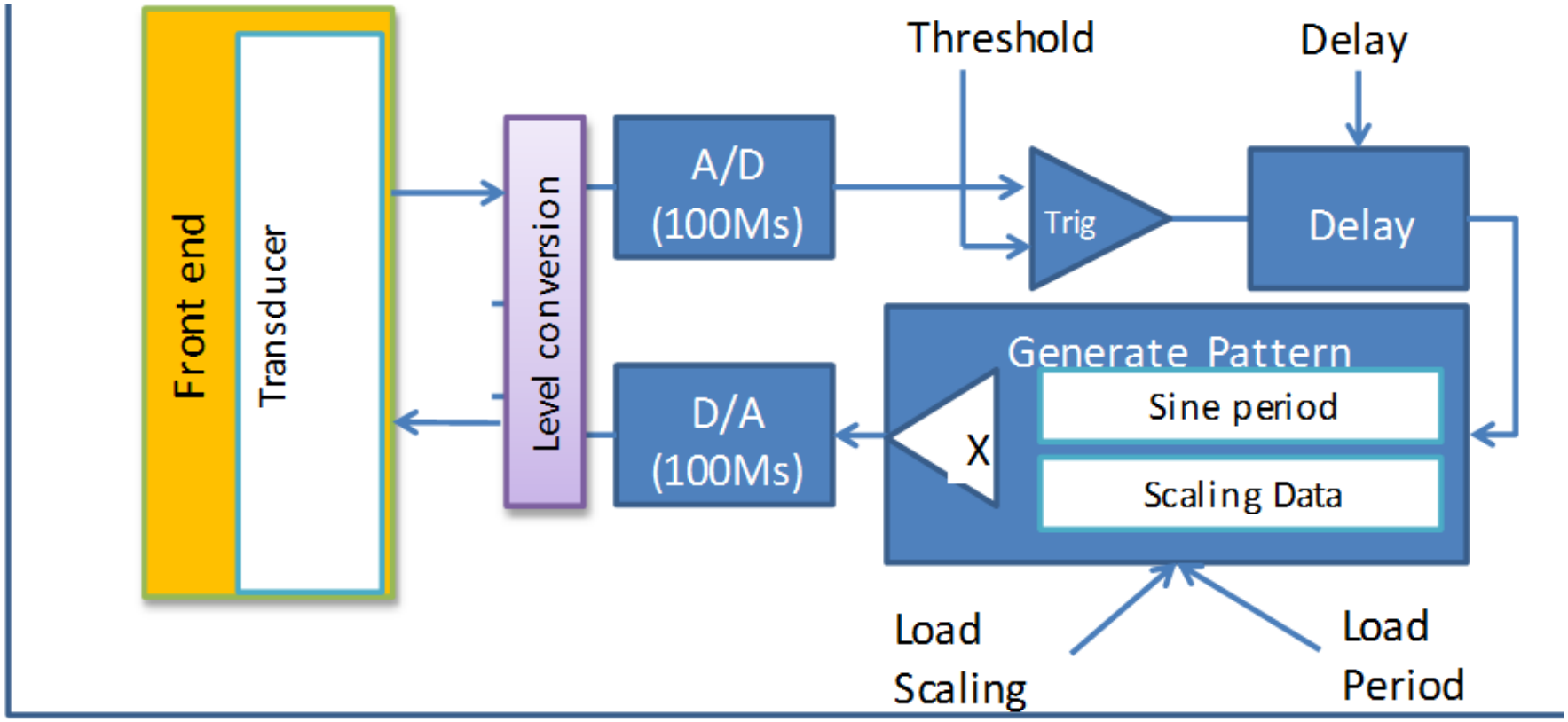
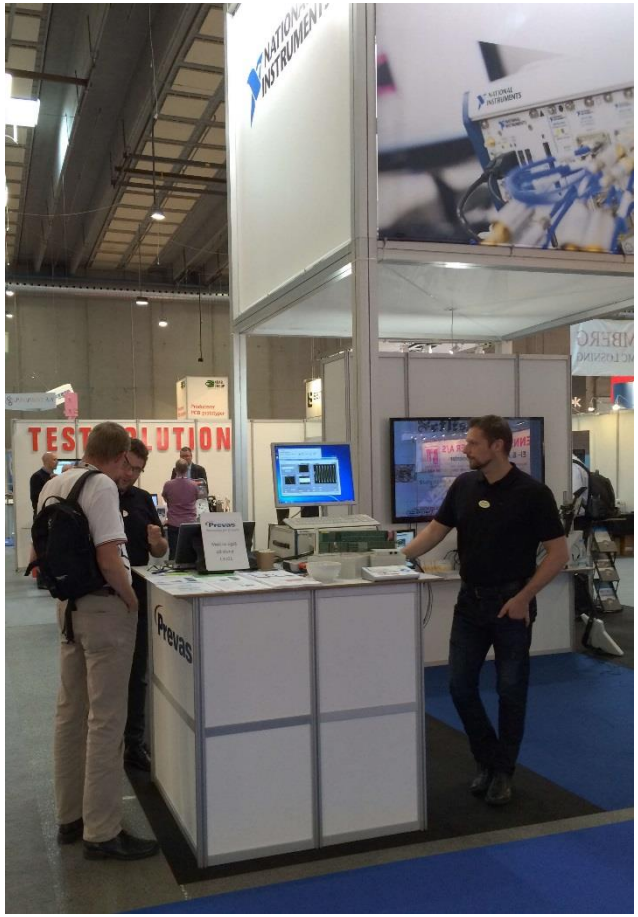
Block diagram on final implementation



Example: Ultrasonic flow sensor simulator – Finished system

- **PXI based table top system**
- **Embedded software and hardware “thinks” it placed in real physical conditions, getting emulated impulses from opposite sensor.**
- **Allows programmer much more access**



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Newer FlexRIO 7976R

Flex RIO 7976R

- DSP-focused Xilinx Kintex-7 FPGA programmable with the LabVIEW FPG Module
- 2 GB onboard DDR3 DRAM
- High-speed data streaming to host at 3.2 GB/s
- 66,000 slices, 28kbit blockRAM

Better flexRIO adapter NI 5782

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- Dual 14-bit, 250 MS/s inputs
- Dual 16-bit, 500 MS/s real-time, 1 GS/s interpolated outputs
- 100 MHz real-time bandwidth per channel
- DC- and AC-coupled options
- 12 bidirectional general-purpose digital I/O channels

What can be approved with nwere HW and latest LabVIEW SW

- With flexRIO 7976R whole response can be implemented in DDR3:

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- With flexRIO 7976R whole response can be implemented in DDR3:
  - Memmory can hold any preloaded data.(no need to generate data)
  - Easier LabVIEW code
- Might remove NI6674T due to that the NI5781 can get its clock from flexRIO 7976R AND 10MHz reference can be supplied to the backplane of the PXI chassie.

What can be approved with nwere HW and latest LabVIEW SW

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  - Memmory can hold any preloaded data.(no need to generate data)
  - Easier LabVIEW code
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- The customer could have VHDL code that could be utilized in the flexRIO to improve functions.
- LabVIEW FPGA uses Xilinx envoirment vivaldo instead of ISE on later versions which decrease compilation time dramatically.

Technical agenda

- What is a FPGA
- NI HW and LabVIEW FPGA
  - NI FPGA Targets
  - PXI and flexRIO
  - flexRIO adapters
- Project: SiemensFlow ultrasonic HIL
  - Ultrasonic Flow Theory
  - HIL Test System description and implementation
  - NI HW used in HIL
  - Challanges with sub-nanosecond time resolution
  - LabVIEW programming
  - Final implementation
- Improvments to be made on HIL
- Lesson learned

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Lesson learned, FlexRIO during the project

- Use NI guidelines to minimize timing violations
  - use minimum needed bits
  - pipeline
  - recompile if failed with low time
- Divide application up into smaller functions that can be tested separately

- If you are to use clip nodes, take some VHDL training to understand the basic and also the “language”.

- Investigate IP cores before devoloping

- Work with saved bit files for deployment on targets.
- It saves time by minimizing the number of compilations.

- Using the FPGA to calculate parameters decrease the channel count and improves the system performance. (and makes the main program less complex)
- Make sure that verification of system is set before developing starts

Questions

QUESTIONS ?