

# VarioTAP technology moves Boundary scan to a higher level



# Presentation of DSE Test Solutions A/S

- ♦ More than 25 years in T&M business
- ♦ Location – Horsens DK
- ♦ App. 25 employees
  - Knowledge based organization
  - Approx. 60% with long educations (B.Sc, M.Sc)
- ♦ 3 Business areas
  - Testers for the electronic industry
  - Wire testers
  - Biomass moisture testers



## **Mission:**

*Applying our in-depth experience and knowledge of test and measurement, we design unique system solutions and products that create value for our customers, our partners and ourselves.*

# Platform based FCT solutions

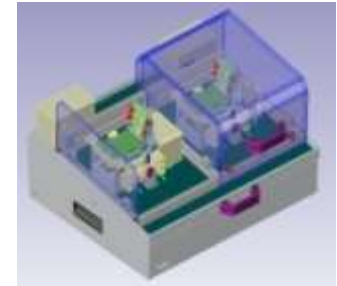


Based on:

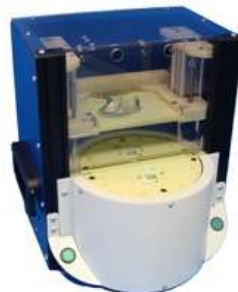
- NI software
- Standard instrumentation
- JTAG - Boundary scan
- Vision
- Custom designs



# Fixtures standard and custom



- From simple mechanic to full automatic
- RF shielded
- Turntable
- Safety cover
- Manual or pneumatic operated
- Custom designed fixture in 3D solid works





# Software platforms and tools

Two generic platforms:

- DSE test Engine
- NI Test Stand

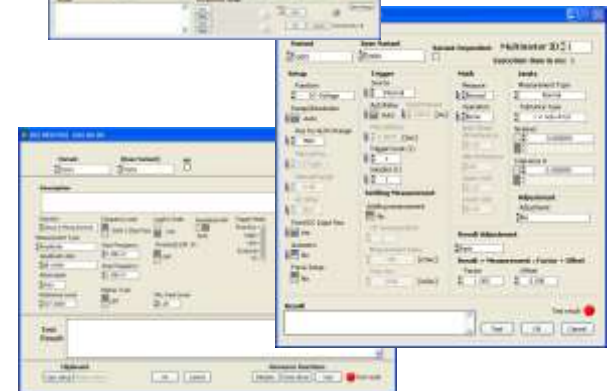
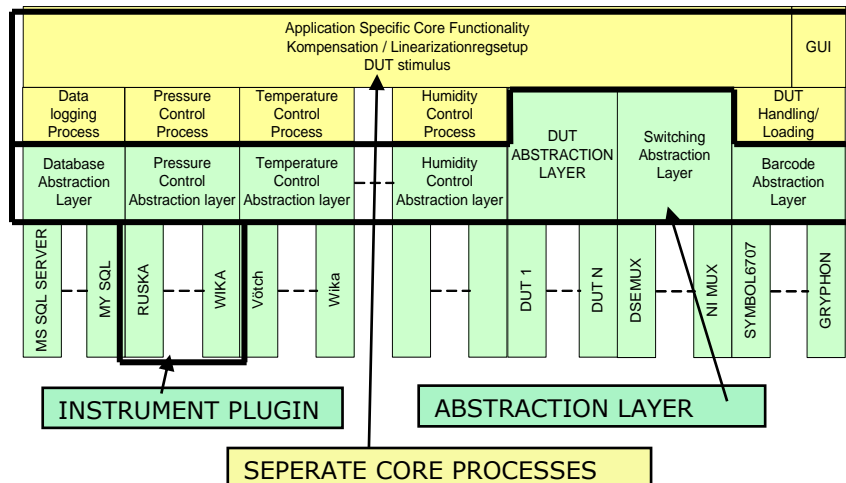
All applications base on LabVIEW



Resources with graphical interface for all functions and instruments.



## DSE TestStand framework



# Introduction to JTAG / Boundary Scan



Definition

# Boundary Scan

**IEEE 1149.4**

**IEEE 1149.1**

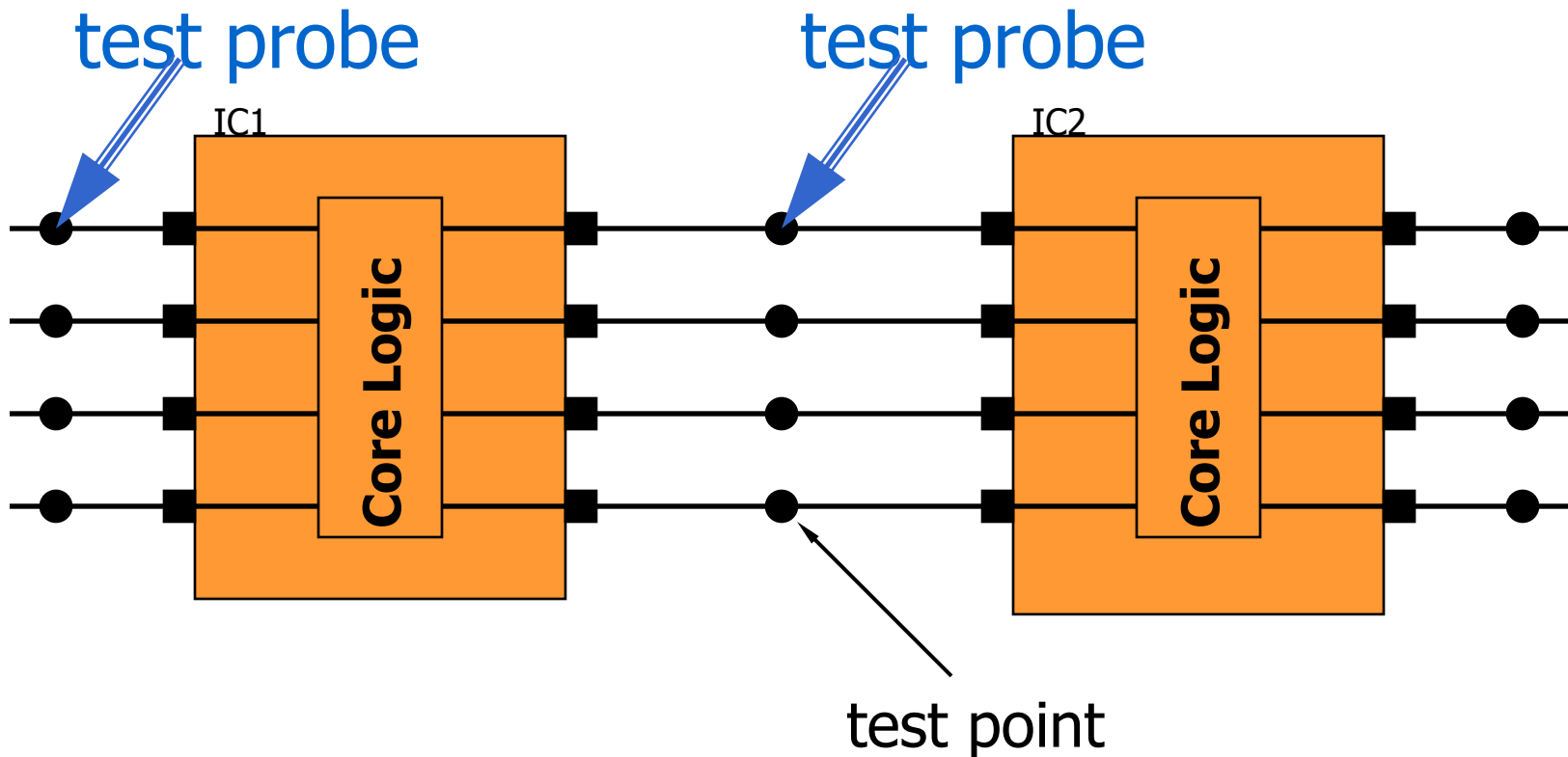
**JTAG**

# Definition

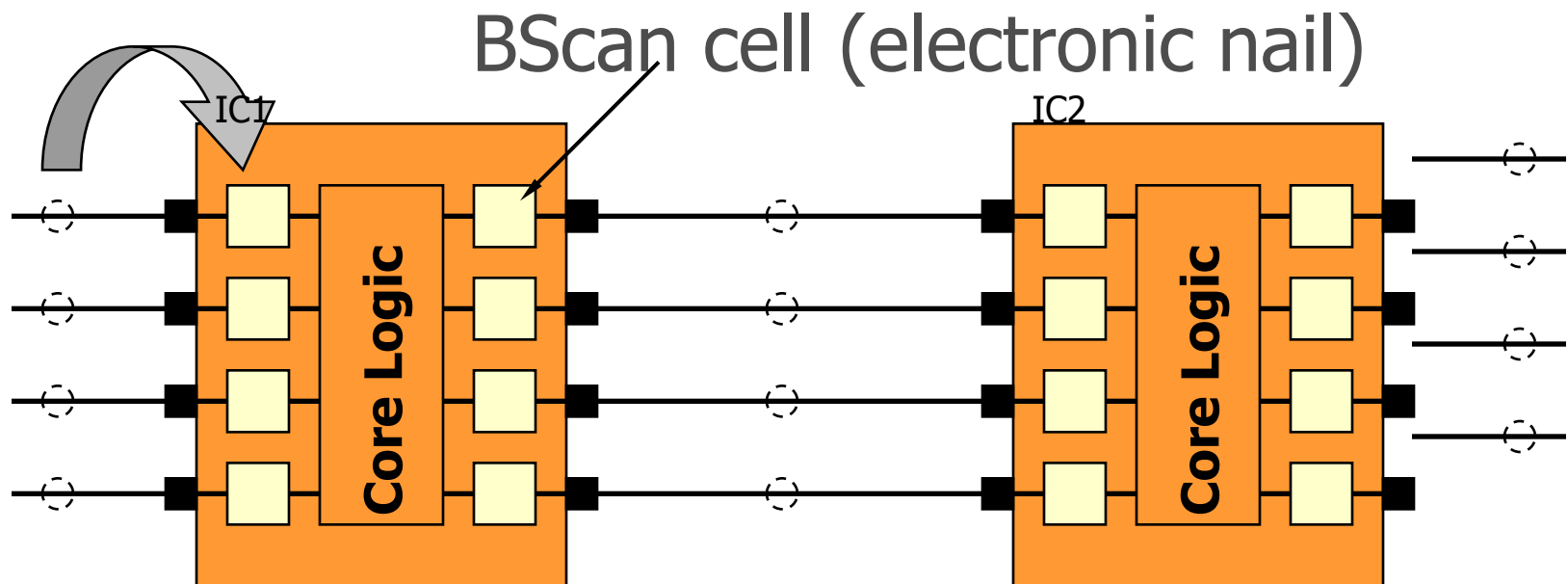
JTAG	<b>J</b> oint <b>T</b> est <b>A</b> ction <b>G</b> roup
Boundary Scan	Test technology for boards containing ICs that have boundary scan registers integrated in the ICs
IEEE 1149.1	Standard for the digital connection test adopted by the Joint Test Action Group



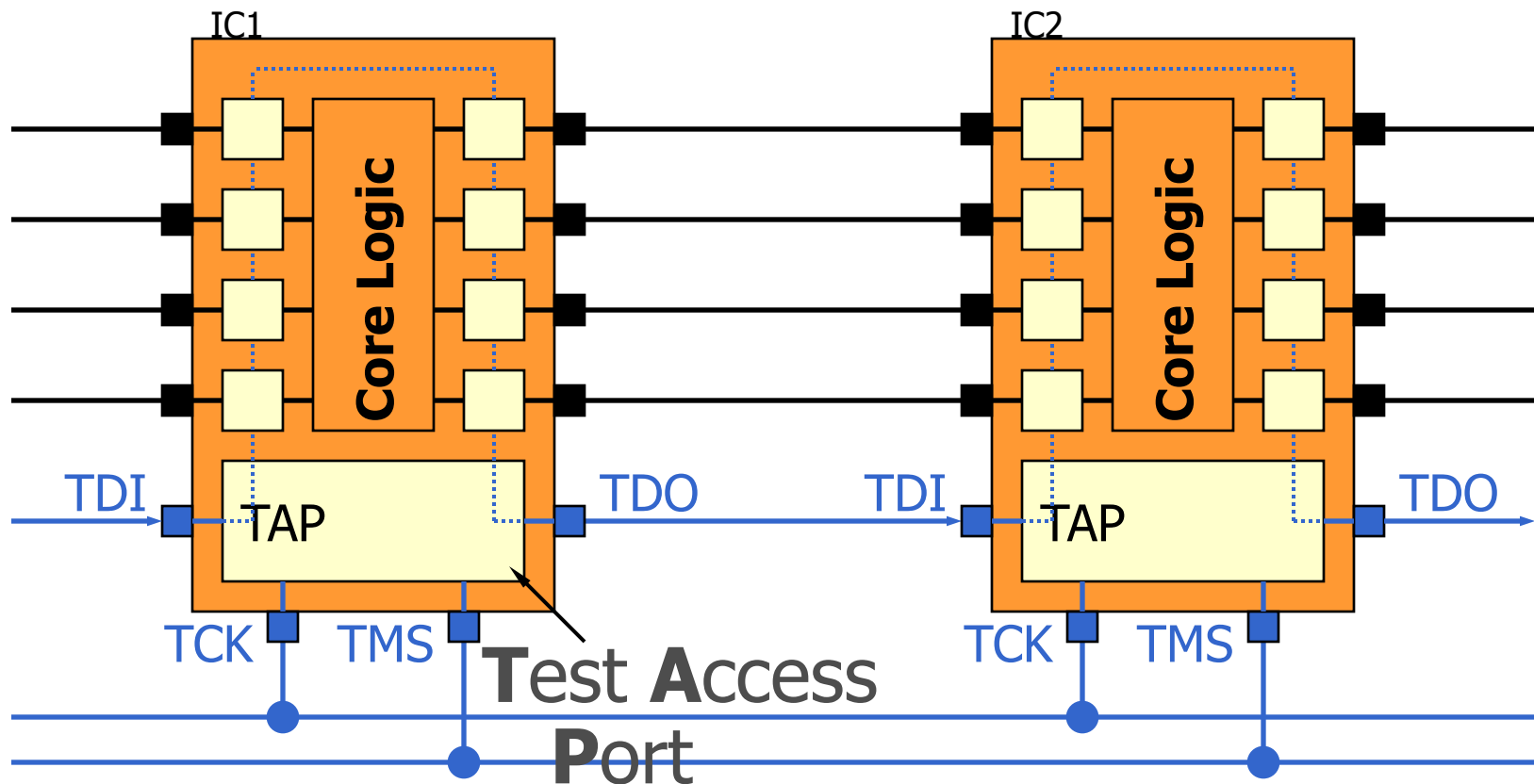
# In-Circuit Test (ICT)



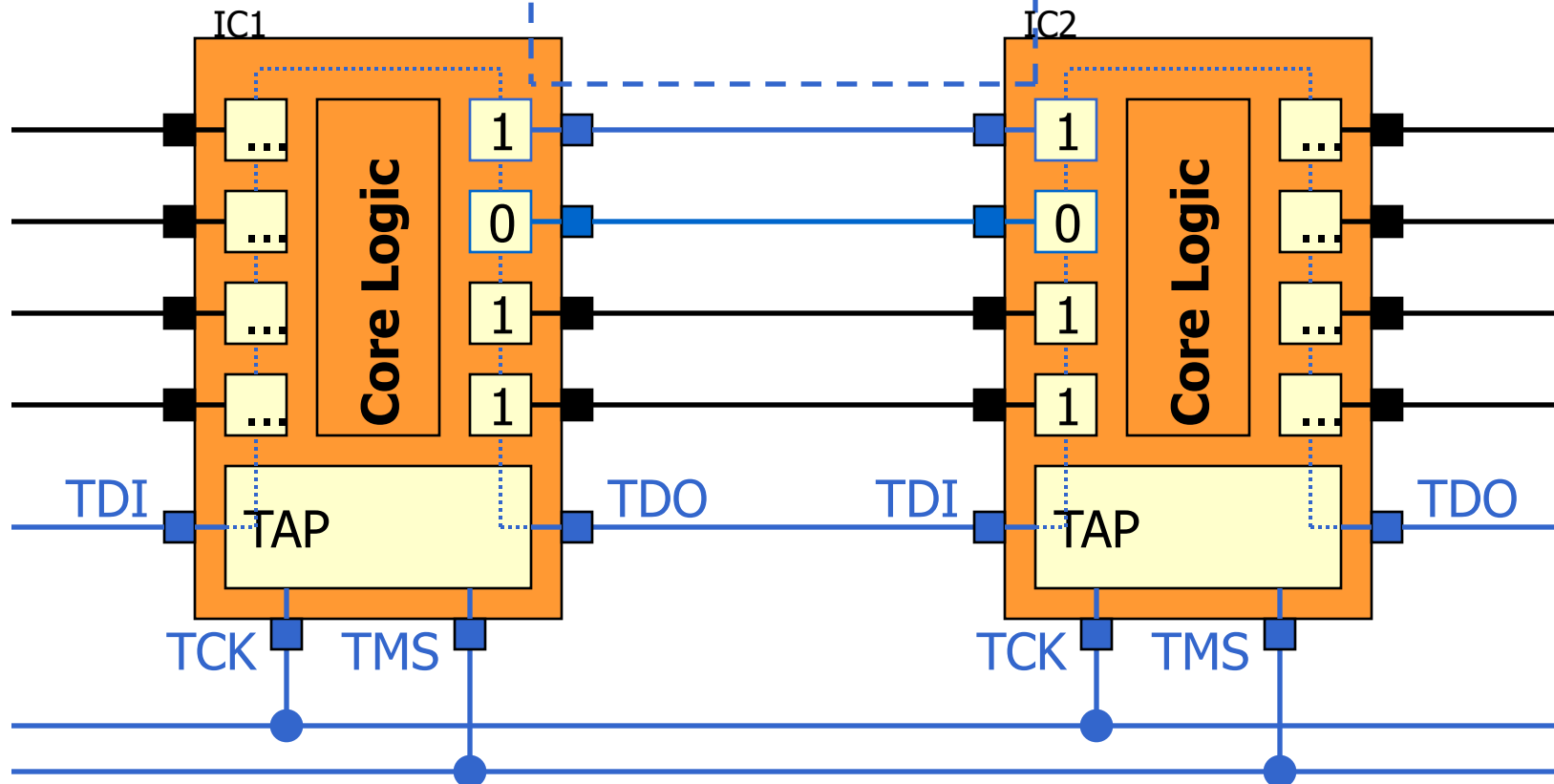
# Bscan Test (similar to static ICT)



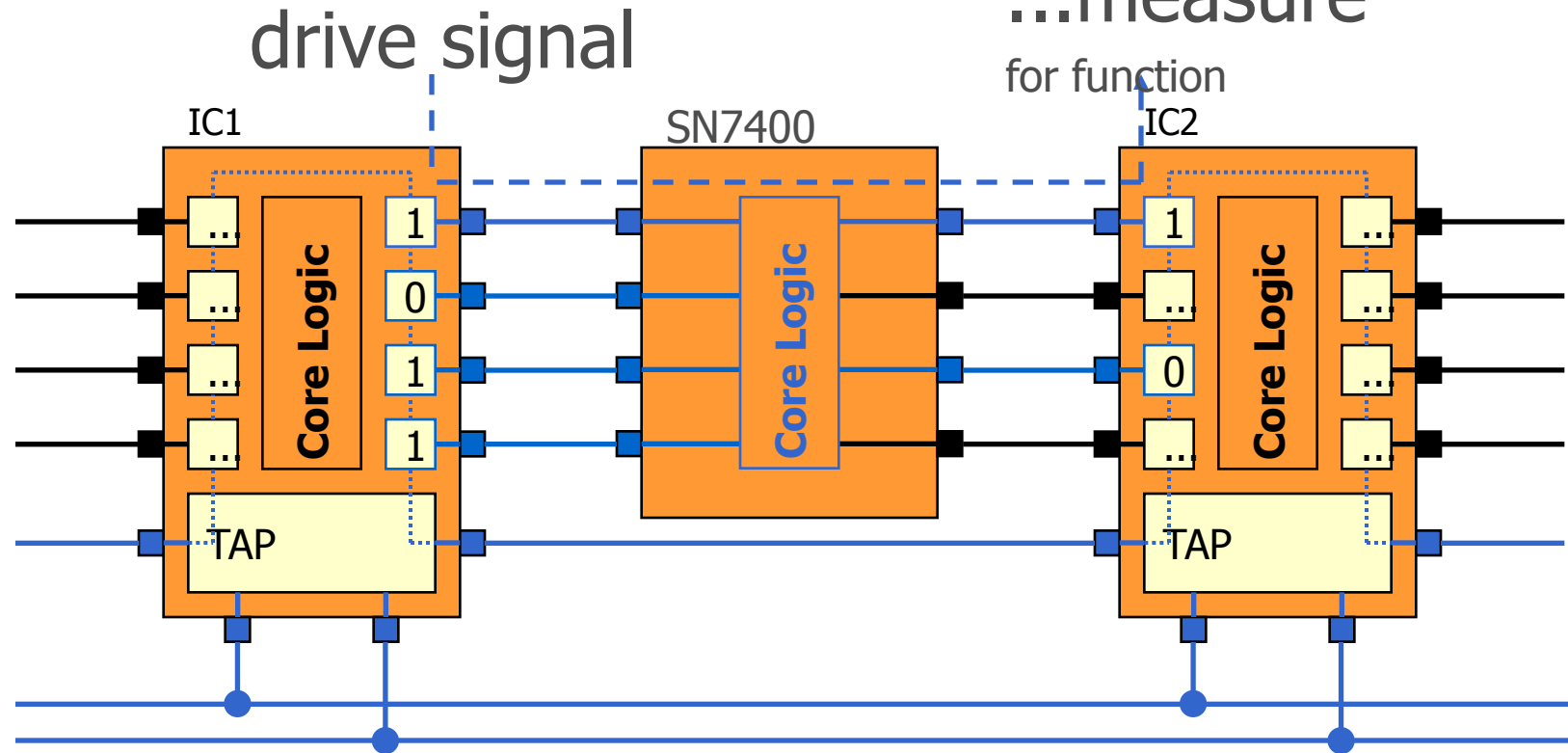
# IEEE 1149.1 test bus



for connection, shorts and stuck-at



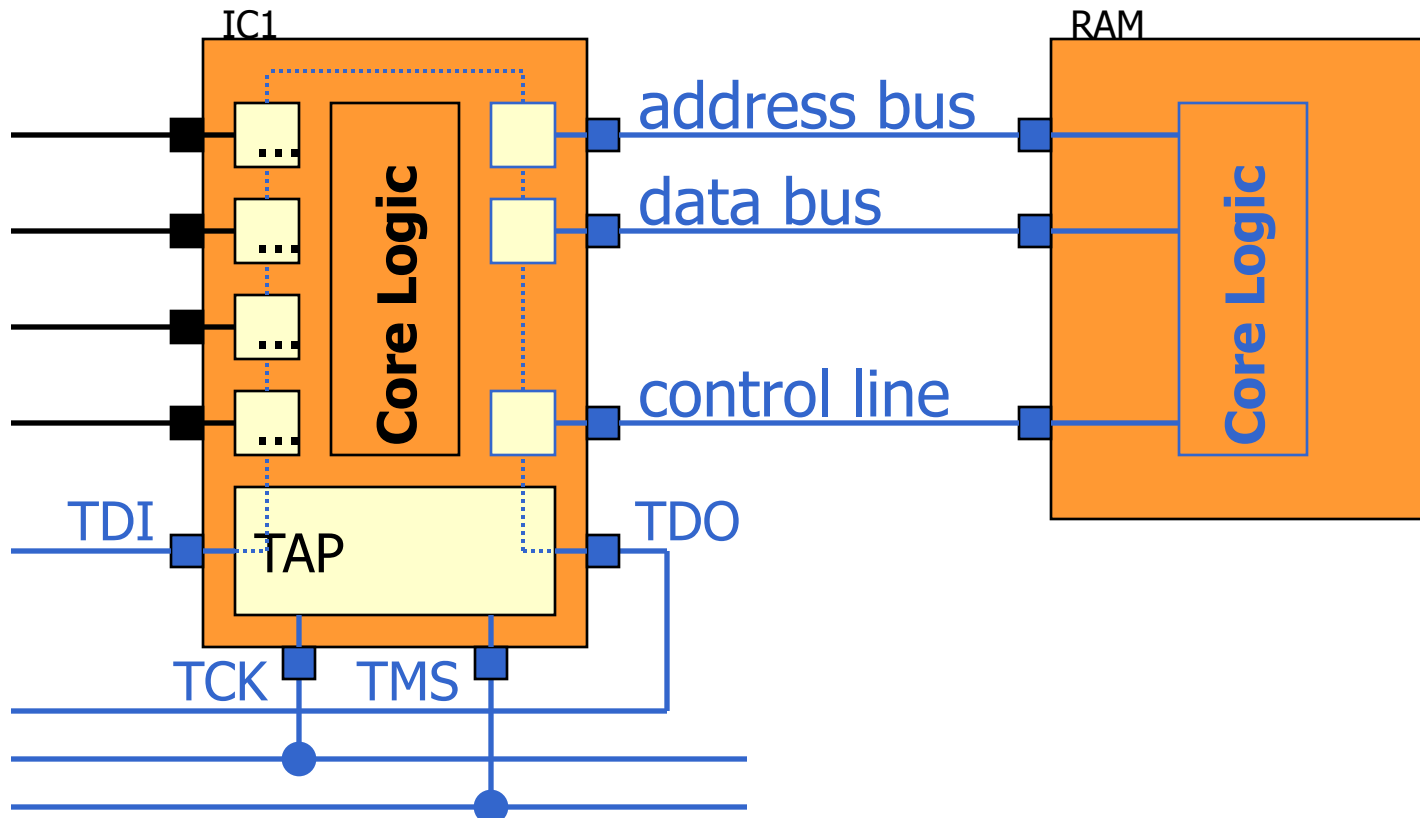
# Testing non-Bscan ICs



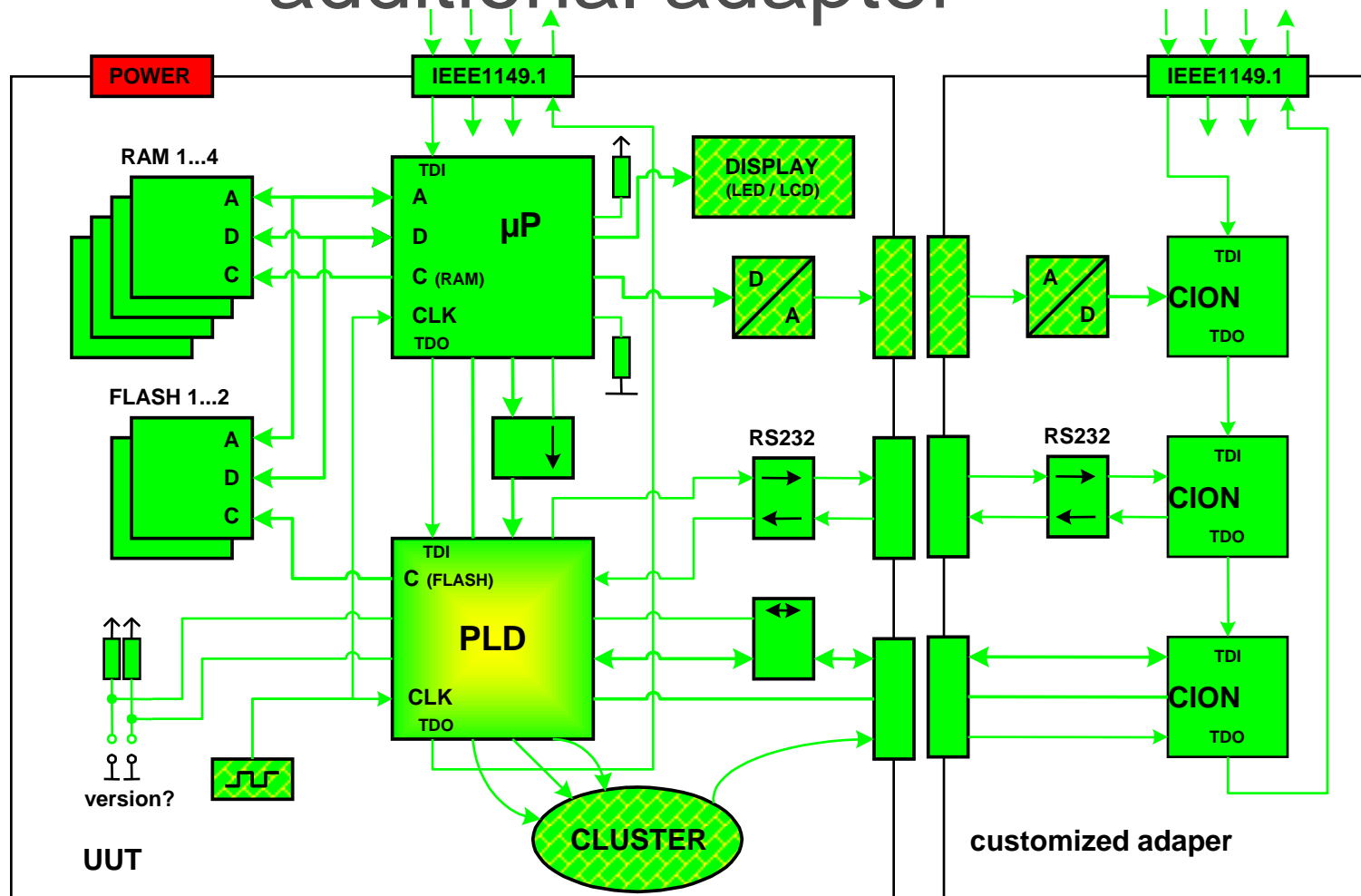


# Test of RAM with BScan

1. Shorts and Stuck-At faults at the interconnection test
2. Open faults at the RAM test (walking one / zero)



# Test coverage of BScan with additional adapter



# Advantages

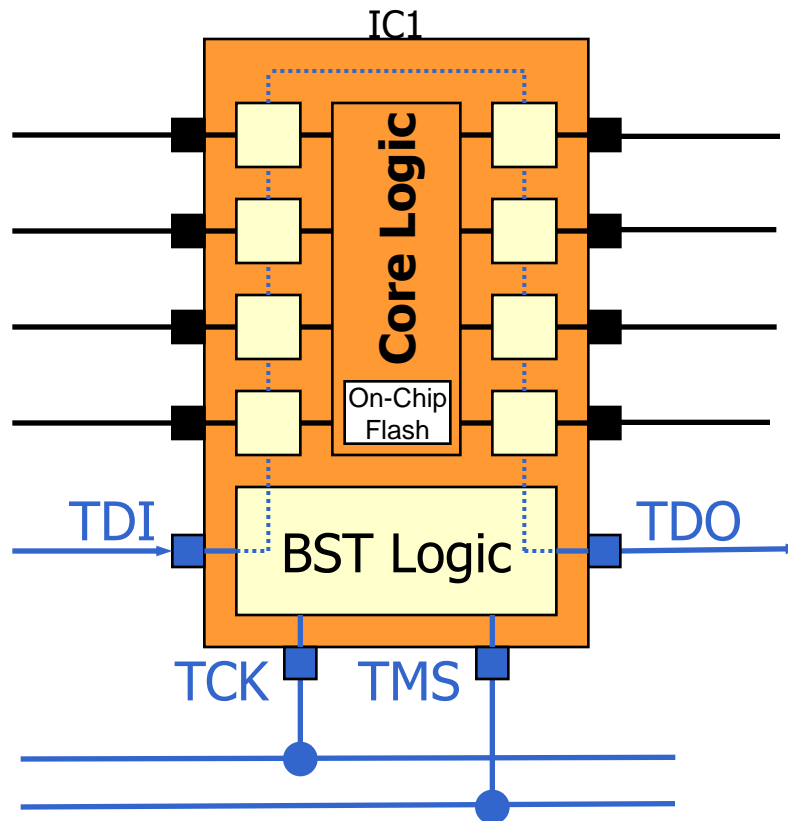
- **Access: Only 4 Bscan plus power signals needed.**
- **Automatic test generation is done out of netlist and library information.**
- **Fast infrastructure test secures integrity of the Bscan chain.**
- **The interconnection test finds „the tough problems“ below BGAs and similar components and inside the PCB (micro- and burried vias etc.)**
- **In-Circuit Programming tools helps re-configuring devices and changing Flash contents.**

# New challenges

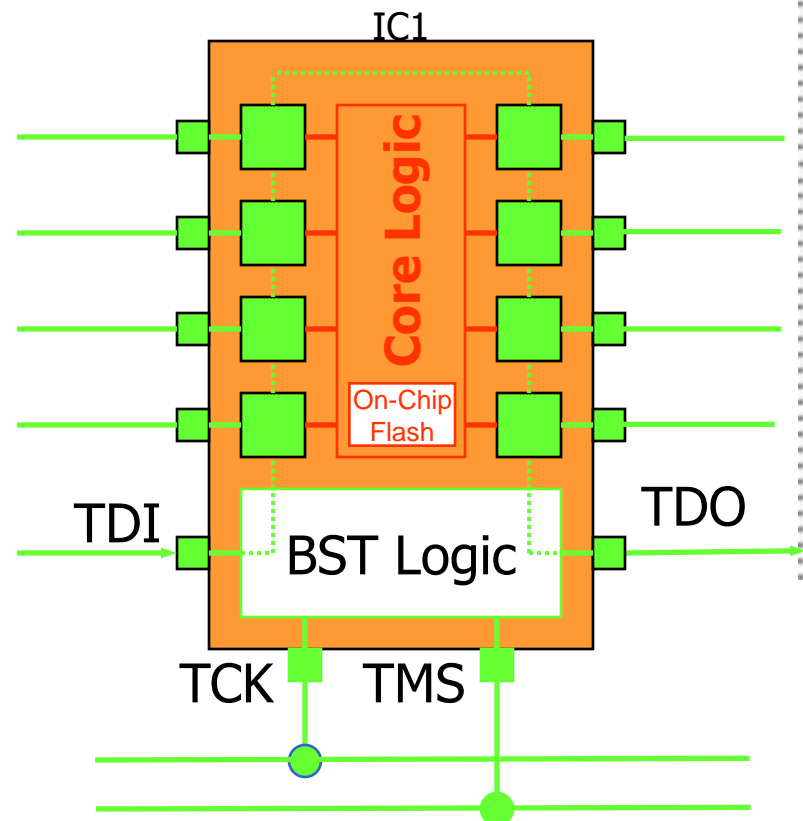


# On-Chip Flashes

Boundary Scan IC with  
On-Chip Flash

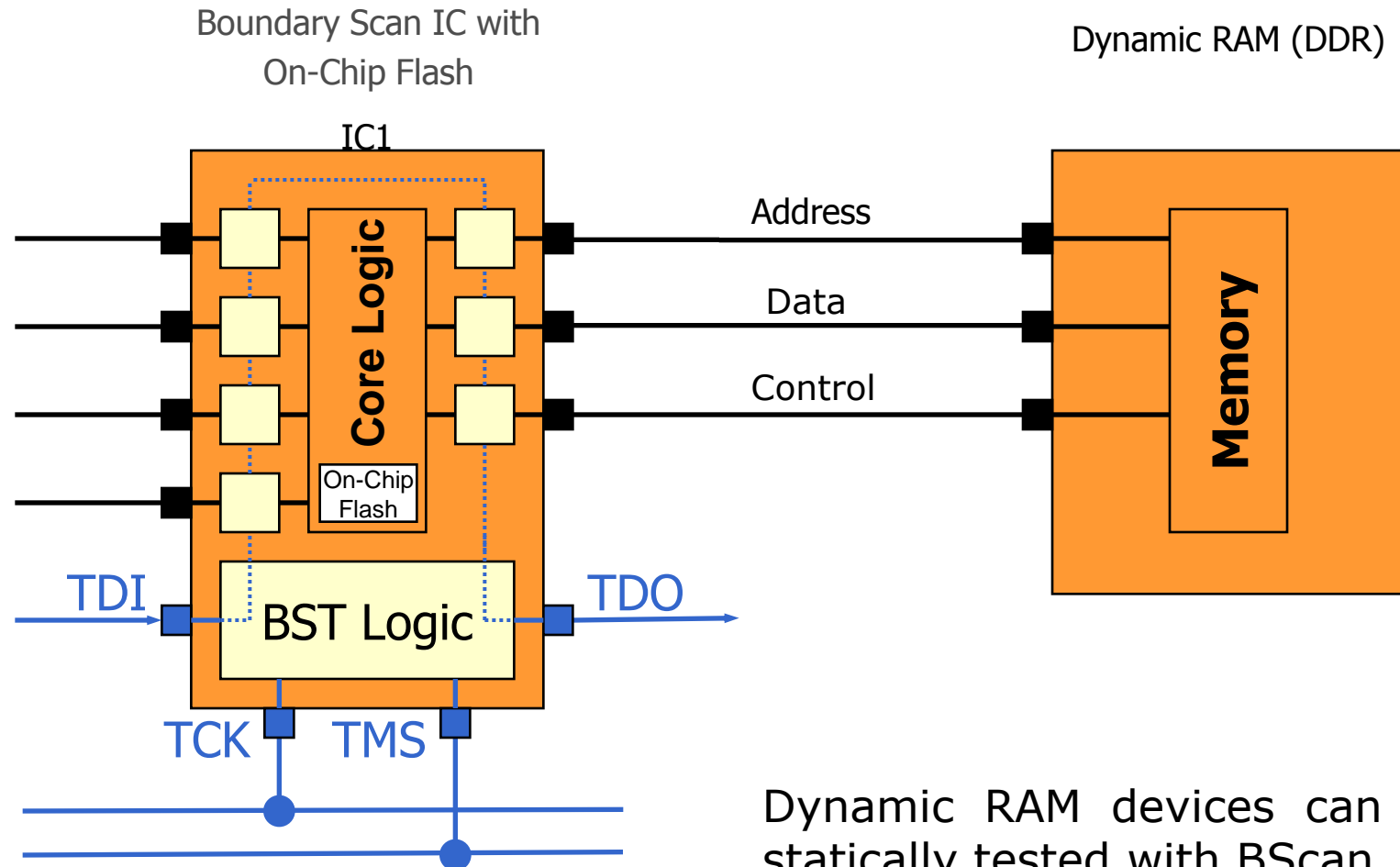


Boundary Scan IC with  
On-Chip Flash



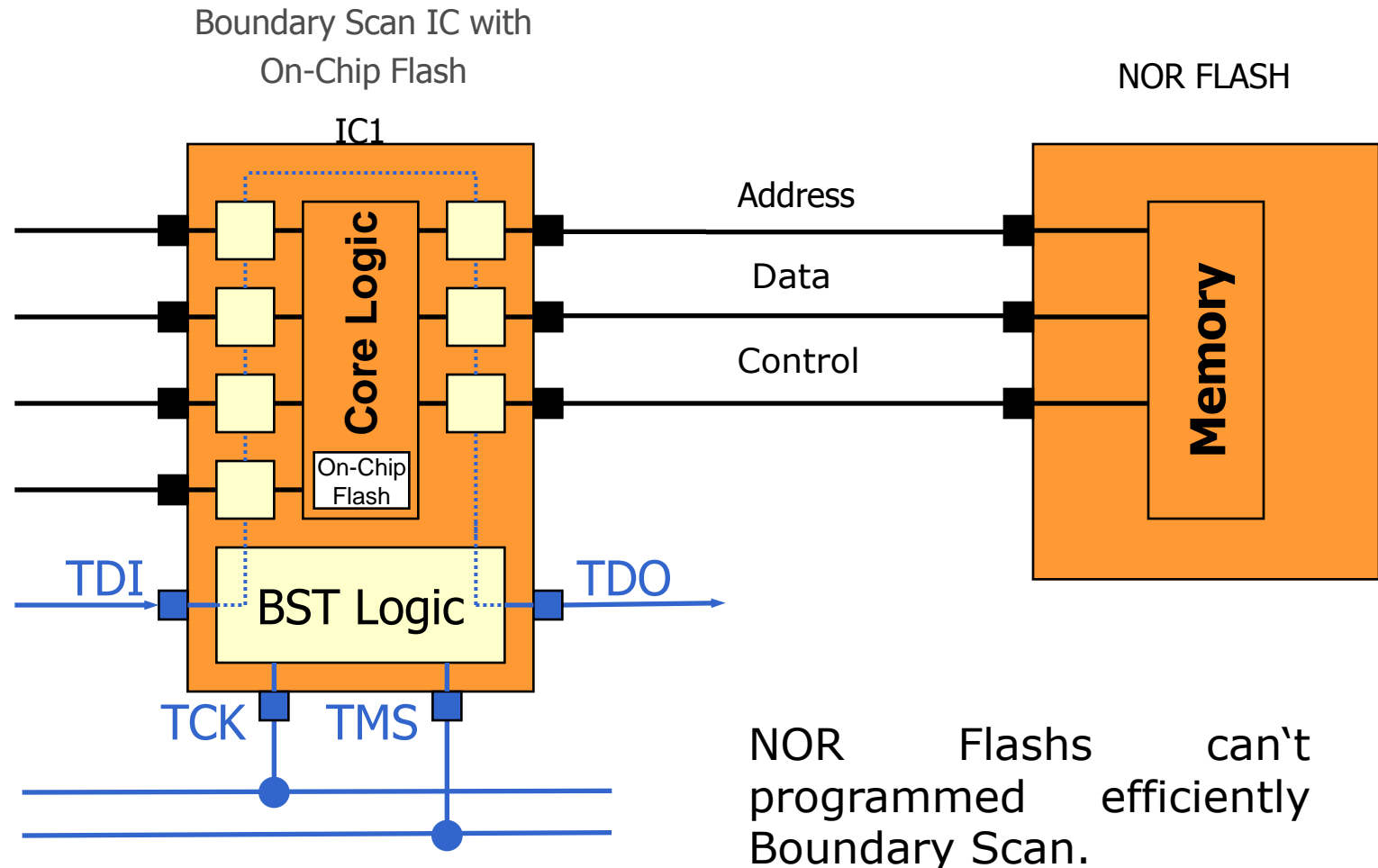


## Dynamic RAM - Devices

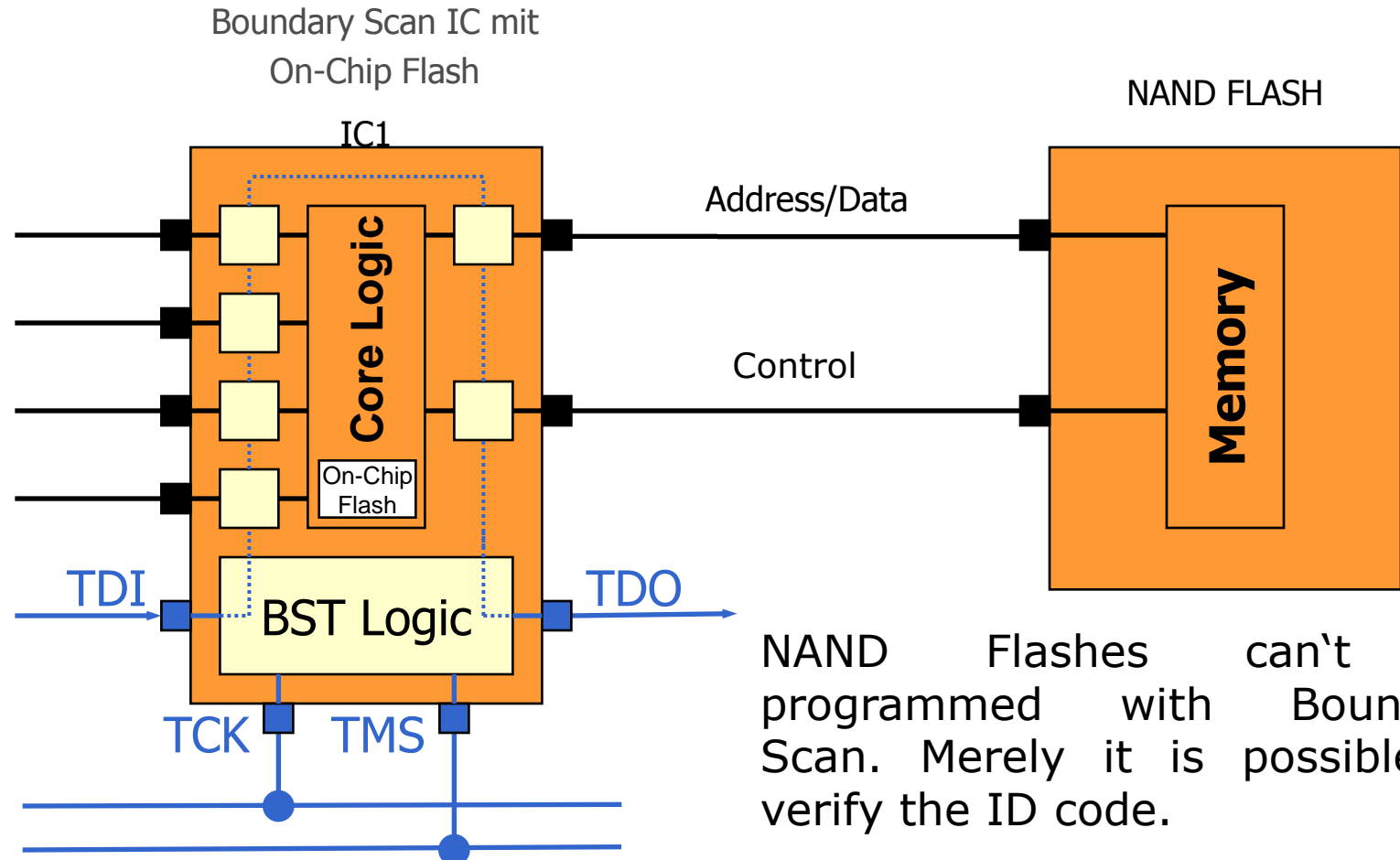


Dynamic RAM devices can only statically tested with BScan.

## Externe Flashes – NOR Flash



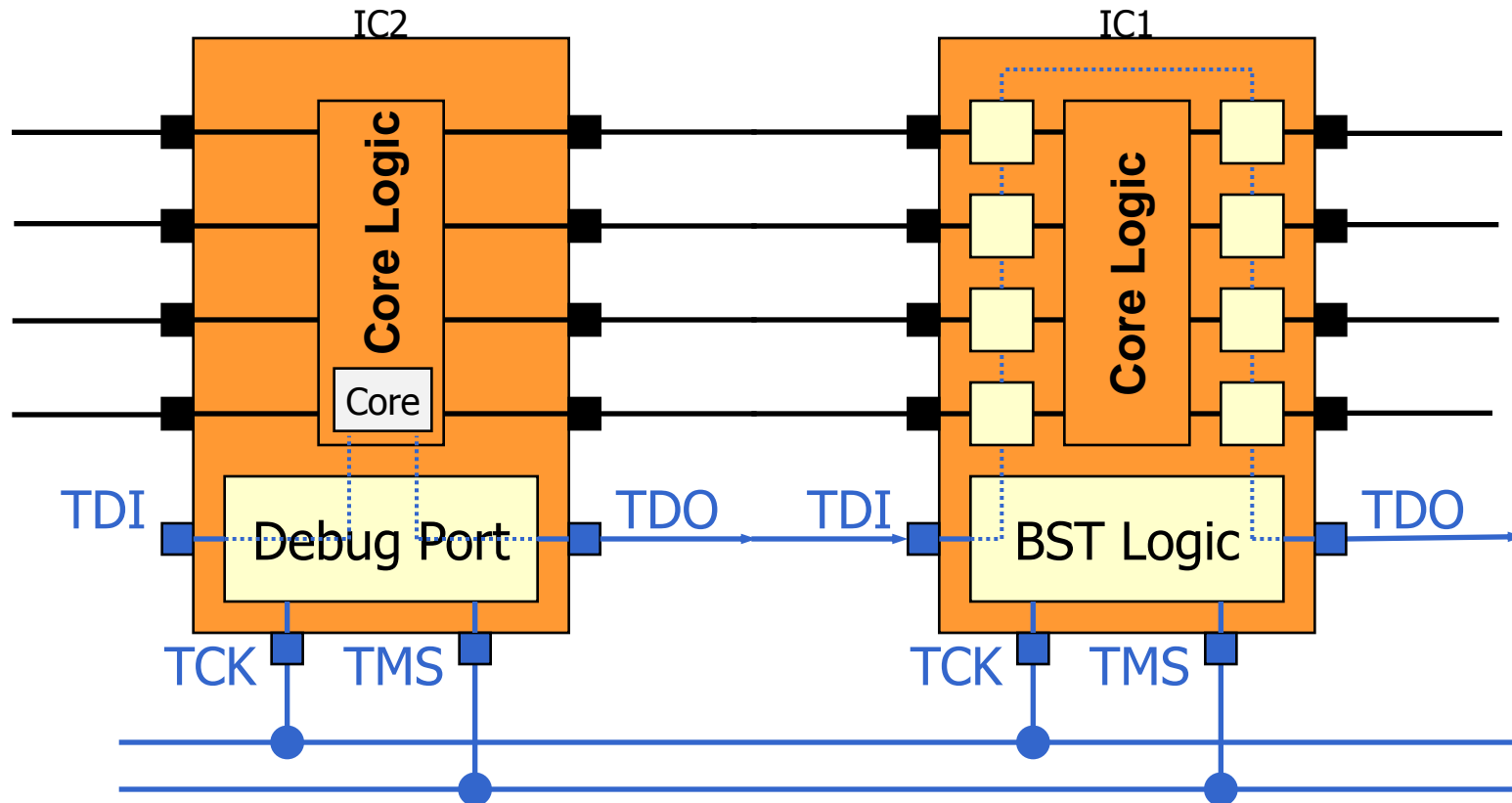
## External Flashes – NAND Flash



## Different Structures

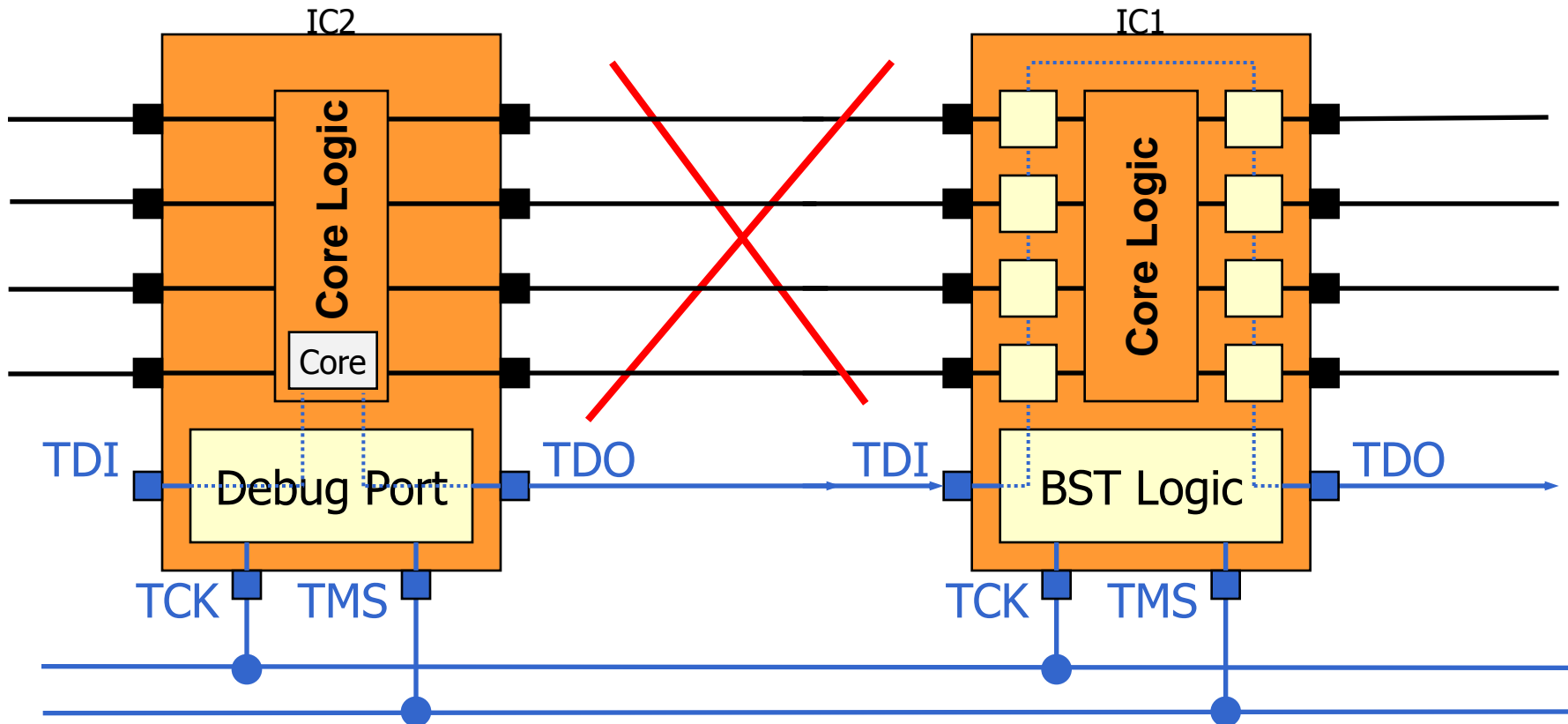
Device with Debug Port according to IEEE 1149.1

Device according to Boundary Scan Standard IEEE 1149.1



## Different Structures

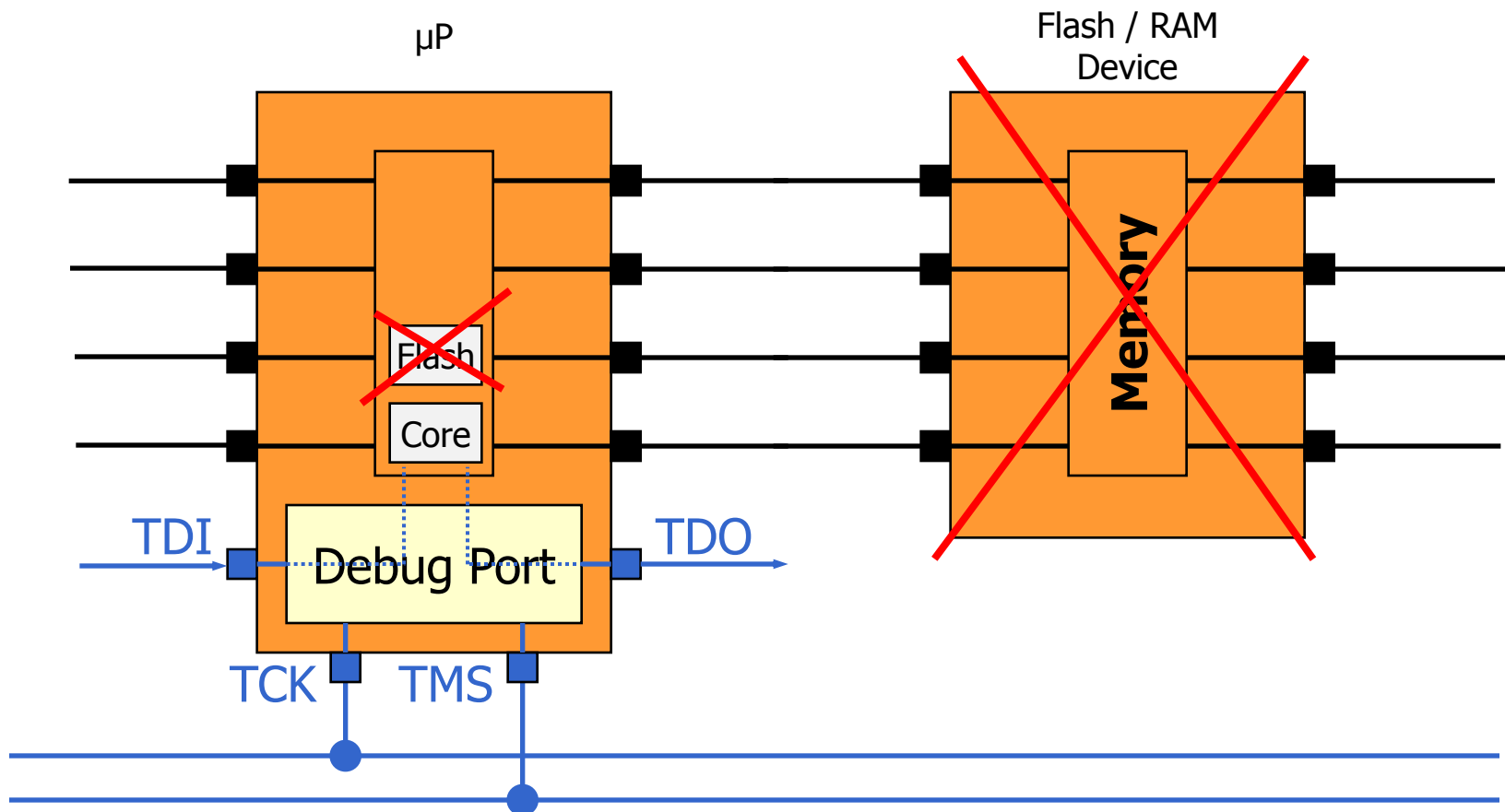
The connection between the devices can't be tested.





## Different Structures

Internal as well as external Flash devices can't be programmed.



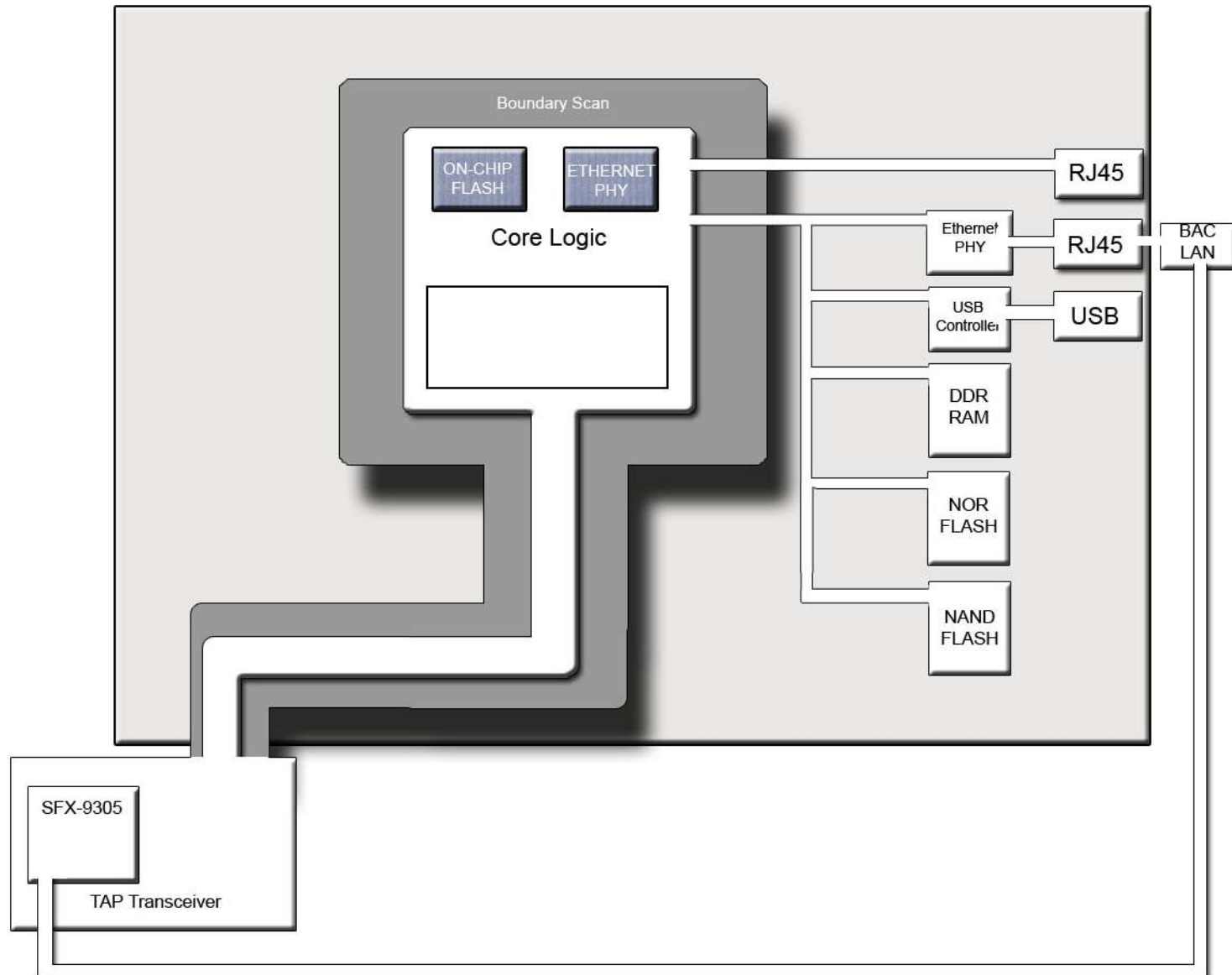
# The challenge

- ♦ Programming of OCF (On-Chip Flash)
- ♦ Test of dynamic Structures (e.g. DDR Ram)
- ♦ Efficient Programming of Flash Devices
- ♦ Bad Block Table Handling for NAND Flash Devices
- ♦ Handling of Non Boundary Scan capable JTAG Devices
- ♦ Complete Integration in existent Test systems
- ♦ Uncomplicated handling

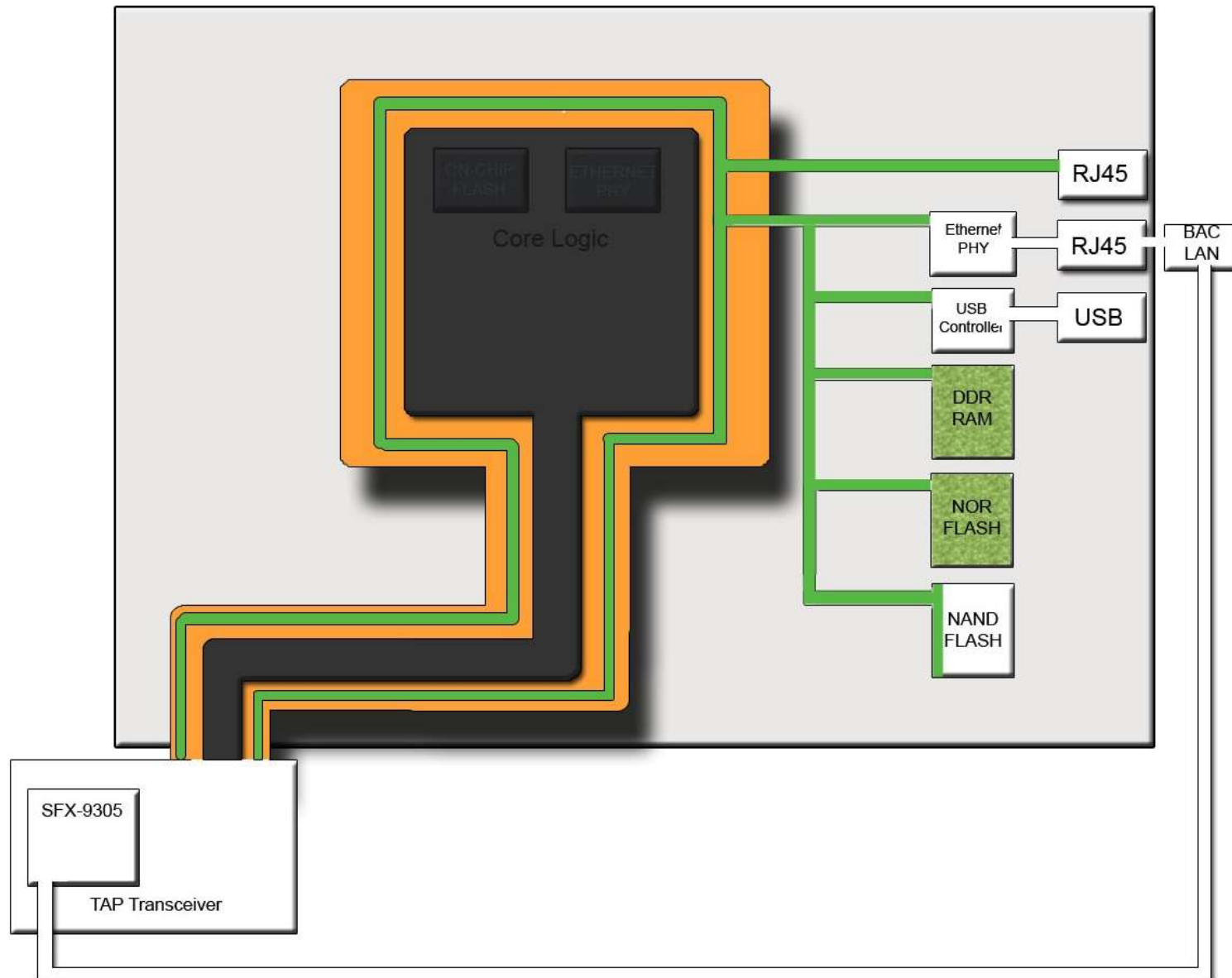
# The central idea of VarioTAP™



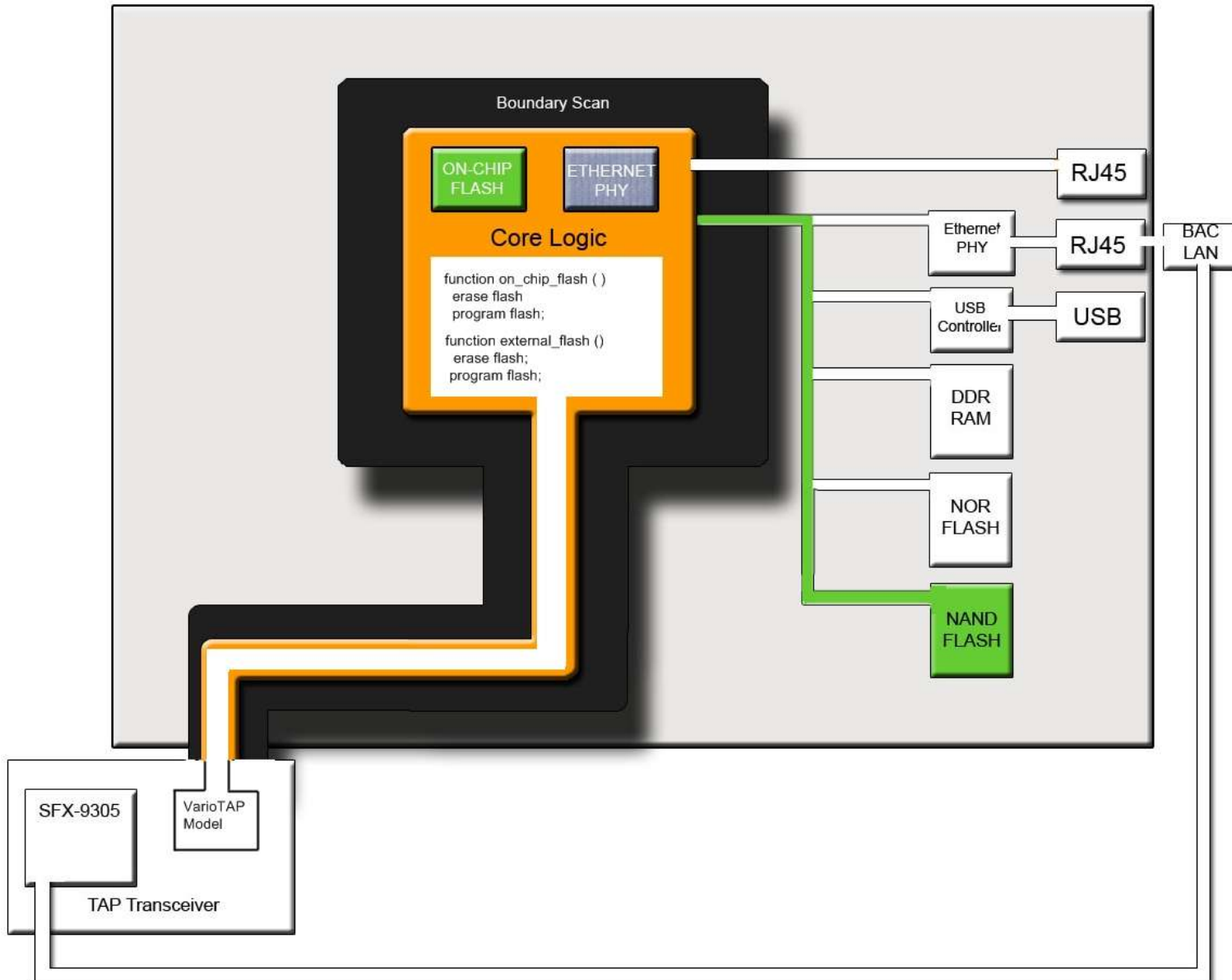
# VarioTAP – A Digital Board



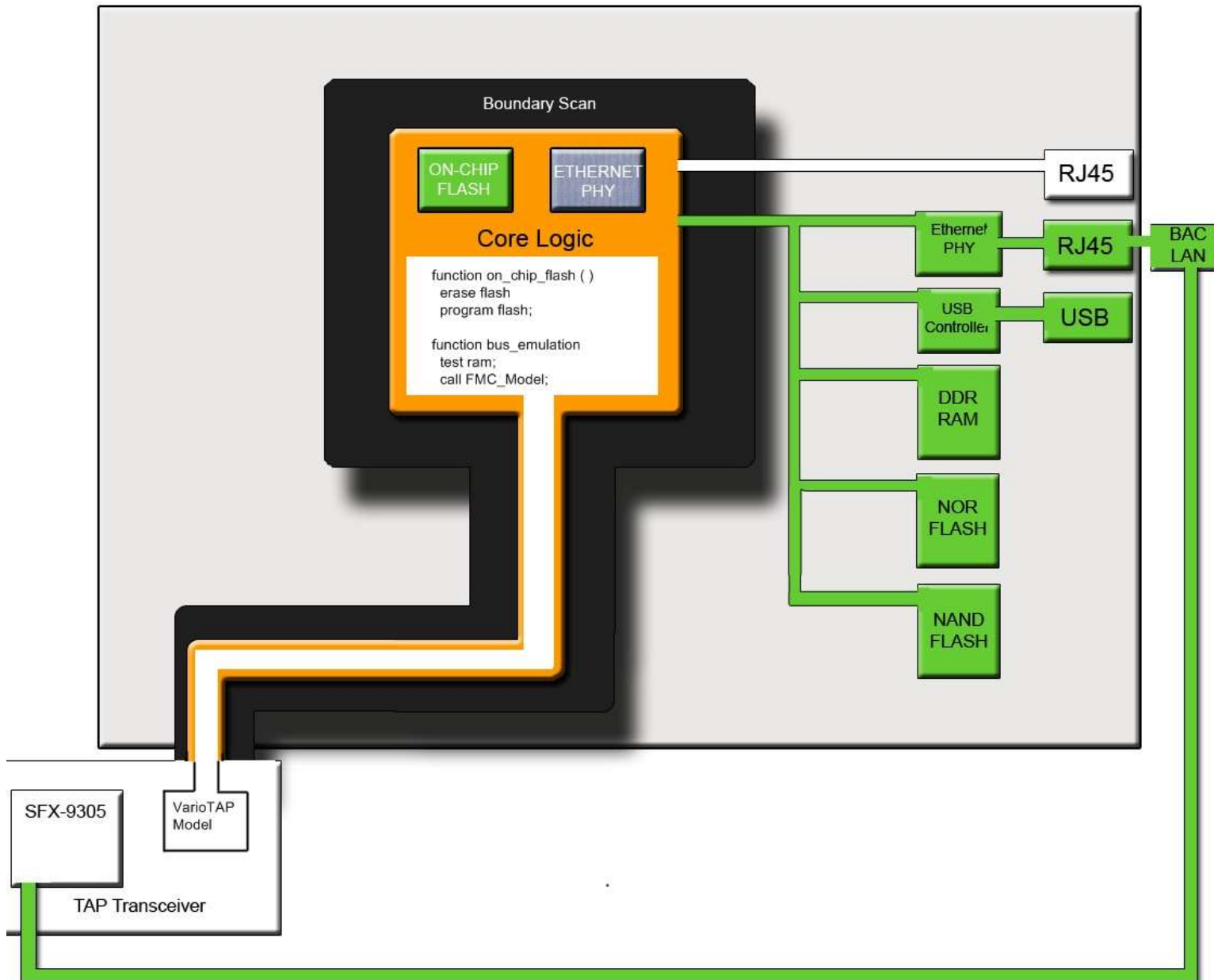
# VarioTAP – Test Coverage BScan



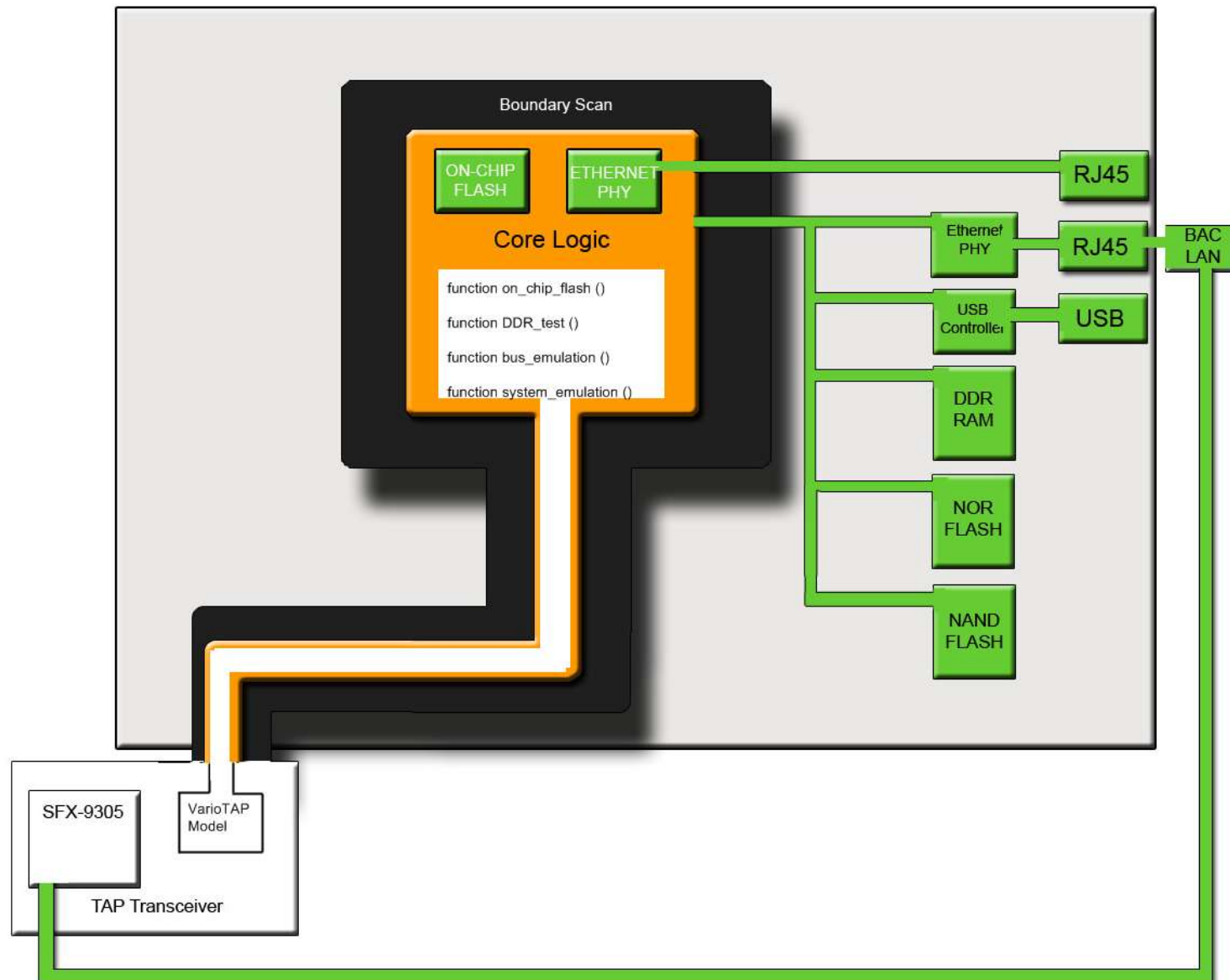
# VarioTAP – On-Chip Flash



# VarioTAP – Bus Emulation



# VarioTAP – System Emulation





# DSE Test Engine

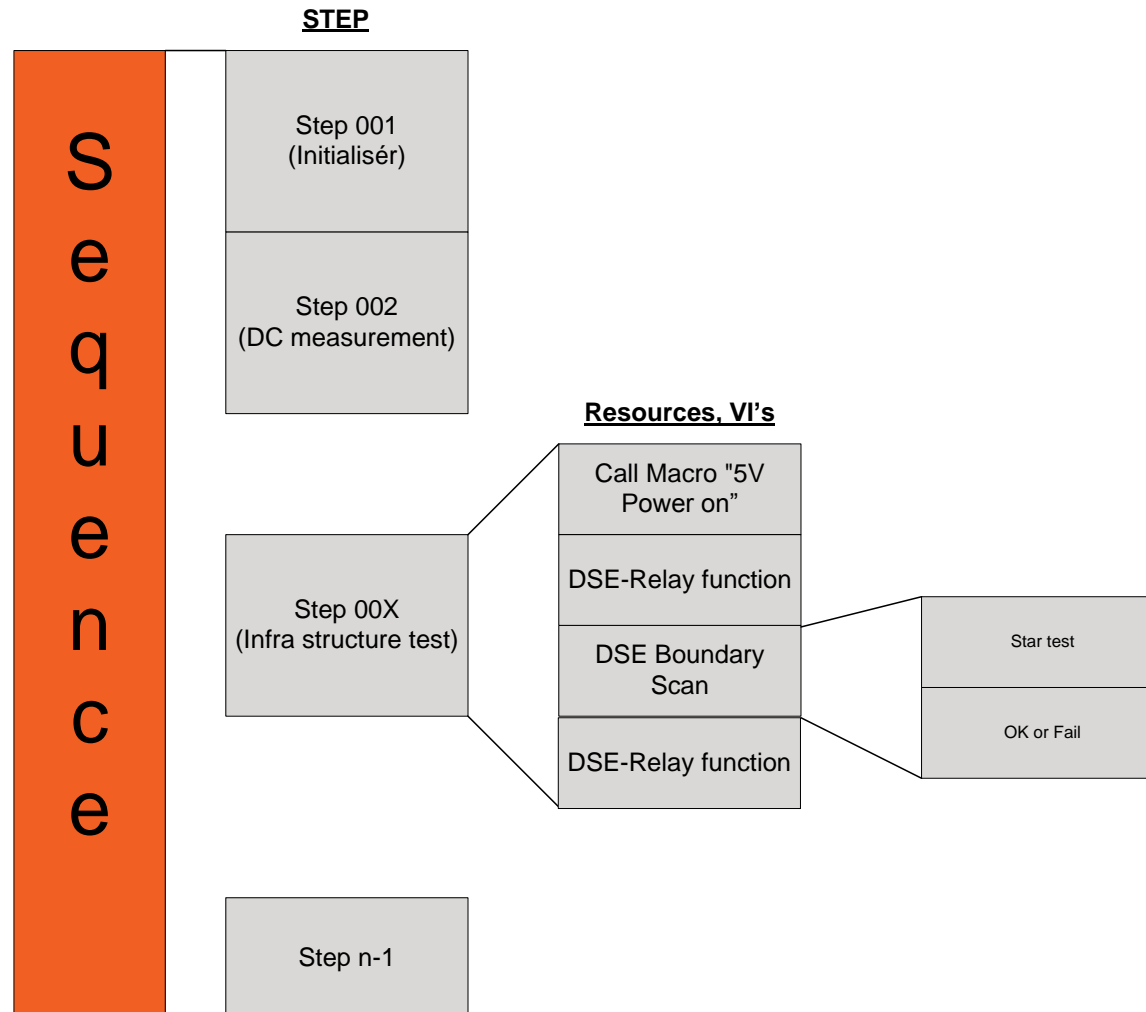


**[www.dse.dk](http://www.dse.dk)**

**DSE your gateway to a world of test technology**  
Software — Statistical analysis — Fixtures — Inline handling  
Boundary scan — Turnkey solutions

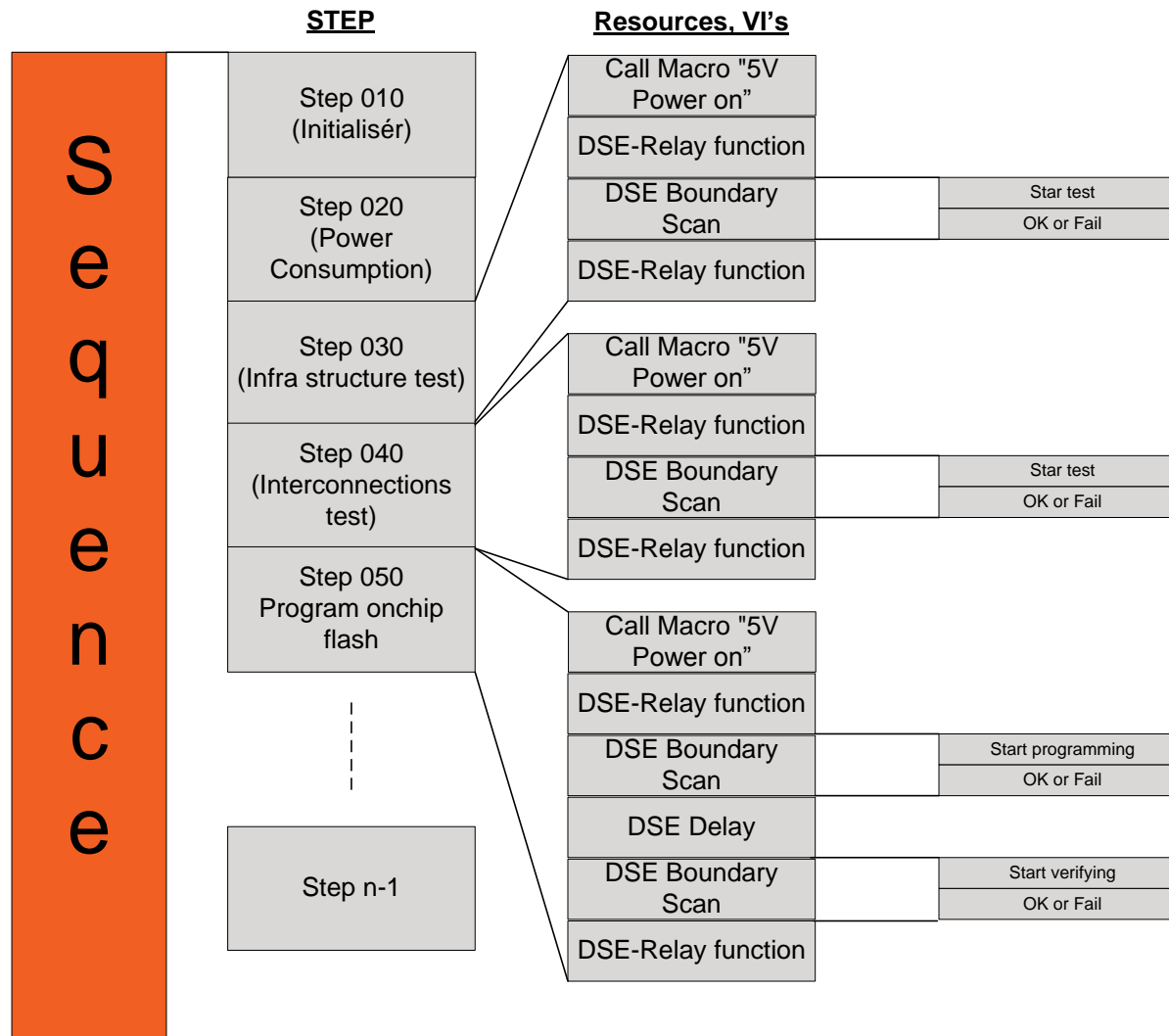
# DSE Test Engine

## Test sequence



# DSE Test Engine

## Test sequence



**Case:**

**ARM 9 only debug port**

**FPGA Boundary scan port**

**2 SPI flash 2MB**

**DDR2 RAM**

**NAND flash, bad block handling**

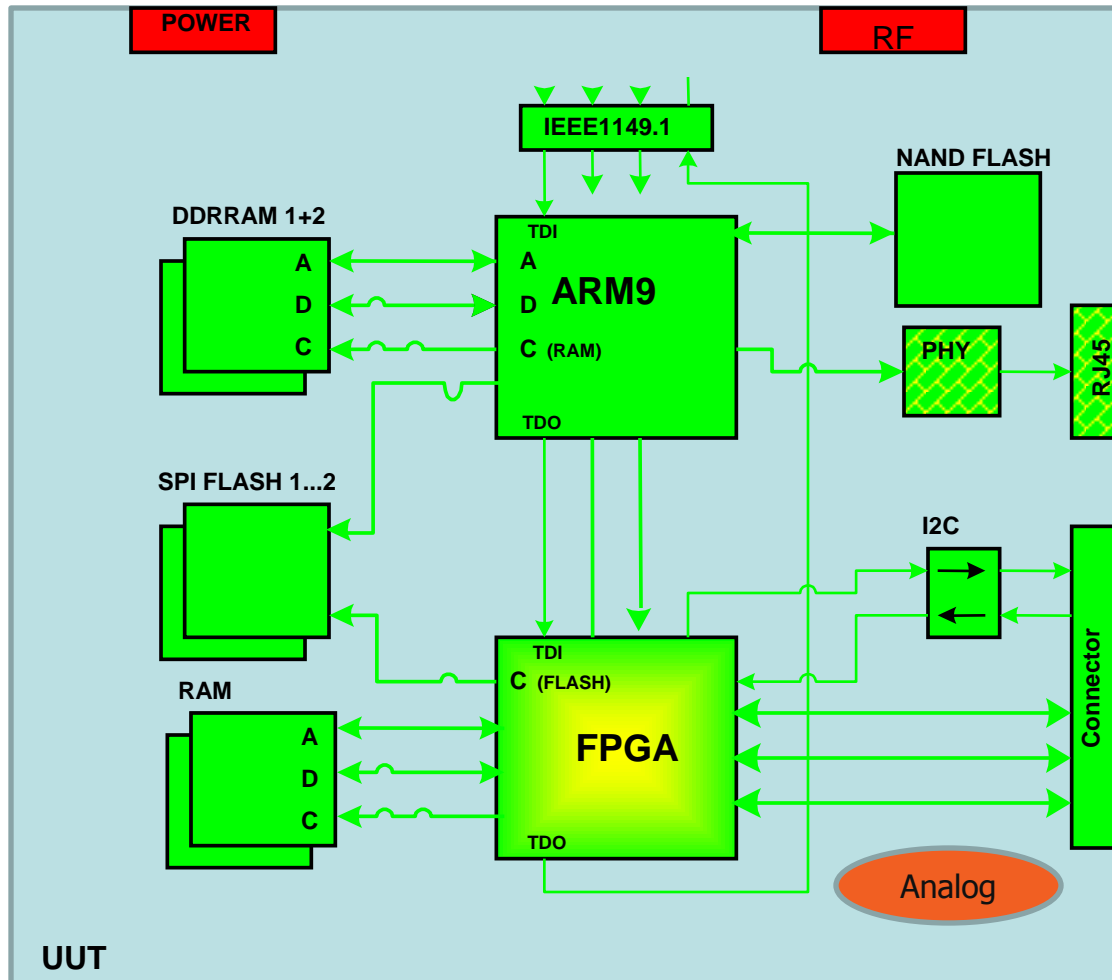
**RJ45 comm through PHY**

**Manual test I2C comm**

**Power measurements**

**Analog measurements**

**NO DEDICATED TESTSOFTWARE MADE!!!**



# Further information

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# Thank you for your attention!

