



NIDays

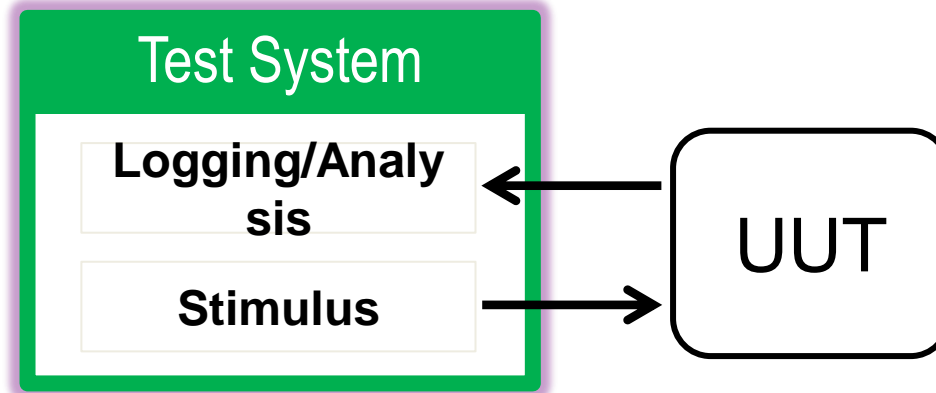
WORLDWIDE GRAPHICAL SYSTEM DESIGN
CONFERENCE



Introducing NI VeriStand for creating Hardware In the Loop Test Systems

Presenter name
NI-Days 2010

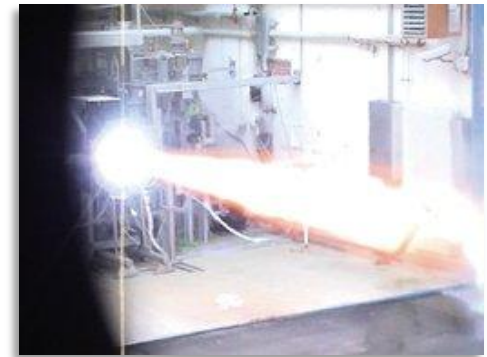
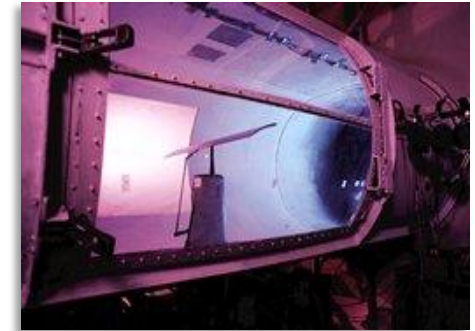
What Is Real-Time Testing?



The use of a real-time environment as part of a test system to increase performance or reliability.

Real-Time Testing Examples

- Stimulus – Response Testing
- Durability Testing
- Environmental Testing
- Wind Tunnel Testing
- Dynamometer Testing
- Hardware-in-the-Loop (HIL) Testing
- Model-in-the-Loop (MIL) Testing





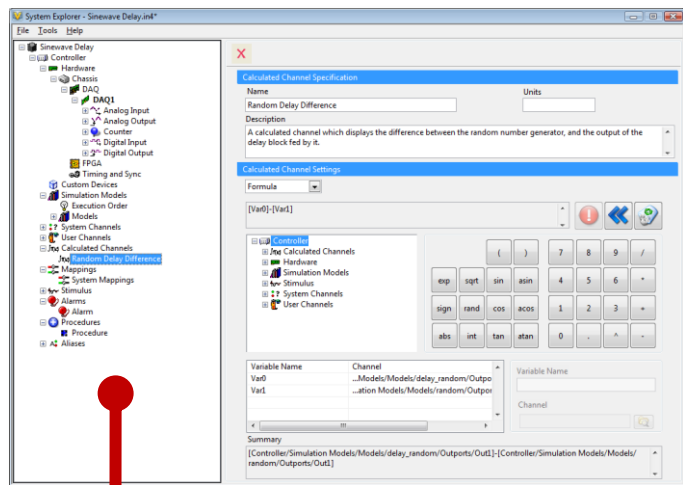
NI VeriStand™

Real-Time Testing and Simulation Software

- Stimulus Generation
- Data Logging
- Configurable I/O
- Alarming
- Calculated Channels
- Run-Time Editable User Interface
- User Management
- Multichassis Synchronization
- Closed-Loop Control
- Deterministic Model Execution

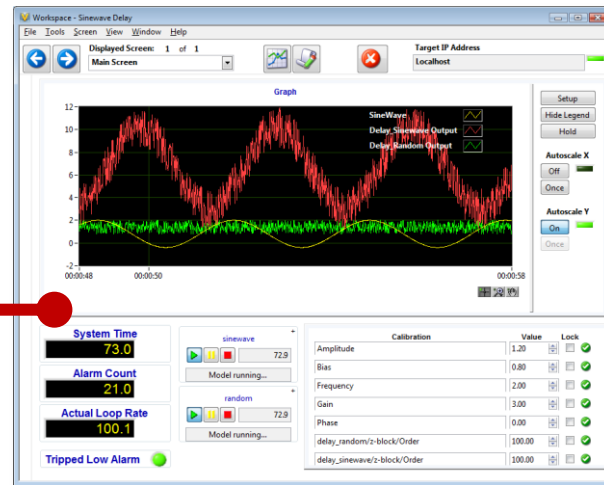


Configure Real-Time Application



I/O
Calc
Channel
Alarms
Controllers

Run-Time
Editable



Create UI at Run Time

Deploy Real-Time Stimulus/Logging Profiles

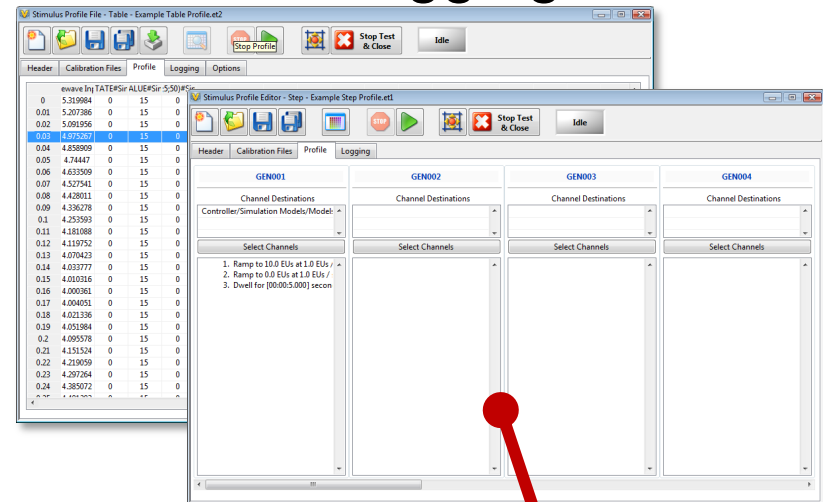
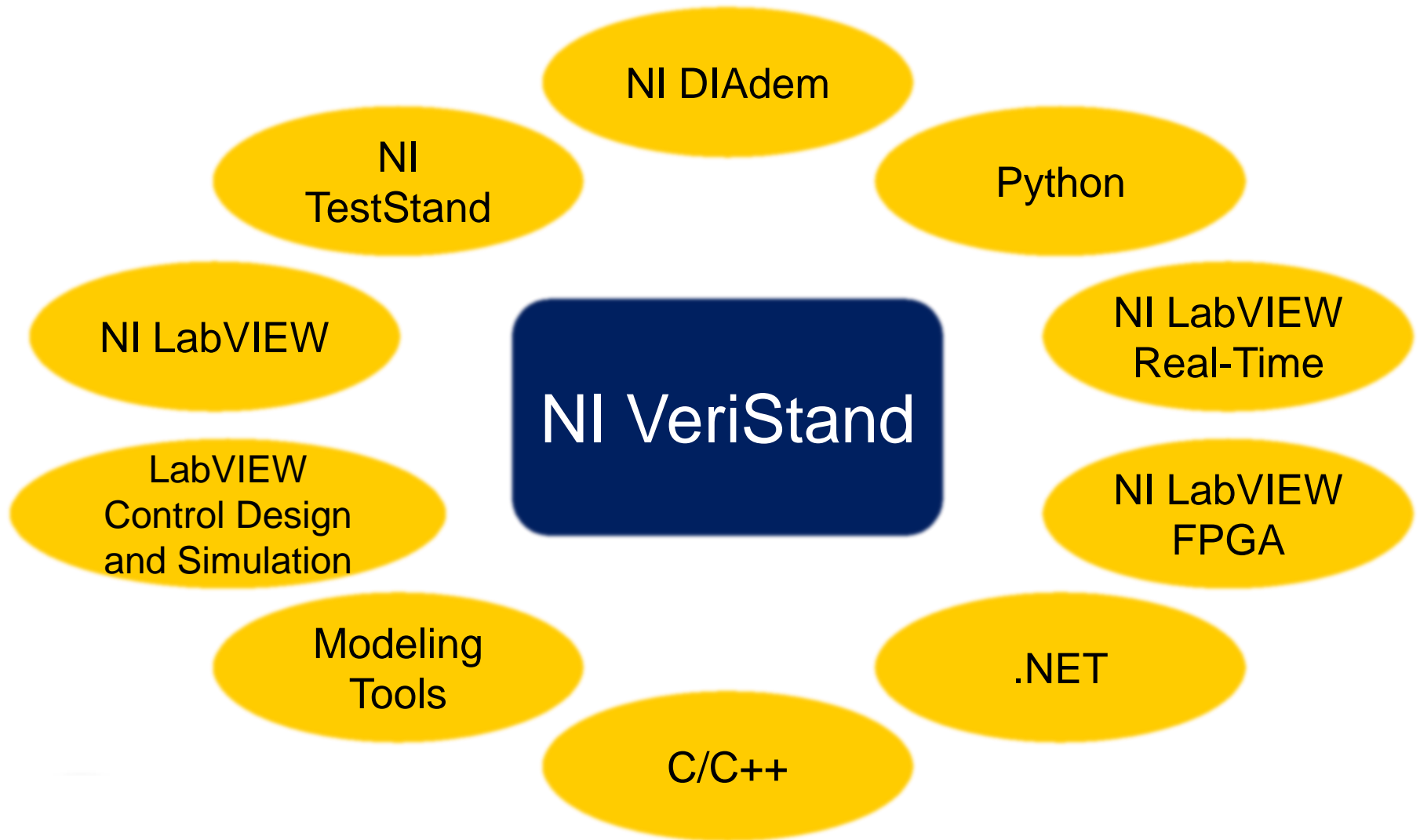


Table- and Step-Based
Stimulus

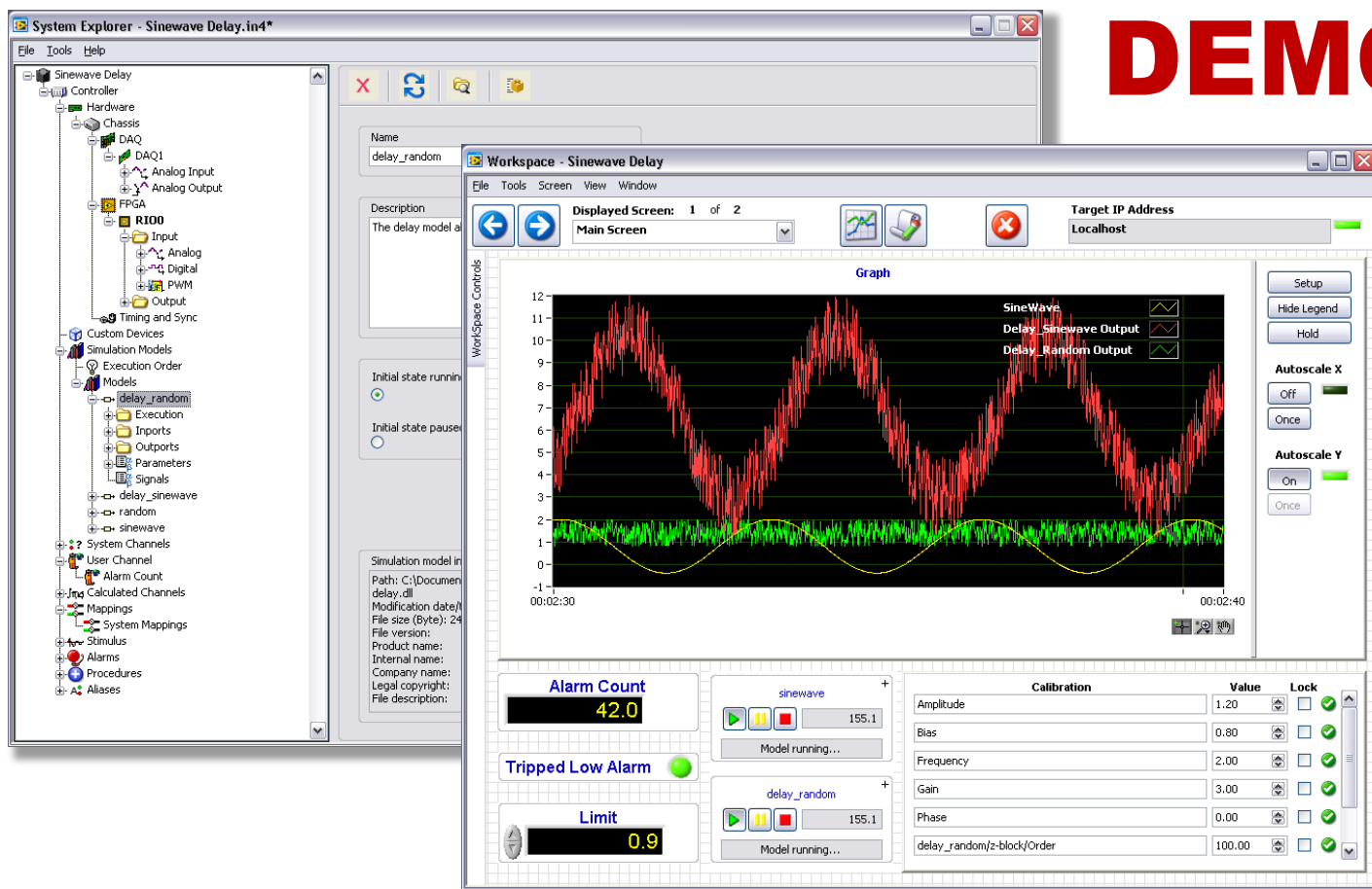
Open Software Environment



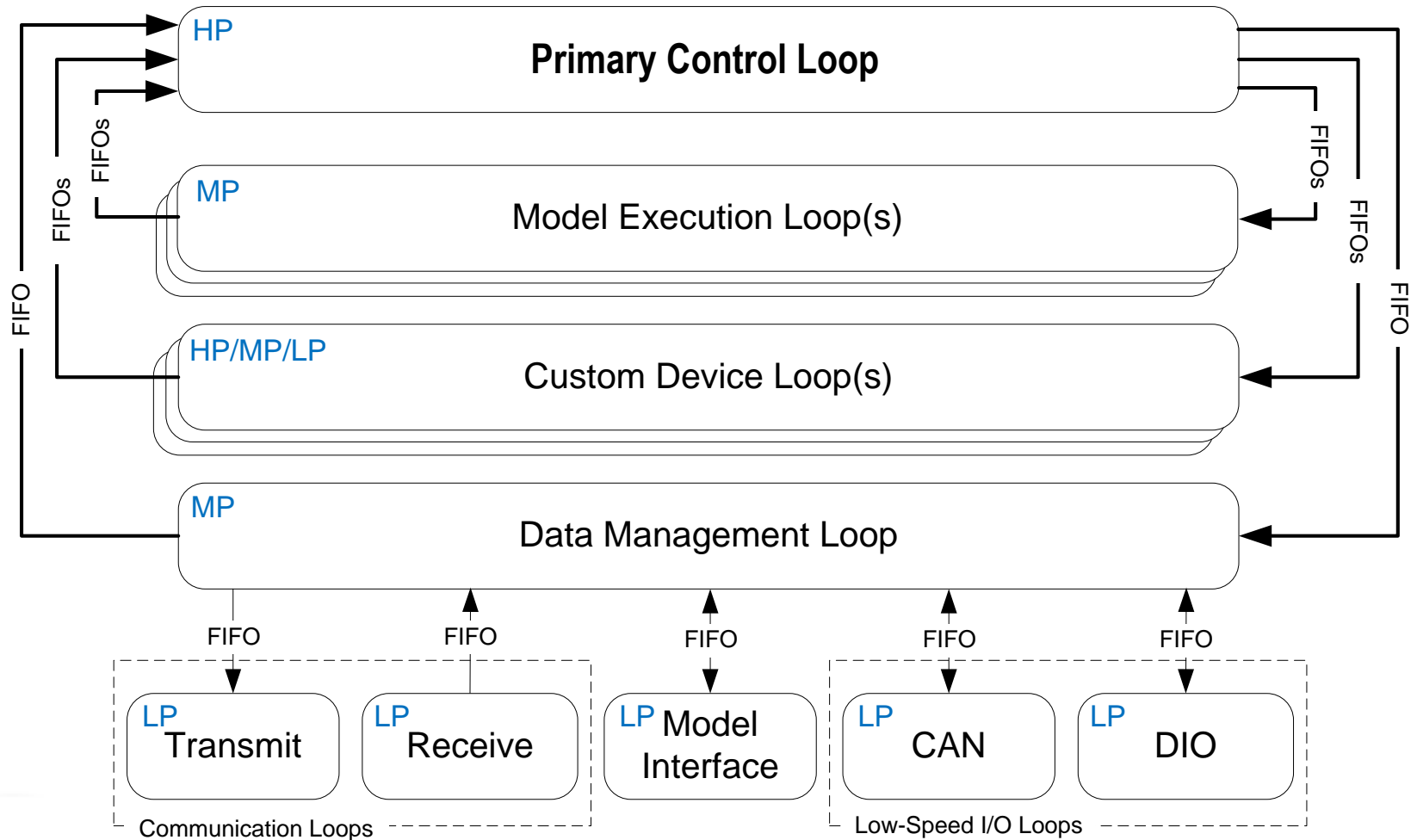
NI VeriStand™

Real-Time Testing and Simulation Software

DEMO



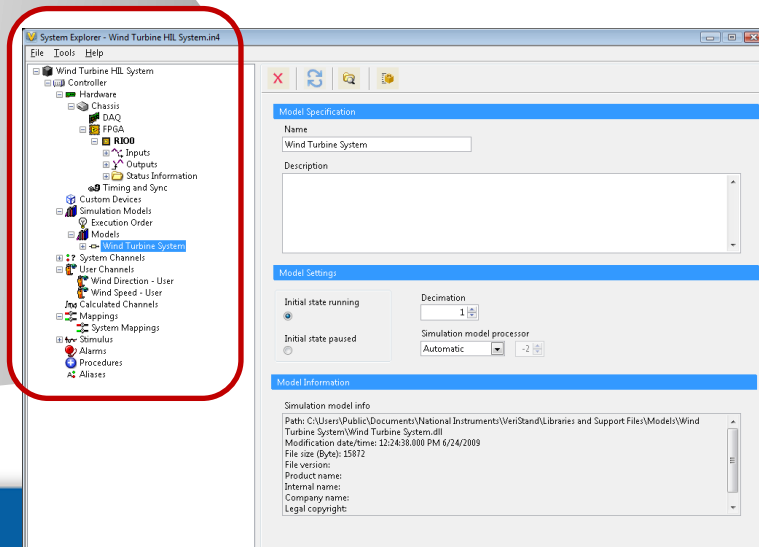
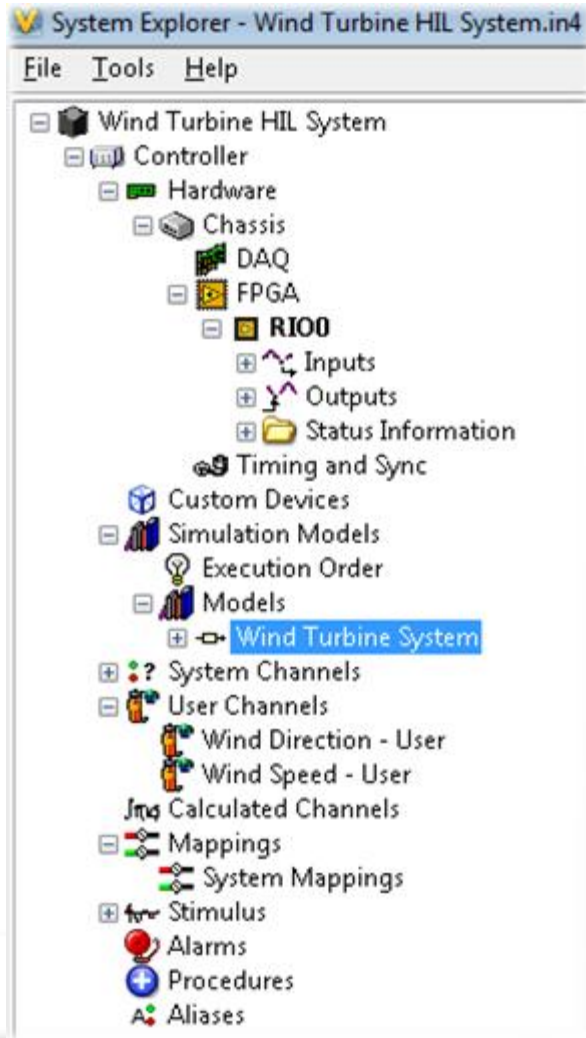
NI VeriStand Engine Architecture



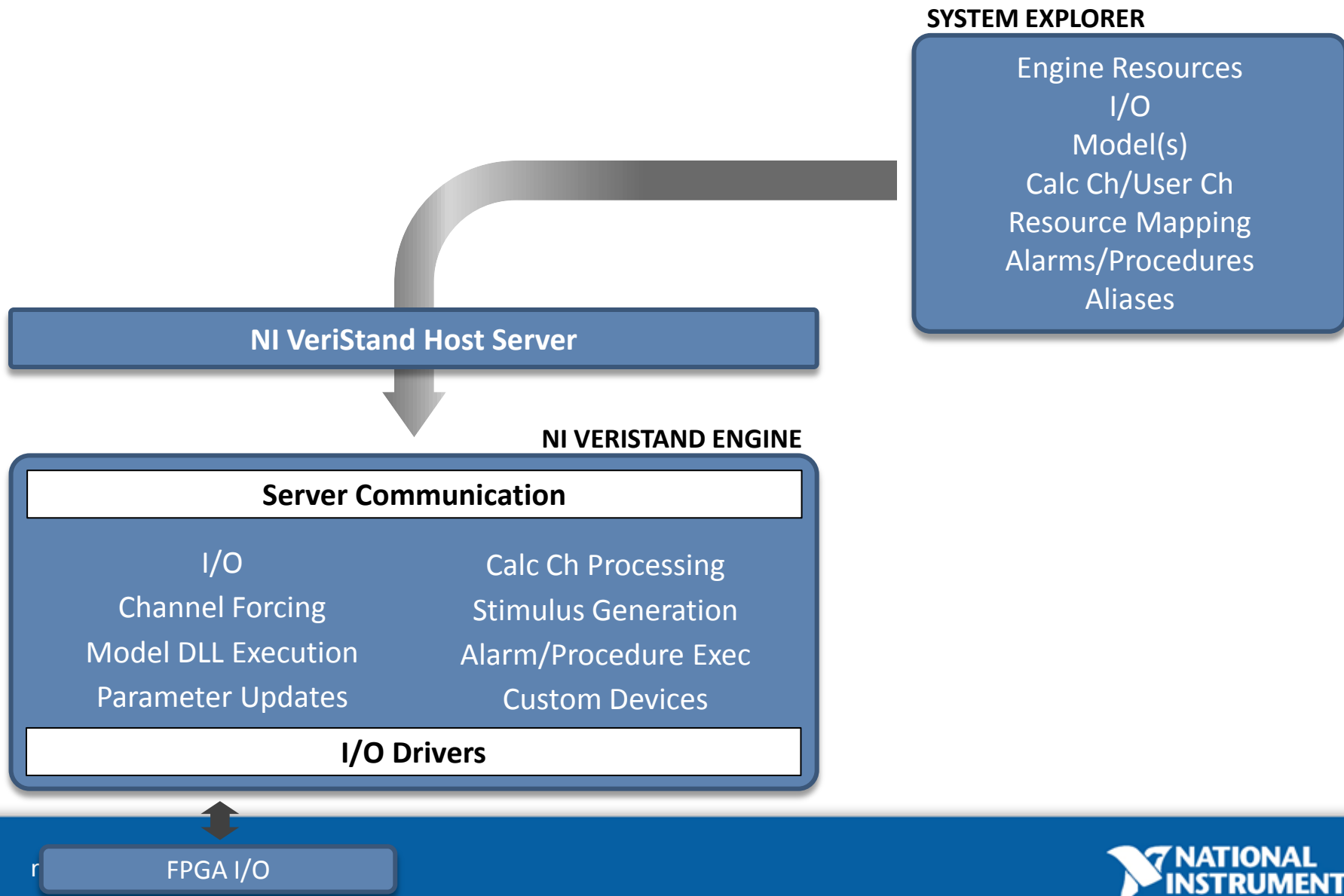
NI VeriStand Framework

SYSTEM EXPLORER

Engine Resources
I/O
Model(s)
Calc Ch/User Ch
Resource Mapping
Alarms/Procedures
Aliases

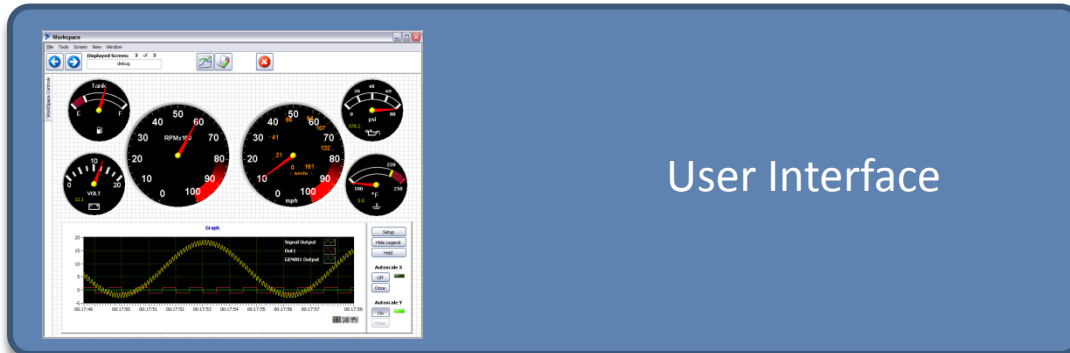


NI VeriStand Framework



NI VeriStand Framework

WORKSPACE



NI VeriStand Host Server



NI VERISTAND ENGINE

Server Communication

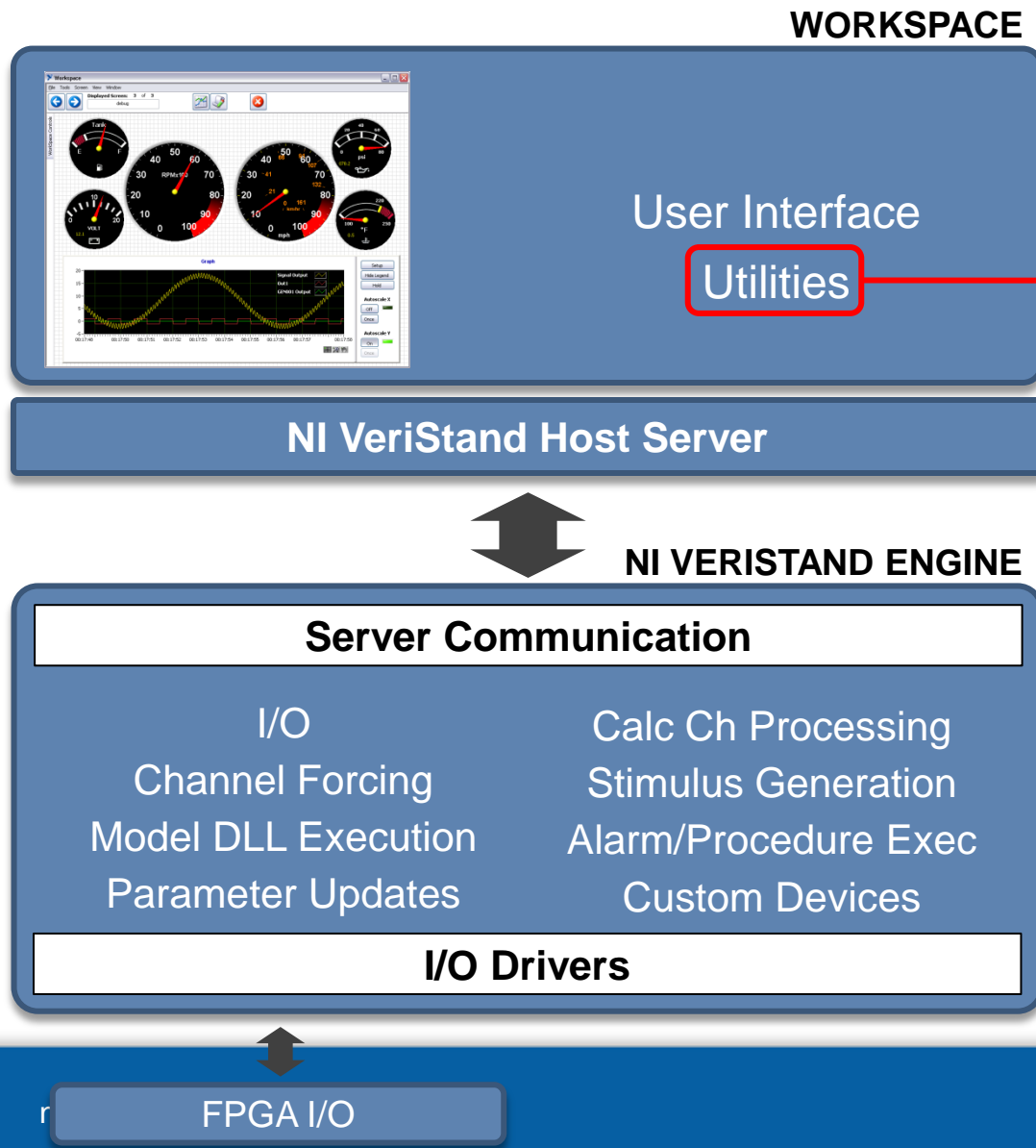
I/O	Calc Ch Processing
Channel Forcing	Stimulus Generation
Model DLL Execution	Alarm/Procedure Exec
Parameter Updates	Custom Devices

I/O Drivers



FPGA I/O

NI VeriStand Framework



OBSERVE

- Alarm Monitor
- CAN Bus Monitor
- Channel Data Viewer
- TDMS File Viewer
- Real-Time Consol Viewer

ACTION

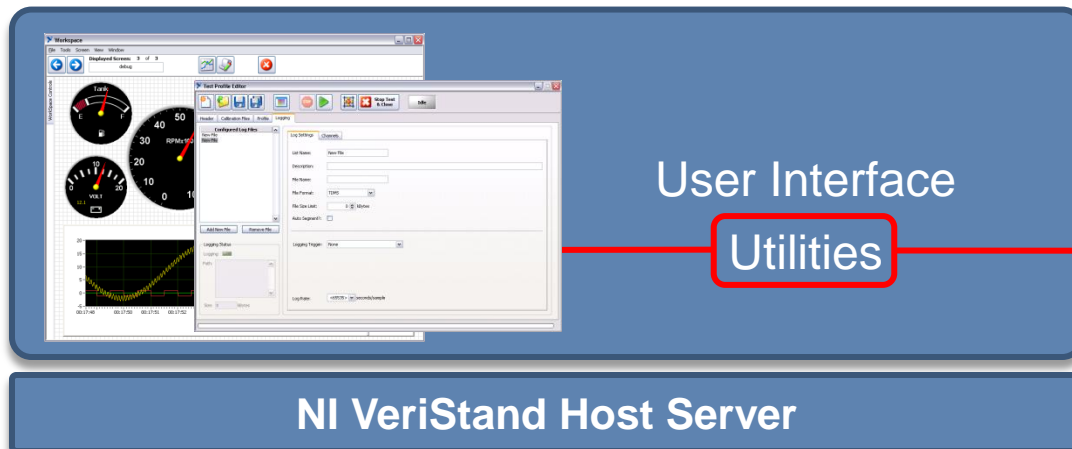
- Channel Scaling and Calibration
- Channel Value Forcing
- Stimulus Profile Editor

CONFIGURATION

- Model Parameter Manager
- Alarm Manager

NI VeriStand Framework

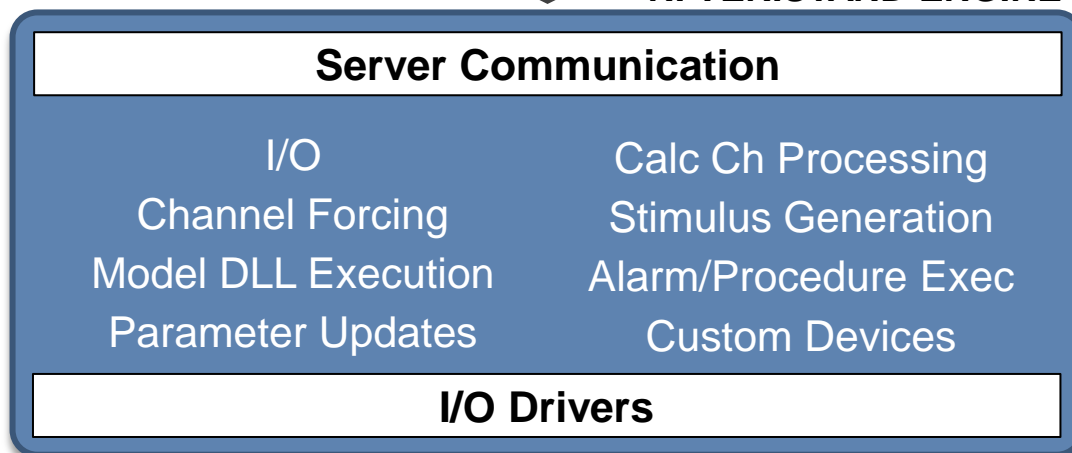
WORKSPACE



STIMULUS PROFILE EDITOR

- Profile Setup
- Load Model Parameters
- Stimulus Profiles
- Data Logging

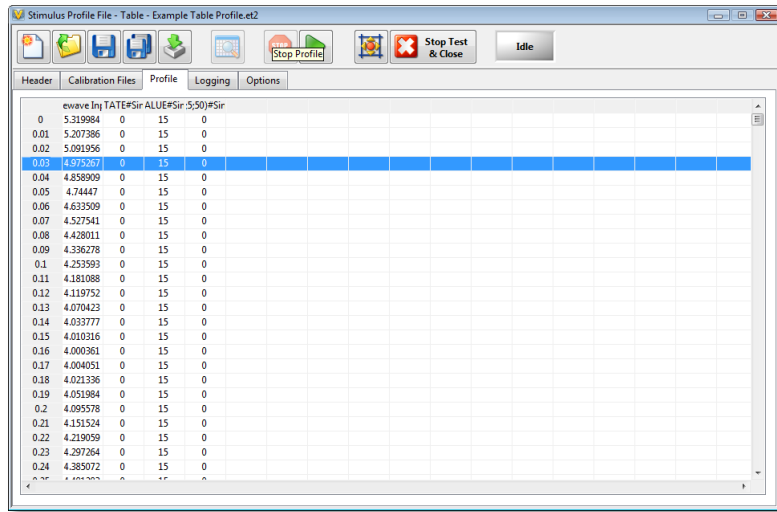
NI VERISTAND ENGINE



FPGA I/O

NI VeriStand Stimulus Profiles

Stimulus Profile File - Table - Example Table Profile.et2



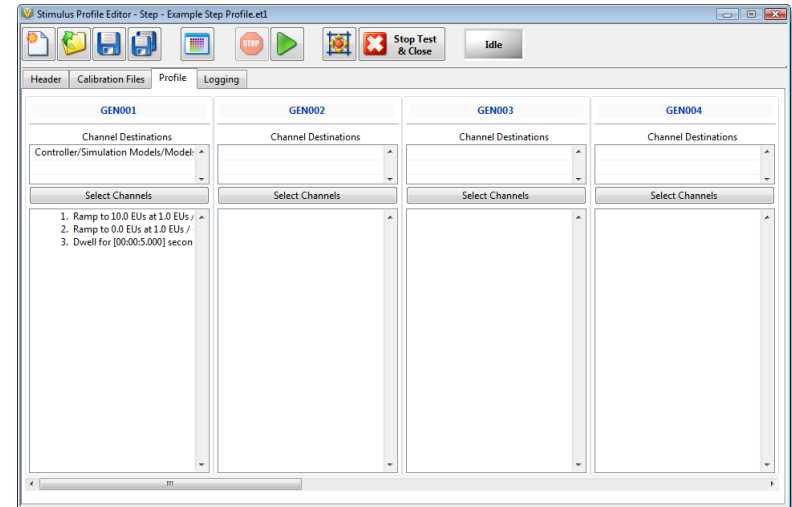
Header Calibration Files Profile Logging Options

ewave Inj TATE#Sir ALUE#Sir :5:50)#Sir

0	5.319984	0	15	0
0.01	5.207386	0	15	0
0.02	5.091956	0	15	0
0.03	4.979267	0	15	0
0.04	4.858909	0	15	0
0.05	4.744447	0	15	0
0.06	4.633509	0	15	0
0.07	4.527541	0	15	0
0.08	4.428011	0	15	0
0.09	4.336278	0	15	0
0.1	4.253593	0	15	0
0.11	4.181088	0	15	0
0.12	4.119752	0	15	0
0.13	4.070423	0	15	0
0.14	4.033777	0	15	0
0.15	4.010316	0	15	0
0.16	4.000361	0	15	0
0.17	4.004051	0	15	0
0.18	4.021336	0	15	0
0.19	4.051984	0	15	0
0.2	4.095578	0	15	0
0.21	4.151524	0	15	0
0.22	4.219059	0	15	0
0.23	4.297264	0	15	0
0.24	4.385072	0	15	0

Table-Based Stimulus Profiles

Stimulus Profile Editor - Step - Example Step Profile.et1



Header Calibration Files Profile Logging

GEN001 GEN002 GEN003 GEN004

Channel Destinations

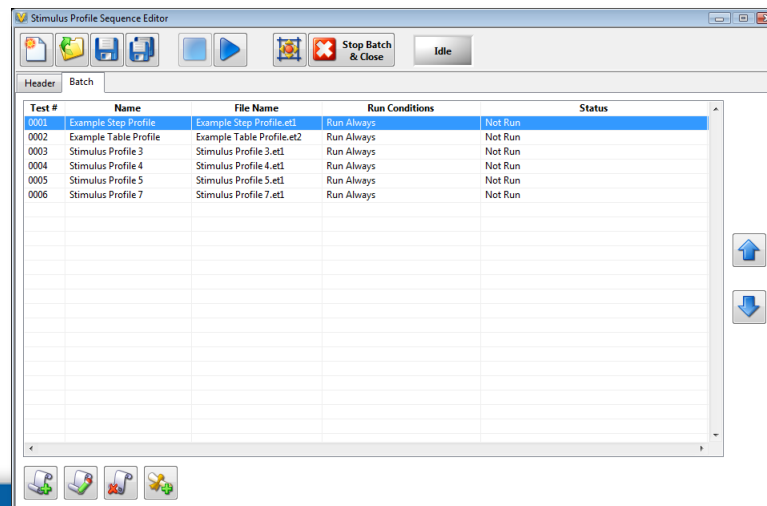
Controller/Simulation Models/Model:

Select Channels

1. Ramp to 10.0 EUs at 1.0 EUs /
2. Ramp to 0.0 EUs at 1.0 EUs /
3. Dwell for [00:00:5.000] second

Step-Based Stimulus Profiles

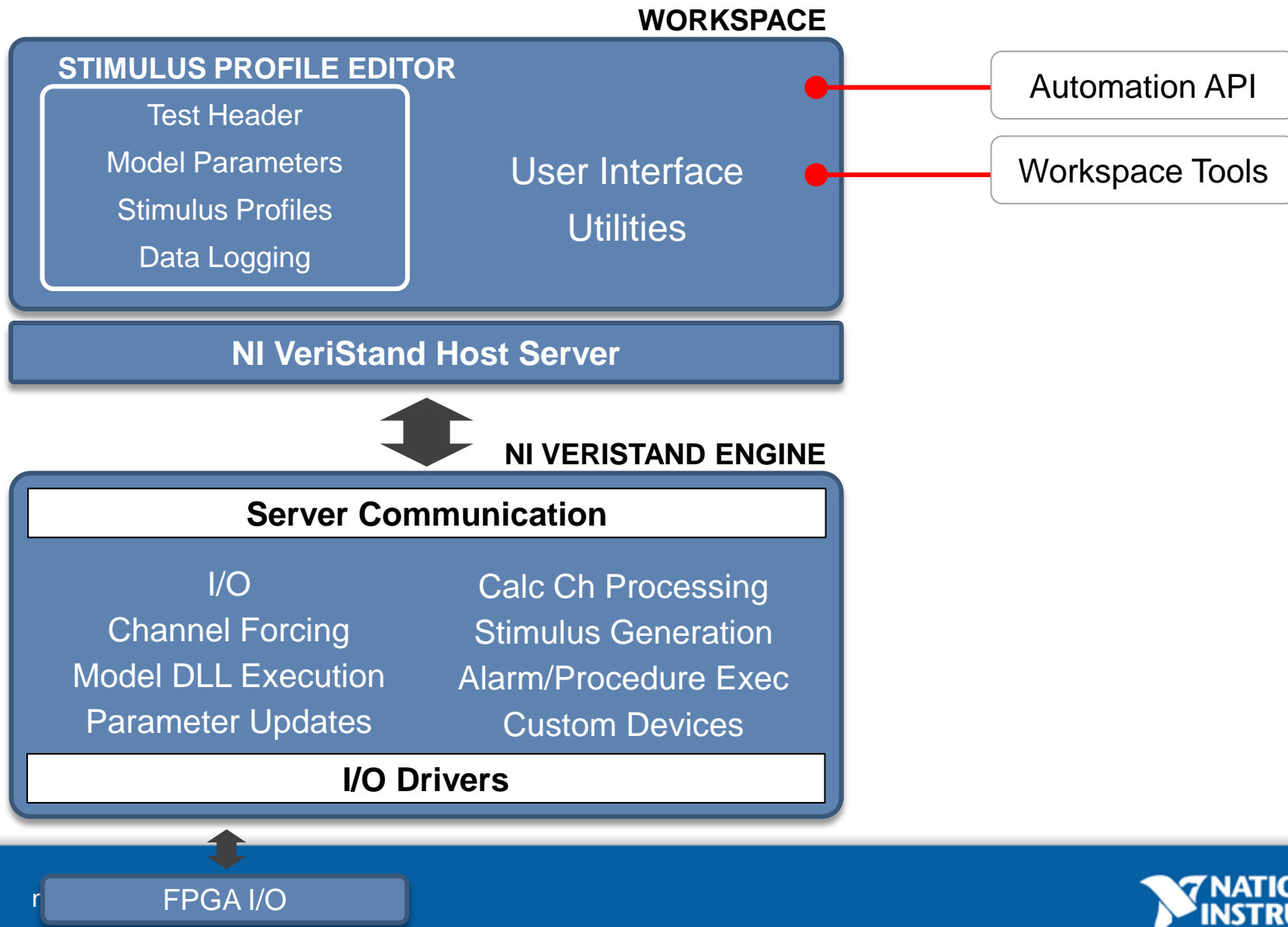
Stimulus Profile Sequence Editor



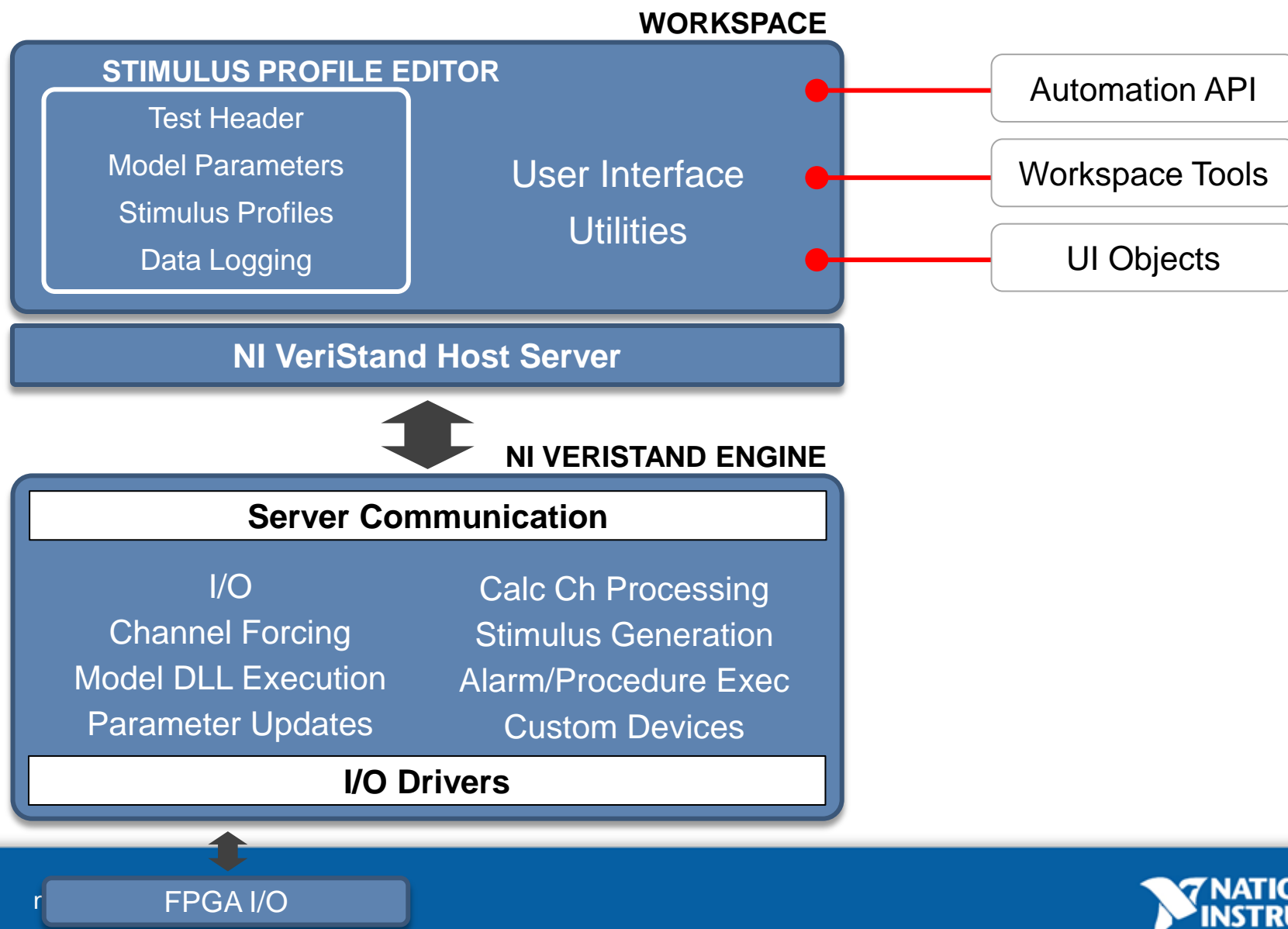
Header Batch

Test #	Name	File Name	Run Conditions	Status
0001	Example Step Profile	Example Step Profile.et1	Run Always	Not Run
0002	Example Table Profile	Example Table Profile.et2	Run Always	Not Run
0003	Stimulus Profile 3	Stimulus Profile 3.et1	Run Always	Not Run
0004	Stimulus Profile 4	Stimulus Profile 4.et1	Run Always	Not Run
0005	Stimulus Profile 5	Stimulus Profile 5.et1	Run Always	Not Run
0006	Stimulus Profile 7	Stimulus Profile 7.et1	Run Always	Not Run

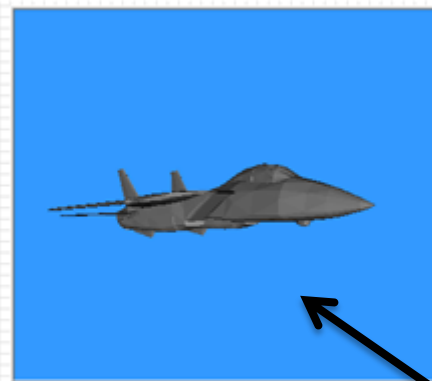
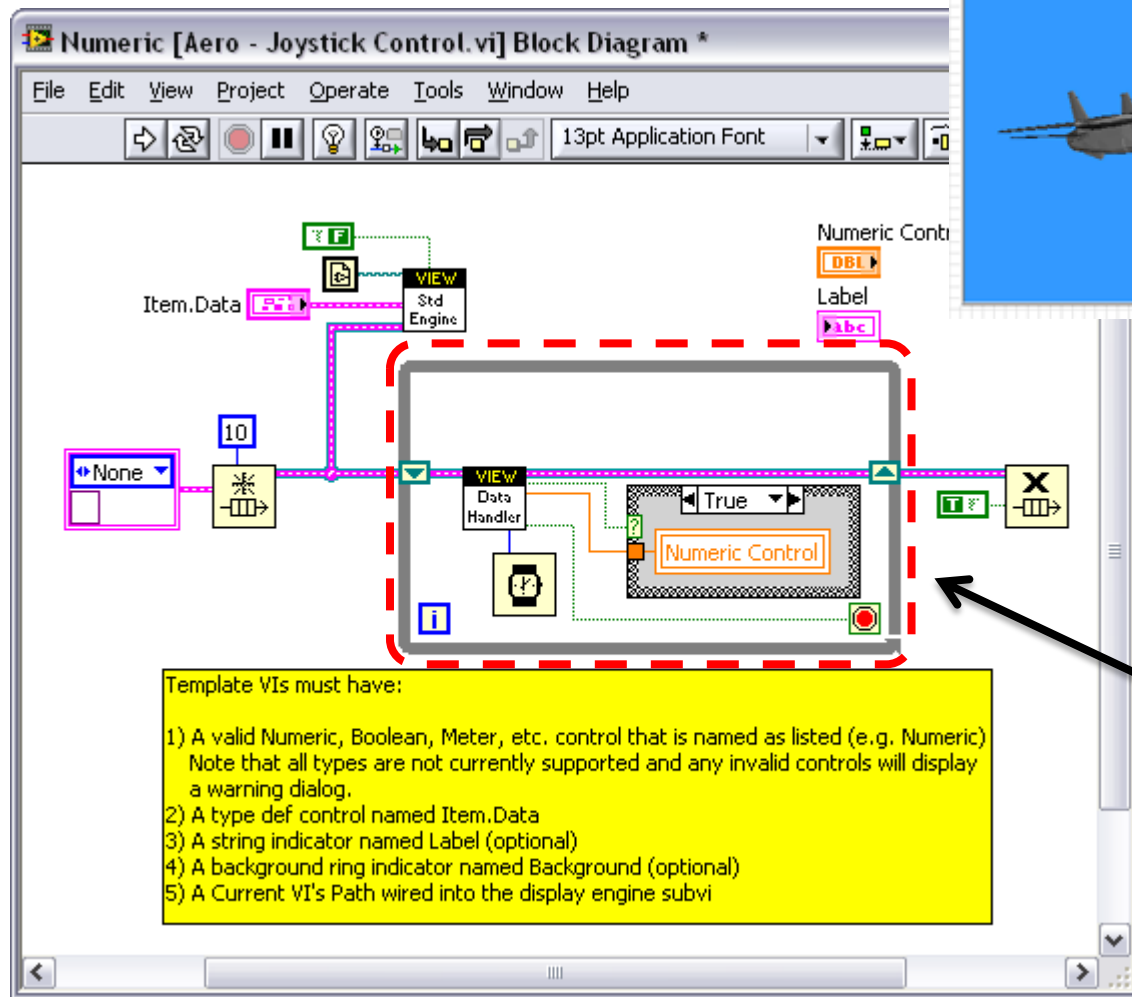
NI VeriStand Customization



NI VeriStand Customization



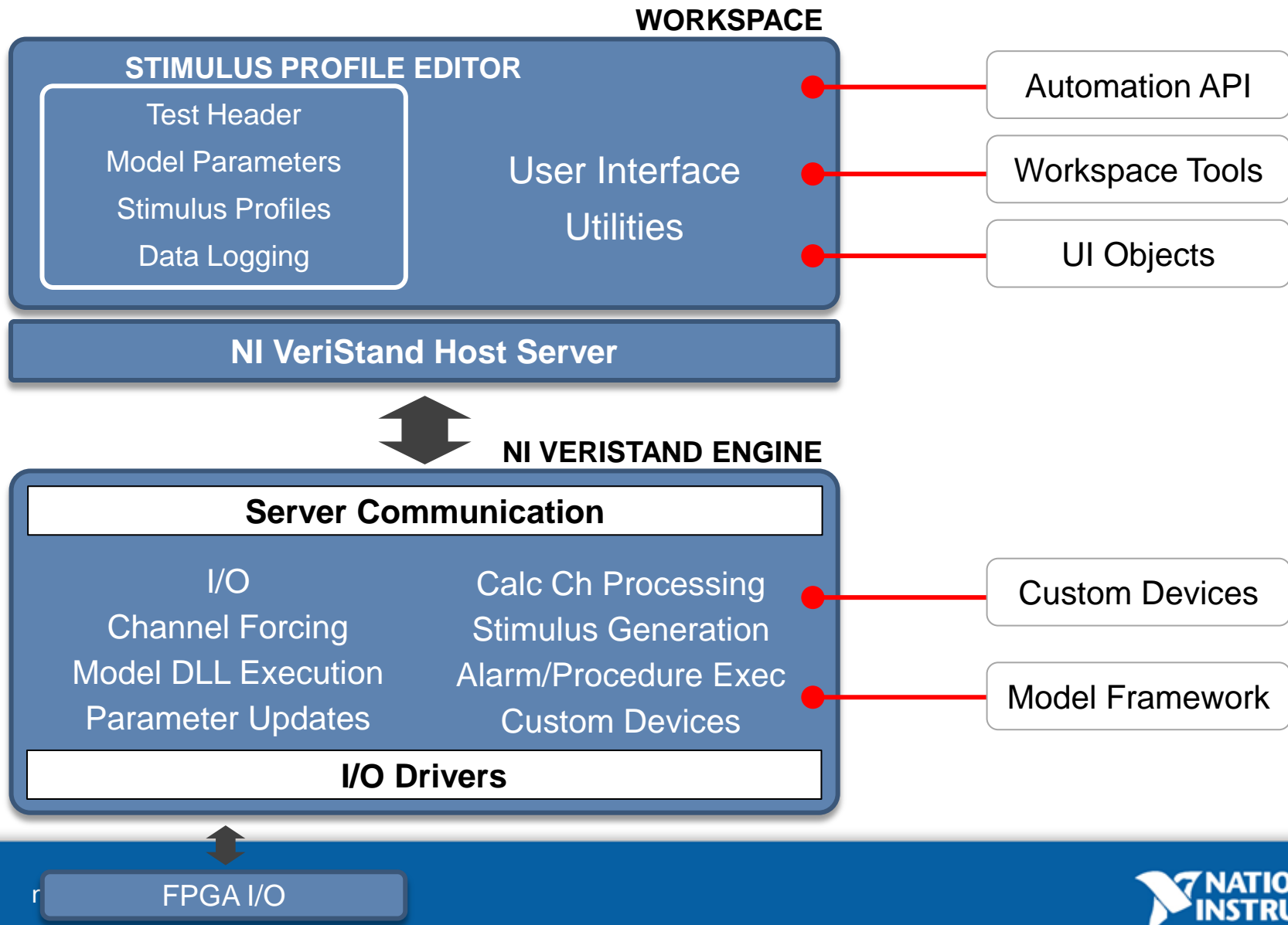
Custom UI Object



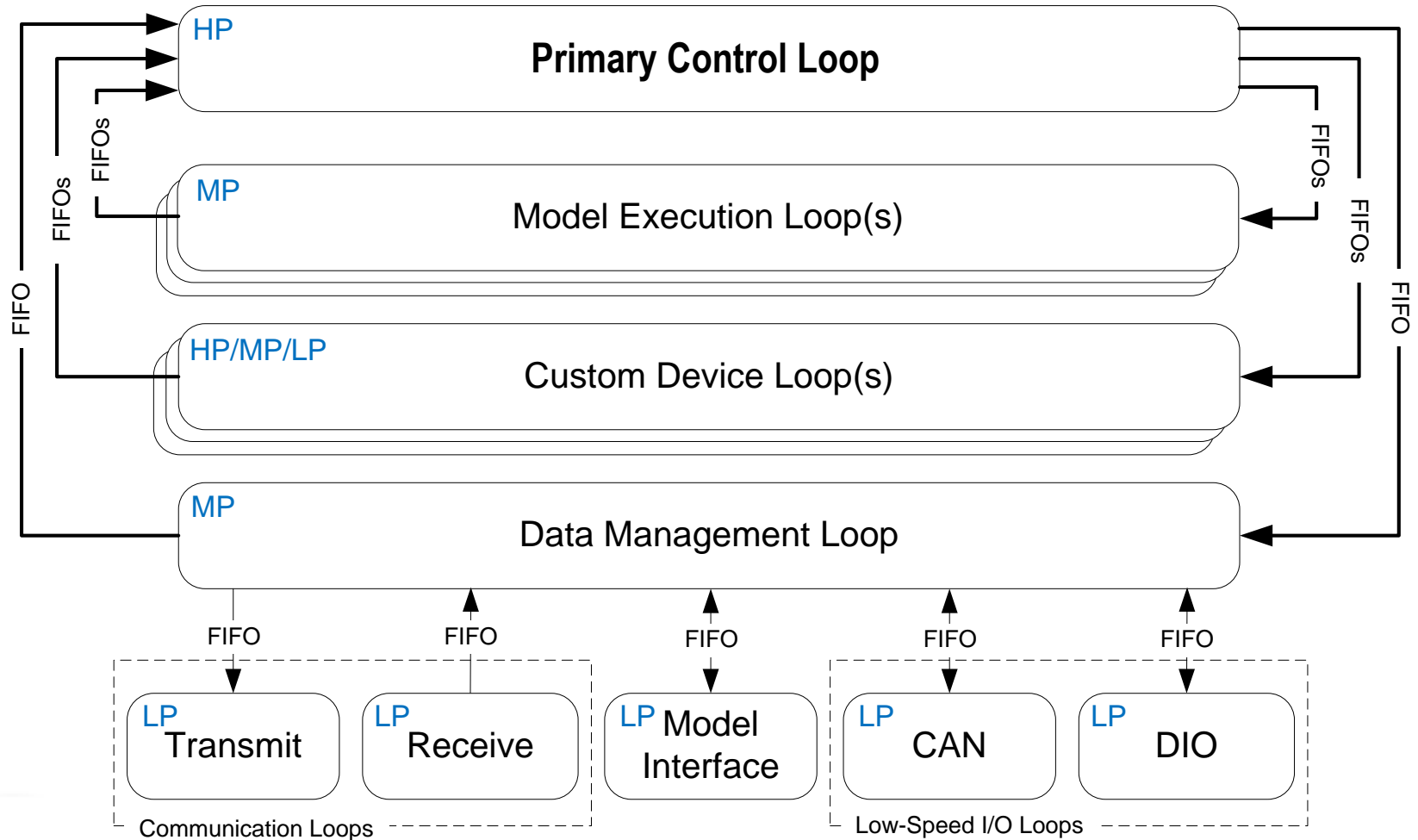
Create custom UI object

Add custom functionality

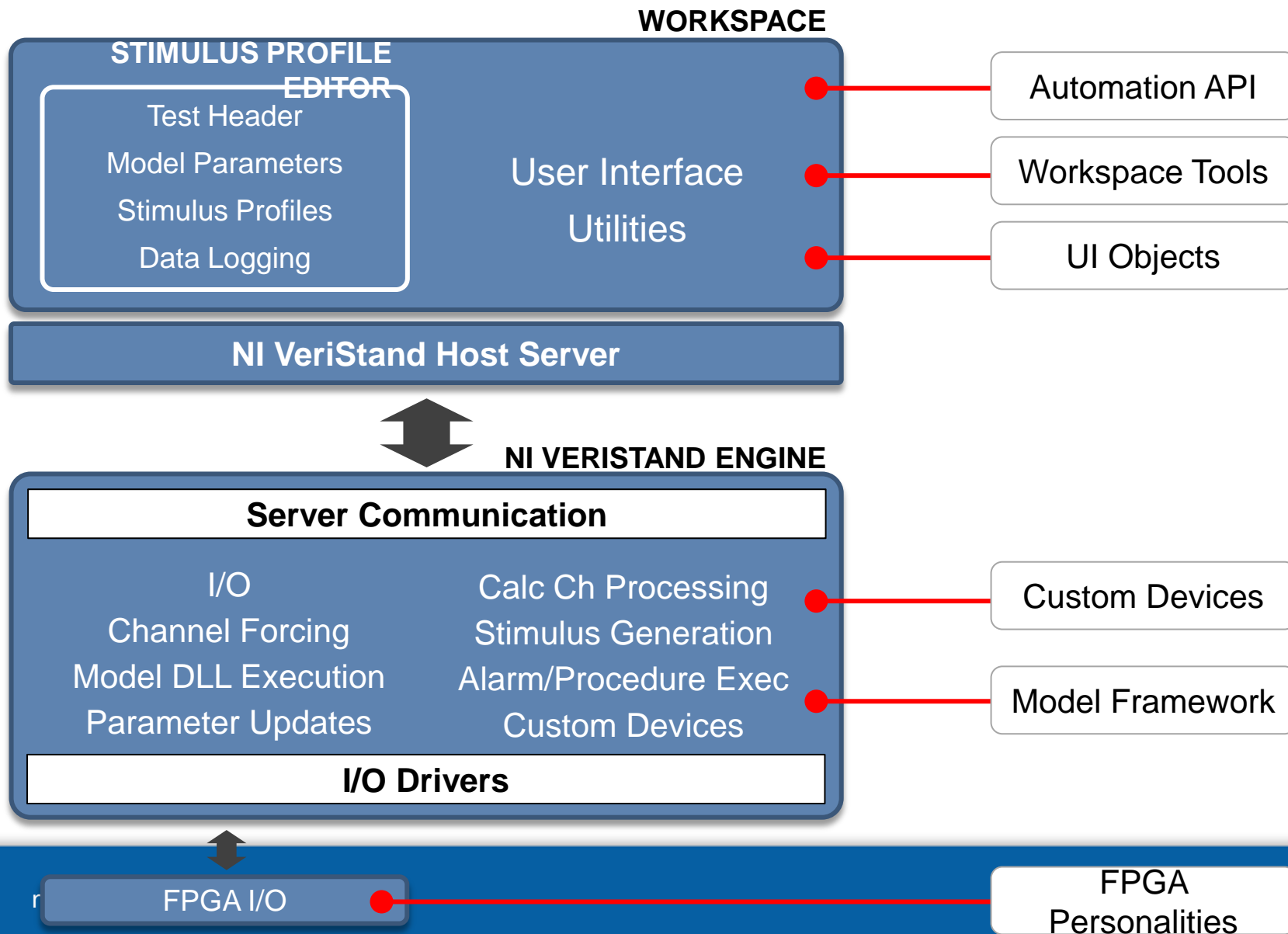
NI VeriStand Customization



NI VeriStand Engine Architecture

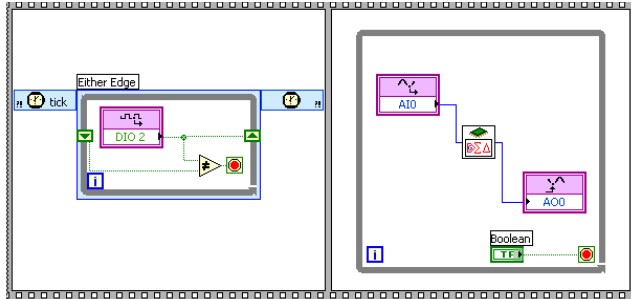


NI VeriStand Customization

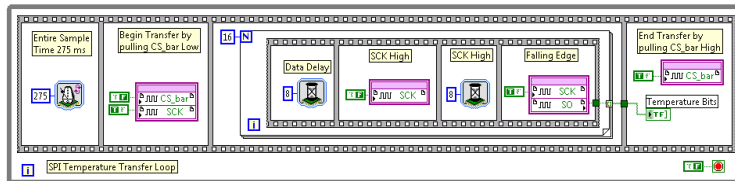


Custom FPGA Personalities

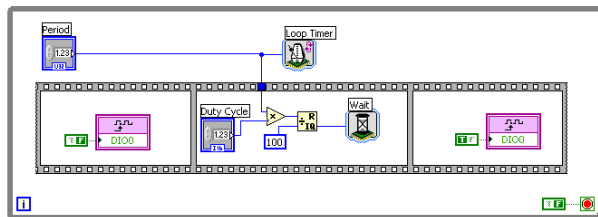
Timing and Synchronization



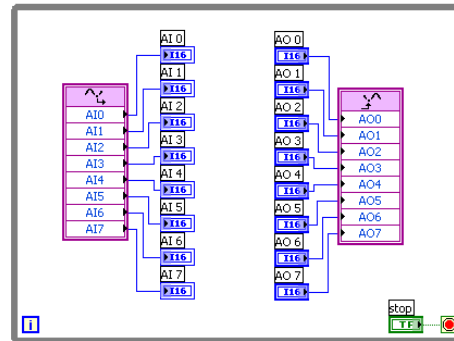
Digital Protocols



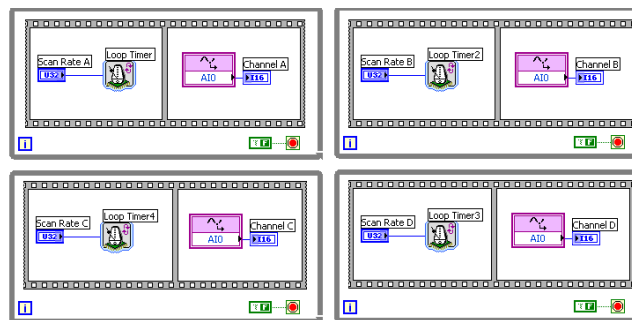
PWM



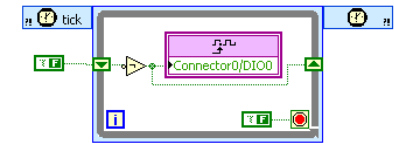
Analog I/O



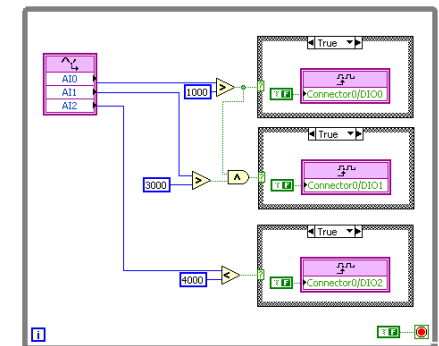
Multirate/Async I/O



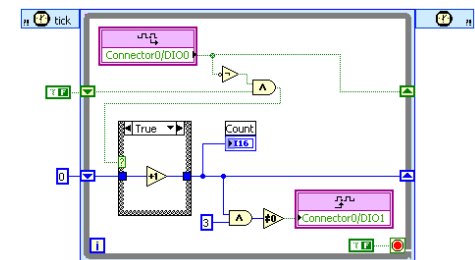
Clocks



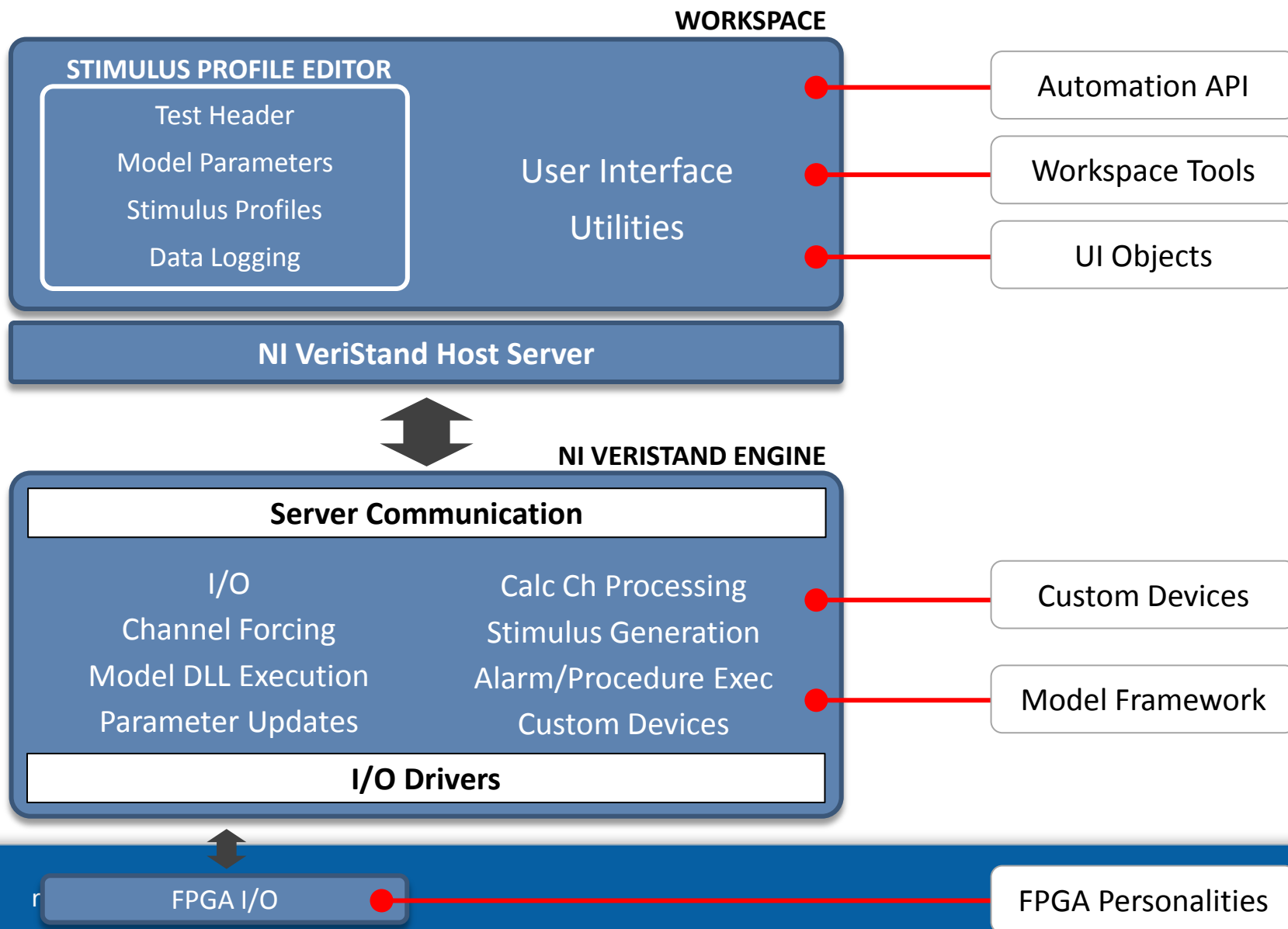
Triggering



Counters



NI VeriStand Customization



Hardware Support



Real-Time PXI

- Most NI-DAQmx Devices (inc NI X Series and SCXI)
- NI R Series Devices
- NI CAN Devices
- Goepel LIN Interface



Real-Time PC



Real-Time Industrial Controller

- Lambda Power Supply
- NI Timing and Sync
- NI-XNET Devices
- NI FIU Devices
- *Custom Devices*



Windows PC*

* I/O Support through *Custom Devices* only

Supported Modeling Environments

Supported

- The MathWorks, Inc. Simulink® software
- LabVIEW Control Design and Simulation
- MapleSim models from Maplesoft
- SimulationX from ITI
- Tesis DYNA models
- NI MATRIXx SystemBuild
- Esterel SCADE Suite
- C/C++
- FORTRAN

In Work

- CarSim from Mech Sim Corp.
- GT-POWER engine models from Gamma Technologies Inc.
- AMESim models from LMS
- WaveRT from Ricardo
- VI-grade models
- Visual Solutions (VisSim)
- Dynasim models from Dymola

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Additional Resources

ni.com/veristand

- Demonstration Videos
- Getting Started Resources
- White Papers
- Add-Ons
- Download Evaluation Version
- NI-Days Hands-On session, starting at __:__