
ENGINEER
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Prototypisierung für Autonomes Fahren – Test von Automotive Ethernet (AVB/TSN)

AED Engineering

Engineer Testsysteme

Peter Förster

Engineer Interne R&D

Tobias Rummel

Agenda

- AED Engineering
  - Reference Projects R&D
  - Reference Projects Test Systems
- AED PXIe FPGA Card
  - HW Setup
  - Functionality
  - Possible Use Cases
- TSN Interfaces
  - Challenges for TSN Validation
  - HW Setup
  - Possible Test Scenarios

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Im Jahr 2006 von Geschäftsführer Carlos Urquizar aus Freude an Elektrik- und Elektronikentwicklung gegründet, spielt auch heute noch die Begeisterung unserer Mitarbeiter für ihre Arbeit die entscheidende Rolle. Diese Begeisterung bringen unsere Spezialisten auch in Ihre Entwicklung ein. So entsteht das Ergebnis, das Ihnen einen Wettbewerbsvorteil bringt.

Wir bieten.

In-House-Entwicklung und technisches Consulting im Bereich Elektronikentwicklung

Wir beraten.

Die Branchen Luft- und Raumfahrt, Automotive, Nachrichtentechnik,
Mess- und Regelungstechnik

Wir forschen.

In dem Bereich der Informations- und Kommunikationstechnik

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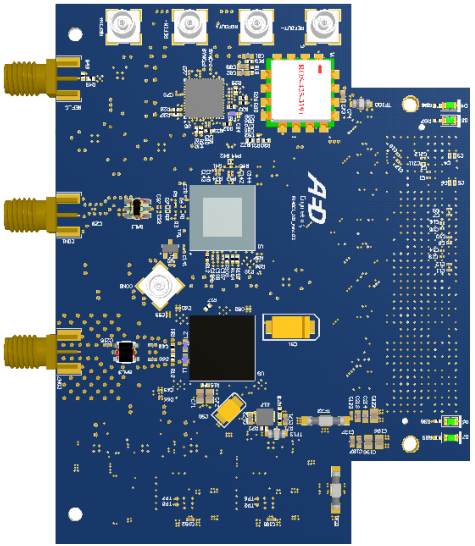
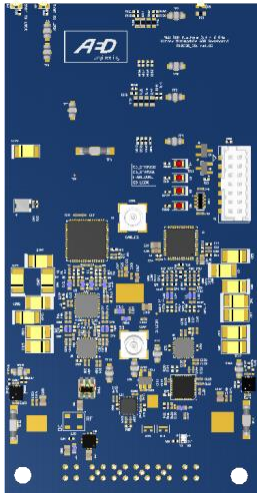
R&D Examples

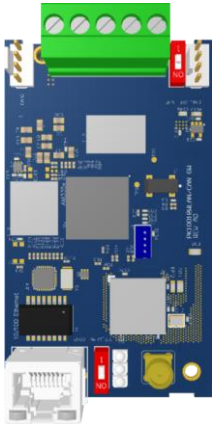
Cognitive-Software-Defined-Radio-Platform



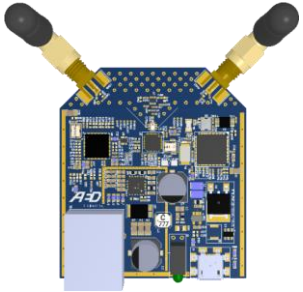
Multichannel Coordinator



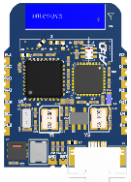
Multi-Protocol-Module



IEEE 802.15.4 Gateway



Ultra Low Power Wireless Sensor



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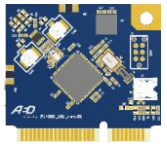

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Areas of Expertise

- LabVIEW
  - RT, FPGA
- Optical Inspection/Machine Vision
- VeriStand
- Component Testing
- Automotive

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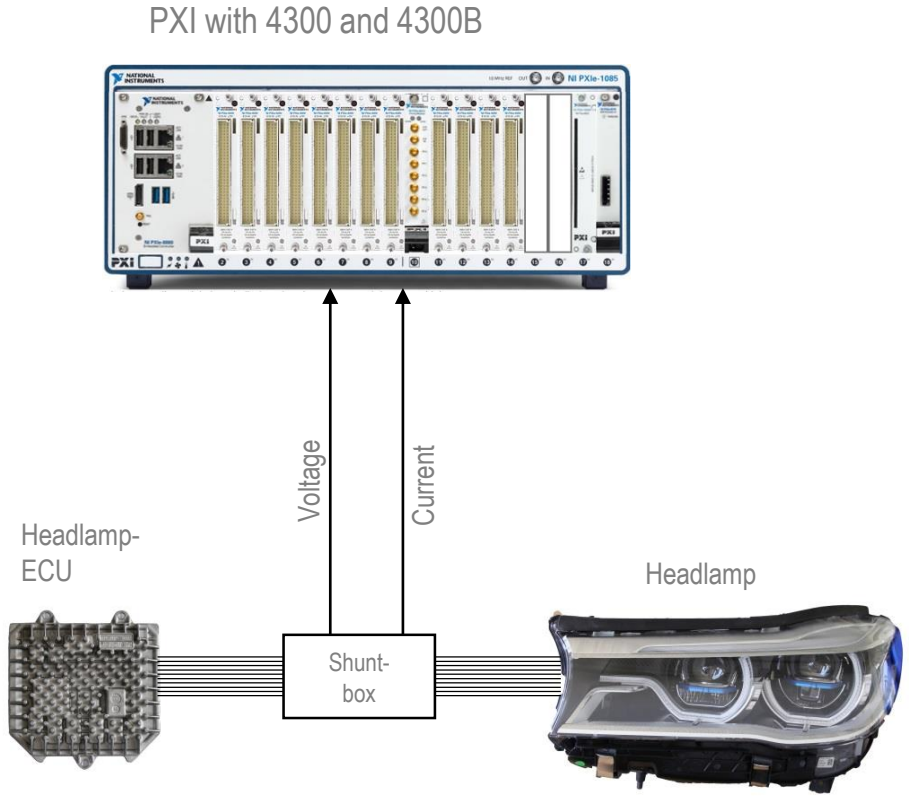
Headlamp Test System

- Evaluation of LED Channels
- Exact analysis of Signals
  - Voltage
  - Current
  - Duty Cycle
  - Overshoots
- Simulated or real loads
- FPGA Coprocessing of 240 Channels at 250 kS/s



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PXIe Peripherie Module FMC Carrier

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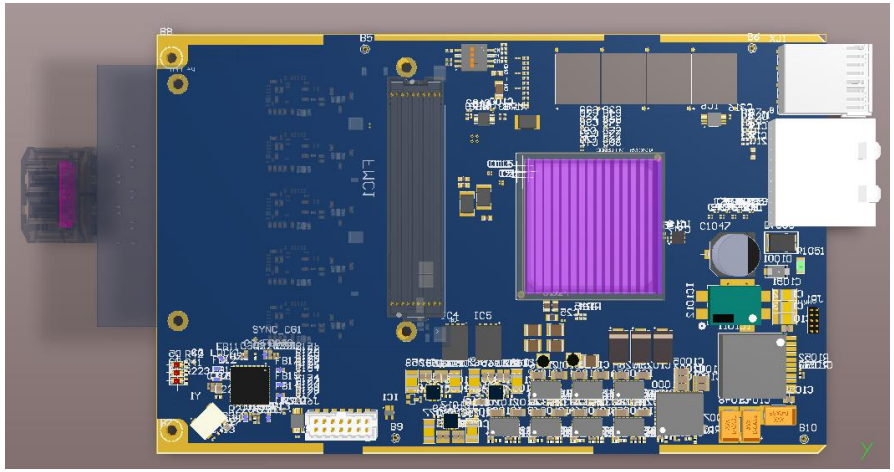
PXI Express Peripherie Modul – FMC Carrier:



Peripherie Module Overview:

- 3U Eurocard form factor 160 mm x 100 mm x 1,60mm
- PCIe Gen2: x8 up to 4GB/s
- Full Timing- und Synchronisation functionality
- Full Trigger functionality of PXI and PXIe specification
- Complete power supply onboard

Developed after:

- ANSI VITA 57.1
- CompactPCI Express
- PXI-1 Hardware Specification (Rev. 2.2)
- PXI-5 PXI Express Hardware Specification
- Xilinx FPGA (Kintex 7) Specifications

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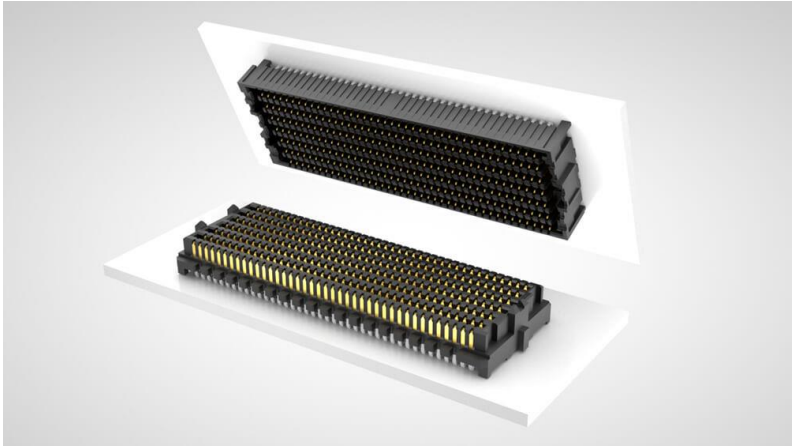
Advantage of the FMC Carrier:

- Flexible frontend
  - Fast exchange of frontends (FMC Modules)
  - High-Pin-Count compatible with Low-Pin-Count (LPC)
  - FMC connectors supports many signaling standards e.g. LVTTL, LVCMOS, SSTL, LVDS, LVPECL
  - High bandwidth of Input / Output possibilities
    - No Input / Output limitation depending on the connected e.g. PHYs or connectors



- Savings of cost and time
  - No development of a new board
    - High costs for components e.g. FPGAs
    - High costs for PCB manufacturing especially for high-speed material
    - Time intensive
  - New application e.g. Ethernet Switch or ADC only needs a new FMC Module
    - Saves costs for components and manufacturing
    - less time for development

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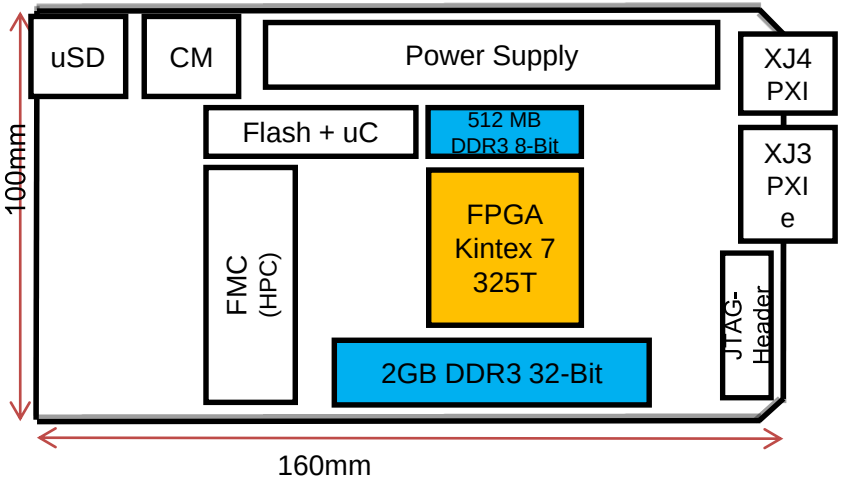
Quelle: www.pxisa.org

Boardfeatures:

1. Programable Resources:

- Xilinx Kintex-7 325T FFG900 FPGA
- Atmel ATSAMD20G18A for IPMI (**I**ntelligent **P**ower **M**anagement **I**nterface):
  - Control and sequencing for DC/DC converters and LDOs onboard
  - Programming clock generator TI LMK03806 over SPI
  - Data storage over SPI



2. Memory:

- 2 GB DDR3 SDRAM (4 x 512 x 8), 800Mhz for programmable logic
- 512 MB DDR3 SDRAM, 800Mhz for MicroBlaze (soft processor core)
- QSPI-Flash for FPGA configuration to meet time requirements for PCIe bootup
- QSPI-Flash for user storage
- Micor SD card for e.g. OS

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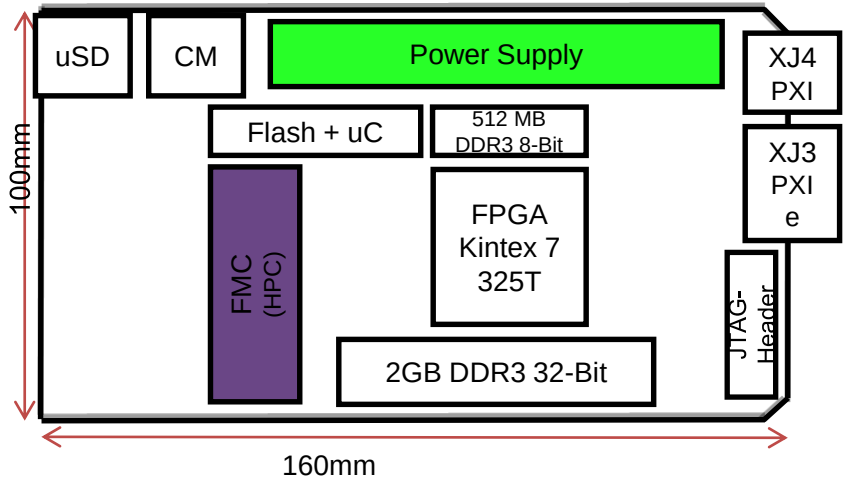
Boardfeatures:

3. Connectivity:

- One high pin count (HPC) slot for one single width mezzanine (all pins)
- PXI (eHM) and PXIe (ADF) connector for:
  - Timing and synchronization application
  - PCIe x8 Gen2 4GByte/s
  - Power supply from backplane (12.0V and 3.3V)
- JTAG header

4. Onboard Power supply for:

- FPGA (HR / HP Banks, Transceiver, Core)
- Memories (QSPI, DDR3 SDRAM)
- Microcontroller (ATMEL SAMD20)
- FPGA mezzanine connector (FMC)
- Clock generator TI LMK03806



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Boardfeatures:

5. IPMI (Atmel ATSAMD20G18A):

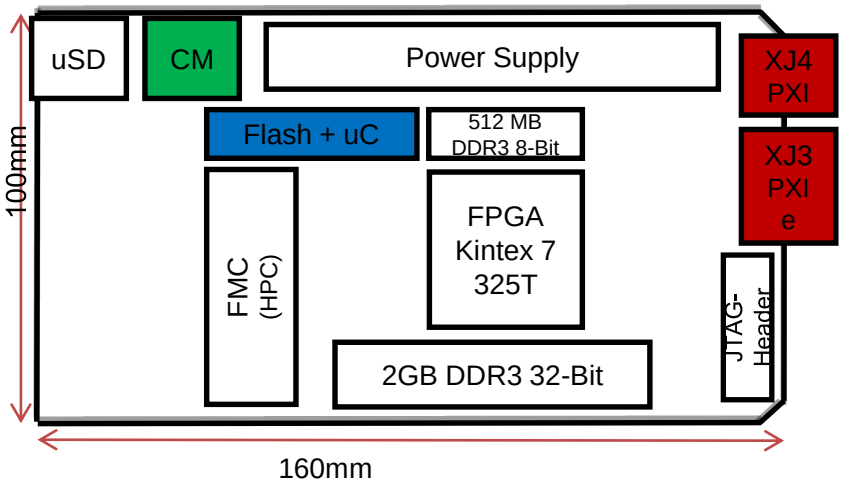
- Temperature monitoring for:
  - FPGA, DDR3 SDRAM and power supply
  - Voltage monitoring over PGood signals

6. Clock management TI LMK03806:

- 240, 200, 100MHz LVDS user system clock (programmable logic)
- 200MHz LVDS FPGA SDRAM clock
- 100MHz PCIe reference clock

7. PXI(e) Timing und Synchronisation:

- PXI_Trigger[0:7], Differentielle Trigger PXIe_DSTARB
- PXI(e)_Clock10/100, Differentielle Clock PXIe_DSTARA
- Local Bus



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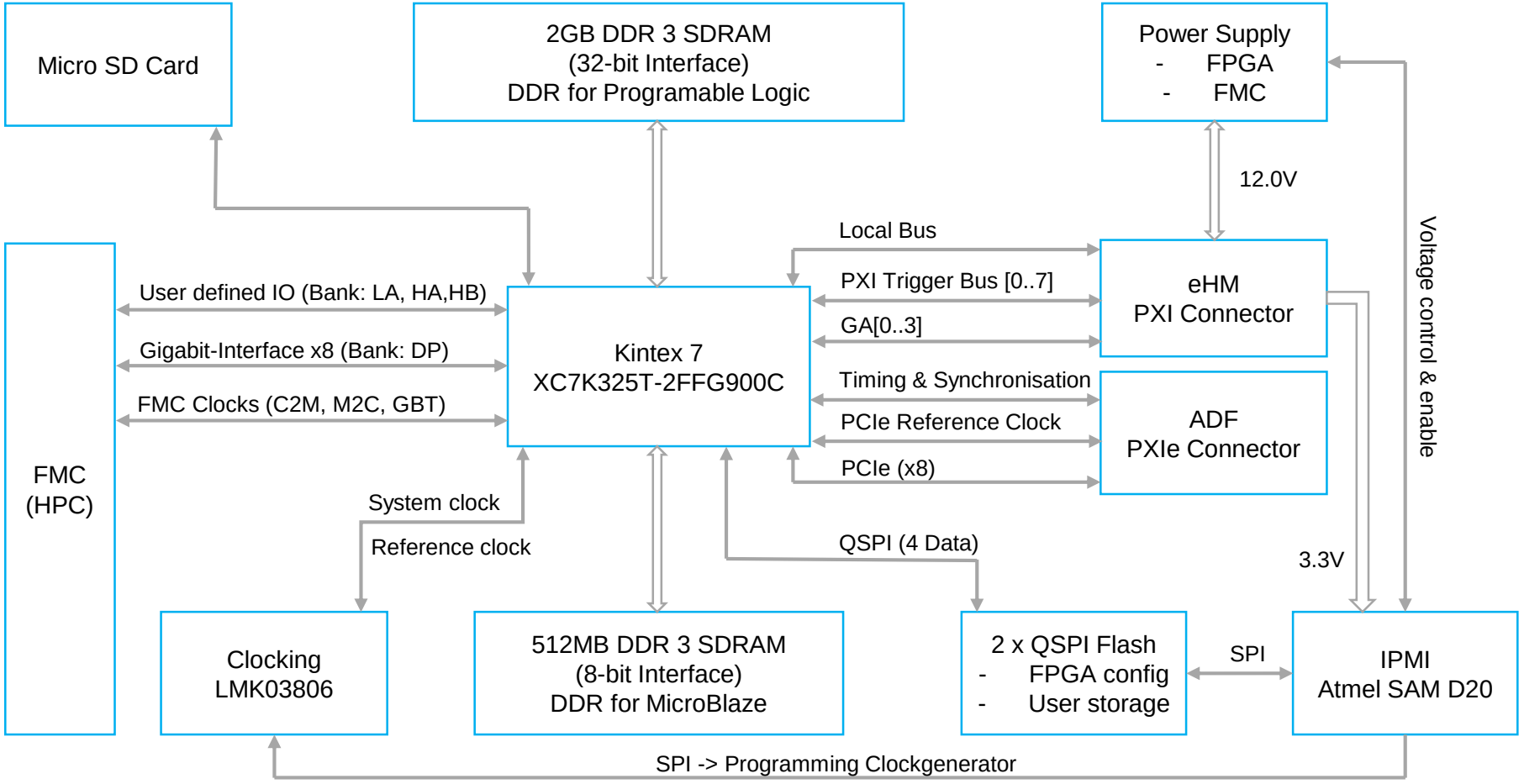

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Xilinx Kintex-7 325T FFG900 FPGA

	Feature:	Description:
Logic Resources:	Logic Cells	326080
	Flip-Flops	407600
	Slices	50950
Memory Resources:	Distributed RAM (Kb)	4000
	Block Ram	16020
I/O Resources:	Single-Ended I/O	500
	Differential I/O Pairs	240
Integrated IP Resources:	DSP48 Slices	840
	PCIe Gen2	1
	GTX Transceivers (12.5Gb/s max.)	16

FMC HPC (High-Pin-Count)

Ports:	Description:
HA, HB & LA Banks	User defined I/Os 80 Differential Pairs or 160 Single-Ended (up to 2Gbps)
CLK_C2M, CLK_M2C	Differential Clock to / or from Carrier Card or Mezzanine Card
DP Bank	Gigabit Transceiver Interface (up to 10 Lanes and 10Gbps)
GBTCLK	Differential Reference Clock for Gigabit Transceiver
GA[1:0]	Geographical Address for module identification
I²C	Standard I²C Interface for onboard (FMC) EEPROM (IPMI Support)
JTAG	Standard JTAG Interface specified in IEEE1149.1
PRSNT_M2C	Identification if FMC Module is present
PG_M2C, PG_C2M	Signals if power (Module or Carrier) are in tolerance

Use cases

- PXIe based FPGA development with VHDL
  - Use of custom Front Ends
  - Synchronization to PXIe periphery
  - Use of complete XILINX Tool chain
- Basis for HW interface development
  - TSN/AVB Interface
    - Broad-R-reach
    - Other PHY
  - Cognitive-Software-Defined-Radio-Platform

TSN/AVB

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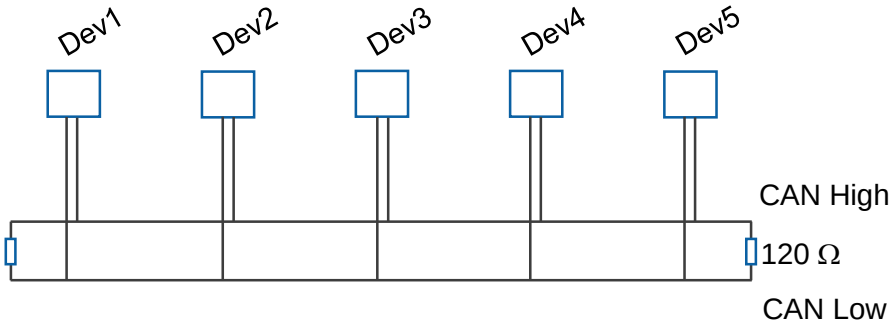
Changes in Bus Topology

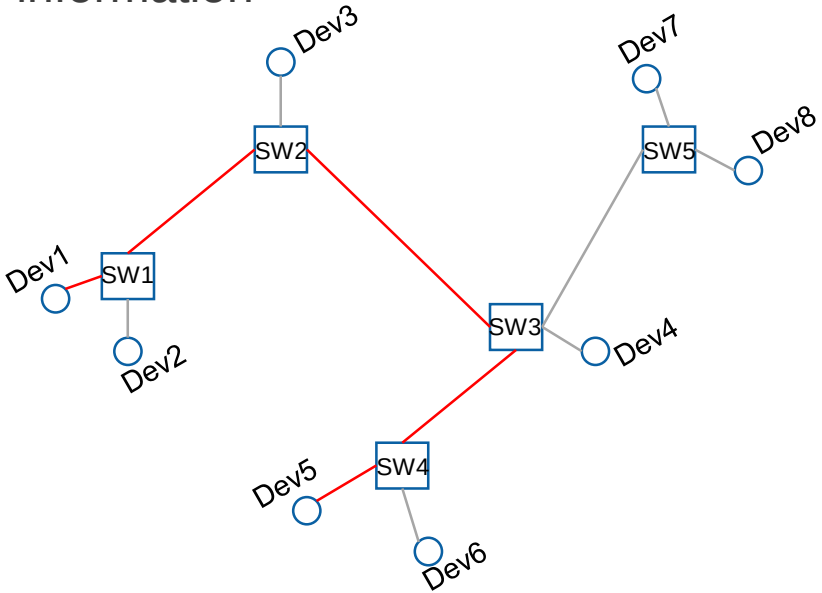
CAN

- Bus Topology: All Devices are connected to the same backbone
- All Devices Receive alle signals at the same time



Automotive Ethernet

- Switch Topology: Traffic needs to be directed
- Devices receive only relevant information



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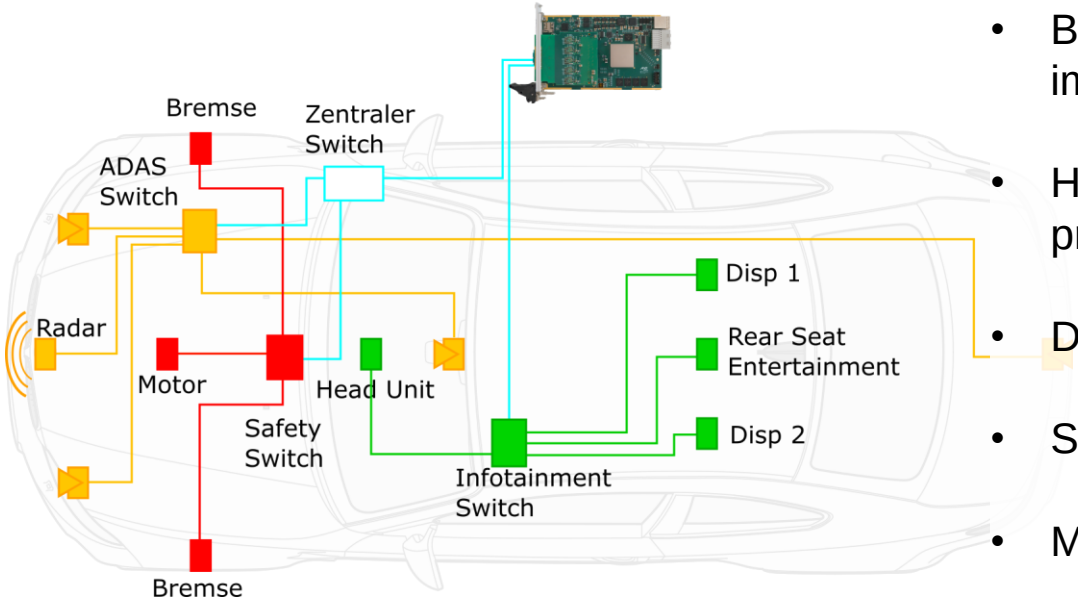
ADAS Systems- a new challenge



- Bigger Data through video and other imaging systems
- High priority traffic mixed with lower priority traffic
- Determinism
- Synchronisation
- Multiple Protocols (AVB/TSN)

➔Traffic becomes an important focus point during development

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AVTP Presentation Time

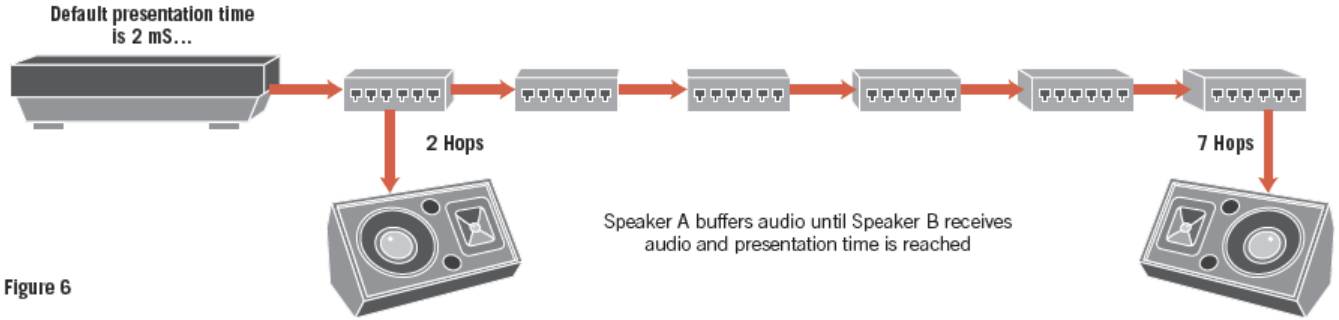

Figure 6

To compensate for different transport lengths to the listeners, the sender adds a presentation timestamp to all media.
The listener then relates the playback time to the gPTP Timestamp to achieve synchronous Playback.

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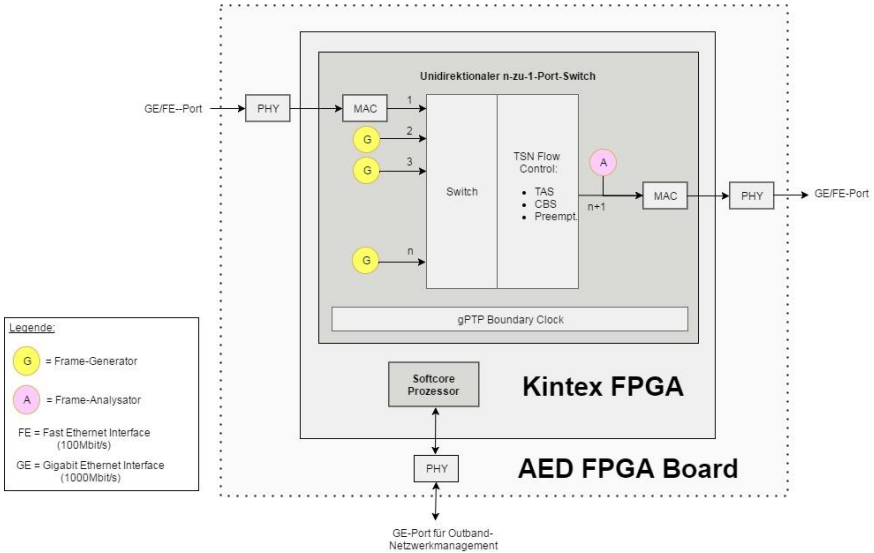
AVB/TSN Switch



- Implementation in FPGAs and ASICs
- Features:
  - Endpoint or N-Port Switch Functionality
  - VLAN (IEEE802.1 Q)
  - Credit-Based Shaper (IEEE802.1 Qav)
  - Time-Aware Shaper (IEEE802.1 Qbv)
  - Frame Preemption (IEEE802.1 Qbu)
  - gPTP Master/Slace Time Synchronization (IEEE802.1 ASbt)
  - Static (Re-)configuration by WebGUI or by Central Network Management Controller

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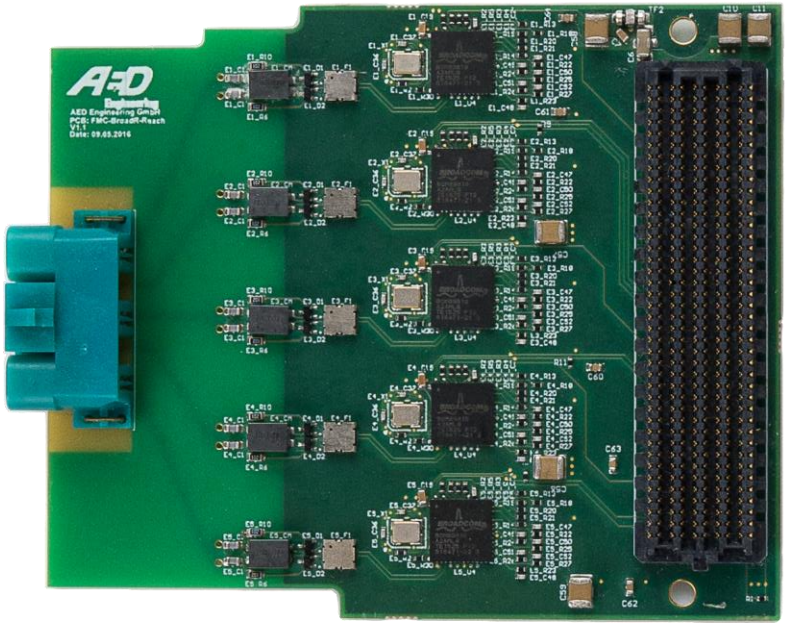
AED 100Mbps BroadR-Reach FMC-Card



- 5x BroadR-Reach Single-Port Automotive 100Mbps PHY Broadcom BCM89810
- Analog-Frontend incl. Magnetics + MTD-5x connector
- Power Supply Conversion for analog und digital Components
- 100mm * 74mm
- 6-layer PCB

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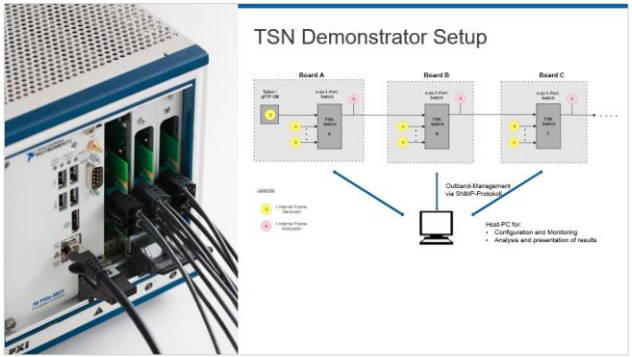
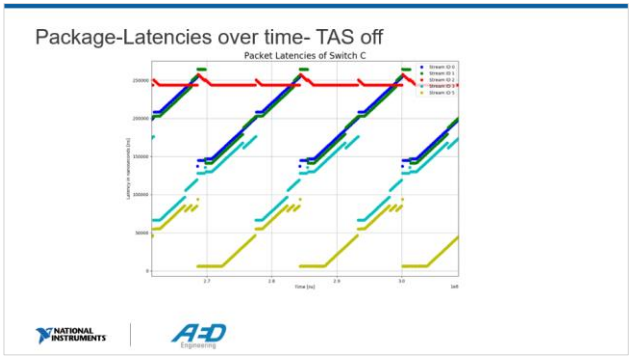
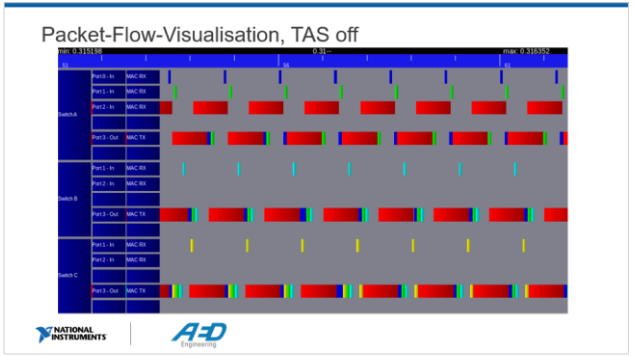
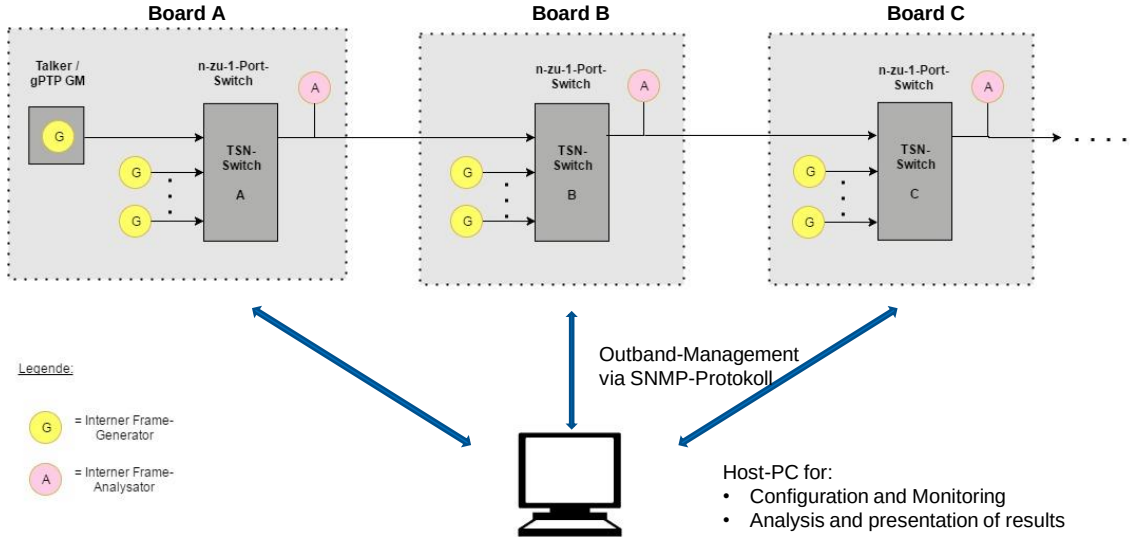

TSN Demonstrator Setup
Board A
Board B
Board C
Outband-Management
via SNMP-Protocol
Host-PC for:
• Configuration and Monitoring
• Analysis and presentation of results

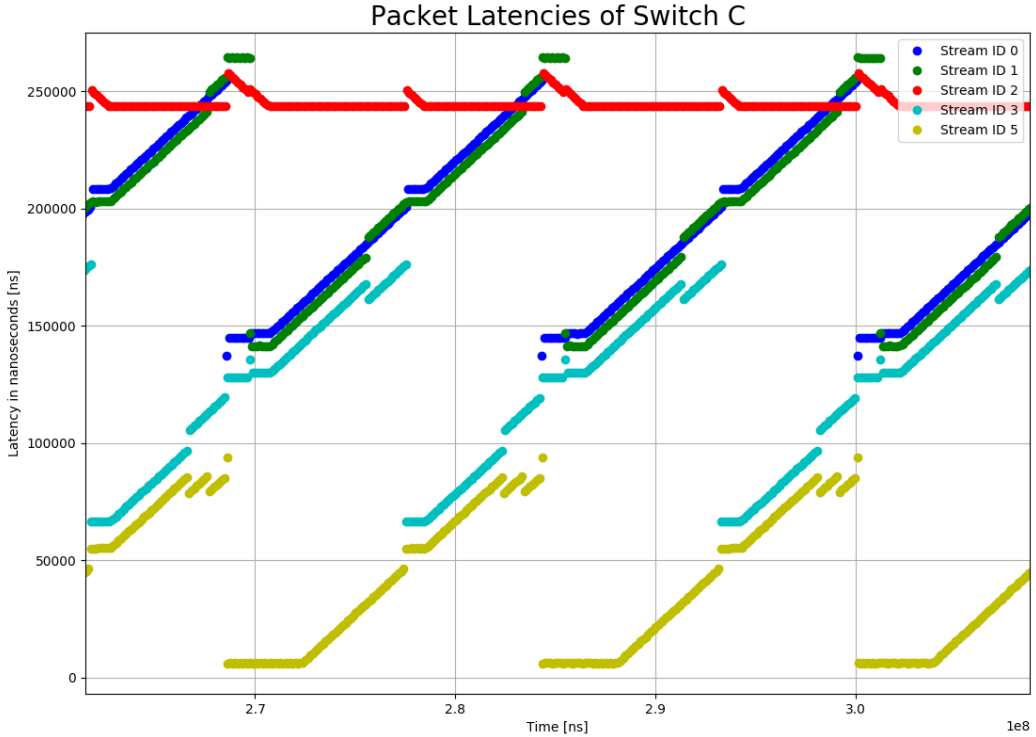

Package-Latencies over time- TAS off
Packet Latencies of Switch C


Packet-Flow-Visualisation, TAS off

TSN Demonstrator Setup



Package-Latencies over time- TAS off



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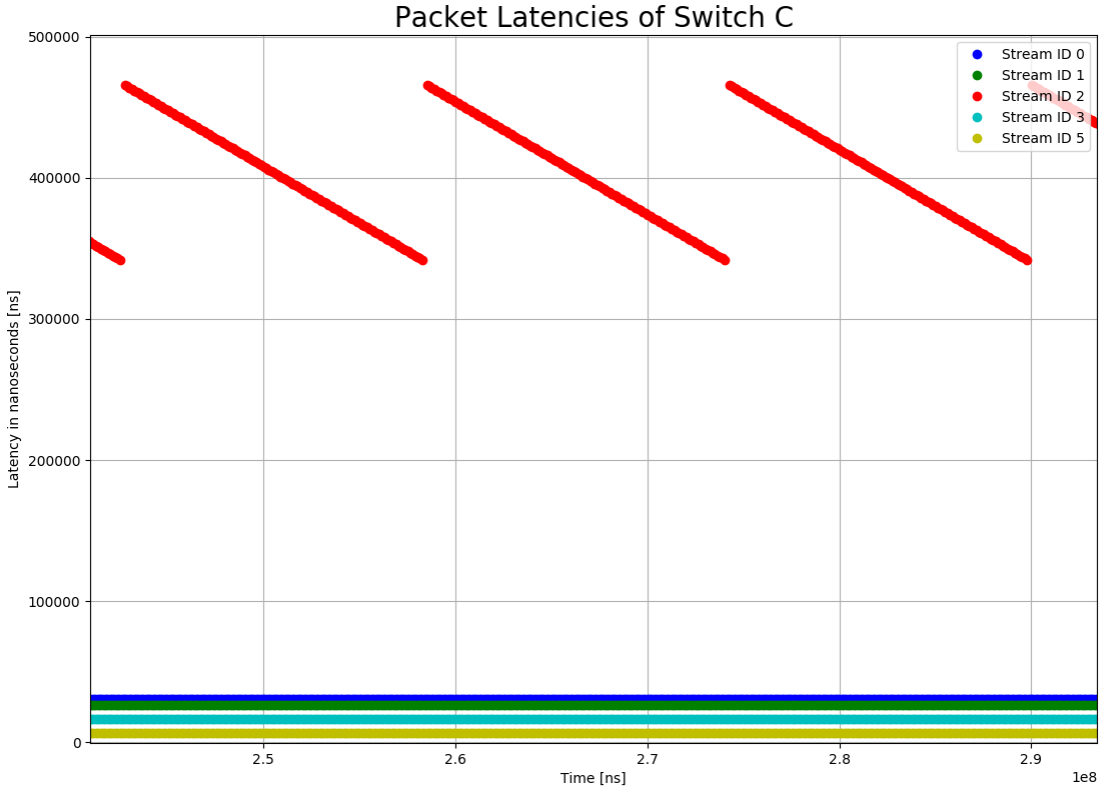
Package-Latencies over time- TAS on



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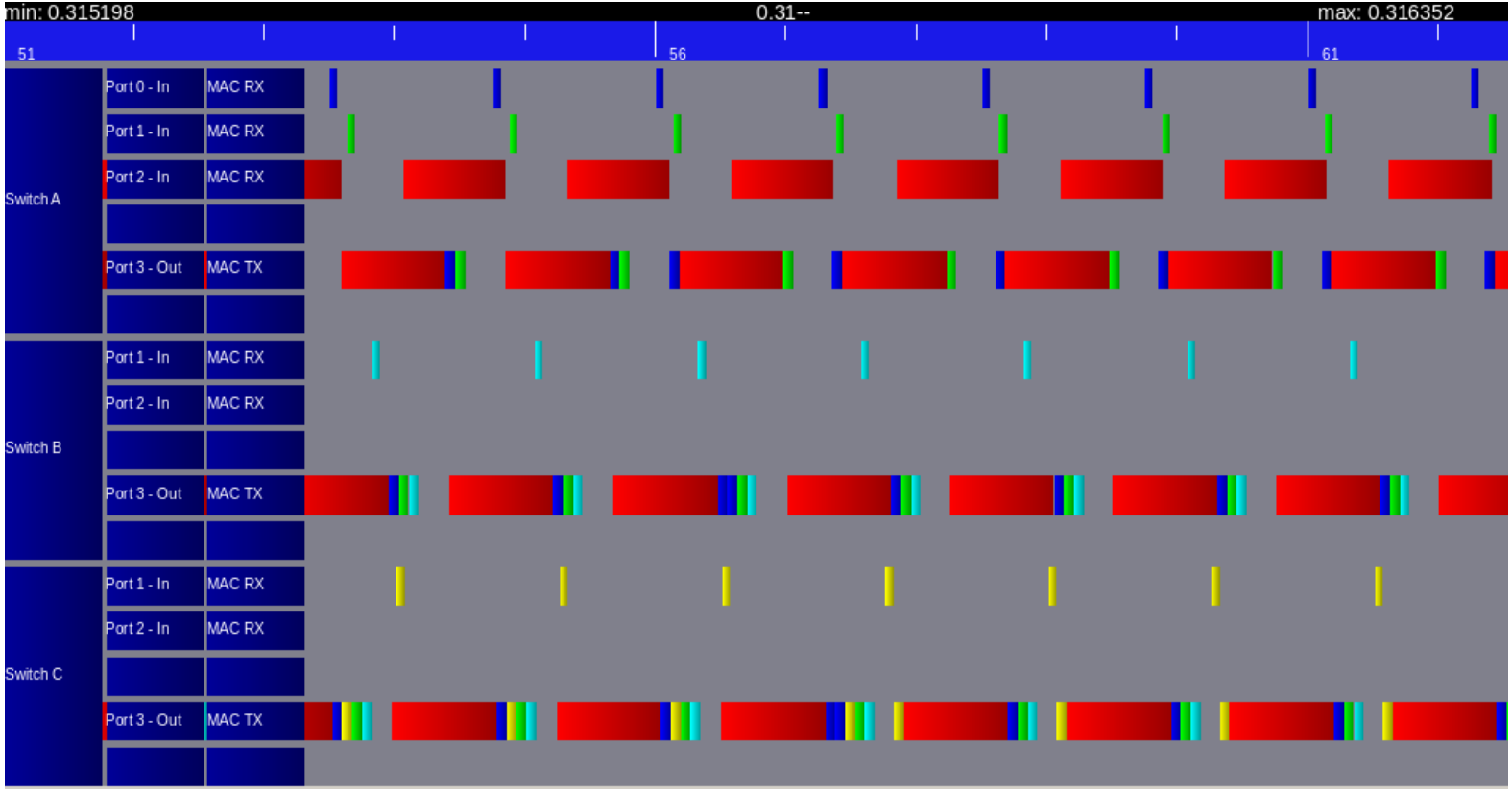
Packet-Flow-Visualisation, TAS off



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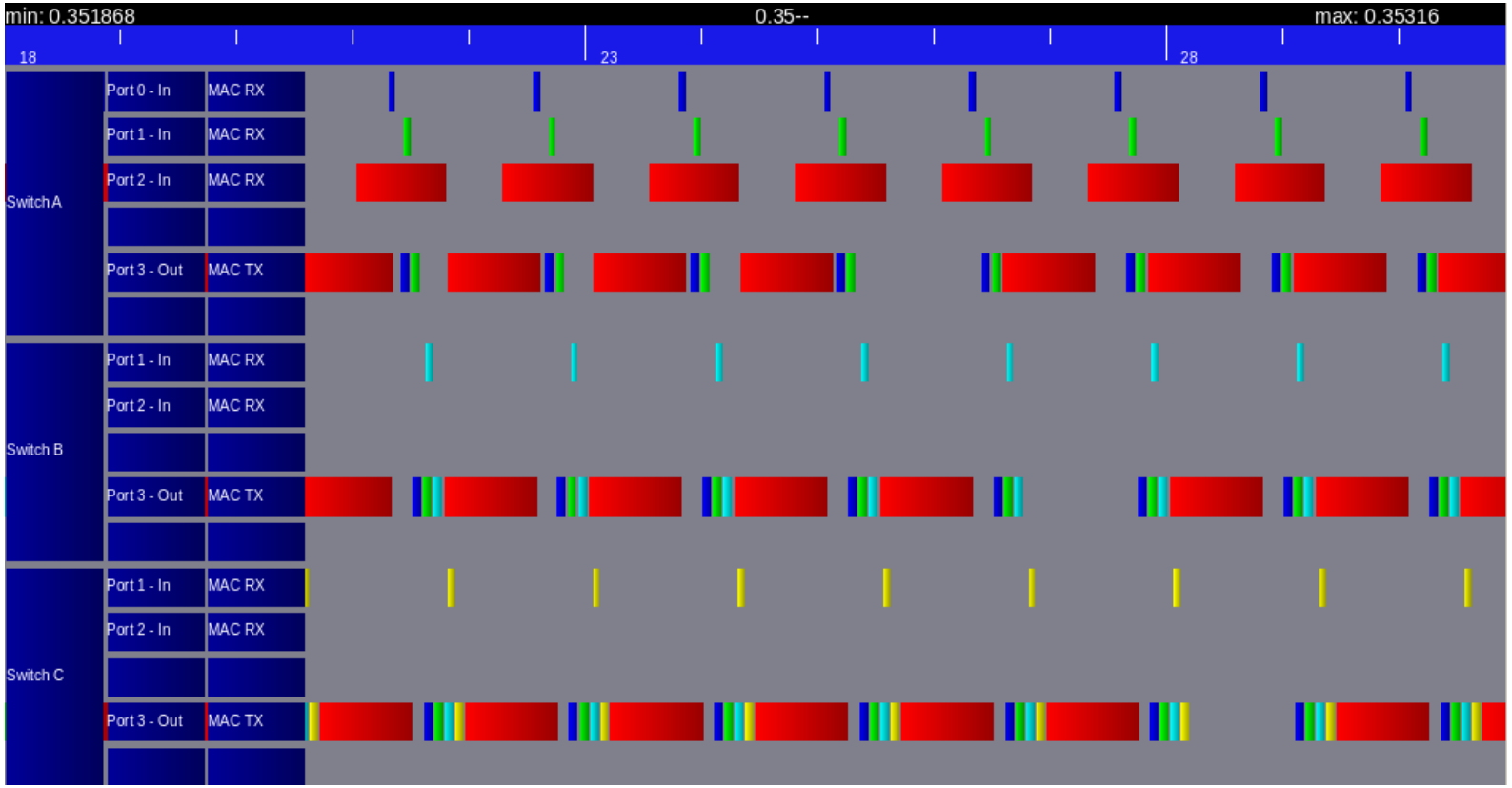
Packet-Flow-Visualisation, TAS off



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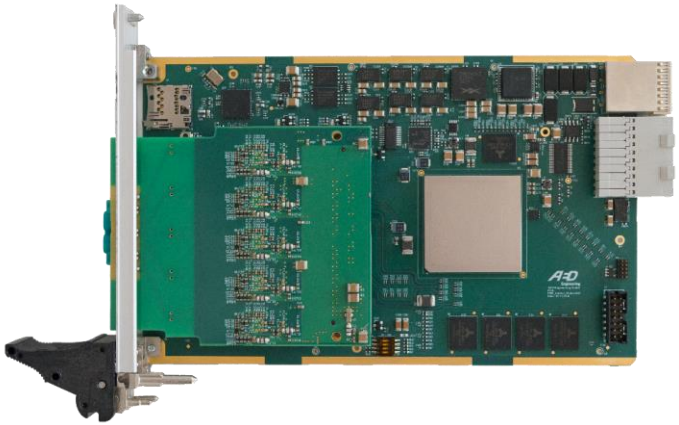
PXI AVB/TSN Switch

- Kintex 7 based design
  - Programmable with VHDL
  - Adaptable to various software stacks
  - Various frontends possible through FMC
- Timing and synchronisation within PXI Chassis
  - Time critical tasks/HiL
- Operating Modes
  - Sniffing
  - Recording and playback
  - Error injection
  - Response time testing



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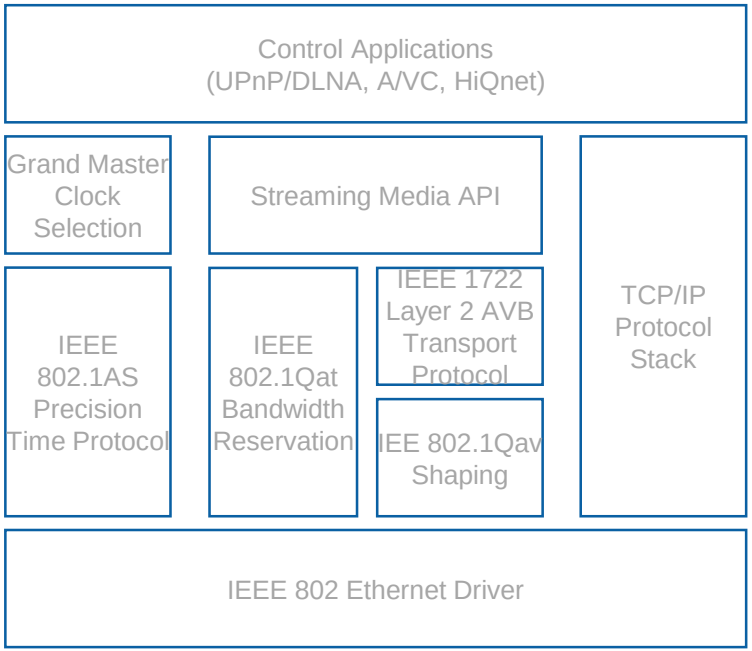
Advantage of Modular architecture



Adaptable Softwarestack:

- Components of the stack can easily be exchanged for custom components

Fault Injection:

- Precisely simulate malfunctions at every level of the stack

Response Time Testing:

- Get precise timing of each software component

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Peter Förster
Engineer Testsysteme

Tobias Rummel
Engineer Hardwareentwicklung

AED Engineering GmbH
Taunusstraße 51
80807 München

+49 151 672 00 652
+49 89 159 84848 24