



ENGINEER
NEXT
NIDays

The logo features the words "ENGINEER" and "NEXT" in a large, white, sans-serif font, stacked vertically. A yellow graphic element, resembling a stylized 'X' or a folded ribbon, is positioned between the two words. Below this, the word "NIDays" is written in a smaller, white, sans-serif font, enclosed within a white rectangular border. The entire logo is set against a blue background with diagonal stripes in various shades of blue, orange, and green.



Accelerating Mixed Signal Functional Tests using NI Source Measure Units & Digital Pattern Instruments

Archan Mudwel

Technical Marketing Engineer

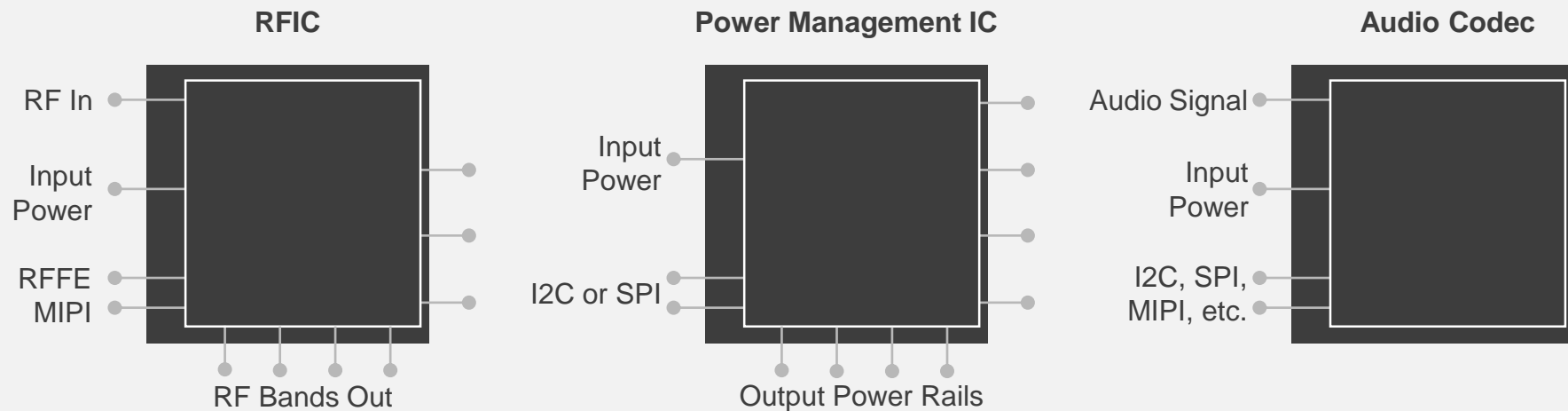
Optimizing Test Execution is a Competitive Advantage



“Some ASIC manufacturers report that testing time consumes 40-50% of the entire IC product development cycle.”

Source: IC Insights, McClean Report 2015

Why Focus on Source Measure Units and Digital Instruments?



Key Innovations for Semiconductor Test

NI Vector Signal Transceiver (VST)

- FPGA-based servoing for measurement acceleration
- Up to 1 GHz instantaneous bandwidth for wide range of wireless technologies
- R&D-grade measurement performance with up to -50 dB EVM for 802.11ax



NI Source Measure Units (SMUs)

- Broad IV range: 200V(20W), 3A (10A pulse)
- Current resolution to 10fA
- Max sampling to 1.8MS/s
- SourceAdapt™ Technology for fast settling in presence of capacitive loads
- Best in class channel density



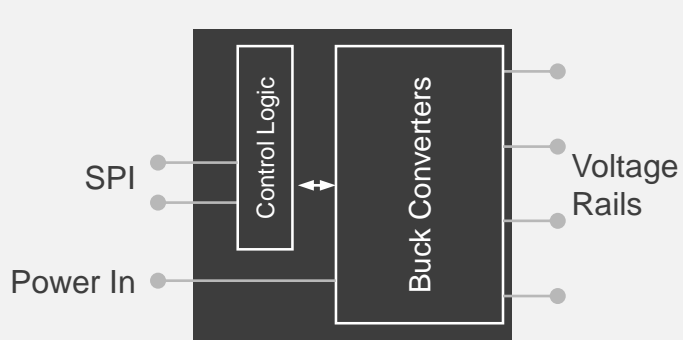
NI Digital Pattern Instrument

- ATE-class digital (with PPMU) in PXI
- Out of the box Digital Pattern Editor software
- Time sets, drive formats, opcodes, HRAM, Source and capture, history RAM, Shmoo



Digital Instruments

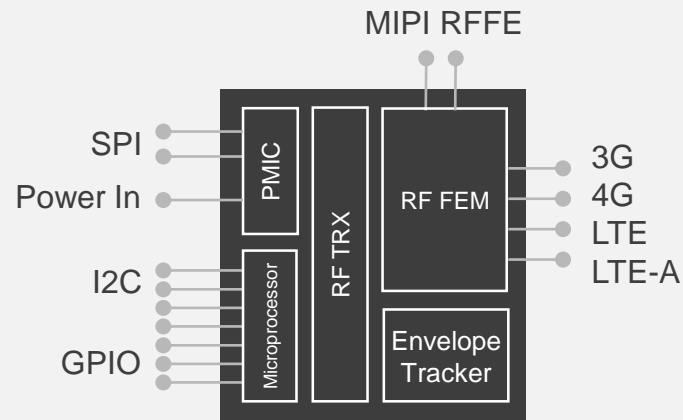
Evolution of Single-Silicon Packages to Modules



Single-Function
Packaged Part

Simple Digital
Interface

Limited Edge
Placement Needs



Application-Specific
Module

Correlated Signal
Inputs and Outputs

Multiple Buses and
Interface Types

Complex Edge
Placement
Requirements

ATE Not Designed to Serve Validation

- Too expensive
- Custom cooling
- High power connections
- Designated space in labs
- I/O options are fixed and aging
- Renting ATE from other groups
- Trying to partner overseas to use production ATE
- Lack of ATE availability limits test productivity



PXI Digital Pattern Instrument

Built for Test of Semiconductor Devices

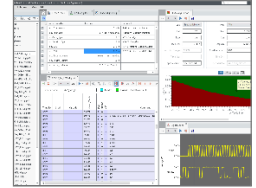
- RFICs and Transceivers
- Power Management ICs
- MEMS
- IoT Devices with Integrated MCUs and Sensors



PXIe-6570 Digital Pattern Instrument

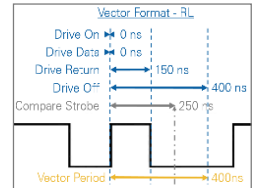
ATE Development and Debug Features

- Source and Capture Memory
- History RAM, Digital Scope, Pin View, and System View
- Shmoo Plots



ATE Test Capability

- Time Sets and Edge Placement
- Opcodes
- Multi-site Support
- Integrated Per-Pin PPMU Access
- Up to 256 Synchronized Channels

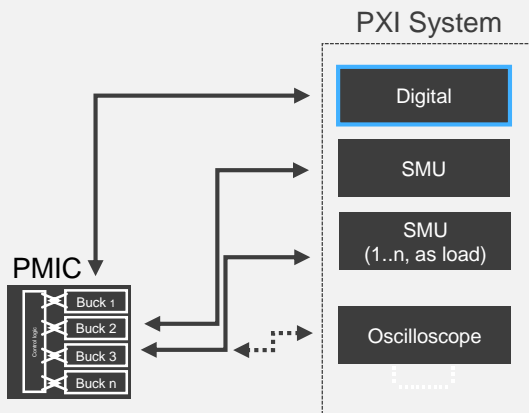


Digital: ATE-Class Instruments and Tools

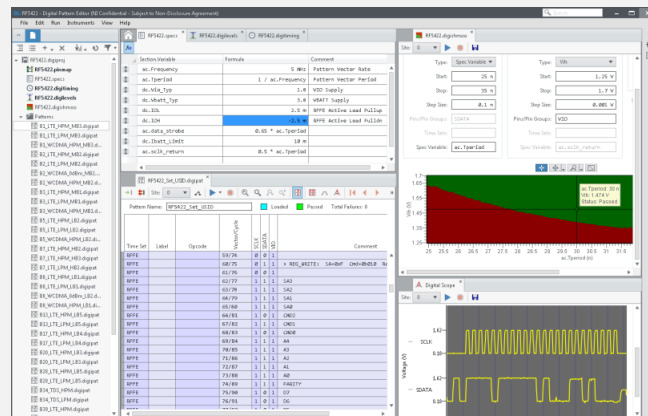
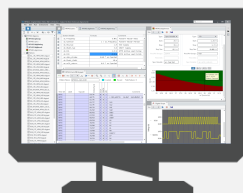
- DUT-centric paradigm: pin map assigns instrument pins to DUT pins
- Extensive test capability: timing sets, debugging tools, shmoo plotting, IV measurements
- Instrument integration: Multi-module and cross-instrument logical execution op-codes

Why it matters

- ATE-class digital test instruments throughout test phases
- Consistency paves the way for code reuse and correlation with production ATEs



NI Digital Pattern Editor

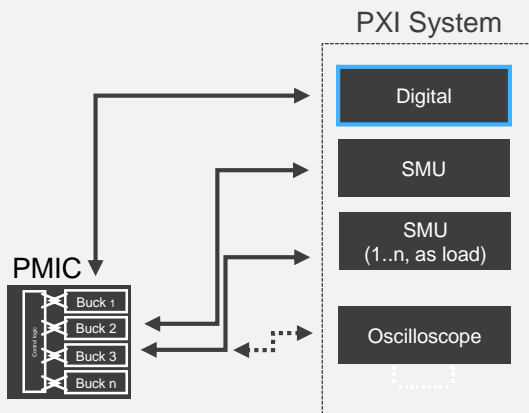


Digital: Consistent Terminology with ATE

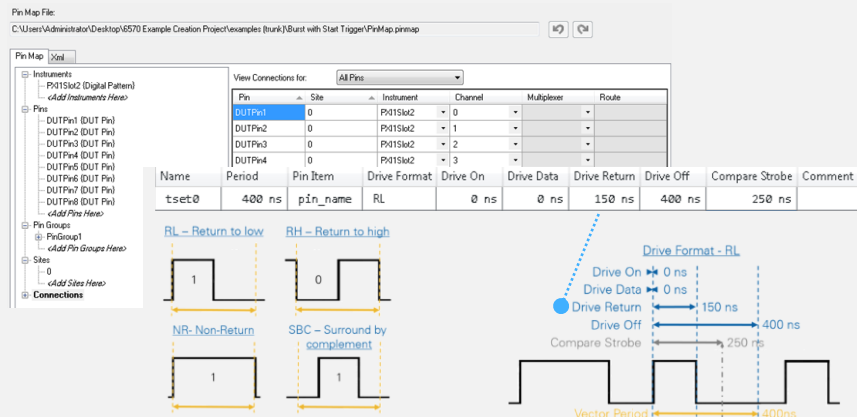
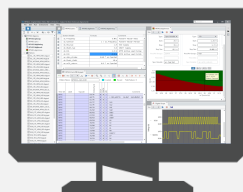
- DUT centric programming by pin
- Timing sets with cycle-to-cycle edge placement and drive formats
- Pin electronics for edge placement and IV measurements

Why it matters

- Paradigm consistency paves the way for reuse (patterns, code modules) and easier correlation with production ATEs



NI Digital Pattern Editor

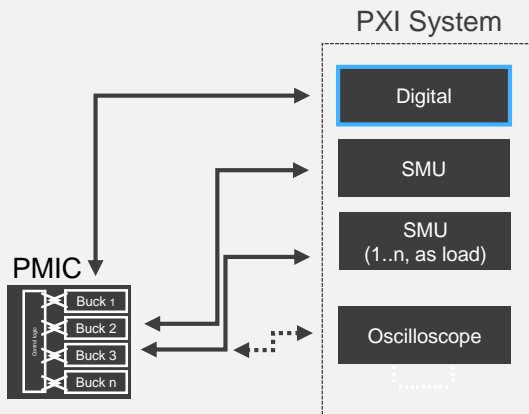


Digital: Pattern Editor Software

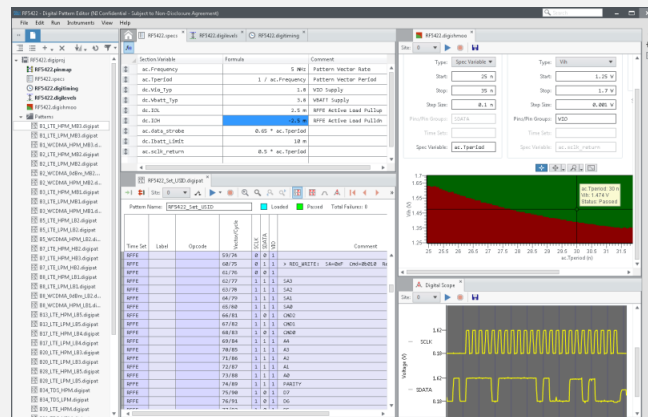
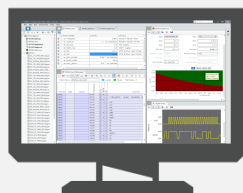
- Create, Edit, and Import Digital Test Patterns
- Debug tools like History RAM and Digital Scope
- Shmoo plotting for margining and characterization

Why it matters

- Out-of-the-box functionality to import/create, debug and burst patterns
- Go from configuration to test faster with out-of-the-box application software



NI Digital Pattern Editor

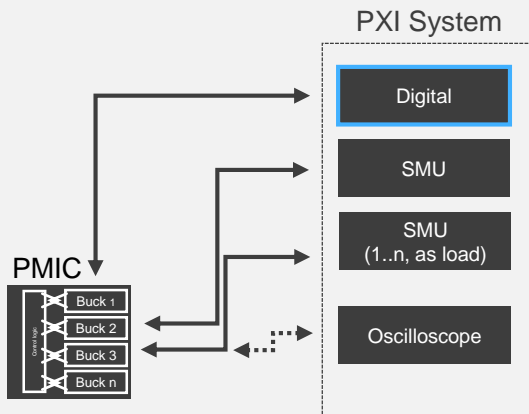


Digital: Test System Integration

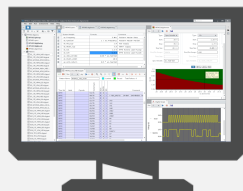
- Logical operations within patterns like looping, jumping, and matching
- Multi-module, cross-module, and cross-instrument operations

Why it matters

- Flexible execution of patterns including dynamic source and capture memory operations
- Integrated measurement capability of all instruments within a digital pattern

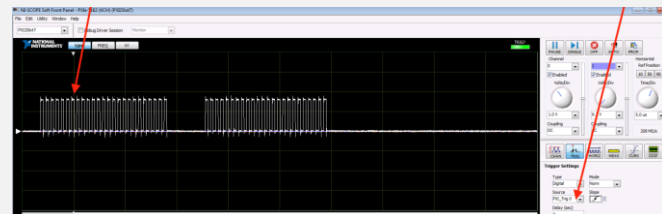


NI Digital Pattern Editor



Opcode
call
capture
capture_start
capture_stop
clear_seqflag
clear_signal
end_loop
exit_loop
exit_loop_if
halt
jump
jump_if
keep_alive
match
pulse_signal
repeat
return
set_loop
set_seqflag
set_signal
source
source_start
write_reg

Time Set	Label	Opcode	Vector/Cycle	CS	SDU	MOD	Mask	Comment
SPI_IO			1/-	1	0	0	X	Write @xAS to Register @x12
SPI_IO			2/-	0	1	0	X	Write Command = @x00
SPI_IO			3/-	0	1	0	X	
SPI_IO			4/-	0	1	0	X	
SPI_IO			5/-	0	1	0	X	
SPI_IO			6/-	0	1	1	X	
SPI_IO			7/-	0	1	0	X	
SPI_IO			8/-	0	1	1	X	
SPI_IO		pulse_signal(event0)	9/-	1	1	1	X	Trigger Scope
SPI_IO			10/-	0	1	1	X	
SPI_IO			11/-	0	1	0	X	8 Bit Address



PXI Digital Pattern Instrument



PXIe-6570 Digital Pattern Instrument



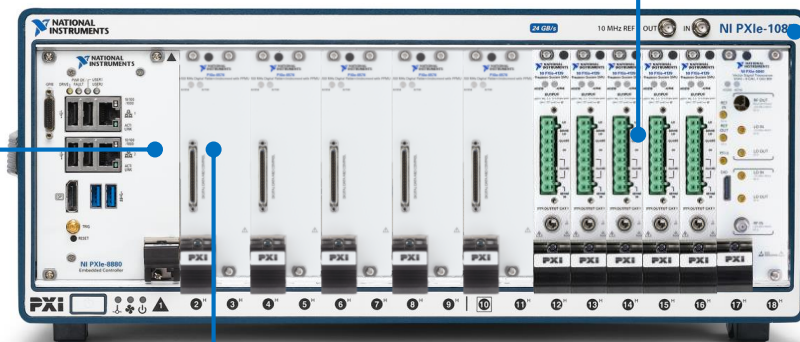
NI Semiconductor Test System (STS)

Pin Electronics	DCL: -2V to +6V, 32 mA PPMU: -2V to +6V, 32 mA Active load: 24 mA
Channels	32, in 2 PXI Express Slots
Vector Rate	100 MHz (10 ns vector period)
Pattern Timing	31 Timing Sets, Edge Placement Resolution 39.0625 ps
Pattern Formats	Non-Return, Return to Low, Return to High (100 MHz max) Surround By Complement (50 MHz max)
Vector Memory Depth	128 M/Channel
Opcode Functionality	Flow Control, Sequencer Flags and Registers, Signal, Source and Capture, Subroutine
Source and Capture Engines	4 each, 1 M/channel, Included with Product, Not Separately Licensed
SCAN Support	Flattened SCAN Patterns, up to 128 M
Operating System Support	Windows 7, 64-bit; Windows 10, 64-bit

A Modular Approach to Digital Test

Synchronized PXI Instruments

- Expand Digital Count to Up to 256 Channels per PXI System
- Sub-Nanosecond Synchronization with other PXI Modules
- Full Suite of Instruments from DC to mmWave



PXIe-8880 Controller

- Intel Xeon 8 Core Processor (2.3 GHz)
- 24 GB/s System Bandwidth
- Up to 24 GB DDR4 1866 MHz RAM
- Gen 3 PCIe Express Technology

PXIe-6570 Digital Pattern Instrument

- 32 Channels per Module
- Up to 256 Synchronized Channels
- 31 Timing Sets
- 100 MHz Vector Rate
- 128 M Vector Memory

PXIe-1085 Chassis

- 18 PXI Express slots
- Up to 24 GB/s System Bandwidth
- Peer-to-Peer Data Streaming
- 10 MHz OCXO
- Gen 3 PCIe Express Technology

NI Digital Pattern Editor

Developing, Editing, or Importing Digital Patterns

Pin and Channel Map

Specifications, Timing, Levels, and Pattern Files

Standard ASCII Format for Pattern Files

Debugging Tools for Digital Tests

History RAM Overlay and Viewer

Pin and System Views

Digital Scope

Shmoo Plot Tool

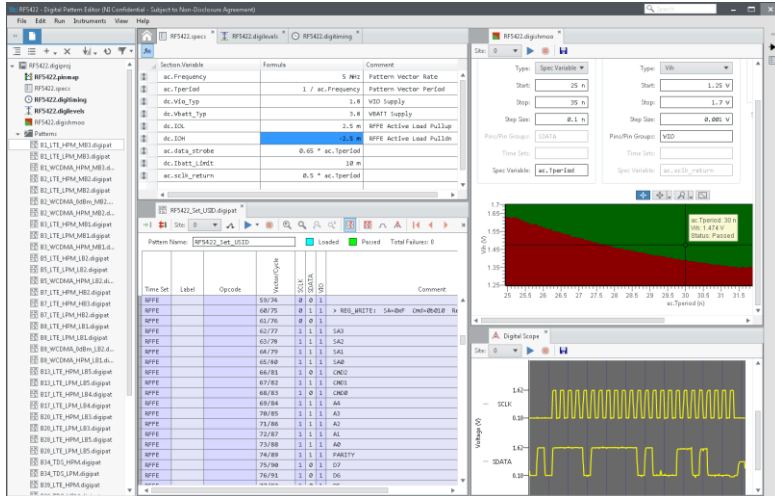
Sweep Specifications, Timing, and Voltage Levels

Sweep Multiple Sites in Parallel

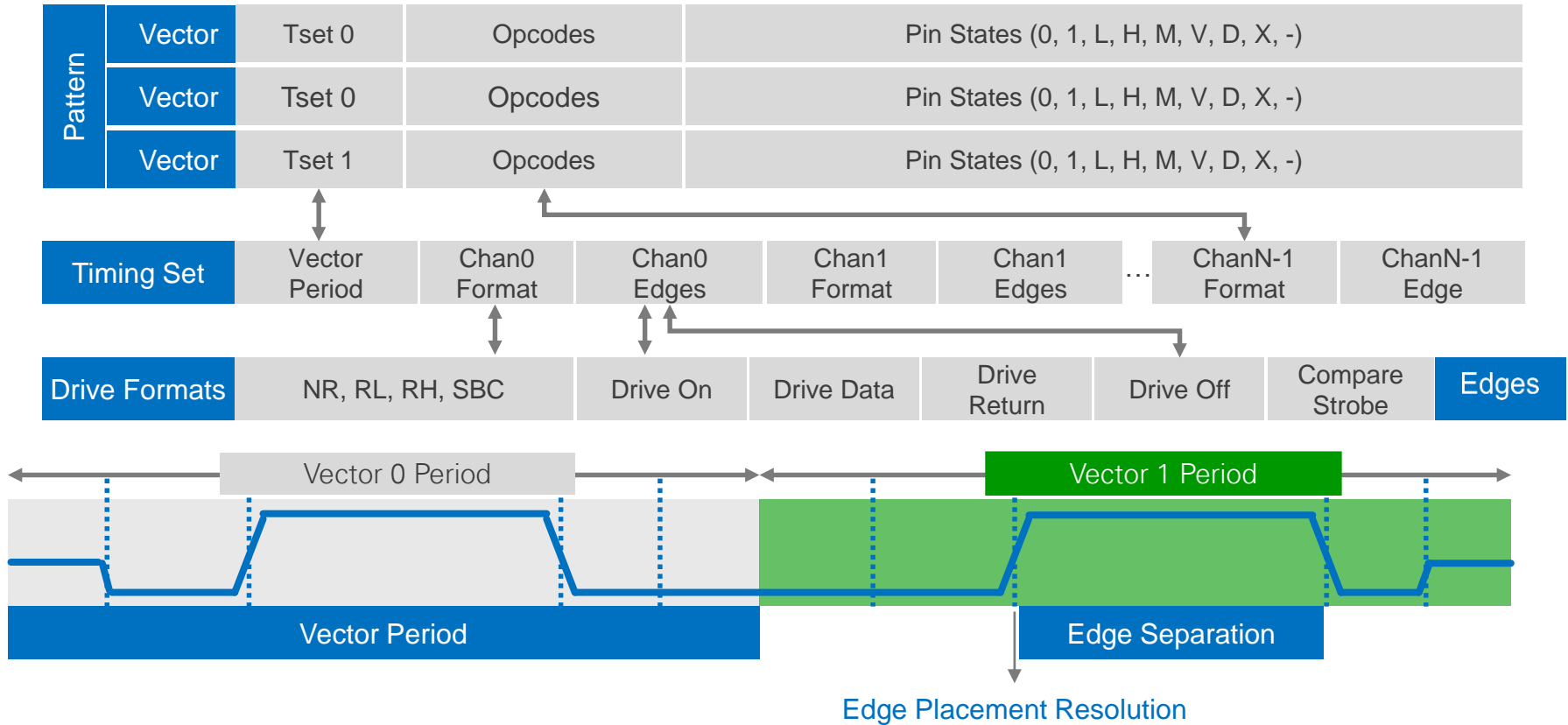
Integration with TestStand Semiconductor Module

STDF Reports, Binning, Handler Integration

Add Break Points in Code to Debug



Semiconductor ATE Digital



Source Measure Units

Functionality of Source Measure Units



DC VOLTAGE SOURCE



DC CURRENT SOURCE



PULSE GENERATOR



WAVEFORM GENERATOR



VOLTMETER



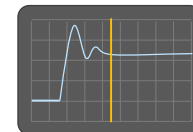
AMMETER



OHMMETER



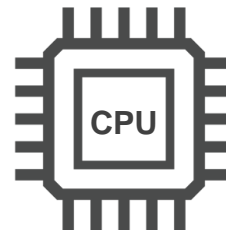
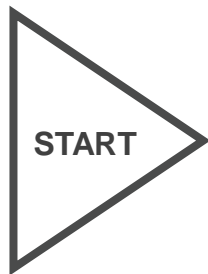
ISOLATED DIGITIZER



PROGRAMMABLE LOAD



SMU Measurement Flow



TRIGGER

SOURCE

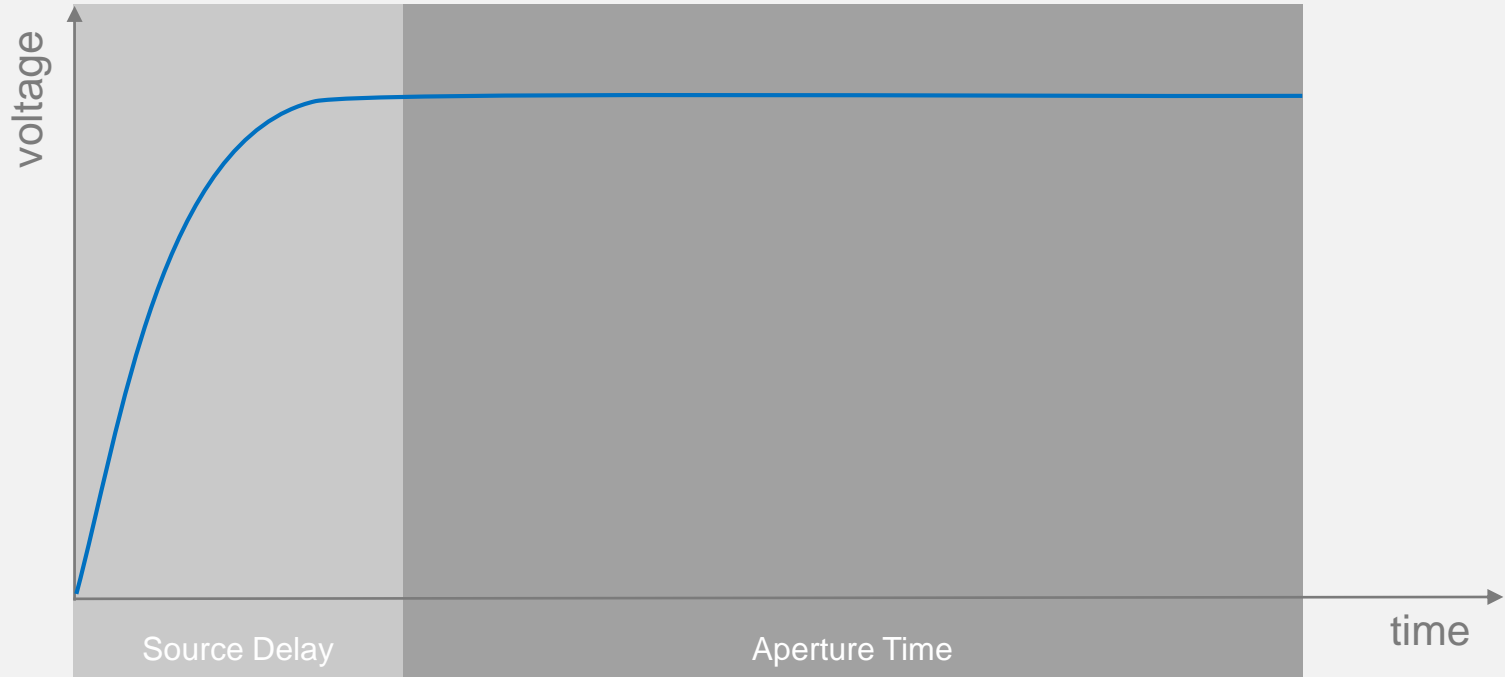
MEASURE

PROCESS

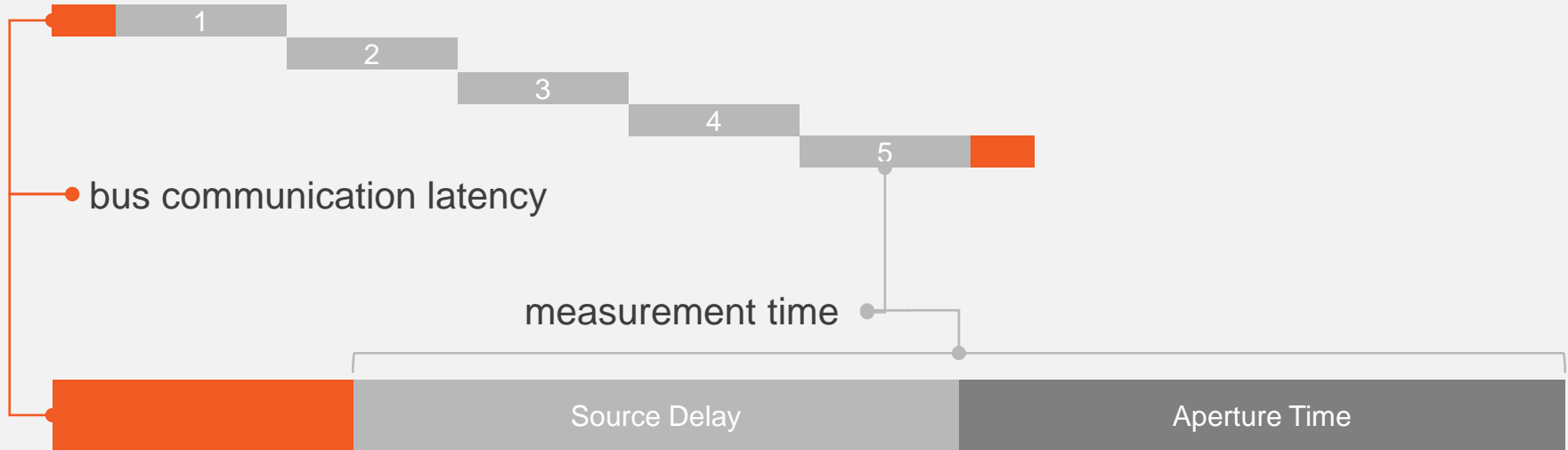
You can take high precision measurements quickly

Removing small inefficiencies in timing can reduce your cost of test

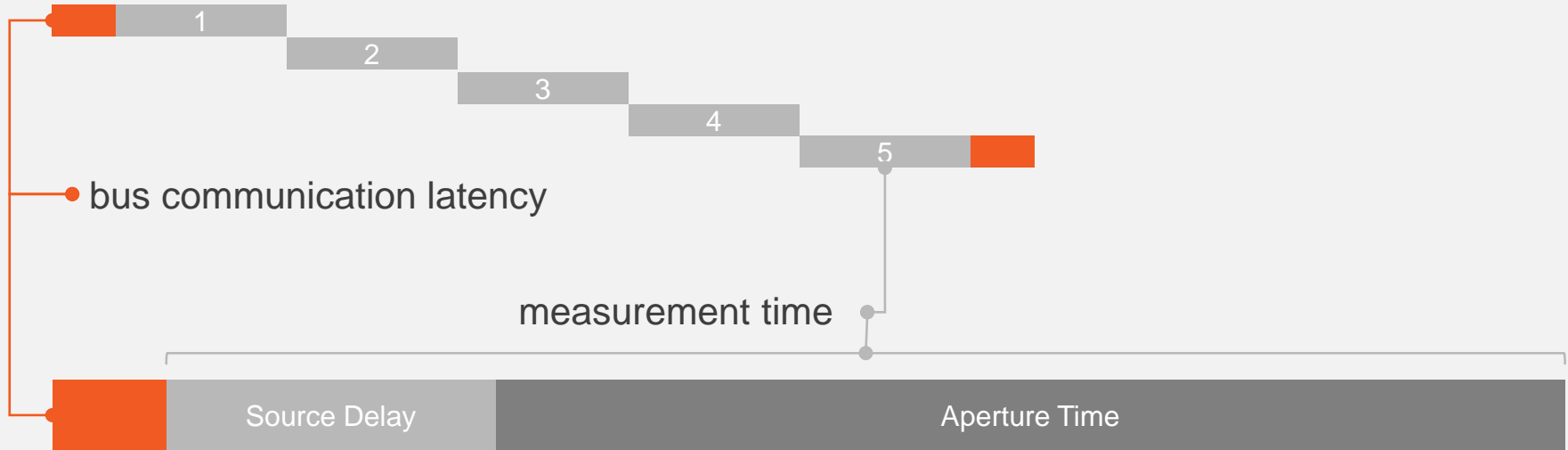
Measurement Cycle



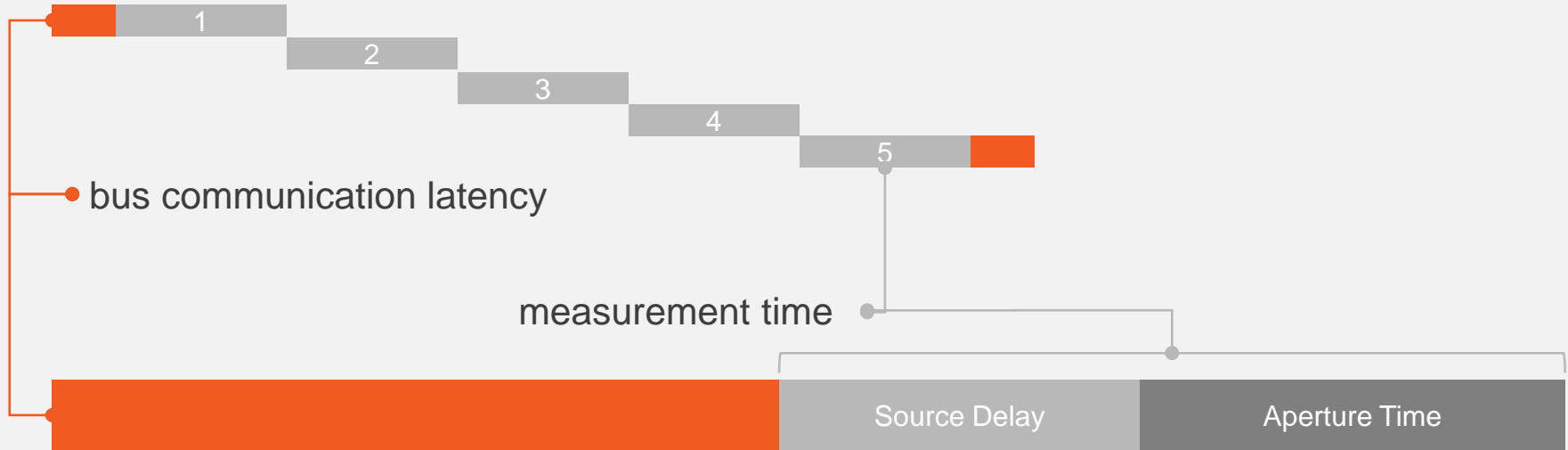
Measurement vs. Overhead



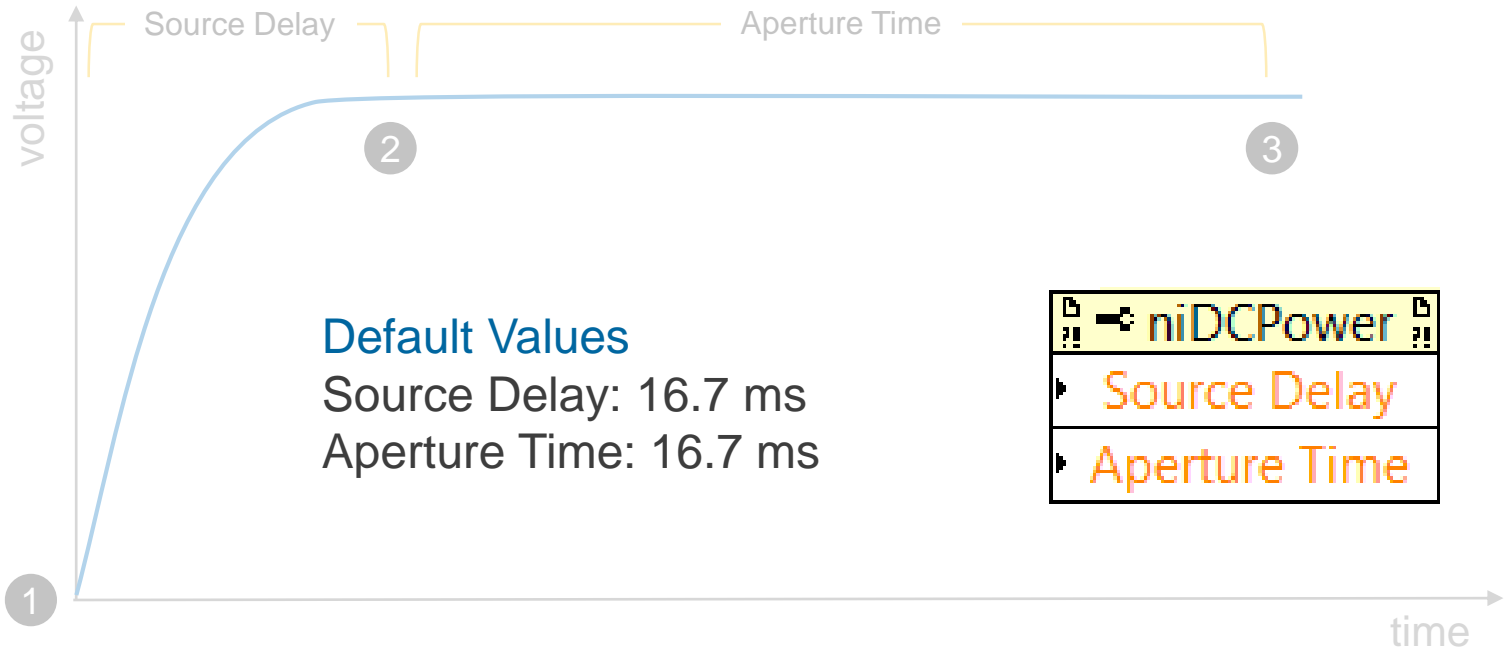
Measurement vs. Overhead



Measurement vs. Overhead

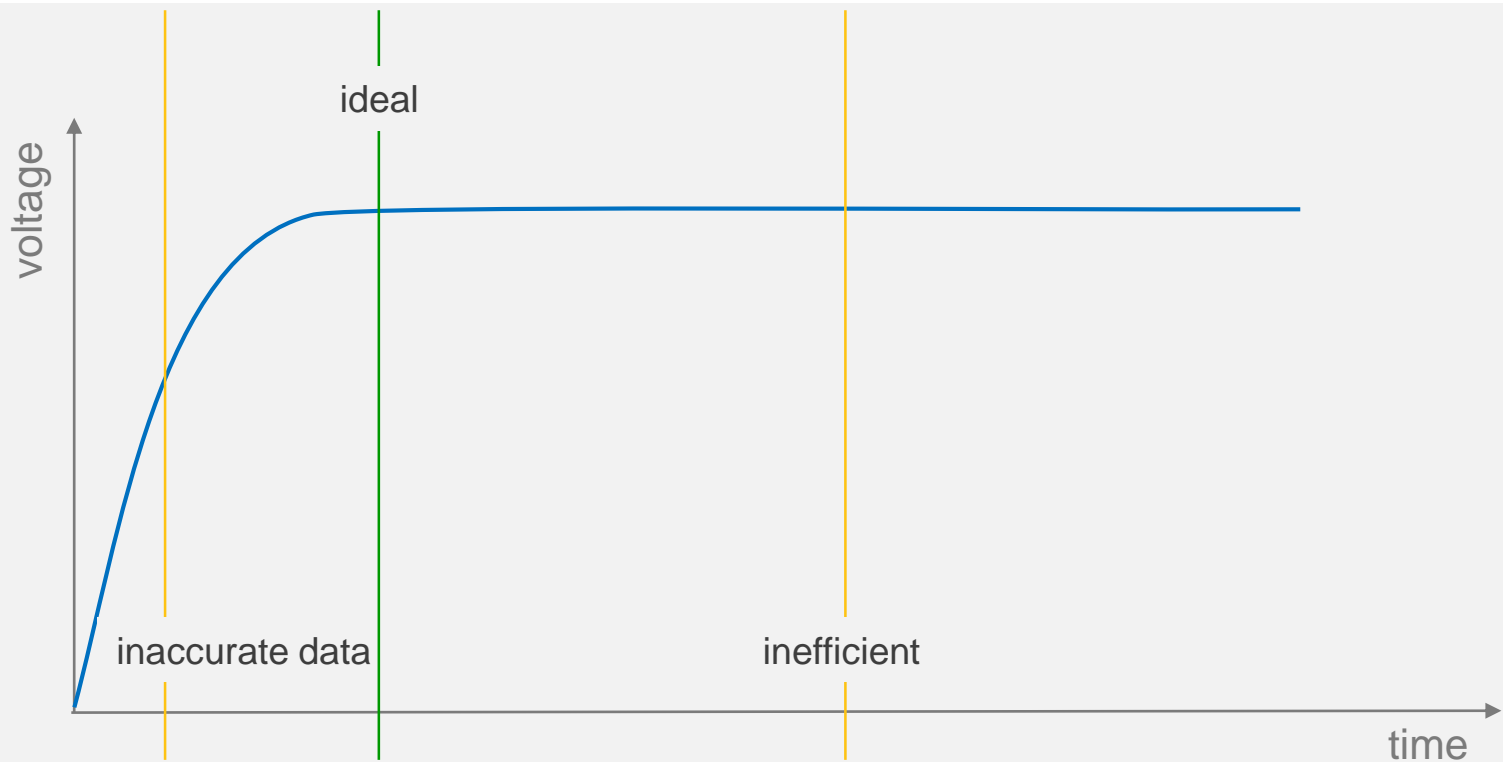


Source and Measure Cycle



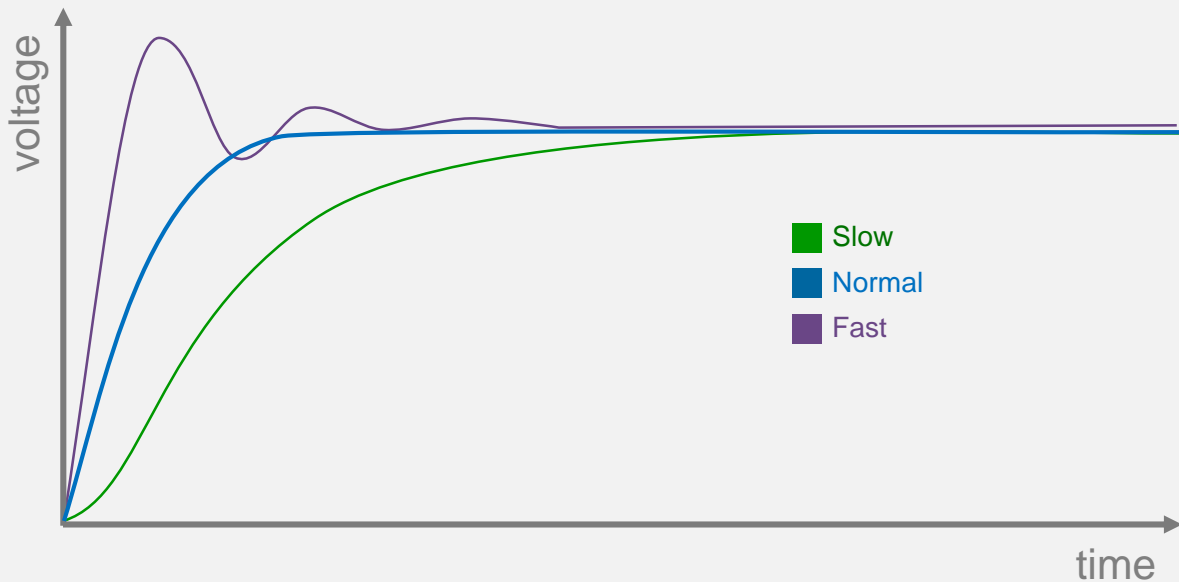
Source Delay

16.7m → niDCPower
Source Delay



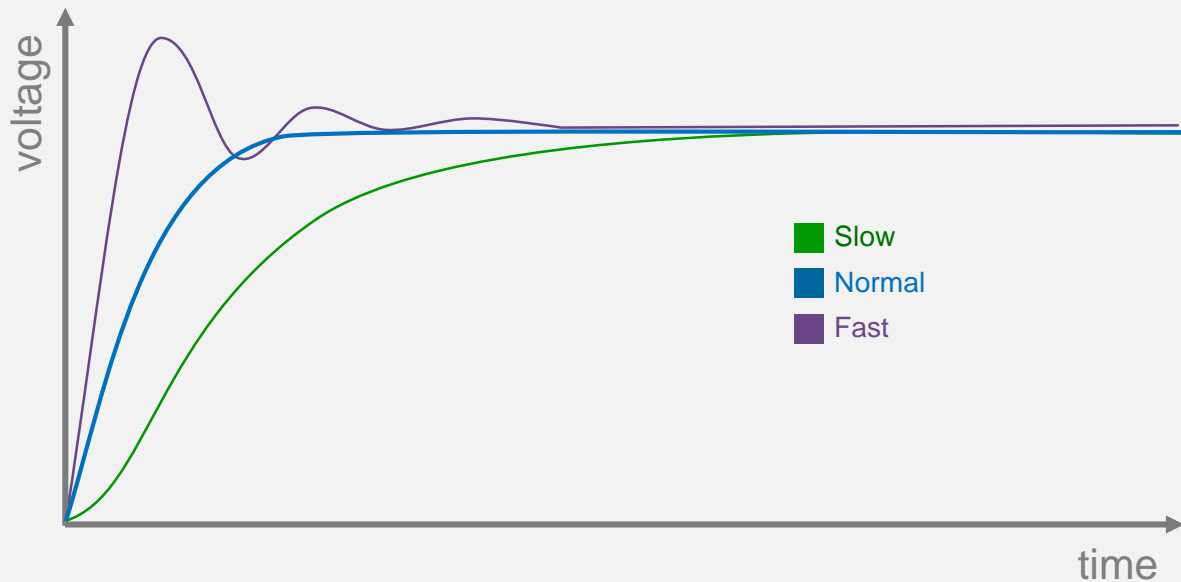
Optimizing Source Delay

Normal



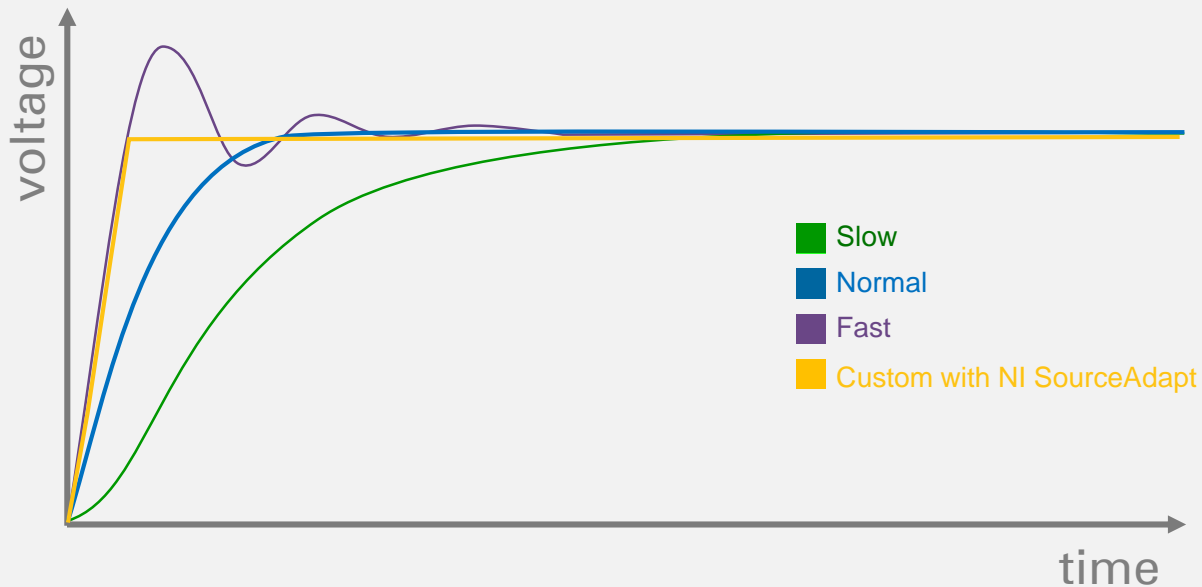
Transient Response and Rise Time

Normal niDCPower Transient Response

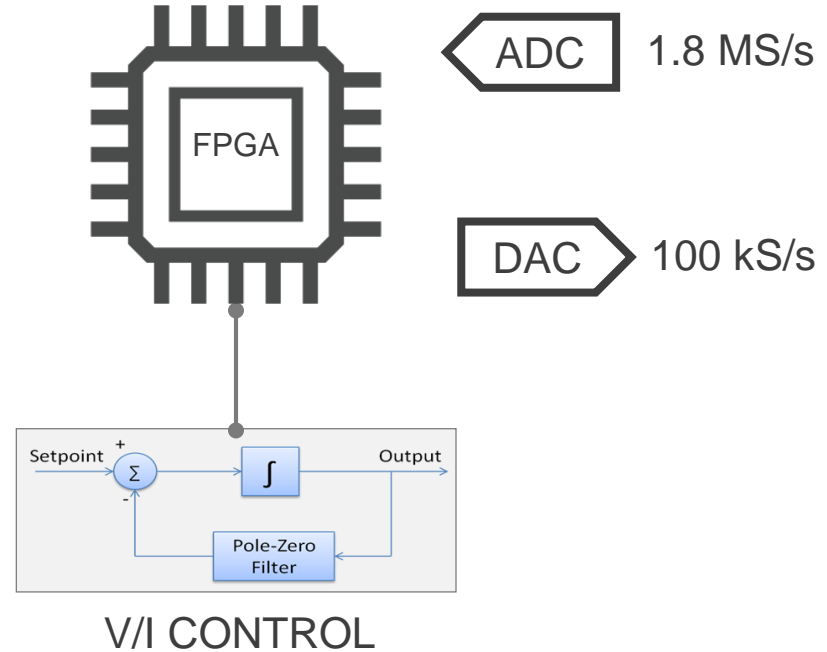
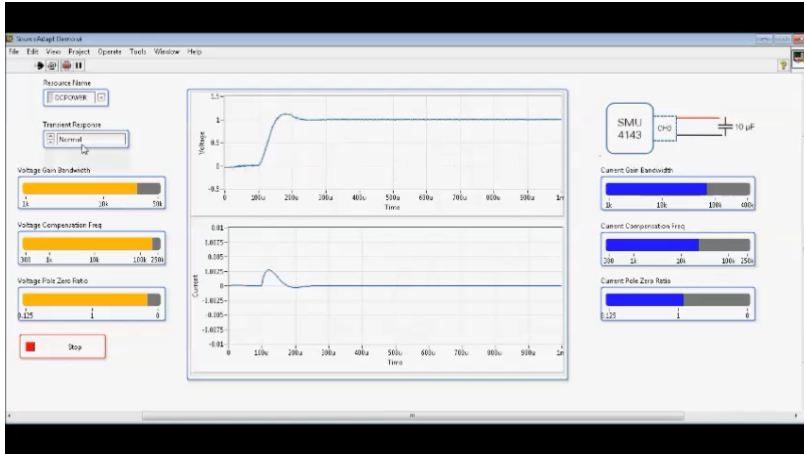


Transient Response and Rise Time

Custom



SourceAdapt: Digital Control Loop

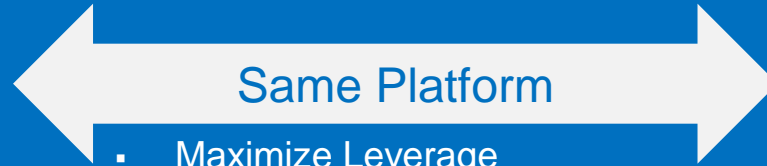


Labs



A Smarter Approach

Production Floor



Same Platform

- Maximize Leverage
 - Code, setup, training
- Simpler correlation
- Faster test cycles
- Lower cost





Smarter Test System

- Open, Flexible Software
- Modular Hardware
- Vibrant Ecosystem
- “Customer knows best”
- Deployable from Validation to Production

A smart test system is more than a fixed-functionality instrument— it is built for automation and customization, across validation to production, with ultimate goal of meeting business needs.

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