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Developing a Synchronised Distributed Data Acquisition System

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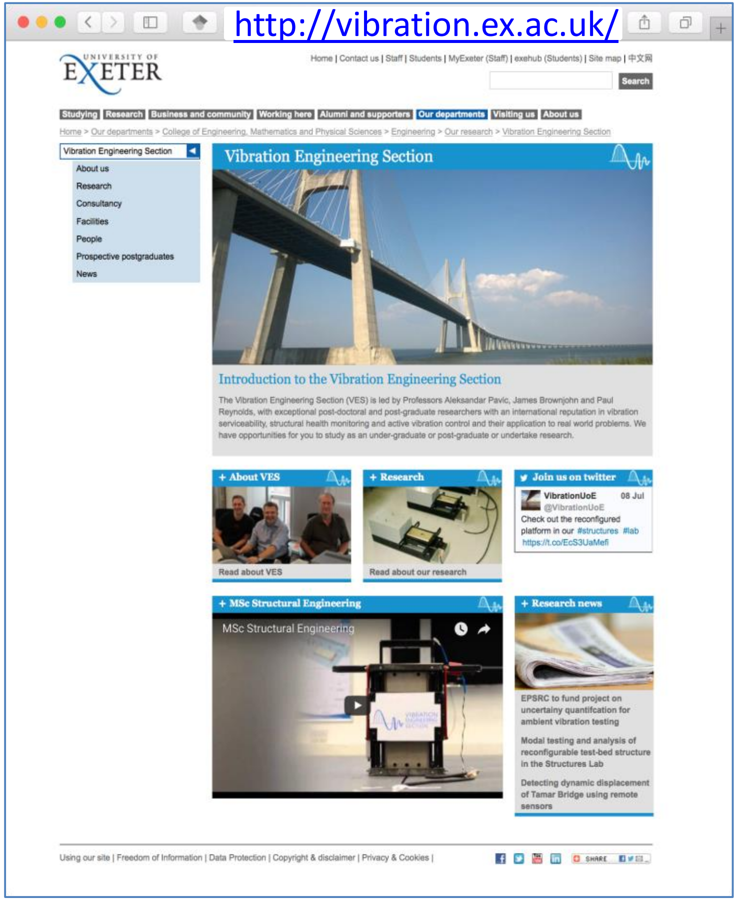
London, UK

Contents

- Introduction
- System Design
- Hardware
- Field Testing
- Concluding Remarks

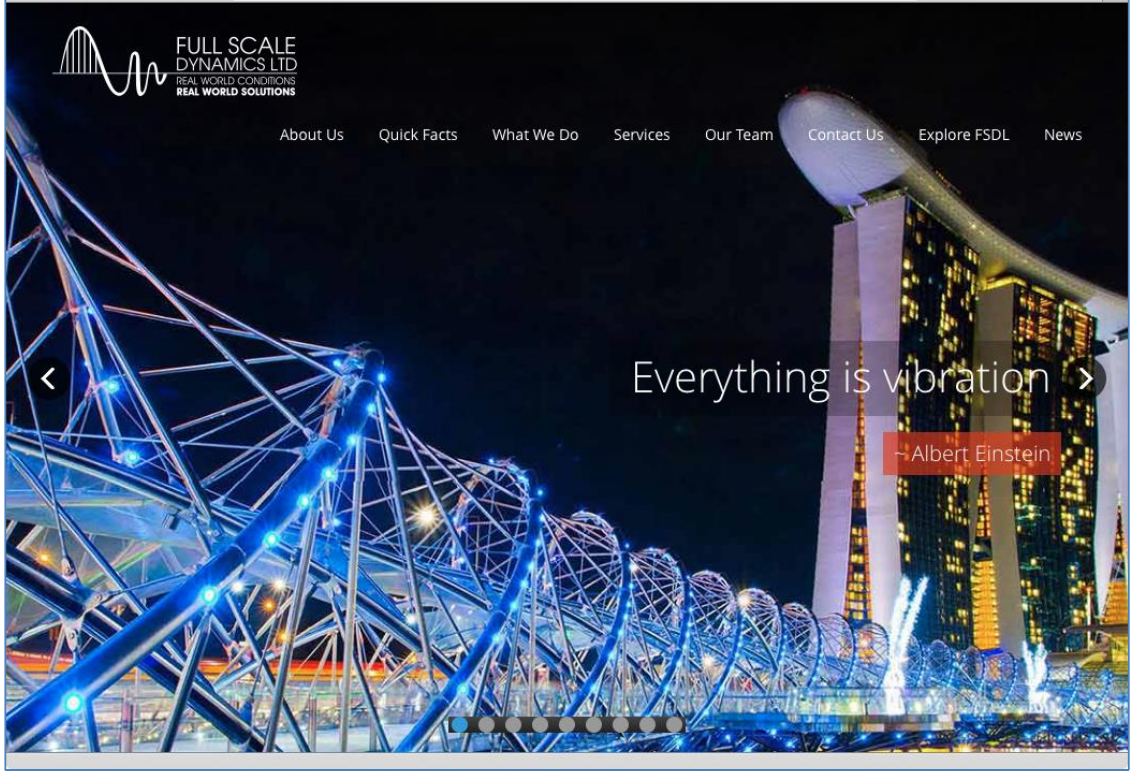
Vibration Engineering Section (VES)



http://vibration.ex.ac.uk/

Full Scale Dynamics Limited

http://www.fullscaledynamics.com/



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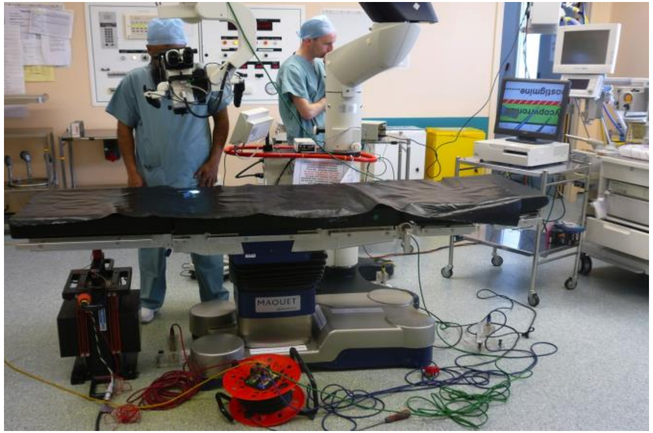
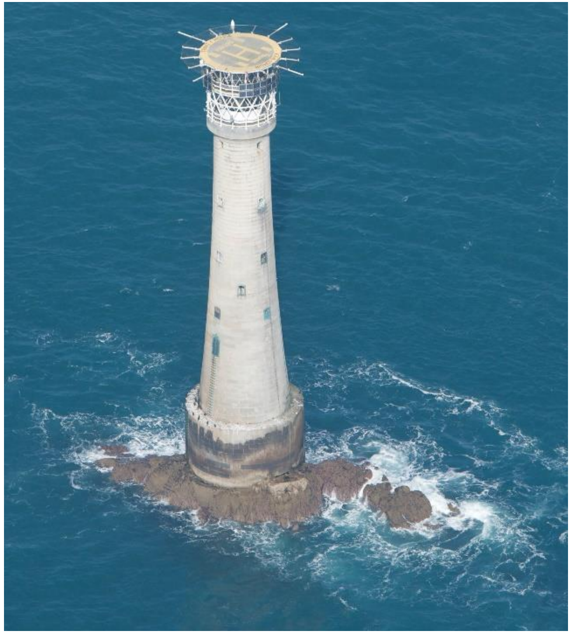
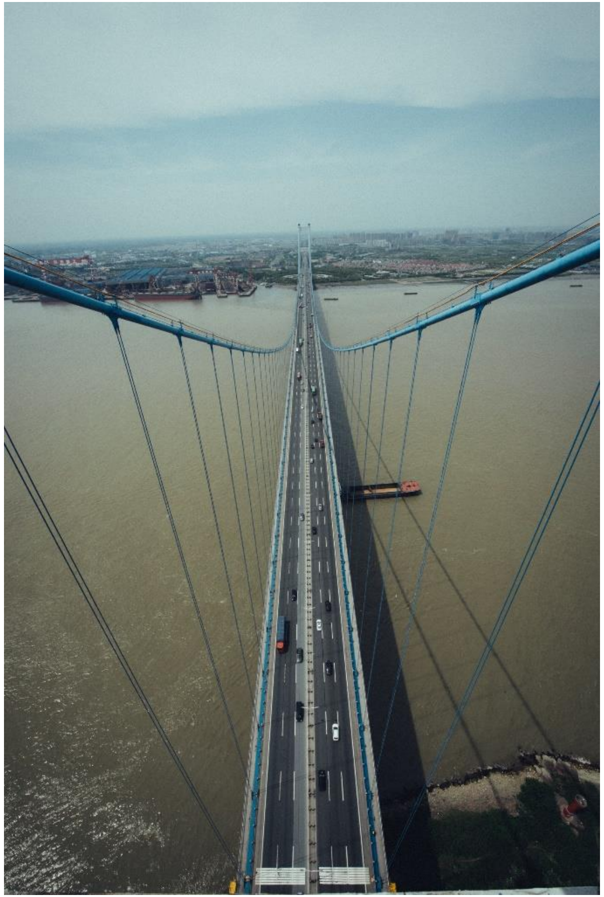
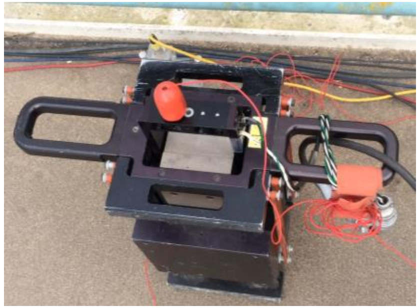






Field modal testing

Free vibration test
(zero input)



Forced vibration test
(Known input)

Ambient vibration test
(Unknown input)

- Testing under **ambient condition** (no input info) is the future for extreme long/tall structures but results have significant uncertainty
- Uncertainties are critical in ambient tests!
- BAYOMALAW project aims to understand how best to manage these uncertainties

Data Acquisition System Requirements

- Distributed sensors separated over long distances
  - NO CABLES!
- All sensors synchronised to a common clock
- Long duration data acquisition with no drift in clock
- Able to work inside / with no reliable GPS signal
- Option to add additional units at a later stage

Design

- CompactRIO platform
- Oven Controlled Crystal Oscillator (OCXO) @ 10MHz

SYSTEM DESIGN

General Design

Task 1 – Data acquisition triggered from a local clock (FPGA)

Task 2 – Update the slave clocks based on a ‘master’ clock (FPGA)

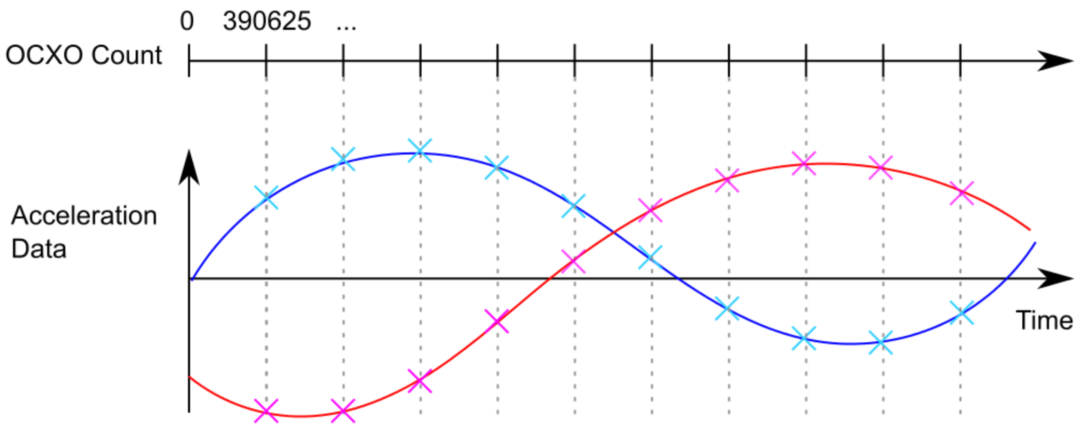
Task 3 – Log the synchronised samples to file (Real Time)

FPGA Design

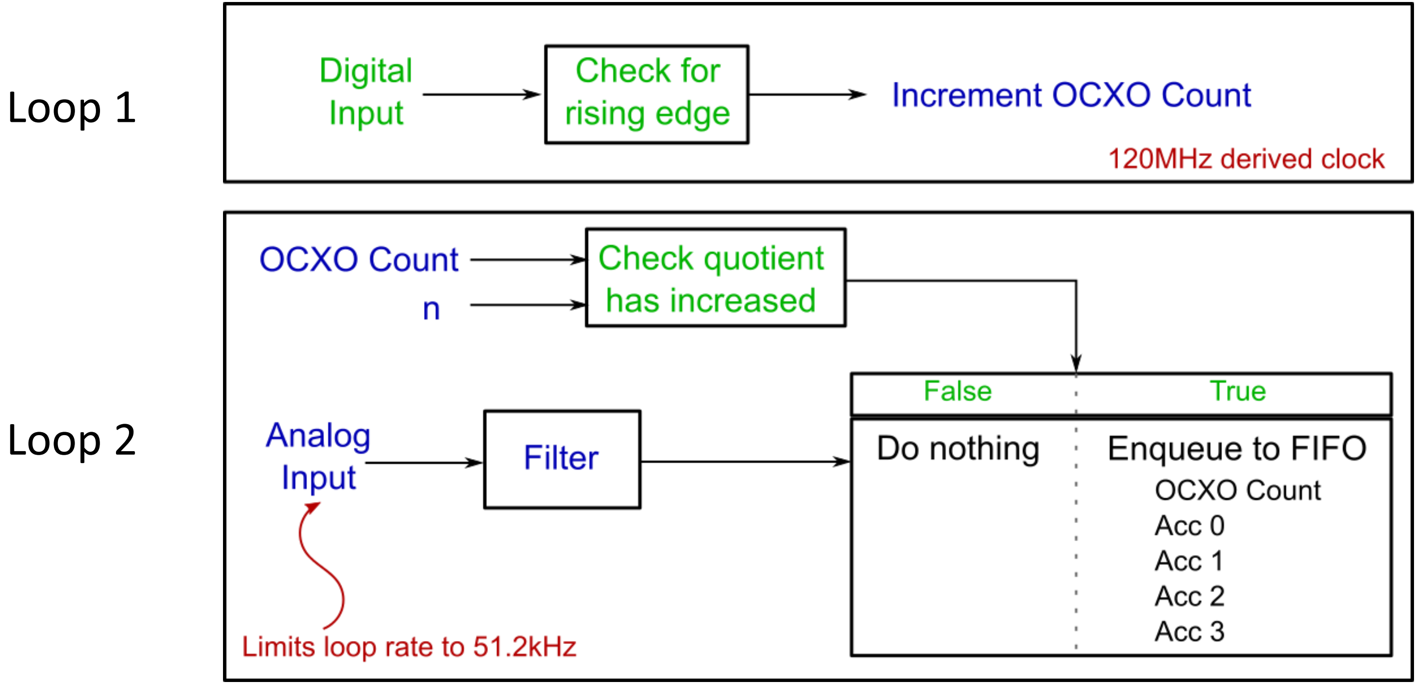
Task 1 – Data acquisition based on local clock

- Connect OCXO to Digital Input
- Increment OCXO Count on rising edge
- Trigger to take a sample after ‘n’ counts
  - E.g. OCXO frequency = 10MHz
  - Sampling frequency = 25.6Hz
  - n = 390,625
- Filter to reduce aliasing issues!

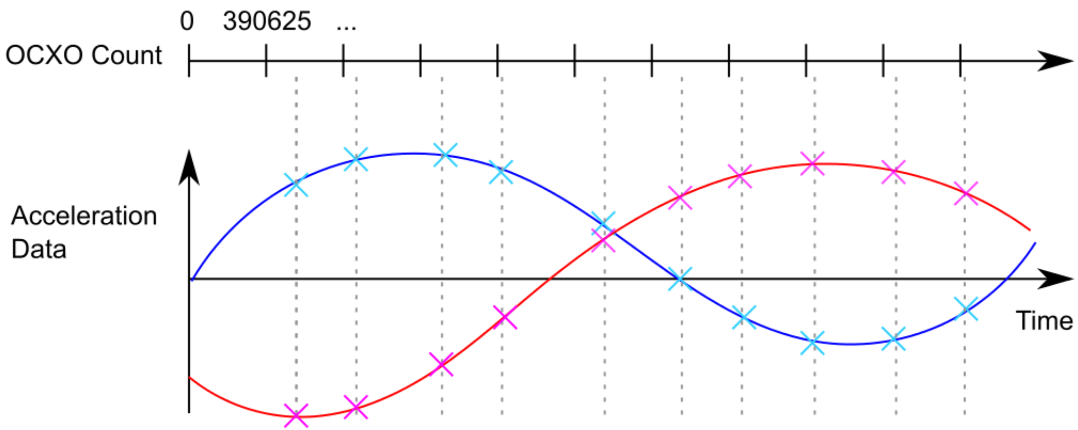
FPGA Design



FPGA Design


Loop 1
Digital Input
Check for rising edge
Increment OCXO Count
120MHz derived clock
Loop 2
OCXO Count
n
Check quotient has increased
False
True
Analog Input
Filter
Do nothing
Enqueue to FIFO
OCXO Count
Acc 0
Acc 1
Acc 2
Acc 3
Limits loop rate to 51.2kHz

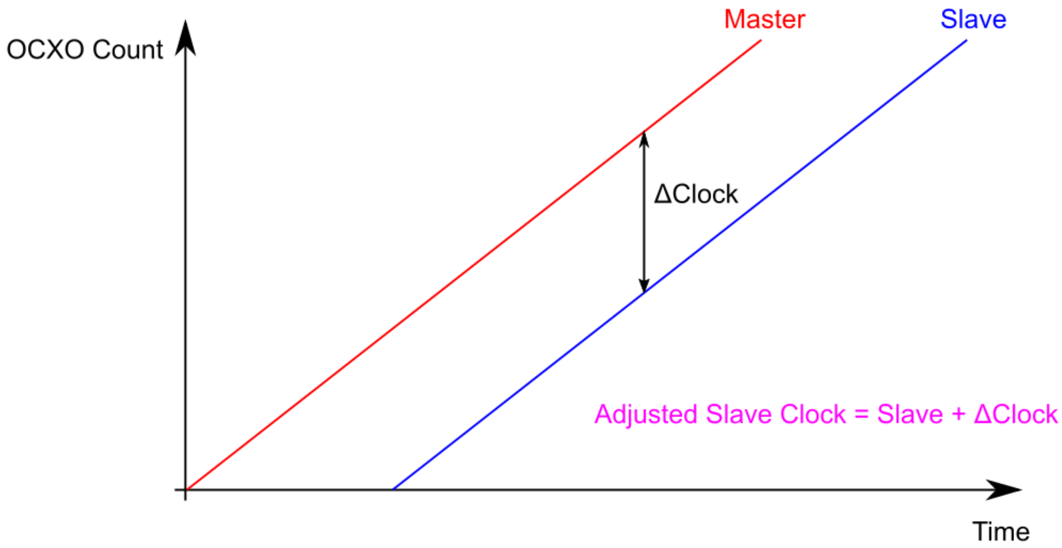
FPGA Design



Could interpolate if REALLY wanted to

FPGA Design

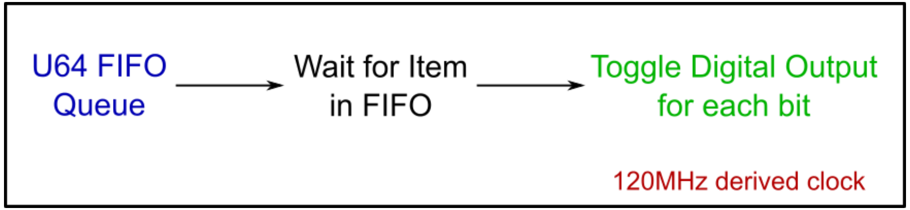
Task 2 – Update the slave clocks based on a 'master' clock



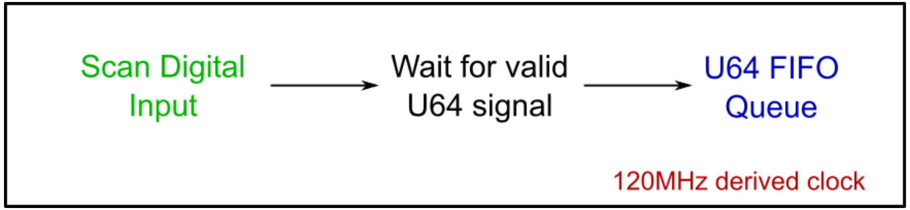
FPGA Design

- Send OCXO Clock from ‘Master’ unit to ‘Slave’ units
- Use Digital I/O line – synchronise using a BNC cable
- “FPGA Send Data.vi” and “FPGA Receive Data.vi”
  - Nick Williamson @ National Instruments
  - “Passing fast data between compact RIO targets using single DIO”

Loop 3 (Master)



Loop 3 (Slave)



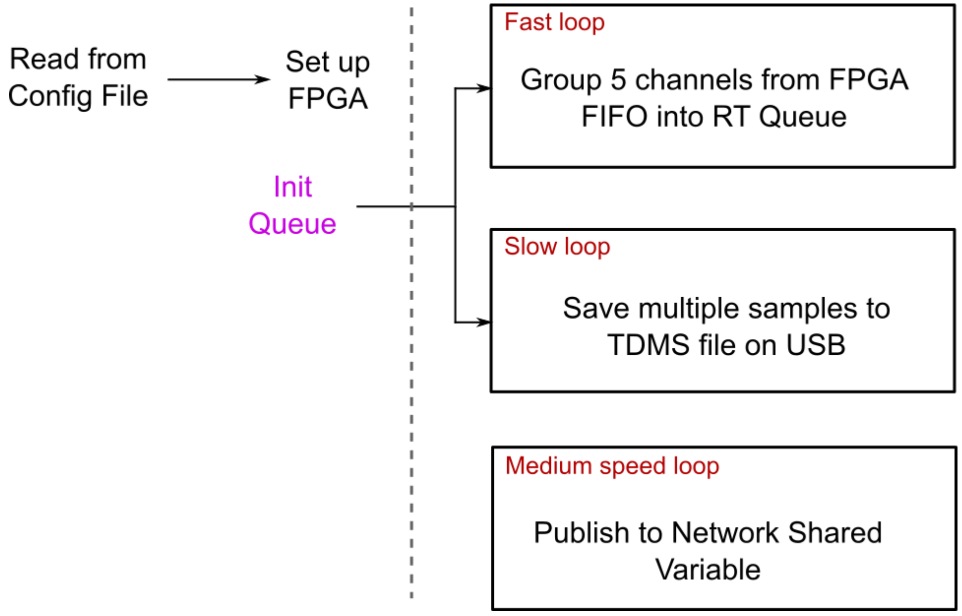
FPGA Design

Final FPGA code has four loops:

1. Increment OCXO count
2. Acquire + filter data, then put in FIFO
3. Send OR receive ‘master’ clock
   - Update Δclock
4. Flash LED code
   - Device is Master
   - Device is Slave and IS NOT synchronised
   - Device is Slave and IS synchronised

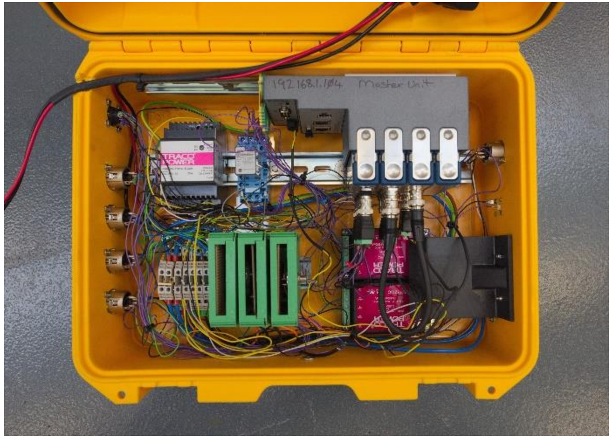
RT Design

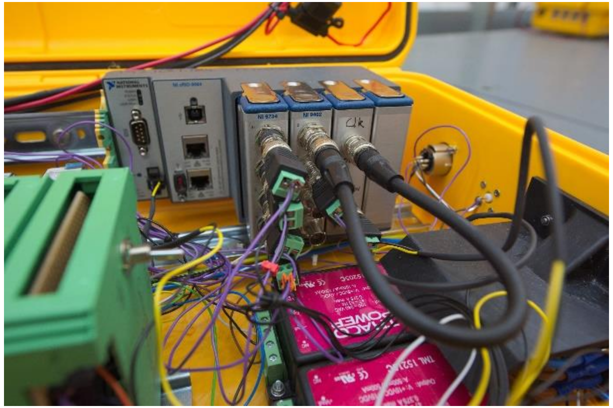
Task 3 – Log the synchronised samples to file



HARDWARE

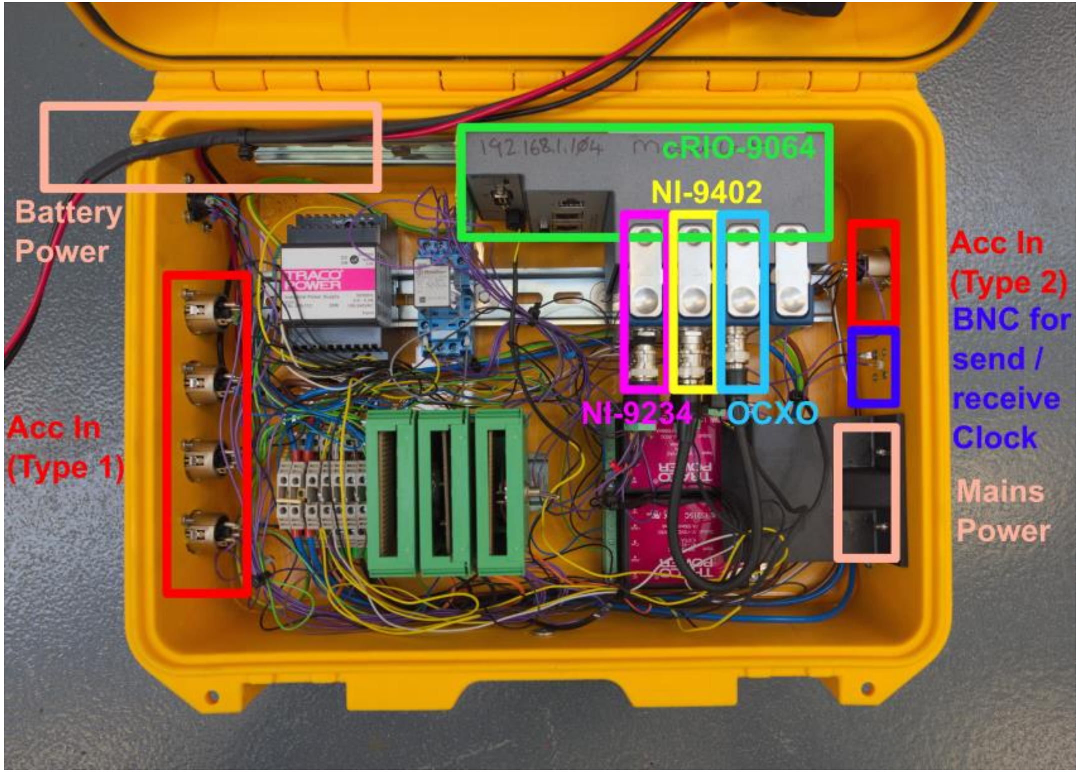
Hardware



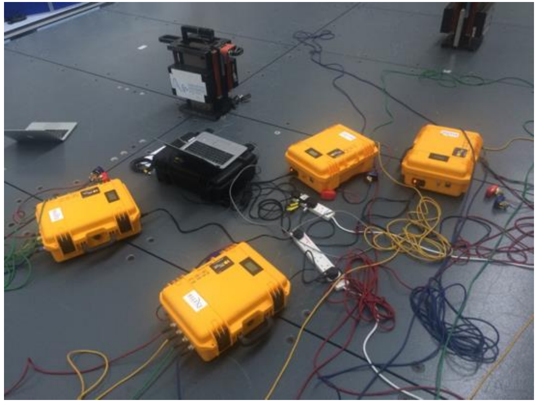


Hardware

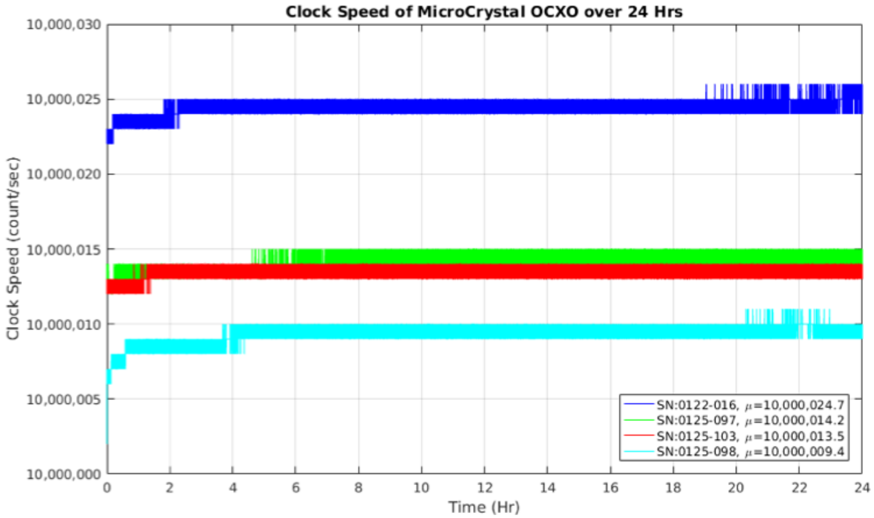
- NI cRIO-9064
- NI-9234 (4 Channel Analog In)
- NI-9402 (4 Channel Digital IO)
- OCXO
- Connect one of two accelerometer types
- Power through mains or battery
- DIN rail mounted

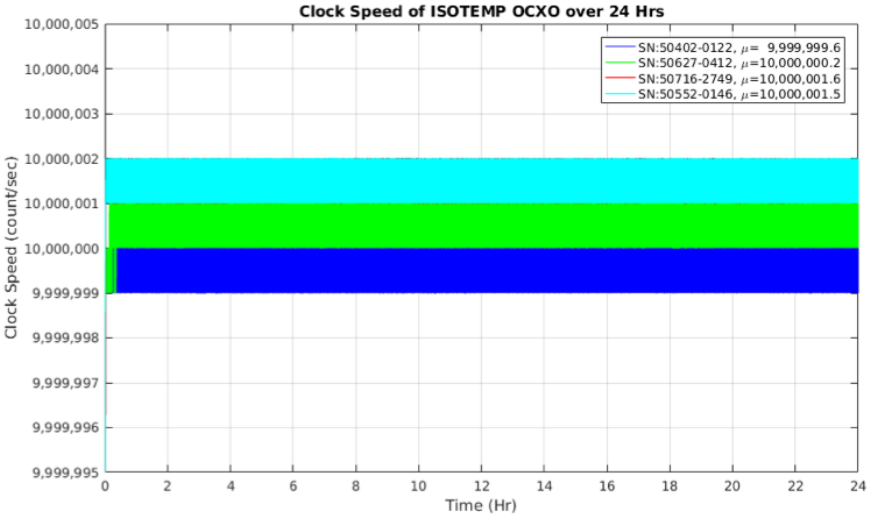


Testing in Exeter



Test OCXO against GPS





OCXO type 1: **2ppm** difference
→ 20° phase at 1Hz after 8 hours

OCXO type 2: **0.2ppm** difference
→ 2° phase at 1Hz after 8 hours

FIELD TESTING

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Jiangyin Bridge (April 2017)

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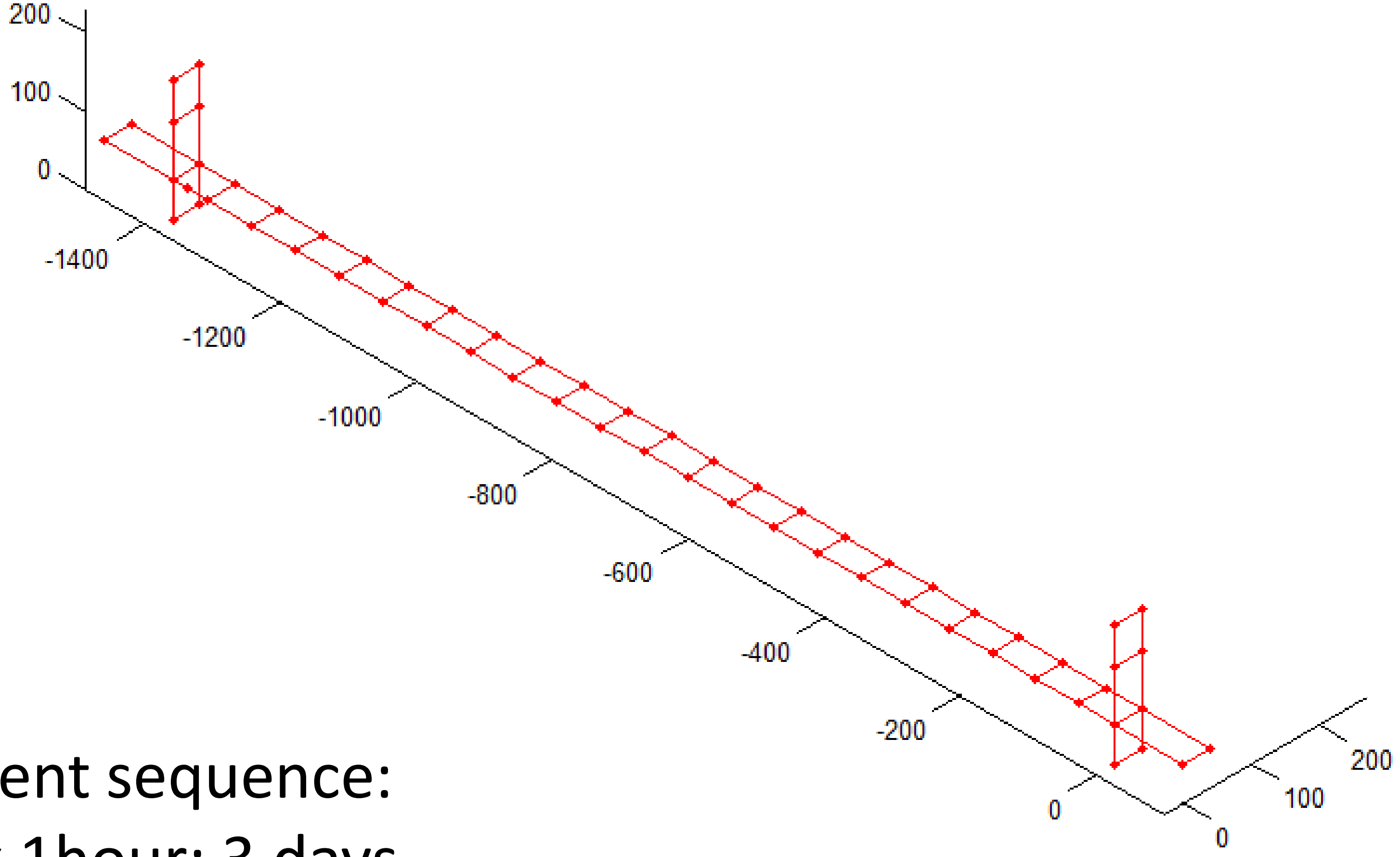
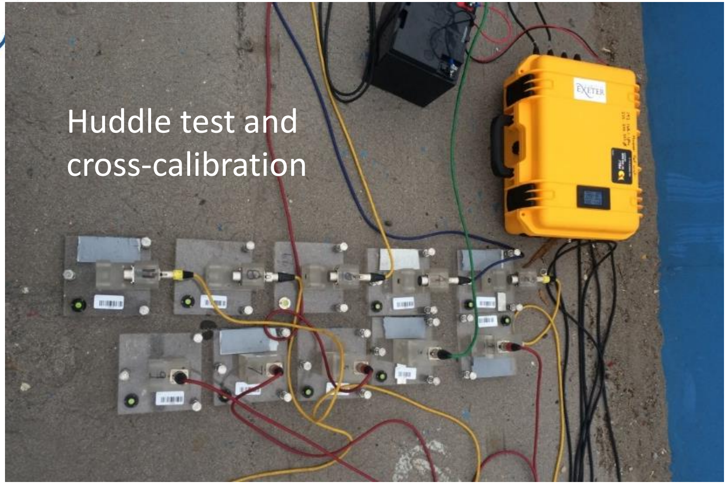
Jiangyin Bridge (April 2017)



Measurement sequence:
13 setups x 1hour; 3 days

Jiangyin Bridge (April 2017)



Huddle test and cross-calibration

Setting slaves to master time

Lateral and vertical reference accelerometers

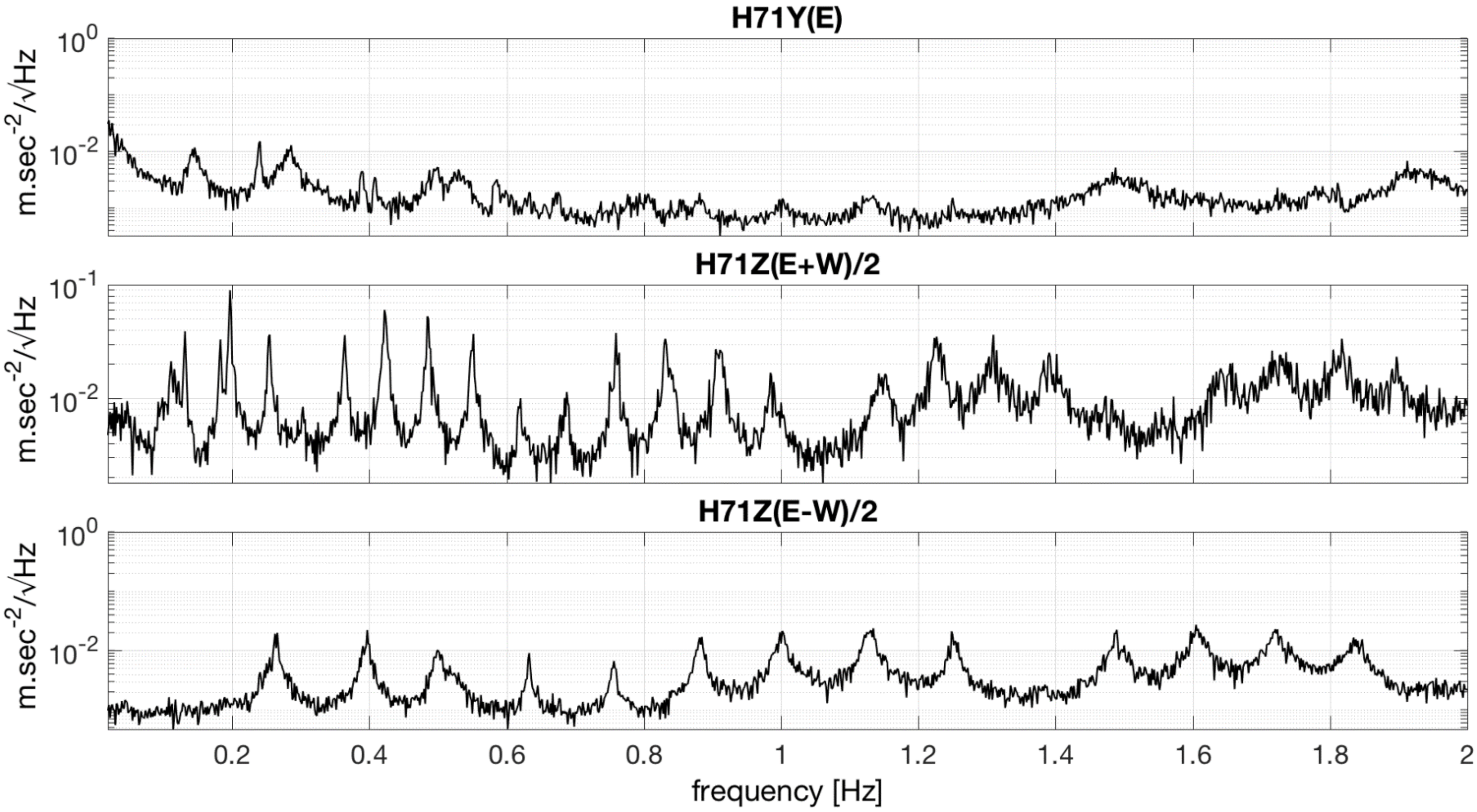
Checking the data (LAN cable to DAQ or remove USB drive)

Modal (log) acceleration PSD

Lateral

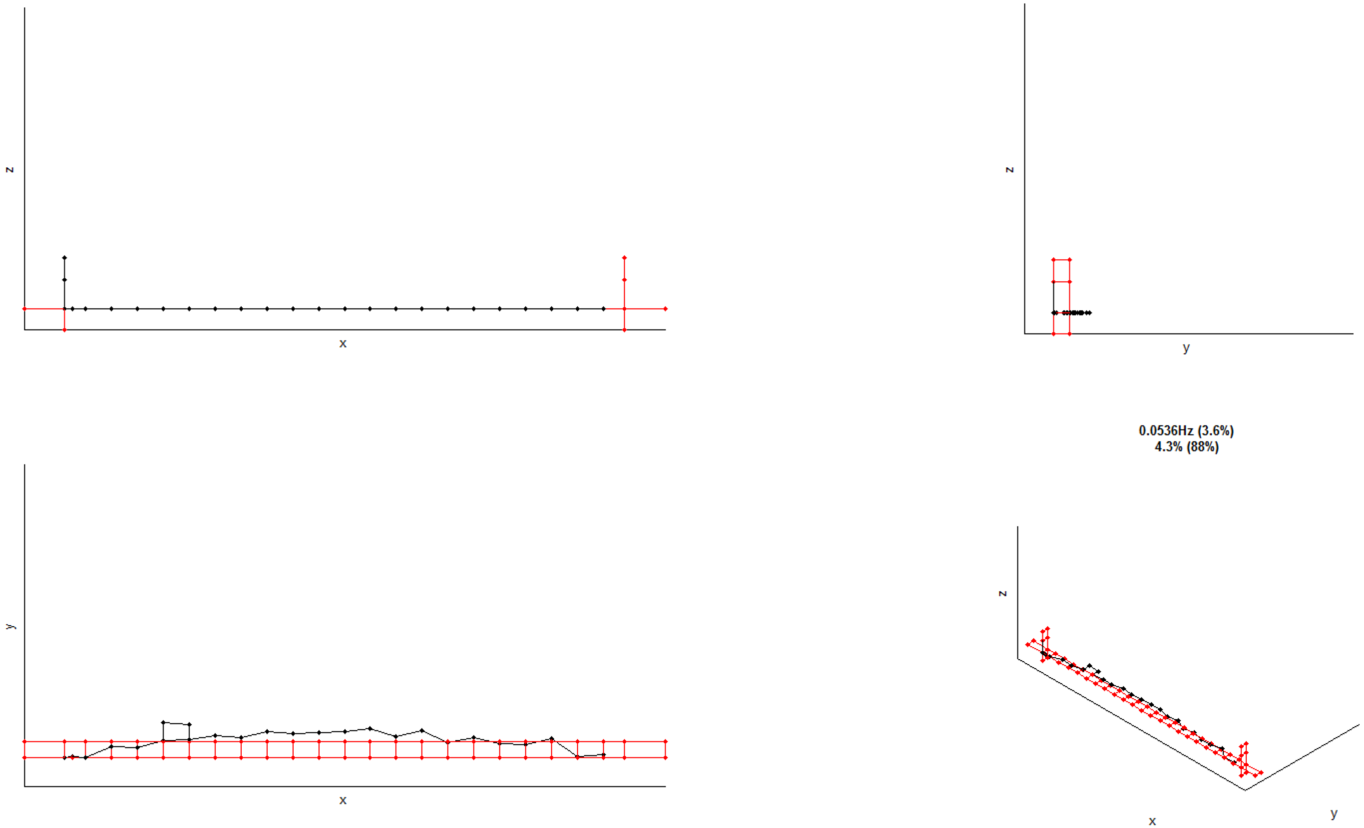
Vertical

Torsional



Modes: Lateral 1

f =0.0536 Hz ($\pm$3.6%) ζ =4.4% ($\pm$88%)



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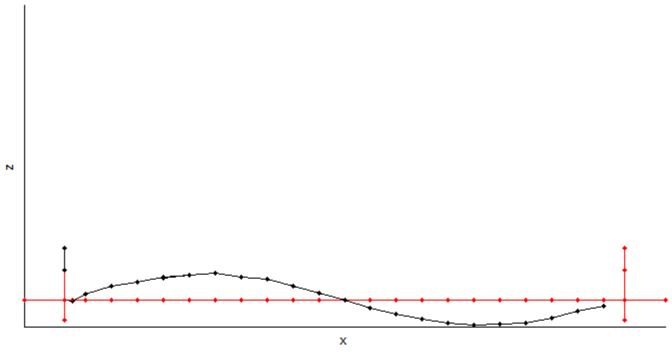
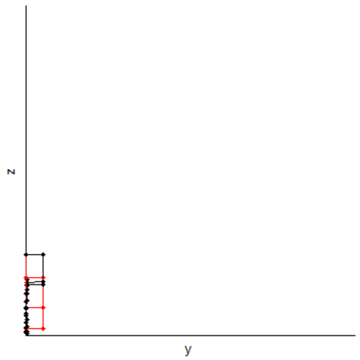
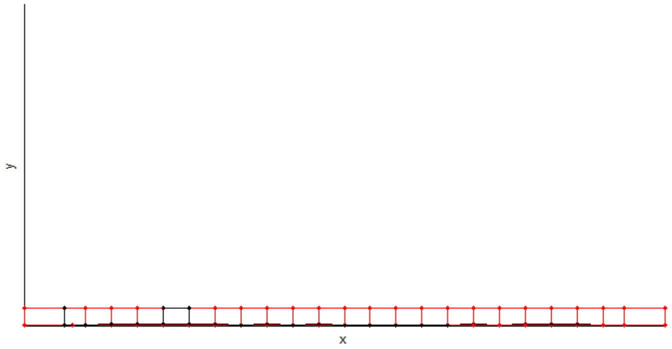
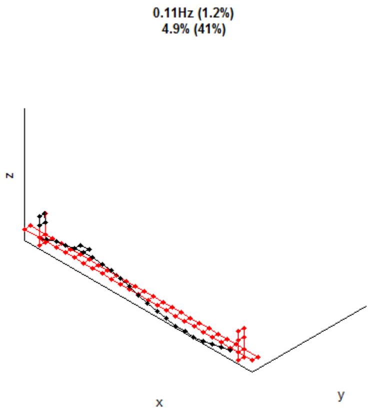
Modes: Vertical 1

f =0.110 Hz ($\pm$1.2%) ζ =4.9% ($\pm$41%)



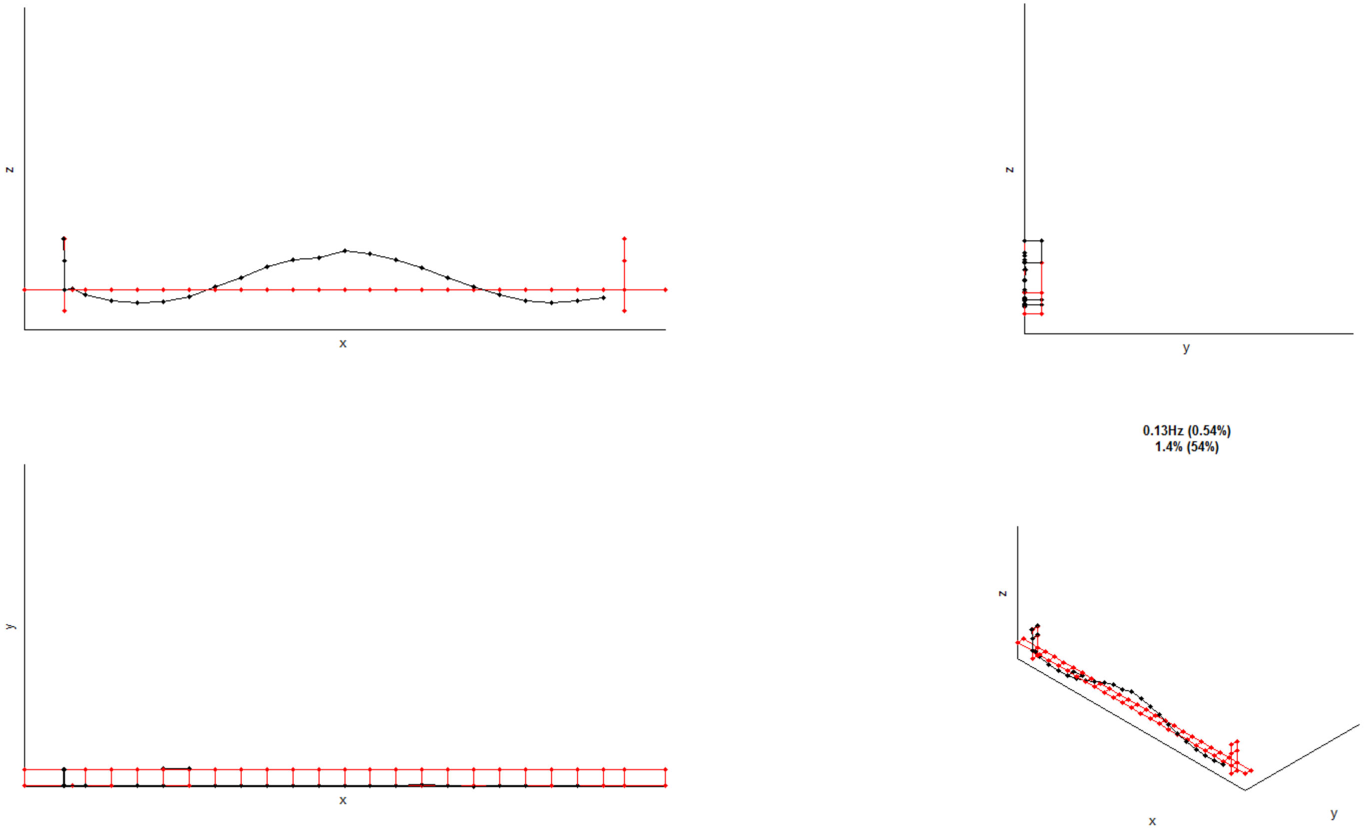






Modes: Vertical 2

f =0.130 Hz ($\pm$0.54%) ζ =1.4% ($\pm$54%)



Queensferry Crossing

Comprehensive SHM system requires identification of:

- global dynamic properties
- multimode damping and frequency for all 288 stay cables

Test plan (October 2017)

- Minimum 58 TPs for measuring accelerations
- Will use ten recorder boxes with 3 or 4 accelerometer signals per box: uni-axial and tri-axial.
- One set of accelerometers will be maintained at the same location close to tower in one of the main spans.
- First mode 0.15 Hz - 0.20 Hz with damping ~ 2%
  - 1 hour duration is suggested

CONCLUDING REMARKS

Concluding Remarks

- Developed a novel distributed data acquisition system
- Highly synchronised
  - Minimal phase difference over long duration measurements
- Highly distributed
  - Suitable for long span bridges, tall buildings, inside / outside
- Highly modular
  - Expanding capabilities to test even larger structures

Acknowledgements

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  - BAYOMALAW project (EN/N017897/1)

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Thanks for listening!

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- Any questions?

Extra slides …

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