DAQ

PC-DIO-96/PnP
User Manual

Digital I/O Board for ISA

September 1996 Edition
Part Number 320289C-01

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About This Manual

This manual describes the mechanical and electrical aspects of the PC-DIO-96/PnP and contains information concerning its operation and programming.

The PC-DIO-96PnP is a member of the National Instruments PC Series of I/O channel expansion boards for ISA computers. These boards are designed for high-performance data acquisition and control for applications in laboratory testing, production testing, and industrial process monitoring and control.

This manual also applies to the PC-DIO-96, a non-Plug and Play device. The boards are identical except for the differences listed in Appendix E, *Using Your PC-DIO-96 (Non-PnP) Board*.

Organization of This Manual

The *PC-DIO-96/PnP User Manual* is organized as follows:

- Chapter 1, *Introduction*, describes the PC-DIO-96/PnP; lists what you need to get started; describes software programming choices, optional equipment, and custom cables; and explains how to unpack the PC-DIO-96/PnP.
- Chapter 2, *Installation and Configuration*, describes how to install and configure the PC-DIO-96PnP board.
- Chapter 3, *Signal Connections*, includes timing specifications and signal connection instructions for the PC-DIO-96/PnP I/O connector.
- Chapter 4, *Theory of Operation*, contains a functional overview of the PC-DIO-96PnP board and explains the operation of each functional unit making up the PC-DIO-96PnP.
- Appendix A, *Specifications*, lists the specifications of the PC-DIO-96/PnP.
- Appendix B, *OKI 82C55A Data Sheet*, contains the manufacturer data sheet for the OKI 82C55A (OKI Semiconductor) CMOS

programmable peripheral interface. This interface is used on the PC-DIO-96/PnP board.

- Appendix C, *OKI 82C53 Data Sheet*, contains the manufacturer data sheet for the OKI 82C53 integrated circuit (OKI Semiconductor). This circuit is used on the PC-DIO-96/PnP board.
- Appendix D, *Register-Level Programming*, describes in detail the address and function of each of the PC-DIO-96/PnP control and status registers. This appendix also includes important information about register-level programming the PC-DIO-96/PnP along with program examples written in C and assembly language.
- Appendix E, *Using Your PC-DIO-96 (Non-PnP) Board*, describes the differences between the PC-DIO-96PnP and PC-DIO-96 boards, the PC-DIO-96 board configuration, and the installation of the PC-DIO-96 into your computer.
- Appendix F, *Customer Communication*, contains forms you can use to request help from National Instruments or to comment on our products.
- The *Glossary* contains an alphabetical list and description of terms used in this manual, including abbreviations, acronyms, metric prefixes, mnemonics, and symbols.
- The *Index* alphabetically lists the topics in this manual, including the page where you can find each one.

Conventions Used in This Manual

The following conventions are used in this manual:

82C53	82C53 refers to the OKI 82C53 (OKI Semiconductor) CMOS programmable interval timer.
82C55A	82C55A refers to the OKI 82C55A (OKI Semiconductor) CMOS programmable peripheral interface.
< >	Angle brackets containing numbers separated by an ellipses represent a range of values associated with a bit or signal name (for example, ACH<0..7>).
bold	Bold text denotes the names of menus, menu items, or dialog box buttons or options.
bold italic	Bold italic text denotes a note, caution, or warning.
italic	Italic text denotes emphasis, a cross reference, or an introduction to a key concept.

`monospace`	Text in this font denotes text or characters that are to be literally input from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames, and extensions, and for statements and comments taken from program code.
NI-DAQ	NI-DAQ refers to the NI-DAQ software for PC compatibles unless otherwise noted.
PC-DIO-96/PnP	PC-DIO-96/PnP refers to both the Plug and Play and non-Plug and Play compatible versions of the board.
PC-DIO-96PnP	PC-DIO-96PnP refers to the Plug and Play version of the PC-DIO-96/PnP.
PC-DIO-96	PC-DIO-96 refers to the non-Plug and Play version of the PC-DIO-96/PnP.
PnP	PnP (Plug and Play) refers to a device that is fully compatible with the industry standard Plug and Play ISA Specification. All bus-related configuration is performed through software, freeing the user from manually configuring jumpers or switches to set the product's base address and interrupt level. Plug and Play systems automatically arbitrate and assign system resources to a PnP product.
non-PnP	Non-PnP (non-Plug and Play) refers to a device that requires a user to configure the product's base address and interrupt level with switches and jumpers. This configuration must be performed prior to installing the product in the computer.
PPI *x*	PPI *x*, where the *x* is replaced by A, B, C, or D, refers to one of the four programmable peripheral interface (PPI) chips on the PC-DIO-96/PnP.
SCXI	SCXI stands for Signal Conditioning eXtensions for Instrumentation and is a National Instruments product line designed to perform front-end signal conditioning for National Instruments plug-in DAQ boards.

Abbreviations, acronyms, metric prefixes, mnemonics, and symbols are listed in the *Glossary*.

National Instruments Documentation

The *PC-DIO-96/PnP User Manual* is one piece of the documentation set for your data acquisition (DAQ) system. You could have any of several types of manuals, depending on the hardware and software in your system. Use the different types of manuals you have as follows:

- *Getting Started with SCXI*—If you are using SCXI, this is the first manual you should read. It gives an overview of the SCXI system and contains the most commonly needed information for the modules, chassis, and software.
- Your SCXI hardware user manuals—If you are using SCXI, read these manuals next for detailed information about signal connections and module configuration. They also explain in greater detail how the module works and contain application hints.
- Your DAQ hardware user manuals—These manuals have detailed information about the DAQ hardware that plugs into or is connected to your computer. Use these manuals for hardware installation and configuration instructions, specification information about your DAQ hardware, and application hints.
- Software documentation—Examples of software documentation you may have are the LabVIEW, LabWindows®/CVI, and NI-DAQ documentation sets. After you set up your hardware system, use either the application software (LabVIEW or LabWindows/CVI) documentation or the NI-DAQ documentation to help you write your application. If you have a large and complicated system, it is worthwhile to look through the software documentation before you configure your hardware.
- Accessory installation guides or manuals—If you are using accessory products, read the terminal block and cable assembly installation guides or accessory board user manuals. They explain how to physically connect the relevant pieces of the system. Consult these guides when you are making your connections.
- *SCXI Chassis User Manual*—If you are using SCXI, read this manual for maintenance information on the chassis and installation instructions.

Related Documentation

If you are a register-level programmer, the following documents contain information that you may find helpful as you read this manual:

- Your computer technical reference manual
- *Plug and Play ISA Specification*

Customer Communication

National Instruments wants to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix F, *Customer Communication*, at the end of this manual.

Chapter 1

Introduction

This chapter describes the PC-DIO-96/PnP; lists what you need to get started; describes software programming choices, optional equipment, and custom cables; and explains how to unpack the PC-DIO-96/PnP.

About the PC-DIO-96/PnP

Thank you for purchasing the National Instruments PC-DIO-96/PnP. *PnP* refers to the Plug and Play technology used in this board. See the *Conventions Used in this Manual* section in *About This Manual* for an explanation. The PC-DIO-96/PnP is a 96-bit, parallel, digital I/O interface for ISA computers. Four 82C55A programmable peripheral interface (PPI) chips control the 96 bits of digital I/O. The 82C55A can operate in either a unidirectional or bidirectional mode and can generate interrupt requests to the host computer. You can program the 82C55A for almost any 8-bit or 16-bit digital I/O application. All digital I/O communication is through a standard, 100-pin, male connector. The PC-DIO-96/PnP also includes an 82C53 counter/timer that can send periodic interrupts to the host system.

If you have the non-PnP version of the PC-DIO-96/PnP, see Appendix E, *Using Your PC-DIO-96 (Non-PnP) Board*, for the differences between the PnP version and the non-PnP version.

You can use the PC-DIO-96/PnP in a wide range of digital I/O applications. With the PC-DIO-96/PnP, you can interface any PC to any of the following:

- Other computers
  - Another PC with a National Instruments PC-DIO-96/PnP, PC-DIO-24, or AT-DIO-32F
  - IBM Personal System/2 with a National Instruments MC-DIO-24 or MC-DIO-32F

  - Macintosh II with a National Instruments NB-DIO-24, NB-DIO-32F, or PCI-DIO-96
  - Any other computer with an 8-bit or 16-bit parallel interface
- Centronics-compatible printers and plotters
- Panel meters
- Instruments and test equipment with BCD readouts and/or controls
- Optically isolated, solid-state relays and I/O module mounting racks

☞ **Note:** ***The PC-DIO-96/PnP cannot sink sufficient current to drive the SSR-OAC-5 and SSR-OAC-5A output modules. However, it can drive the SSR-ODC-5 output module and all SSR input modules available from National Instruments.***

If you need to drive an SSR-OAC-5 or SSR-OAC-5A, you can either use a non-inverting digital buffer chip between the PC-DIO-96/PnP and the SSR backplane, or you can use a DIO-23F or MIO Series board with appropriate connections (for example, SC-205X and cables).

With the PC-DIO-96/PnP, a PC can serve as a digital I/O system controller for laboratory testing, production testing, and industrial process monitoring and control.

Detailed specifications of the PC-DIO-96/PnP are in Appendix A, *Specifications*.

What You Need to Get Started

To set up and use your PC-DIO-96/PnP, you will need the following:

- ❑ PC-DIO-96/PnP board
- ❑ *PC-DIO-96/PnP User Manual*
- ❑ One of the following software packages and documentation:

  NI-DAQ for PC Compatibles

  LabVIEW for Windows

  LabWindows/CVI
- ❑ Your computer

Software Programming Choices

There are several options to choose from when programming your National Instruments DAQ and SCXI hardware. You can use LabVIEW, LabWindows/CVI, NI-DAQ, or register-level programming. NI-DAQ version 4.6.1 or earlier supports LabWindows for DOS.

LabVIEW and LabWindows/CVI Application Software

LabVIEW and LabWindows/CVI are innovative program development software packages for data acquisition and control applications. LabVIEW uses graphical programming, whereas LabWindows/CVI enhances traditional programming languages. Both packages include extensive libraries for data acquisition, instrument control, data analysis, and graphical data presentation.

LabVIEW features interactive graphics, a state-of-the-art user interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of VIs for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW. The LabVIEW Data Acquisition VI Library is functionally equivalent to the NI-DAQ software.

LabWindows/CVI features interactive graphics, a state-of-the-art user interface, and uses the ANSI standard C programming language. The LabWindows/CVI Data Acquisition Library, a series of functions for using LabWindows/CVI with National Instruments DAQ hardware, is included with the NI-DAQ software kit. The LabWindows/CVI Data Acquisition Library is functionally equivalent to the NI-DAQ software.

Using LabVIEW or LabWindows/CVI software will greatly reduce the development time for your data acquisition and control application.

NI-DAQ Driver Software

The NI-DAQ driver software is included at no charge with all National Instruments DAQ hardware. NI-DAQ is not packaged with SCXI or accessory products, except for the SCXI-1200. NI-DAQ has an extensive library of functions that you can call from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high-speed A/D conversion), analog output (D/A conversion), waveform generation,

digital I/O, counter/timer operations, SCXI, RTSI, self-calibration, messaging, and acquiring data to extended memory.

NI-DAQ has both high-level DAQ I/O functions for maximum ease of use and low-level DAQ I/O functions for maximum flexibility and performance. Examples of high-level functions are streaming data to disk or acquiring a certain number of data points. An example of a low-level function is writing directly to registers on the DAQ device. NI-DAQ does not sacrifice the performance of National Instruments DAQ devices because it lets multiple devices operate at their peak performance.

NI-DAQ also internally addresses many of the complex issues between the computer and the DAQ hardware such as programming interrupts and DMA controllers. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to your code. Whether you are using conventional programming languages, LabVIEW, or LabWindows/CVI, your application uses the NI-DAQ driver software, as illustrated in Figure 1-1.

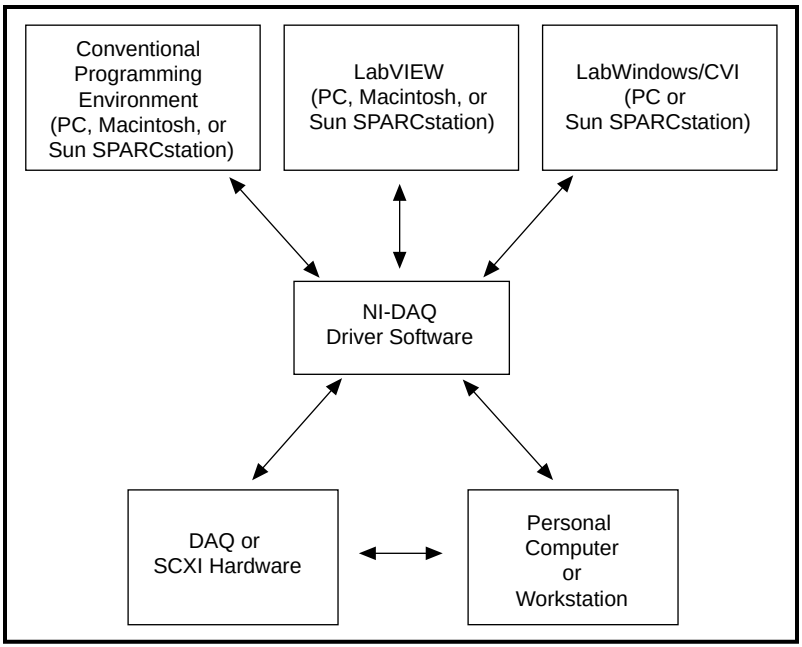


Figure 1-1. The Relationship between the Programming Environment, NI-DAQ, and Your Hardware

Register-Level Programming

The final option for programming any National Instruments DAQ hardware is to write register-level software. Writing register-level programming software can be very time-consuming and inefficient, and is not recommended for most users.

Even if you are an experienced register-level programmer, consider using NI-DAQ, LabVIEW, or LabWindows/CVI to program your National Instruments DAQ hardware. Using the NI-DAQ, LabVIEW, or LabWindows/CVI software is easier than, and as flexible as, register-level programming, and can save weeks of development time.

Optional Equipment

National Instruments offers a variety of products to use with your PC-DIO-96/PnP board, including cables, connector blocks, and other accessories, as follows:

- Cables and cable assemblies
- Connector blocks and unshielded 50-pin screw terminals
- SCXI modules and accessories for isolating, amplifying, exciting, and multiplexing signals for relays and analog output. With SCXI you can condition and acquire up to 3,072 channels.
- Low channel count signal conditioning modules, boards, and accessories, including conditioning for strain gauges and RTDs, simultaneous sample and hold, and relays.

For more specific information about these products, refer to your National Instruments catalog or call the office nearest you.

Custom Cabling

National Instruments offers cables and accessories for you to prototype your application or to use if you frequently change board interconnections.

You can interface the PC-DIO-96/PnP to a wide range of printers, plotters, test instruments, I/O racks and modules, screw terminal panels, and almost any device with a parallel interface. The PC-DIO-96/PnP digital I/O connector is a standard, 100-pin header connector. Adapters for this header connector expand the interface to four 50-pin ribbon cables, each of which has the pinout of a PC-DIO-24. The pin assignments of the expansion cables are compatible with the standard

24-channel I/O module mounting racks (such as those manufactured by Opto 22 and Gordos).

The CB-100 cable termination accessory is available from National Instruments for use with the PC-DIO-96/PnP board. This kit includes two 50-conductor, flat-ribbon cables and a connector block. You can attach signal input and output wires to screw terminals on the connector block and therefore connect signals to the PC-DIO-96/PnP I/O connector.

The CB-100 is useful for initial prototyping of an application or in situations where PC-DIO-96/PnP interconnections are frequently changed. Once a final field wiring scheme has been developed, however, you may want to develop your own cable. This section contains information for the design of custom cables.

The PC-DIO-96/PnP I/O connector is a 100-pin, Centronics-style, male, ribbon-cable header connector. The manufacturer and the appropriate part number for this connector is as follows:

- Robinson Nugent (part number P50E-100P1-RR1-TG)

The mating connector for the PC-DIO-96/PnP is a 100-position, polarized, Centronics-style, female, ribbon-socket connector with strain relief. National Instruments uses a polarized (keyed) connector to prevent inadvertent upside-down connection to the PC-DIO-96/PnP. This 100-pin connector attaches to two 50-pin cables, each of which can be connected to a 50-pin connector on the other end. The recommended manufacturer and the appropriate part number for the 100-pin mating connector is as follows:

- Robinson Nugent (part number P50E-100S-TG)

The recommended manufacturer part numbers for 50-pin, female, ribbon-socket connectors suitable for use with the preceding connector are:

- Electronic Products Division/3M (part number 3425-7650)
- T&B/Ansley Corporation (part number 609-5041CE)

Recommended manufacturers and the appropriate part numbers for the standard ribbon cable (50-conductor, 28 AWG, stranded) that can be used with both the 100-pin and the 50-pin connectors are:

- Electronic Products Division/3M (part number 3365/50)
- T&B/Ansley Corporation (part number 171-50)

Unpacking

Your PC-DIO-96/PnP board is shipped in an antistatic package to prevent electrostatic damage to the board. Electrostatic discharge can damage several components on the board. To avoid such damage in handling the board, take the following precautions:

- Ground yourself via a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of your computer chassis before removing the board from the package.
- Remove the board from the package and inspect the board for loose components or any other sign of damage. Notify National Instruments if the board appears damaged in any way. *Do not* install a damaged board into your computer.
- *Never* touch the exposed pins of connectors.

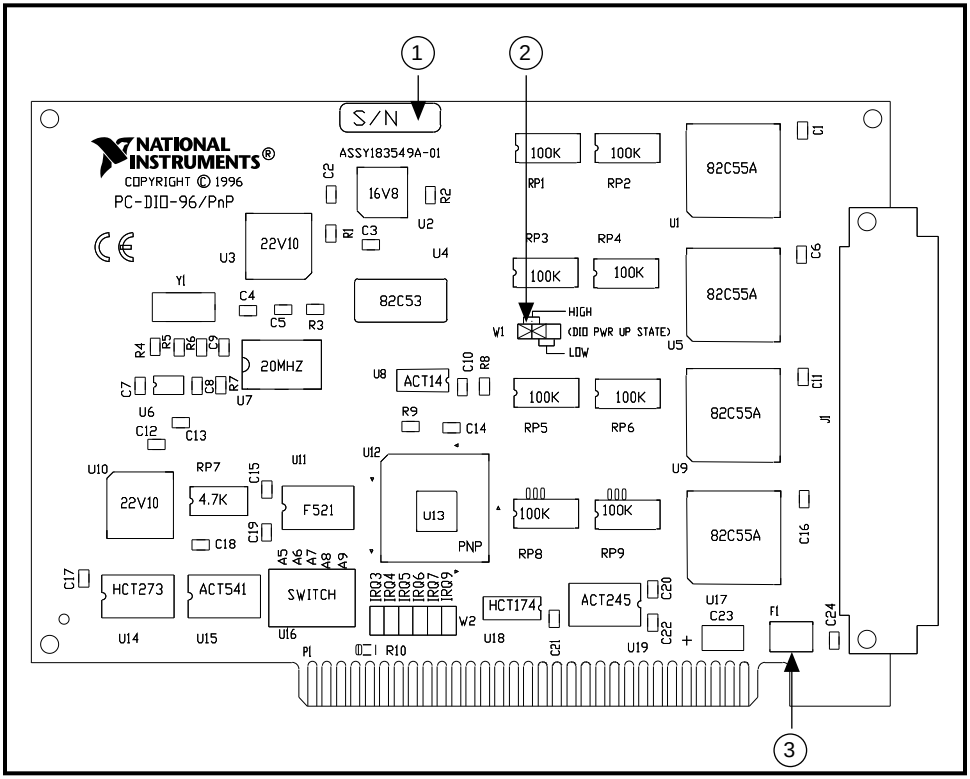
Installation and Configuration

Chapter 2

This chapter describes how to install and configure the PC-DIO-96PnP board.

Installation

☞ **Note:** ***You should install your driver software before installing your hardware. Refer to your NI-DAQ release notes for software installation instructions.***



1	Serial Number	2	W1	3	F1

Figure 2-1. PC-DIO-96PnP Parts Locator Diagram

☞ **Note:** ***The PC-DIO-96PnP uses 100 kΩ resistors for polarity selection at power-up. These signals are pulled up to VCC (+5 VDC, factory default) or pulled down to GND by selection of jumper W1. The location of W1 is shown in Figure 2-1. For more information, see the*** *Digital I/O Power-up State Selection* ***section in Chapter 3,*** *Signal Connections****.***

You can install the PC-DIO-96PnP in any available expansion slot in your computer. The following are general installation instructions, but consult your computer user manual or technical reference manual for specific instructions and warnings.

1. Turn off and unplug your computer.
2. Remove the top cover or access port to the I/O channel.
3. Remove the expansion slot cover on the back panel of the computer.
4. Insert the PC-DIO-96PnP board into any 8-bit or 16-bit slot. It may be a tight fit, but *do not force* the board into place.
5. Screw the mounting bracket of the PC-DIO-96PnP board to the back panel rail of the computer.
6. Visually verify your installation.
7. Replace the cover.
8. Plug in and turn on your computer.

Your PC-DIO-96PnP is now installed.

Hardware Configuration

Plug and Play

The PC-DIO-96PnP is fully compatible with the industry-standard Intel/Microsoft Plug and Play Specification. A Plug and Play system arbitrates and assigns resources through software, freeing you from manually setting switches and jumpers. These resources include the board base I/O address and interrupt channels. Each PC-DIO-96PnP is configured at the factory to request these resources from the Plug and Play Configuration Manager.

The Configuration Manager receives all of the resource requests at startup, compares the available resources to those requested, and assigns the available resources as efficiently as possible to the Plug and Play boards. Application software can query the Configuration Manager to determine the resources assigned to each board without your involvement. The Plug and Play software is installed as a device driver or as an integral component of the computer BIOS.

Base I/O Address and Interrupt Selection

To change base I/O address or interrupt selection, refer to the NI-DAQ Configuration Utility online help file. You can configure the PC-DIO-96PnP to use base addresses in the range of 100 to 3E0 hex. Each board occupies 16 bytes of address space and must be located on a 16-byte boundary. Therefore, valid addresses include 100, 110, 120…, 3E0 hex.

The PC-DIO-96PnP can use interrupt channels 3, 4, 5, 6, 7, and 9.

Non-Plug and Play

To configure the non-Plug and Play PC-DIO-96 board, refer to Appendix E, *Using Your PC-DIO-96 (Non-PnP) Board*.

Signal Connections

Chapter 3

This chapter includes timing specifications and signal connection instructions for the PC-DIO-96/PnP I/O connector.

Warning: ***Connections that exceed any of the maximum ratings of input or output signals on the PC-DIO-96/PnP can damage the board and the computer. The description of each signal in this section includes information about maximum input ratings. National Instruments is NOT liable for any damages resulting from any such signal connections.***

I/O Connector Pin Description

Figure 3-1 shows the pin assignments for the PC-DIO-96/PnP digital I/O connector.

APC7	1	51	CPC7
BPC7	2	52	DPC7
APC6	3	53	CPC6
BPC6	4	54	DPC6
APC5	5	55	CPC5
BPC5	6	56	DPC5
APC4	7	57	CPC4
BPC4	8	58	DPC4
APC3	9	59	CPC3
BPC3	10	60	DPC3
APC2	11	61	CPC2
BPC2	12	62	DPC2
APC1	13	63	CPC1
BPC1	14	64	DPC1
APC0	15	65	CPC0
BPC0	16	66	DPC0
APB7	17	67	CPB7
BPB7	18	68	DPB7
APB6	19	69	CPB6
BPB6	20	70	DPB6
APB5	21	71	CPB5
BPB5	22	72	DPB5
APB4	23	73	CPB4
BPB4	24	74	DPB4
APB3	25	75	CPB3
BPB3	26	76	DPB3
APB2	27	77	CPB2
BPB2	28	78	DPB2
APB1	29	79	CPB1
BPB1	30	80	DPB1
APB0	31	81	CPB0
BPB0	32	82	DPB0
APA7	33	83	CPA7
BPA7	34	84	DPA7
APA6	35	85	CPA6
BPA6	36	86	DPA6
APA5	37	87	CPA5
BPA5	38	88	DPA5
APA4	39	89	CPA4
BPA4	40	90	DPA4
APA3	41	91	CPA3
BPA3	42	92	DPA3
APA2	43	93	CPA2
BPA2	44	94	DPA2
APA1	45	95	CPA1
BPA1	46	96	DPA1
APA0	47	97	CPA0
BPA0	48	98	DPA0
+5 V	49	99	+5 V
GND	50	100	GND

Figure 3-1. Digital I/O Connector Pin Assignments

I/O Connector Signal Connection Descriptions

Pin	Signal Name	Description
1, 3, 5, 7, 9, 11, 13, 15	APC<7..0>	Bidirectional Data Lines for Port C of PPI A—APC7 is the MSB, APC0 the LSB.
17, 19, 21, 23, 25, 27, 29, 31	APB<7..0>	Bidirectional Data Lines for Port B of PPI A—APB7 is the MSB, APB0 the LSB.
33, 35, 37, 39, 41, 43, 45, 47	APA<7..0>	Bidirectional Data Lines for Port A of PPI A—APA7 is the MSB, APA0 the LSB.
2, 4, 6, 8, 10, 12, 14, 16	BPC<7..0>	Bidirectional Data Lines for Port C of PPI B—BPC7 is the MSB, BPC0 the LSB.
18, 20, 22, 24, 26, 28, 30, 32	BPB<7..0>	Bidirectional Data Lines for Port B of PPI B—BPB7 is the MSB, BPB0 the LSB.
34, 36, 38, 40, 42, 44, 46, 48	BPA<7..0>	Bidirectional Data Lines for Port A of PPI B—BPA7 is the MSB, BPA0 the LSB.
51, 53, 55, 57, 59, 61, 63, 65	CPC<7..0>	Bidirectional Data Lines for Port C of PPI C—CPC7 is the MSB, CPC0 the LSB.
67, 69, 71, 73, 75, 77, 79, 81	CPB<7..0>	Bidirectional Data Lines for Port B of PPI C—CPB7 is the MSB, CPB0 the LSB.
83, 85, 87, 89, 91, 93, 95, 97	CPA<7..0>	Bidirectional Data Lines for Port A of PPI C—CPA7 is the MSB, CPA0 the LSB.
52, 54, 56, 58, 60, 62, 64, 66	DPC<7..0>	Bidirectional Data Lines for Port C of PPI D—DPC7 is the MSB, DPC0 the LSB.
68, 70, 72, 74, 76, 78, 80, 82	DPB<7..0>	Bidirectional Data Lines for Port B of PPI D—DPB7 is the MSB, DPB0 the LSB.
84, 86, 88, 90, 92, 94, 96, 98	DPA<7..0>	Bidirectional Data Lines for Port A of PPI D—DPA7 is the MSB, DPA0 the LSB.
49, 99 (see note below)	+5 V	+5 Volts—These pins are connected to the computer's +5 VDC supply.
50, 100	GND	Ground—These pins are connected to the computer's ground signal.
Note: ***Pins 49 and 99 are connected to the +5 V PC power supply via a 1 A self-resetting fuse.***		

Port C Pin Assignments

The signals assigned to port C depend on the mode in which the 82C55A is programmed. In mode 0, port C is considered as two 4-bit I/O ports. In modes 1 and 2, port C is used for status and handshaking signals with zero, two, or three lines available for general-purpose input/output. The following table summarizes the signal assignments of port C for each programmable mode. Consult Appendix D, *Register-Level Programming*, for programming information.

Warning: ***During programming, note that each time a port is configured, output ports A and C are reset to 0, and output port B is undefined.***

Table 3-1. Port C Signal Assignments

Programming Mode	Group A					Group B		
	PC7	**PC6**	**PC5**	**PC4**	**PC3**	**PC2**	**PC1**	**PC0**
Mode 0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
Mode 1 Input	I/O	I/O	IBF_A	STB_A*	$INTR_A$	STB_B*	$IBFB_B$	$INTR_B$
Mode 1 Output	OBF_A*	ACK_A*	I/O	I/O	$INTR_A$	ACK_B*	OBF_B*	$INTR_B$
Mode 2	OBF_A*	ACK_A*	IBF_A	STB_A*	$INTR_A$	I/O	I/O	I/O
* Indicates that the signal is active low								

Cable Assembly Connectors

The cable assembly referred to in *Optional Equipment* in Chapter 1, *Introduction*, is an assembly of two 50-pin cables and three connectors. Both cables are joined to a single connector on one end and to individual connectors on the free ends. The 100-pin connector that joins the two cables plugs into the I/O connector of the PC-DIO-96/PnP. The other two connectors are 50-pin connectors, one of which is connected to pins 1 through 50 and the other is connected to pins 51 through 100 of the PC-DIO-96/PnP I/O connector. The cable with the label on it is connected to pins 1 through 50. Figures 3-2 and 3-3 show the pin assignments for the 50-pin connectors on the cable assembly.

APC7	1	2	BPC7
APC6	3	4	BPC6
APC5	5	6	BPC5
APC4	7	8	BPC4
APC3	9	10	BPC3
APC2	11	12	BPC2
APC1	13	14	BPC1
APC0	15	16	BPC0
APB7	17	18	BPB7
APB6	19	20	BPB6
APB5	21	22	BPB5
APB4	23	24	BPB4
APB3	25	26	BPB3
APB2	27	28	BPB2
APB1	29	30	BPB1
APB0	31	32	BPB0
APA7	33	34	BPA7
APA6	35	36	BPA6
APA5	37	38	BPA5
APA4	39	40	BPA4
APA3	41	42	BPA3
APA2	43	44	BPA2
APA1	45	46	BPA1
APA0	47	48	BPA0
+5 V	49	50	GND

Figure 3-2. Cable Assembly Connector Pin Assignments for Pins 1 through 50 of the PC-DIO-96/PnP I/O Connector

CPC7	1	2	DPC7
CPC6	3	4	DPC6
CPC5	5	6	DPC5
CPC4	7	8	DPC4
CPC3	9	10	DPC3
CPC2	11	12	DPC2
CPC1	13	14	DPC1
CPC0	15	16	DPC0
CPB7	17	18	DPB7
CPB6	19	20	DPB6
CPB5	21	22	DPB5
CPB4	23	24	DPB4
CPB3	25	26	DPB3
CPB2	27	28	DPB2
CPB1	29	30	DPB1
CPB0	31	32	DPB0
CPA7	33	34	DPA7
CPA6	35	36	DPA6
CPA5	37	38	DPA5
CPA4	39	40	DPA4
CPA3	41	42	DPA3
CPA2	43	44	DPA2
CPA1	45	46	DPA1
CPA0	47	48	DPA0
+5 V	49	50	GND

Figure 3-3. Cable Assembly Connector Pin Assignments for Pins 51 through 100 of the PC-DIO-96/PnP I/O Connector

Digital I/O Signal Connections

Pins 1 through 48 and pins 51 through 98 of the I/O connector are digital I/O signal pins. The following specifications and ratings apply to the digital I/O lines.

Absolute maximum voltage rating -0.5 to +5.5 V with respect to GND

Digital input specifications (referenced to GND):

Input logic high voltage	2.2 V min	5.3 V max
Input logic low voltage	-0.3 V min	0.8 V max
Maximum input current ($0 < V_{in} < 5$ V)	-1.0 µA min	1.0 µA max

Digital output specifications (referenced to GND):

Output logic high voltage at I_{out} = -2.5 mA	3.7 V min	5.0 V max
Output logic low voltage at I_{out} = 2.5 mA	0.0 V min	0.4 V max
Output current at V_{OL} = 0.5 V	2.5 mA min	—
Output current at V_{OH} = 2.7 V	2.5 mA min	—

Figure 3-4 depicts signal connections for three typical digital I/O applications.

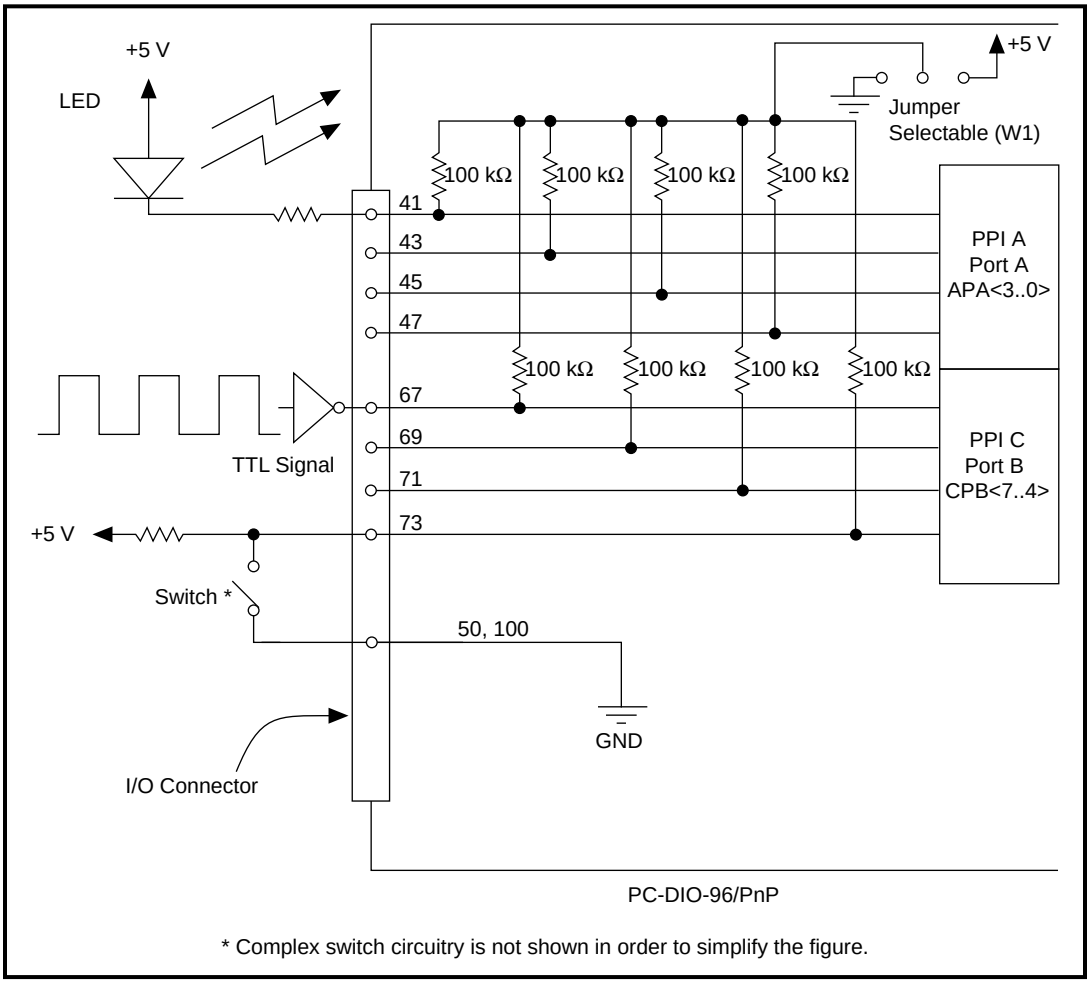


Figure 3-4. Digital I/O Connections

In Figure 3-4, PPI A, port A is configured for digital output, and PPI C, port B is configured for digital input. Digital input applications include receiving TTL signals and sensing external device states such as the state of the switch in Figure 3-4. Digital output applications include sending TTL signals and driving external devices such as the LED shown in Figure 3-4.

Power Connections

Pins 49 and 99 of the I/O connector are connected to the +5 V supply from the PC power supply. These pins are referenced to GND and can be used to power external digital circuitry. This +5 V supply has a 1 A protection fuse in series. This fuse is self-resetting. Simply remove the circuit causing the heavy current load and the fuse will reset itself. For more information on these output pins, see *Output Signals* in Appendix A, *Specifications*.

Power rating	0.5 A per pin at +5 V ±10%

Warning: ***Under no circumstances should these +5 V power pins be connected directly to ground or to any other voltage source on the PC-DIO-96/PnP or any other device. Doing so may damage the PC-DIO-96/PnP and the PC. National Instruments is NOT liable for damage resulting from such a connection.***

Digital I/O Power-up State Selection

You may want to power up the PC-DIO-96/PnP's digital I/O lines in a user-defined state. The PC-DIO-96/PnP facilitates user-configurable pull-up or pull-down. Each DIO channel is connected to a 100 kΩ resistor and can be pulled high or low using jumper W1. You can use W1 to pull all 96 DIO lines high or low. However, if all lines are high, you may want to pull some lines low. To do this properly, you must understand the nature of the drive current on those lines and adhere to TTL logic levels.

High DIO Power-up State

If you select the pulled-high mode, each DIO line will be pulled to VCC (+5 VDC) with a 100 kΩ resistor. If you want to pull a specific line low, connect between that line and ground a pull-down resistor (R_L) whose value will give you a maximum of 0.4 VDC. The DIO lines provide a maximum of 2.5 mA at 3.7 V in the high state. Use the largest possible resistor so that you do not use more current than necessary to perform the pull-down task.

Also, make sure the resistor's value is not so large that leakage current from the DIO line along with the current from the 100 kΩ pull-up resistor drives the voltage at the resistor above a TTL low level of 0.4 VDC.

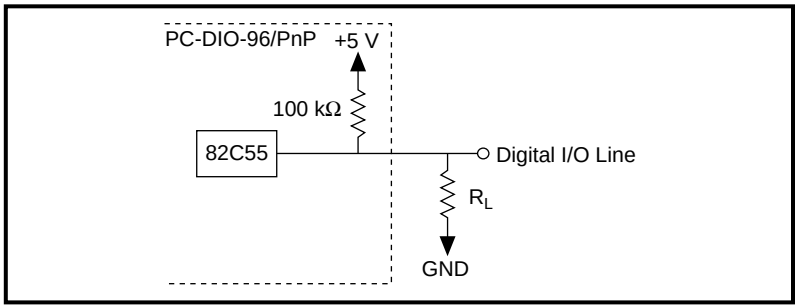


Figure 3-5. DIO Channel Configured for High DIO Power-up State with External Load

Example:
At power up, the board is configured for input and, by default, all DIO lines are high. To pull one channel low, follow these steps:

1. Install a load (R_L). Remember that the smaller the resistance, the greater the current consumption and the lower the voltage (V).
2. Using the following formula, calculate the largest possible load to maintain a logic low level of 0.4 V and supply the maximum driving current (I).

$V = I * R_L \Rightarrow R_L = V / I$, where:

V= 0.4 V	; Voltage across R_L
I = 46 µA + 10 µA	; 4.6 V across the 100 kΩ pull-up resistor and 10 µA from 82C55 leakage current

Therefore:

R_L = 7.1 kΩ	; 0.4 V / 56 µA

This resistor value, 7.1 kΩ, provides a maximum of 0.4 V on the DIO line at power up. You can substitute smaller resistor values, but they will draw more current, leaving less drive current for other circuitry connected to this line. The 7.1 kΩ resistor reduces the amount of a logic high source current by 0.4 mA with a 2.8 V output.

Low DIO Power-up State

If you select pulled-low mode, each DIO line will be pulled to GND (0 VDC) using a 100 kΩ resistor. If you want to pull a specific line high, connect a pull-up resistor that will give you a minimum of 2.8 VDC. The DIO lines are capable of sinking a maximum of 2.5 mA at 0.4 V in the low state. Use the largest possible resistance value so that you do not to use more current than necessary to perform the pull-up task.

Also, make sure the pull-up resistor value is not so large that leakage current from the DIO line along with the current from the 100 kΩ pull-down resistor brings the voltage at the resistor below a TTL high level of 2.8 VDC.

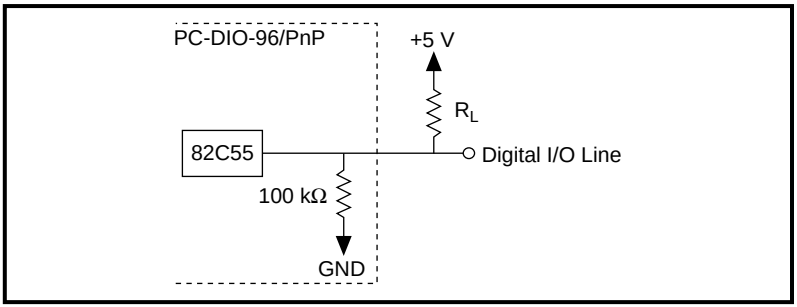


Figure 3-6. DIO Channel Configured for Low DIO Power-up State with External Load

Example:
At power up, the board is configured for input and jumper W1 is set in the low DIO power-up state, which means all DIO lines are pulled low. If you want to pull one channel high, follow these steps:

1. Install a load (R_L). Remember that the smaller the resistance, the greater the current consumption and the lower the voltage (V).
2. Using the following formula, calculate the largest possible load to maintain a logic high level of 2.8 V and supply the maximum sink current (I).

   $V = I * R_L \Rightarrow R_L = V / I$, where:

V = 2.2 V	; voltage across R_L
I = 28 µA + 10 µA	; 2.8 V across the 100 kΩ pull-up resistor and 10 µA from 82C55 leakage current

   Therefore:

RL = 5.7 kΩ	; 2.2 V / 38 µA

This resistor value, 5.7 kΩ, provides a minimum of 2.8 V on the DIO line at power up. You can substitute smaller resistor values but they will draw more current, leaving less sink current for other circuitry connected to this line. The 5.7 kΩ resistor will reduce the amount of a logic low sink current by 0.8 mA with a 0.4 V output.

Timing Specifications

This section lists the timing specifications for handshaking with the PC-DIO-96/PnP. The handshaking lines STB* and IBF synchronize input transfers. The handshaking lines OBF* and ACK* synchronize output transfers.

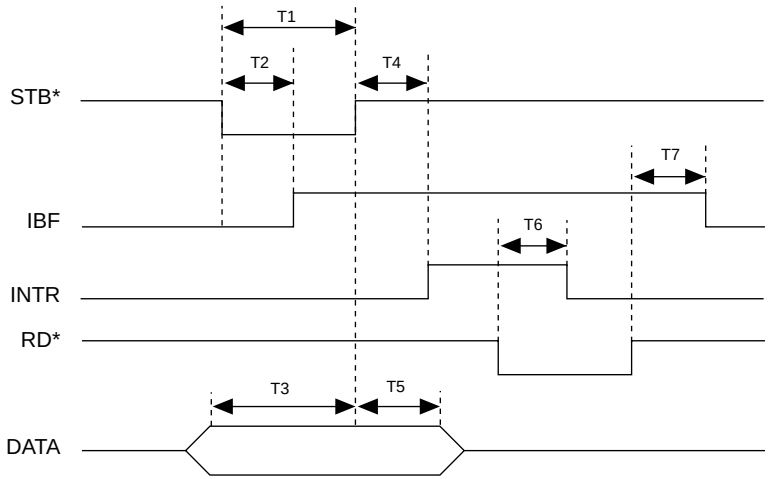
The signals in Table 3-2 are used in the timing diagrams later in this chapter.

Table 3-2. Timing Signal Descriptions

Name	Type	Description
STB*	Input	Strobe Input—A low signal on this handshaking line loads data into the input latch.
IBF	Output	Input Buffer Full—A high signal on this handshaking line indicates that data has been loaded into the input latch. This is an input acknowledge signal.
ACK*	Input	Acknowledge Input—A low signal on this handshaking line indicates that the data written to the port has been accepted. This signal is a response from the external device indicating that it has received the data from the PC-DIO-96/PnP.
OBF*	Output	Output Buffer Full—A low signal on this handshaking line indicates that data has been written to the port.
INTR	Output	Interrupt Request—This signal becomes high when the 82C55A requests service during a data transfer. The appropriate interrupt enable bits must be set to generate this signal.
RD*	Internal	Read Signal—This signal is the read signal generated from the control lines of the computer I/O expansion bus.
WR*	Internal	Write Signal—This signal is the write signal generated from the control lines of the computer I/O expansion bus.
DATA	Bidirectional	Data Lines at the Specified Port—This signal indicates the availability of data on the data lines at a port that is in the output mode. If the port is in the input mode, this signal indicates when the data on the data lines should be valid.

Mode 1 Input Timing

The following figure illustrates the timing specifications for an input transfer in mode 1.

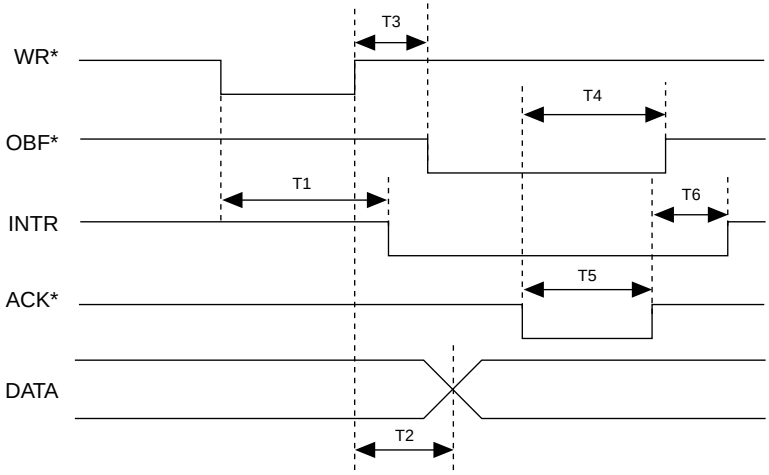


Name	Description	Minimum	Maximum
T1	STB* pulse width	100	–
T2	STB* = 0 to IBF = 1	–	150
T3	Data before STB* = 1	20	–
T4	STB* = 1 to INTR = 1	–	150
T5	Data after STB* = 1	50	–
T6	RD* = 0 to INTR = 0	–	200
T7	RD* = 1 to IBF = 0	–	150

All timing values are in nanoseconds.

Mode 1 Output Timing

The following figure illustrates the timing specifications for an output transfer in mode 1.

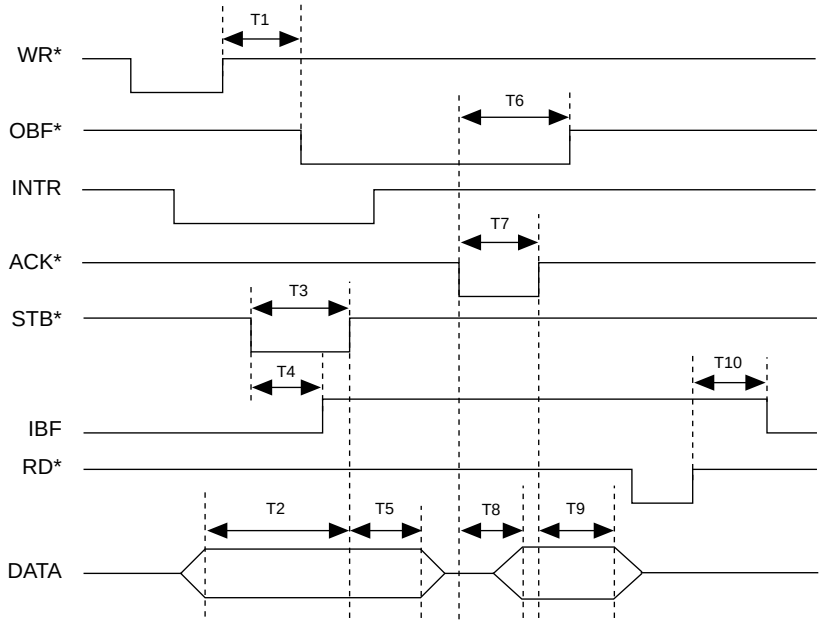


Name	Description	Minimum	Maximum
T1	WR* = 0 to INTR = 0	–	250
T2	WR* = 1 to output	–	200
T3	WR* = 1 to OBF* = 0	–	150
T4	ACK* = 0 to OBF* = 1	–	150
T5	ACK* pulse width	100	–
T6	ACK* = 1 to INTR = 1	–	150

All timing values are in nanoseconds.

Mode 2 Bidirectional Timing

The following figure illustrates the timing specifications for bidirectional transfers in mode 2.



Name	Description	Minimum	Maximum
T1	WR* = 1 to OBF* = 0	–	150
T2	Data before STB* = 1	20	–
T3	STB* pulse width	100	–
T4	STB* = 0 to IBF = 1	–	150
T5	Data after STB* = 1	50	–
T6	ACK* = 0 to OBF = 1	–	150
T7	ACK* pulse width	100	–
T8	ACK* = 0 to output	–	150
T9	ACK* = 1 to output float	20	250
T10	RD* = 1 to IBF = 0	–	150

All timing values are in nanoseconds.

Theory of Operation

Chapter 4

This chapter contains a functional overview of the PC-DIO-96PnP board and explains the operation of each functional unit making up the PC-DIO-96PnP.

The block diagram in Figure 4-1 illustrates the key functional components of the PC-DIO-96PnP board.

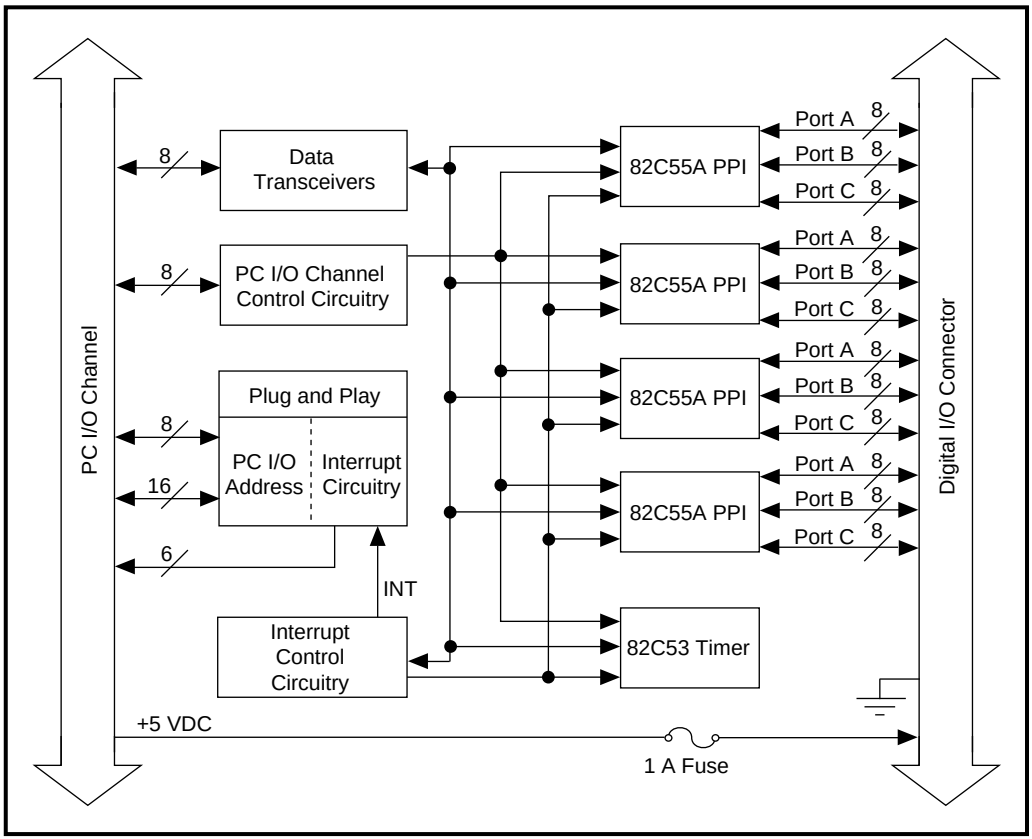


Figure 4-1. PC-DIO-96PnP Block Diagram

The PC I/O channel consists of an address bus, a data bus, interrupt lines, and several control and support signals.

Data Transceivers

The data transceivers control the sending and receiving of data to and from the PC I/O channel.

PC I/O Channel Control Circuitry

The I/O channel control circuitry monitors and transmits the PC I/O channel control and support signals. The control signals identify transfers as read or write, memory or I/O, and 8-bit, 16-bit, or 32-bit transfers. The PC-DIO-96PnP uses only 8-bit transfers.

Plug and Play Circuitry

The board's Plug and Play circuitry automatically arbitrates and assigns system resources. All bus-related configuration, such as setting the board's base address and interrupt level, is performed through software.

Interrupt Control Circuitry

The interrupt channel used by the PC-DIO-96PnP is selected by the Plug and Play circuitry. Two software-controlled registers determine which devices, if any, generate interrupts. Each of the four 82C55A devices has two interrupt lines, PC3 and PC0, connected to the interrupt circuitry.

The 82C53 device has two of its three counter output signals connected to the interrupt circuitry. Any of these 10 signals can interrupt the host computer if the interrupt circuitry is enabled and the corresponding enable bit is set (see Appendix D, *Register-Level Programming*, for more information). Normally, PC3 and/or PC0 of the 82C55A devices are controlled by the handshaking circuitry; however, either of these two lines can be configured for input and used as external interrupts. An interrupt occurs on the low-to-high transition of the signal line. Refer to Appendix D, *Register-Level Programming*, Appendix B, *OKI 82C55A Data Sheet*, or Appendix C, *OKI 82C53 Data Sheet*, for more detailed information.

82C55A Programmable Peripheral Interface

The four 82C55A PPI chips are the heart of the PC-DIO-96PnP. Each of these chips has 24 programmable I/O pins that represent three 8-bit ports: PA, PB, and PC. Each port can be programmed as an input or an output port. The 82C55A has three modes of operation: simple I/O (mode 0), strobed I/O (mode 1), and bidirectional I/O (mode 2). In modes 1 and 2, the three ports are divided into two groups: group A and group B. Each group has eight data bits and four control and status bits from port C (PC). Modes 1 and 2 use handshaking signals from port C to synchronize data transfers. Refer to Appendix D, *Register-Level Programming*, or to Appendix B, *OKI 82C55A Data Sheet*, for more detailed information.

82C53 Programmable Interval Timer

The 82C53 Programmable Interval Timer generates timed interrupt requests to the host computer. The 82C53 has three 16-bit counters, which can each be used in one of six different modes. The PC-DIO-96PnP uses two of the counters to generate interrupt requests; the third counter is not used and is not accessible to the user. Refer to Appendix D, *Register-Level Programming*, or to Appendix C, *OKI 82C53 Data Sheet*, for more detailed information.

Digital I/O Connector

All digital I/O is transmitted through a standard, 100-pin, male connector. Pins 49 and 99 are connected to +5 V through a protection fuse (F1). See Figure 2-1 in Chapter 2, *Installation and Configuration*, for its location. This +5 V supply is often required to operate I/O module mounting racks. Pins 50 and 100 are connected to ground. See the *Optional Equipment* section in Chapter 1, *Introduction*, as well as Chapter 2, *Installation and Configuration*, and Chapter 3, *Signal Connections*, for additional information.

Specifications

Appendix A

This appendix lists the specifications of the PC-DIO-96/PnP. These specifications are typical at 25° C, unless otherwise stated. The operating temperature range is 0° to 70° C.

Digital I/O

Number of channels .....96 I/O

Compatibility .....TTL

Absolute max voltage rating .....-0.5 to +5.5 V with respect to GND

Handshaking .....Requires 1 port

Power-on state .....Configured as inputs, high (jumper selectable)

Data transfers.....Interrupts, programmed I/O

Digital logic levels.....

Level	Min	Max
Input low voltage	-0.3 V	0.8 V
Input high voltage	2.2 V	5.3 V
Input low current (V_{in}= 0.8 V)	—	-1.0 µA
Input high current (V_{in}= 2.4 V)	—	1.0 µA
Output low voltage (I_{out} = 2.5 mA)	0 V	0.4 V
Output high voltage (I_{out}= -2.5 mA)	3.7 V	5.0 V
Input current (0 < V_{in} < 5 V)	-1.0 µA	1.0 µA

Output signals

Pin 49 (at +5 V) ..... 0.5 A max

Pin 99 (at +5 V) ..... 0.5 A max

Note: ***The total combined current output from pins 49 and 99 may be limited by the available current from your computer power supply. To determine the available current, subtract the maximum power consumption of the board from the maximum current per slot. The difference, if less than 1 A, is the maximum combined current available to pins 49 and 99. If the difference is equal to or greater than 1 A, the maximum current available is restricted by the limitations of the connector, as shown previously. If your external circuitry requires 0.5 to 1 A of current, connect pins 49 and 99 in parallel to distribute the current.***

Transfer rates ..... Up to 780 kbytes/s

Note: ***The upper limit on maximum transfer rates is constrained primarily by the software and operating system rather than hardware interface for non-DMA boards such as the PC-DIO-96/PnP. The maximum transfer rate listed here was obtained using inline assembly C code on a 90 MHz Pentium-based computer. Transfer rates will be significantly lower under typical high-level software environments and will vary.***

Power Requirement

+5 VDC (±10%)..... 0.45 A typ, 1 A max

Physical

Dimensions ..... 16.5 by 9.9 cm (6.5 by 3.9 in.)

I/O connector ..... 100-pin male, ribbon-cable

Environment

Operating temperature..... 0° to 70° C

Storage temperature..... -55° to 150° C

Relative humidity..... 5% to 90% noncondensing

Appendix

B

OKI 82C55A Data Sheet

This appendix contains the manufacturer data sheet for the OKI 82C55A* (OKI Semiconductor) CMOS programmable peripheral interface. This interface is used on the PC-DIO-96/PnP board.

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OKI semiconductor

MSM82C55A-2RS/GS/VJS

CMOS PROGRAMMABLE PERIPHERAL INTERFACE

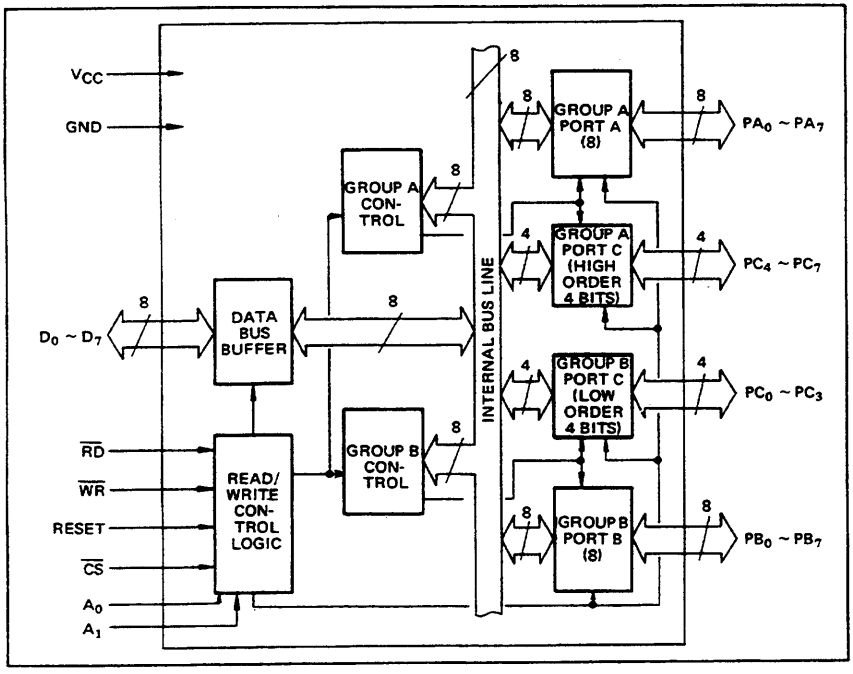
GENERAL DESCRIPTION

The MSM82C55A is a programmable universal I/O interface device which operates as high speed and on low power consumption due to 3 μ silicon gate CMOS technology. It is the best fit as an I/O port in a system which employs the 8-bit parallel processing MSM80C85A CPU. This device has 24-bit I/O pins equivalent to three 8-bit I/O ports and all inputs/outputs are TTL interface compatible.

FEATURES

- High speed and low power consumption due to 3 μ silicon gate CMOS technology
- 3 V to 6 V single power supply
- Full static operation
- Programmable 24-bit I/O ports
- Bidirectional bus operation (Port A)
- Bit set/reset function (Port C)
- TTL compatible
- Compatible with 8255A-5
- 40 pin Plastic DIP (DIP40-P-600)
- 44 pin PLCC (QFJ44-P-S650)
- 44 pin-V Plastic QFP (QFP44-P-910-VK)
- 44 pin-VI Plastic QFP (QFP44-P-910-VIK)

CIRCUIT CONFIGURATION



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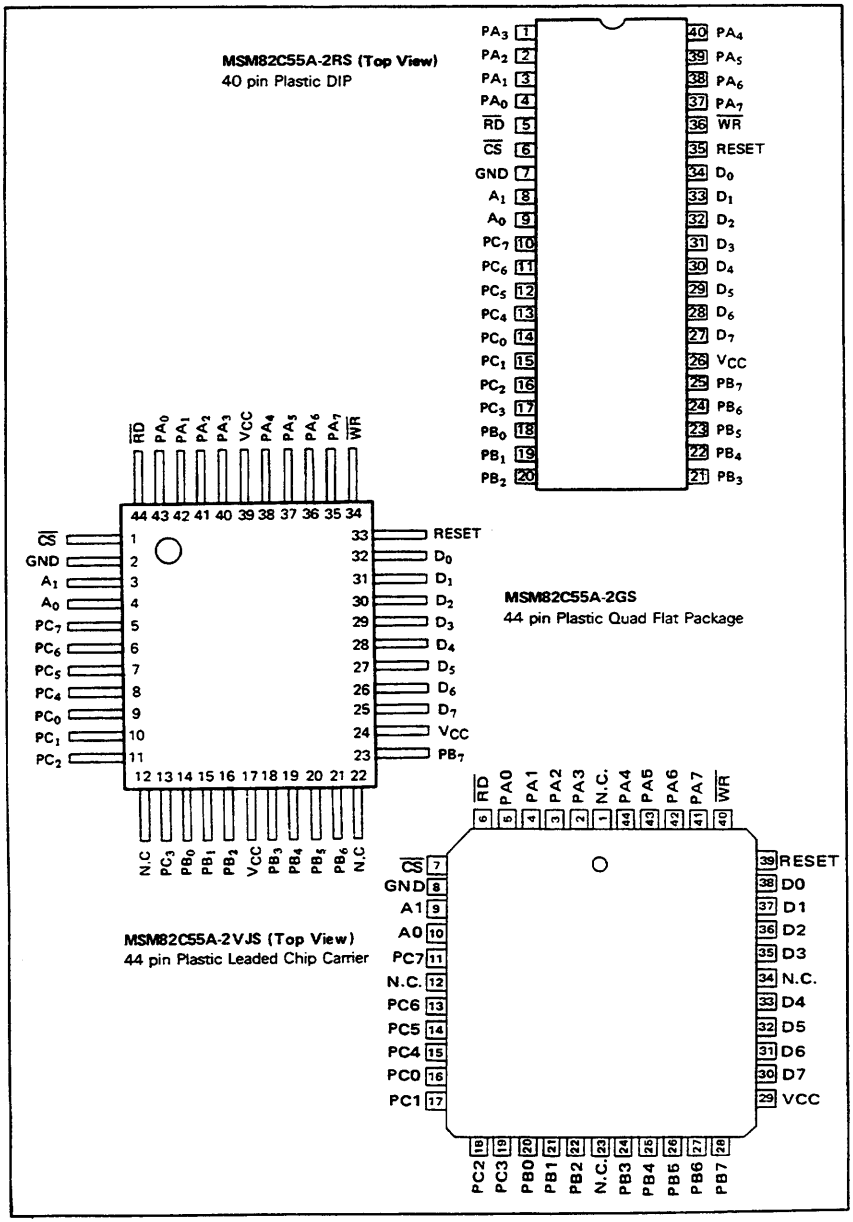
PIN CONFIGURATION



■ I/O-MSM82C55A-2RS/GS/VJS ■

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits			Unit
			MSM82C55A-2RS	MSM82C55A-2GS	MSM82C55A-2VJS	
Ssupply Voltage	V_{CC}	Ta = 25°C with respect to GND	−0.5 to +7			V
Input Voltage	V_{IN}		−0.5 to V_{CC} + 0.5			V
Output Voltage	V_{OUT}		−0.5 to V_{CC} + 0.5			V
Storage Temperature	T_{stg}	−	−55 to +150			°C
Power Dissipation	P_D	Ta = 25°C	1.0	0.7	1.0	W

OPERATING RANGE

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	3 to 6	V
Operating Temperature	T_{OP}	−40 to 85	°C

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Input Voltage	V_{IL}	−0.3		+0.8	V
"H" Input Voltage	V_{IH}	2.2		V_{CC} +0.3	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		MSM82C55A-2			Unit
				Min.	Typ.	Max.	
"L" Output Voltage	V_{OL}	I_{OL} = 2.5 mA	V_{CC} = 4.5V to 5.5V Ta = −40°C to +85°C (C_L = 0pF)			0.4	V
"H" Output Voltage	V_{OH}	I_{OH} = −40 μA		4.2			V
		I_{OH} = −2.5 mA		3.7			V
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$		−1		1	μA
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$		−10		10	μA
Supply Current (standby)	I_{CCS}	$\overline{CS} \geq V_{CC}$ −0.2V $V_{IH} \geq V_{CC}$ −0.2V $V_{IL} \leq$ 0.2V			0.1	10	μA
Average Supply Current (active)	I_{CC}	I/O wire cycle 82C55A-2 ... 8MHzCPU timing				8	mA

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■ I/O·MSM82C55A-2RS/GS/VJS ■

AC CHARACTERISTICS

(V_{CC} = 4.5 to 5.5V, Ta = -40 to +80°C)

Parameter	Symbol	MSM82C55A-2		Unit	Remarks
		Min.	Max.		
Setup Time of address to the falling edge of $\overline{RD}$	t_{AR}	20		ns	
Hold Time of address to the rising edge of $\overline{RD}$	t_{RA}	0		ns	
$\overline{RD}$ Pulse Width	t_{RR}	100		ns	
Delay Time from the falling edge of $\overline{RD}$ to the output of defined data	t_{RD}		120	ns	
Delay Time from the rising edge of $\overline{RD}$ to the floating of data bus	t_{DF}	10	75	ns	
Time from the rising edge of $\overline{RD}$ or $\overline{WR}$ to the next falling edge of $\overline{RD}$ or $\overline{WR}$	t_{RV}	200		ns	
Setup Time of address before the falling edge of $\overline{WR}$	t_{AW}	0		ns	
Hold Time of address after the rising edge or $\overline{WR}$	t_{WA}	20		ns	
$\overline{WR}$ Pulse Width	t_{WW}	150		ns	
Setup Time of bus data before the rising edge of $\overline{WR}$	t_{DW}	50		ns	
Holt Time of bus data after the rising edge of $\overline{WR}$	t_{WD}	30		ns	
Delay Time from the rising edge of $\overline{WR}$ to the output of defined data	t_{WB}		200	ns	
Setup Time of port data before the falling edge of $\overline{RD}$	t_{IR}	20		ns	
Hold Time of port data after the rising edge of $\overline{RD}$	t_{HR}	10		ns	
$\overline{ACK}$ Pulse Width	t_{AK}	100		ns	
$\overline{STB}$ Pulse Width	t_{ST}	100		ns	Load 150pF
Setup Time of port data before the rising edge of $\overline{STB}$	t_{PS}	20		ns	
Hold Time of port data after the rising edge of $\overline{STB}$	t_{PH}	50		ns	
Delay Time from the falling edge of $\overline{ACK}$ to the output of defined data	t_{AD}		150	ns	
Delay Time from the rising edge of $\overline{ACK}$ to the floating of port (Port A in mode 2)	t_{KD}	20	250	ns	
Delay Time from the rising edge of WR to the falling edge of $\overline{OBF}$	t_{WOB}		150	ns	
Delay Time from the falling edge of ACK to the rising edge of $\overline{OBF}$	t_{AOB}		150	ns	
Delay Time from the falling edge of STB to the rising edge of IBF	t_{SIB}		150	ns	
Delay Time from the rising edge of $\overline{RD}$ to the falling edge of IBF	t_{RIB}		150	ns	
Delay Time from the falling edge of $\overline{RD}$ to the falling edge of INTR	t_{RIT}		200	ns	
Delay Time from the rising edge of $\overline{STB}$ to the rising edge of INTR	t_{SIT}		150	ns	
Delay Time from the rising edge of $\overline{ACK}$ to the rising edge of INTR	t_{AIT}		150	ns	
Delay Time from the falling edge of $\overline{WR}$ to the falling edge of INTR	t_{WIT}		250	ns	

Note: Timing is measured at V_L = 0.8 V and V_H = 2.2 V for both input and outputs.

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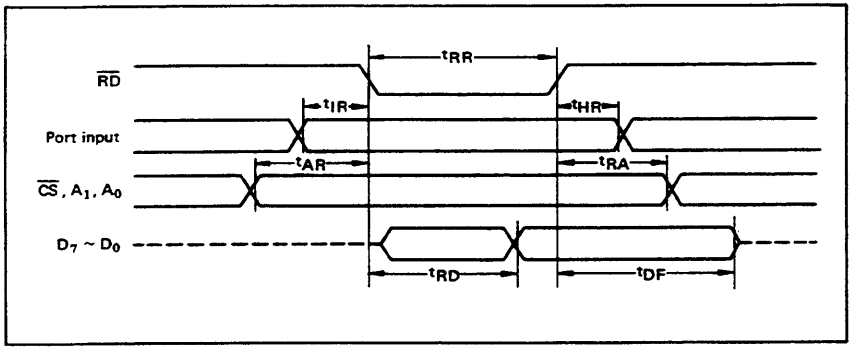
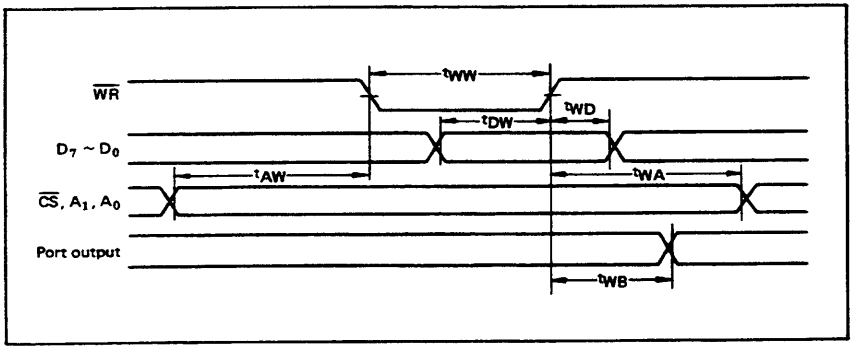
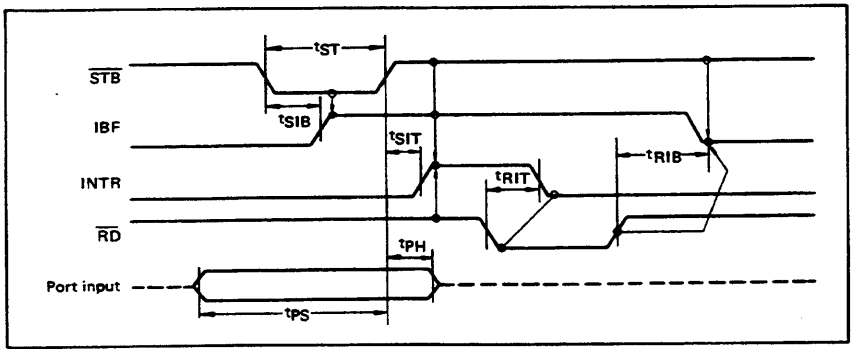
Basic Input Operation (Mode 0)



Basic Output Operation (Mode 0)



Strobe Input Operation (Mode 1)



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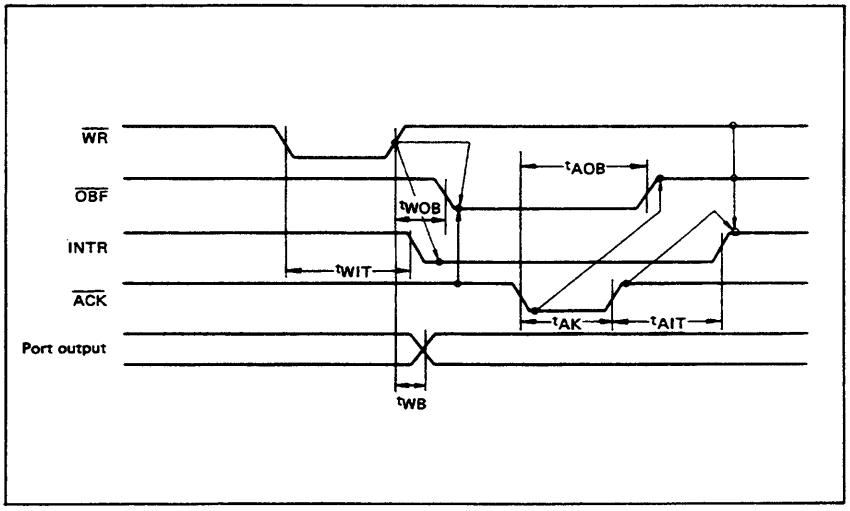
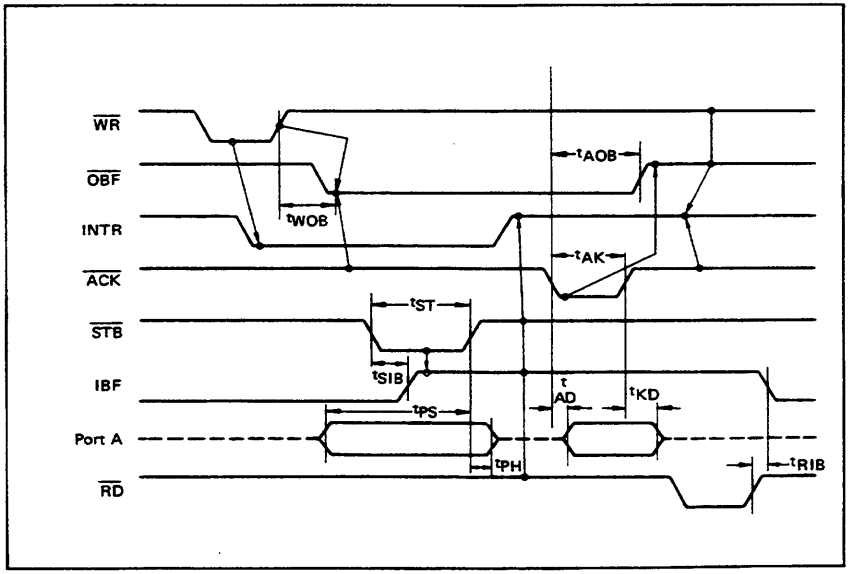
Strobe Output Operation (Mode 1)



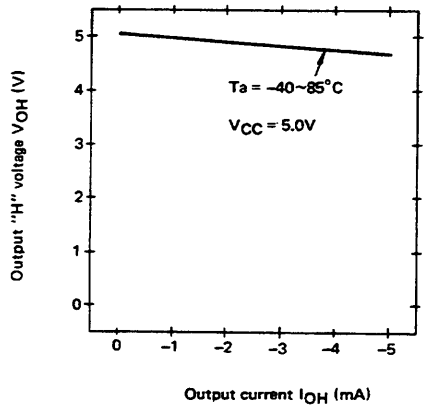
Bidirectional Bus Operation (Mode 2)



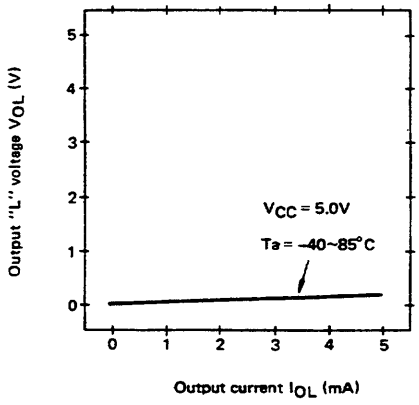
■ I/O·MSM82C55A-2RS/GS/VJS ■

OUTPUT CHARACTERISTICS (REFERENCE VALUE)

1 Output "H" Voltage (V_{OH}) vs. Output Current (I_{OH})



2 Output "L" Voltage (V_{OL}) vs. Output Current (I_{OL})



Note: The direction of flowing into the device is taken as positive for the output current.

■ I/O·MSM82C55A-2RS/GS/VJS ■

FUNCTIONAL DESCRIPTION OF PIN

Pin No.	Item	Input/Output	Function
D7 ~ D0	Bidirectional data bus	Input and output	These are three-state 8-bit bidirectional buses used to write and read data upon receipt of the $\overline{WR}$ and $\overline{RD}$ signals from CPU and also used when control words and bit set/reset data are transferred from CPU to MSM82C55A.
RESET	Reset input	Input	This signal is used to reset the control register and all internal registers when it is in high level. At this time, ports are all made into the input mode (high impedance status). all port latches are cleared to 0. and all ports groups are set to mode 0.
$\overline{CS}$	Chip select input	Input	When the $\overline{CS}$ is in low level, data transmission is enabled with CPU. When it is in high level, the data bus is made into the high impedance status where no write nor read operation is performed. Internal registers hold their previous status, however.
$\overline{RD}$	Read input	Input	When RD is in low level, data is transferred from MSM82C55A to CPU.
$\overline{WR}$	Write input	Input	When WR is in low level, data or control words are transferred from CPU to MSM82C55A.
A0, A1	Port select input (address)	Input	By combination of A0 and A1, either one is selected from among port A, port B, port C, and control register. These pins are usually connected to low order 2 bits of the address bus.
PA7 ~ PA0	Port A	Input and output	These are universal 8-bit I/O ports. The direction of inputs/outputs can be determined by writing a control word. Especially, port A can be used as a bidirectional port when it is set to mode 2.
PB7 ~ PB0	Port B	Input and output	These are universal 8-bit I/O ports. The direction of inputs/outputs can be determined by writing a control word.
PC7 ~ PC0	Port C	Input and output	These are universal 8-bit I/O ports. The direction of inputs/outputs can be determined by writing a control word as 2 ports with 4 bits each. When port A or port B is used in mode 1 or mode 2 (port A only), they become control pins. Especially when port C is used as an output port, each bit can be set/reset independently.
Vcc			+5 V power supply.
GND			GND

BASIC FUNCTIONAL DESCRIPTION

Group A and Group B

When setting a mode to a port having 24 bits, set it by dividing it into two groups of 12 bits each.

Group A: Port A (8 bits) and high order 4 bits of port C (PC7 ~ PC4)

Group B: Port B (8 bits) and low order 4 bits of port C (PC3 ~ PC0)

Mode 0, 1, 2

There are 3 types of modes to be set by grouping as follows:

Mode 0: Basic input operation/output operation (Available for both groups A and B)

Mode 1: Strobe input operation/output operation (Available for both groups A and B)

Mode 2: Bidirectional bus operation (Available for group A only)

When used in mode 1 or mode 2, however, port C has bits to be defined as ports for control signal for operation ports (port A for group A and port B for group B) of their respective groups.

Port A, B, C

The internal structure of 3 ports is as follows:

Port A: One 8-bit data output latch/buffer and one 8-bit data input latch

Port B: One 8-bit data input/output latch/buffer and one 8-bit data input buffer

Port C: One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input)

Single bit set/reset function for port C

When port C is defined as an output port, it is possible to set (to turn to high level) or reset (to turn to low level) any one of 8 bits individually without affecting other bits.

■ I/O·MSM82C55A-2RS/GS/VJS ■

OPERATIONAL DESCRIPTION

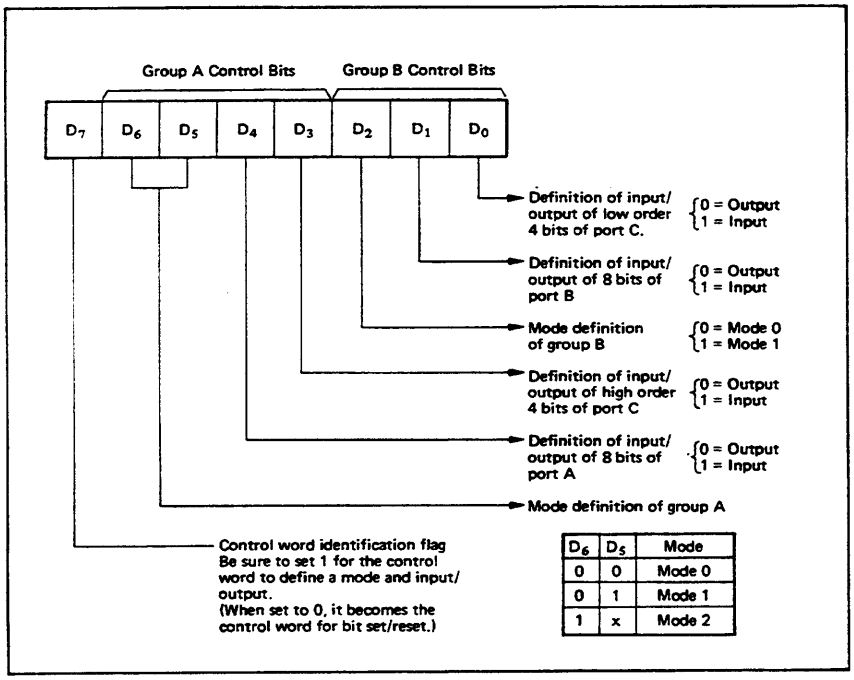
Control Logic

Operations by addresses and control signals, e.g., read and write, etc. are as shown in the table below:

Operation	A1	A0	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Operation
Input	0	0	0	1	0	Port A → Data Bus
	0	1	0	1	0	Port B → Data Bus
	1	0	0	1	0	Port C → Data Bus
Output	0	0	0	0	1	Data Bus → Port A
	0	1	0	0	1	Data Bus → Port B
	1	0	0	0	1	Data Bus → Port C
Control	1	1	0	0	1	Data Bus → Control Register
Others	1	1	0	1	0	Illegal Condition
	x	x	1	x	x	Data bus is in the high impedance status.

Setting of Control Word

The control register is composed of 7-bit latch circuit and 1-bit flag as shown below.



D_6	D_5	Mode
0	0	Mode 0
0	1	Mode 1
1	x	Mode 2

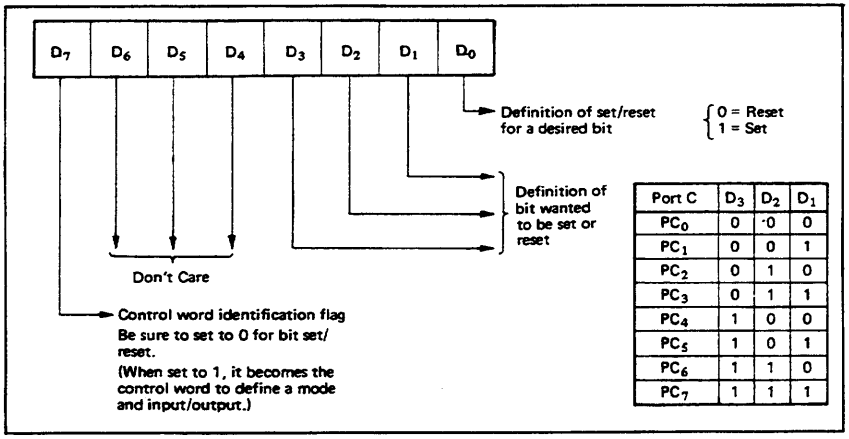
Precaution for mode selection

The output registers for ports A and C are cleared to ϕ each time data is written in the command register and the mode is changed, but the port B state is undefined.

Bit Set/Reset Function

When port C is defined as output port, it is possible to set (set output to 1) or reset (set output to 0) any one of 8 bits without affecting other bits as shown next page.

■ I/O·MSM82C55A-2RS/GS/VJS ■



Port C	D_3	D_2	D_1
PC_0	0	0	0
PC_1	0	0	1
PC_2	0	1	0
PC_3	0	1	1
PC_4	1	0	0
PC_5	1	0	1
PC_6	1	1	0
PC_7	1	1	1

Interrupt Control Function

When the MSM82C55A is used in mode 1 or mode 2, the interrupt signal for the CPU is provided. The interrupt request signal is output from port C. When the internal flip-flop INTE is set beforehand at this time, the desired interrupt request signal is output. When it is reset beforehand, however, the interrupt request signal is not output. The set/reset of the internal flip-flop is made by the bit set/reset operation for port C virtually.

Bit set → INTE is set → Interrupt allowed
Bit reset → INTE is reset → Interrupt inhibited

Operational Description by Mode

1. Mode 0 (Basic input/output operation)

Mode 0 makes the MSM82C55A operate as a basic input port or output port. No control signals such as interrupt request, etc. are required in this mode. All 24 bits can be used as two-8-bit ports and two 4-bit ports. Sixteen combinations are then possible for inputs/outputs. The inputs are not latched, but the outputs are.

Type	Control Word								Group A		Group B	
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Port A	High Order 4 Bits of Port C	Port B	Low Order 4 Bits of Port C
1	1	0	0	0	0	0	0	0	Output	Output	Output	Output
2	1	0	0	0	0	0	0	1	Output	Output	Output	Input
3	1	0	0	0	0	0	1	0	Output	Output	Input	Output
4	1	0	0	0	0	0	1	1	Output	Output	Input	Input
5	1	0	0	0	1	0	0	0	Output	Input	Output	Output
6	1	0	0	0	1	0	0	1	Output	Input	Output	Input
7	1	0	0	0	1	0	1	0	Output	Input	Input	Output
8	1	0	0	0	1	0	1	1	Output	Input	Input	Input
9	1	0	0	1	0	0	0	0	Input	Output	Output	Output
10	1	0	0	1	0	0	0	1	Input	Output	Output	Input
11	1	0	0	1	0	0	1	0	Input	Output	Input	Output
12	1	0	0	1	0	0	1	1	Input	Output	Input	Input
13	1	0	0	1	1	0	0	0	Input	Input	Output	Output
14	1	0	0	1	1	0	0	1	Input	Input	Output	Input
15	1	0	0	1	1	0	1	0	Input	Input	Input	Output
16	1	0	0	1	1	0	1	1	Input	Input	Input	Input

Note: When used in mode 0 for both groups A and B

■ I/O·MSM82C55A-2RS/GS/VJS ■

2. Mode 1 (Strobe input/output operation)

In mode 1, the strobe, interrupt and other control signals are used when input/output operations are made from a specified port. This mode is available for both groups A and B. In group A at this time, port A is used as the data line and port C as the control signal.

Following is a descrption of the input operation in mode 1.

$\overline{STB}$ (Strobe input)

- When this signal is low level, the data output from terminal to port is fetched into the internal latch of the port. This can be made independent from the CPU, and the data is not output to the data bus until the RD signal arrives from the CPU.

IBF (Input buffer full flag output)

- This is the response signal for the $\overline{STB}$. This signal when turned to high level indicates that data is fetched into the input latch. This signal turns to high level at the falling edge of $\overline{STB}$ and to low level at the rising edge of $\overline{RD}$.

INTR (Interrupt request output)

- This is the interrupt request signal for the CPU of the data fetched into the input latch. It is indicated by high level only when the internal INTE flip-flop is set. This signal turns to high level at the rising edge of the $\overline{STB}$ (IBF = 1 at this time) and low level at the falling edge of the $\overline{RD}$ when the INTE is set.

$INTE_A$ of group A is set when the bit for PC_4 is set, while $INTE_B$ of group B is set when the bit for PC_2 is set.

Following is a description of the output operation of mode 1.

$\overline{OBF}$ (Output buffer full flag output)

- This signal when turned to low level indicates that data is written to the specified port upon receipt of the $\overline{WR}$ signal from the CPU. This signal turns to low level at the rising edge of the WR and high level at the falling edge of the ACK.

$\overline{ACK}$ (Acknowledge input)

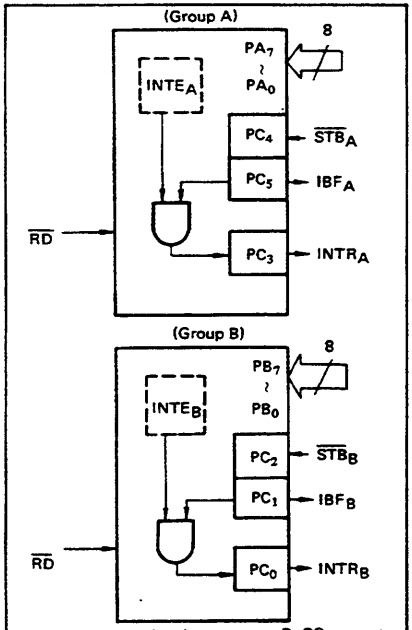
- This signal when turned to low level indicates that the terminal has received data.

INTR (Interrupt request output)

- This is the signal used to interrupt the CPU when a terminal receives data from the CPU via the MSM82C55A-5. It indicates the occurrence of the interrupt in high level only when the internal INTE flip-flop is set. This signal turns to high level at the rising edge of the $\overline{ACK}$ (OBF = 1 at this time) and low level at the falling edge of $\overline{WR}$ when the $INTE_B$ is set.

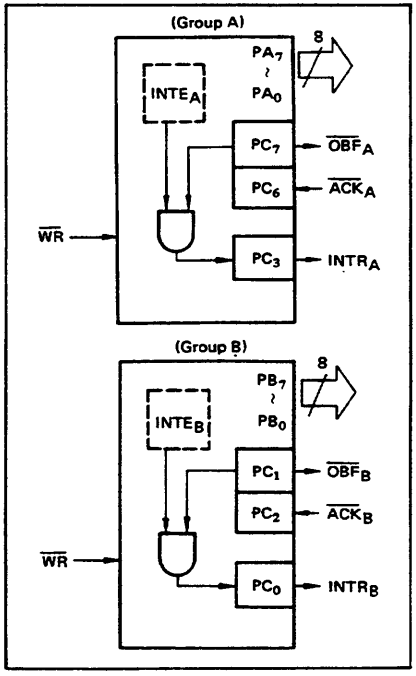
$INTE_A$ of group A is set when the bit for PC_6 is set, while $INTE_B$ of group B is set when the bit for PC_2 is set.

Mode 1 Input



Note: Although belonging to group B, PC_3 operates as the control signal of group A functionally.

Mode 1 output



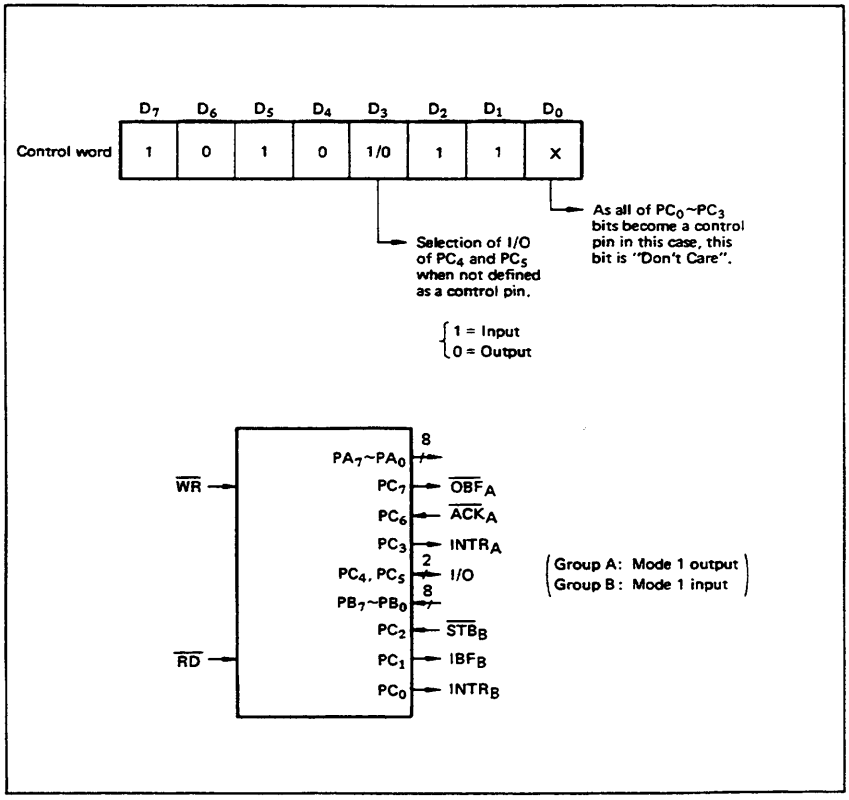
■ I/O·MSM82C55A-2RS/GS/VJS ■

Port C Function Allocation in Mode 1

Combination of Input/Output / Port C	Group A: Input Group B: Input	Group A: Input Group B: Output	Group A: Output Group B: Input	Group A: Output Group B: Output
PC_0	$INTR_B$	$INTR_B$	$INTR_B$	$INTR_B$
PC_1	IBF_B	$\overline{OBF}_B$	IBF_B	$\overline{OBF}_B$
PC_2	$\overline{STB}_B$	$\overline{ACK}_B$	$\overline{STB}_B$	$\overline{ACK}_B$
PC_3	$INTR_A$	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	$\overline{STB}_A$	$\overline{STB}_A$	I/O	I/O
PC_5	IBF_A	IBF_A	I/O	I/O
PC_6	I/O	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC_7	I/O	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

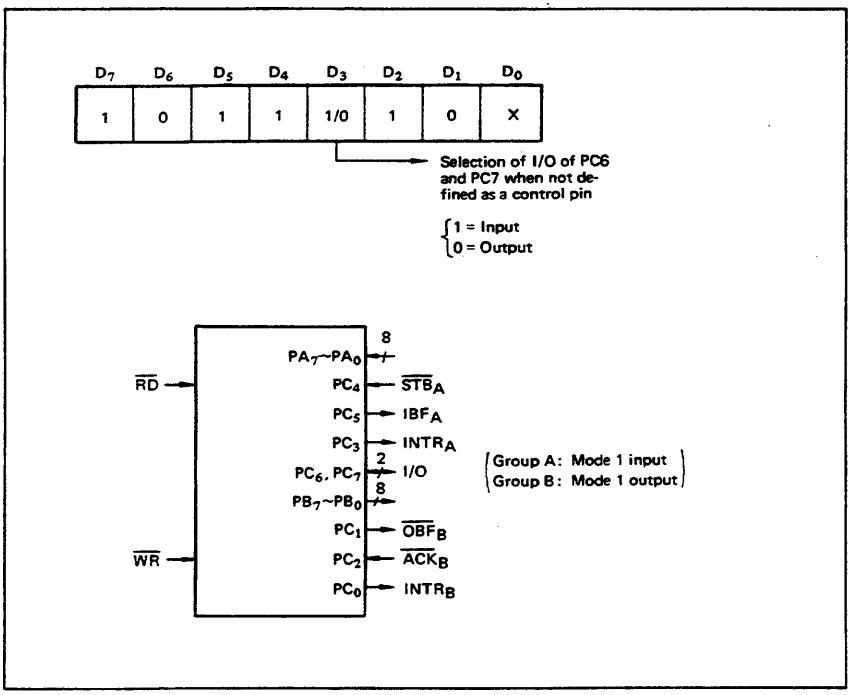
Note: I/O is a bit not used as the control signal, but it is available as a port of mode 0.

Examples of the relation between the control words and pins when used in mode 1 is shown below:
(a) When group A is mode 1 output and group B is mode 1 input.



■ I/O·MSM82C55A-2RS/GS/VJS ■

(b) When group A is mode 1 input and group B is mode 1 output.



3. Mode 2 (Strobe bidirectional bus I/O operation)

In mode 2, it is possible to transfer data in 2 directions through a single 8-bit port. This operation is akin to a combination between input and output operations. Port C waits for the control signal in this case, too. Mode 2 is available only for group A, however.

Next, a description is made on mode 2.

$\overline{OBF}$ (Output buffer full flag output)

- This signal when turned to low level indicates that data has been written to the internal output latch upon receipt of the $\overline{WR}$ signal from the CPU. At this time, port A is still in the high impedance status and the data is not yet output to the outside. This signal turns to low level at the rising edge of the $\overline{WR}$ and high level at the falling edge of the $\overline{ACK}$.

$\overline{ACK}$ (Acknowledge input)

- When a low level signal is input to this pin, the high impedance status of port A is cleared, the buffer is enabled, and the data written to the internal output latch is output to port A. When the input returns to high level, port A is made into the high impedance status.

$\overline{STB}$ (Strobe input)

- When this signal turns to low level, the data output to the port from the pin is fetched into the internal input latch. The data is output to the data bus upon receipt of the RD signal from the CPU, but it remains in the high impedance status until then.

IBF (Input buffer full flag output)

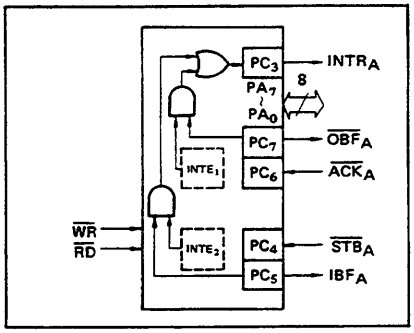
- This signal when turned to high level indicates that data from the pin has been fetched into the input latch. This signal turns to high level at the falling edge of the $\overline{STB}$ and low level at the rising edge of the $\overline{RD}$.

INTR (Interrupt request output)

- This signal is used to interrupt the CPU and its operation in the same as in mode 1. There are two INTE flip-flops internally available for input and output to select either interrupt of input or output operation. The INTE1 is used to control the interrupt request for output operation and it can be reset by the bit set for PC6. INTE2 is used to control the interrupt request for the input operation and it can be set by the bit set for PC4.

I/O·MSM82C55A-2RS/GS/VJS

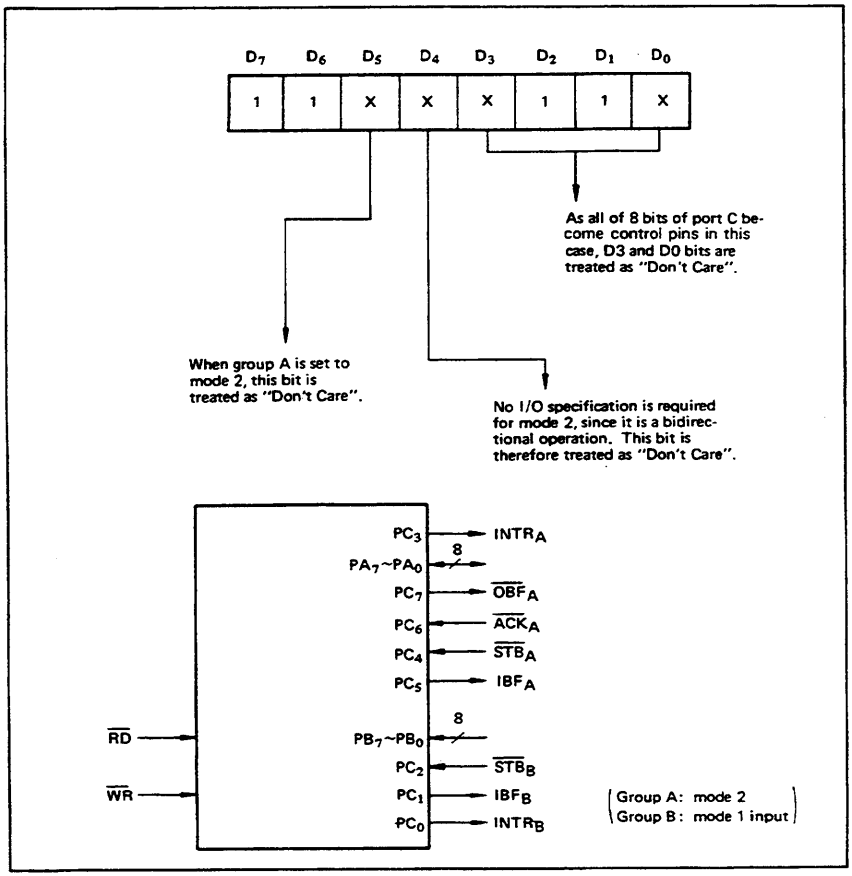
Mode 2 I/O Operation



Port C Function Allocation in Mode 2

Port C	Function
PC_0	Confirmed to the group B mode
PC_1	
PC_2	
PC_3	$INTR_A$
PC_4	$\overline{STB}_A$
PC_5	IBF_A
PC_6	$\overline{ACK}_A$
PC_7	$\overline{OBF}_A$

Following is an example of the relation between the control word and the pin when used in mode 2. When input in mode 2 for group A and in mode 1 for group B.



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4. When Group A is Different in Mode from Group B
Group A and group B can be used by setting them in different modes each other at the same time. When either group is set to mode1 or mode 2, it is possible to set the one not defined as a control pin in port C to both input and output as a port which operates in mode 0 at the 3rd and 0th bits of the control word.

(Mode combinations that define no control bit at port C)

	Group A	Group B	Port C							
			PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0
1	Mode 1 input	Mode 0	I/O	I/O	IBF_A	$\overline{STB}_A$	$INTR_A$	I/O	I/O	I/O
2	Mode 0 output	Mode 0	$\overline{OBF}_A$	$\overline{ACK}_A$	I/O	I/O	$INTR_A$	I/O	I/O	I/O
3	Mode 0	Mode 1 input	I/O	I/O	I/O	I/O	I/O	$\overline{STB}_B$	IBF_B	$INTR_B$
4	Mode 0	Mode 1 output	I/O	I/O	I/O	I/O	I/O	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$
5	Mode 1 input	Mode 1 input	I/O	I/O	IBF_A	$\overline{STB}_A$	$INTR_A$	$\overline{STB}_B$	IBF_B	$INTR_B$
6	Mode 1 input	Mode 1 output	I/O	I/O	IBF_A	$\overline{STB}_A$	$INTR_A$	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$
7	Mode 1 output	Mode 1 input	$\overline{OBF}_A$	$\overline{ACK}_A$	I/O	I/O	$INTR_A$	$\overline{STB}_B$	IBF_B	$INTR_B$
8	Mode 1 output	Mode 1 output	$\overline{OBF}_A$	$\overline{ACK}_A$	I/O	I/O	$INTR_A$	$\overline{ACK}_B$	$\overline{OBF}_B$	$INTR_B$
9	Mode 2	Mode 0	$\overline{OBF}_A$	$\overline{ACK}_A$	IBF_A	$\overline{STB}_A$	$INTR_A$	I/O	I/O	I/O
			Controlled at the 3rd bit (D3) of the control word				Controlled at the 0th bit (D0) of the control word			

When the I/O bit is set to input in this case, it is possible to access data by the normal port C read operation.
When set to output, PC7 ~ PC4 bits can be accessed by the bit set/reset function only. Meanwhile, 3 bits from PC2 to PC0 can be accessed by normal write operation.

The bit set/reset function can be used for all of PC3 ~ PC0 bits. Note that the status of port C varies according to the combination of modes like this.

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5. Port C Status Read

When port C is used for the control signal, that is, in either mode 1 or mode 2, each control signal and bus status signal can be read out by reading the content of port C.

The status read out is as follows:

	Group A	Group B	Status read on the data bus							
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	Mode 1 input	Mode 0	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	I/O	I/O	I/O
2	Mode 1 output	Mode 0	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	I/O	I/O	I/O
3	Mode 0	Mode 1 input	I/O	I/O	I/O	I/O	I/O	$INTE_B$	IBF_B	$INTR_B$
4	Mode 0	Mode 1 output	I/O	I/O	I/O	I/O	I/O	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
5	Mode 1 input	Mode 1 input	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
6	Mode 1 input	Mode 1 output	I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
7	Mode 1 output	Mode 1 input	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
8	Mode 1 output	Mode 1 output	$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
9	Mode 2	Mode 0	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	I/O	I/O	I/O
10	Mode 2	Mode 1 input	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
11	Mode 2	Mode 1 output	$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$

6. Reset of MSM82C55A

Be sure to keep the RESET signal at power ON in the high level at least for 50 μs. Subsequently, it becomes the input mode at a high level pulse above 500 ns.

Note: Comparison of MSM82C55A-5 and MSM82C55A-2

MSM82C55A-5

After a write command is executed to the command register, the internal latch is cleared in PORTA PORTC. For instance, 00H is output at the beginning of a write command when the output port is assigned. However, if PORTB is not cleared at this time, PORTB is unstable. In other words, PORTB only outputs ineffective data (unstable value according to the device) during the period from after a write command is executed till the first data is written to PORTB.

MSM82C55A-2

After a write command is executed to the command register, the internal latch is cleared in All Ports(PORTA,PORTB,PORTC). 00H is ontput at the beginning of a write command when the output port is assigned.

Appendix

C

OKI 82C53 Data Sheet

This appendix contains the manufacturer data sheet for the OKI 82C53* integrated circuit (OKI Semiconductor). This circuit is used on the PC-DIO-96/PnP board.

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OKI semiconductor

MSM82C53-2RS/GS/JS

CMOS PROGRAMMABLE INTERVAL TIMER

GENERAL DESCRIPTION

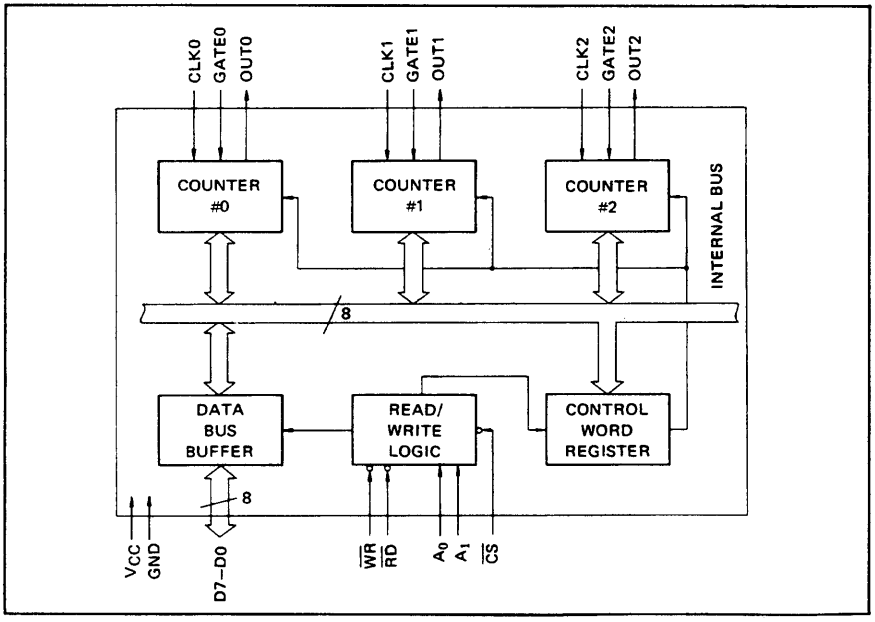
The MSM82C53-2RS/GS/JS is programmable universal timers designed for use in microcomputer systems. Based on silicon gate CMOS technology, it requires a standby current of only 100μA (max.) when the chip is in the nonselected state. During timer operation, power consumption is still very low with only 8 mA (max.) at 8 MHz of current required.

The device consists of three independent counters, and can count up to a maximum of 8 MHz (MSM82C53-2) The timer features six different counter modes, and binary count/BCD count functions. Count values can be set in byte or word units, and all functions are freely programmable.

FEATURES

- Maximum operating frequency of 8 MHz (MSM82C53-2)
- High speed and low power consumption achieved through silicon gate CMOS technology
- Completely static operation
- Three independent 16-bit down-counters
- 3V to 6V single power supply
- Six counter modes abailable for each counter
- Binary and decimal counting possible
- 24 pin Plastic DIP (DIP24-P-600): MSM82C53-2RS
- 28 pin Plastic QFJ (QFJ28-P-S450): MSM82C53-2JS
- 32 pin-V Plastic SOP (SSOP32-P-430-VK): MSM82C53-2GS-VK

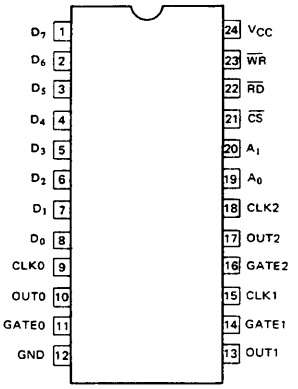
FUNCTIONAL BLOCK DIAGRAM



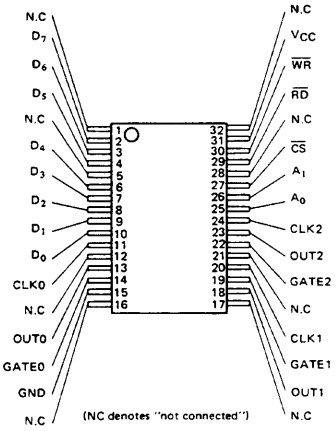
■ I/O-MSM82C53-2RS/GS/JS ■

PIN CONFIGURATION (Top View)

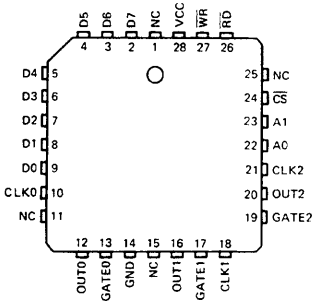
24 pin Plastic DIP



32 pin Plastic SOP



28 pin Plastic QFJ



■ I/O-MSM82C53-2RS/GS/JS ■

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Limits			Unit
			MSM82C53-2RS	MSM82C53-2GS	MSM82C53-2JS	
Ssupply Voltage	V_{CC}	Respect to GND	−0.5 to +7			V
Input Voltage	V_{IN}		−0.5 to V_{cc} + 0.5			V
Output Voltage	V_{OUT}		−0.5 to V_{cc} + 0.5			V
Storage Temperature	T_{stg}		−55 to +150			°C
Power Dissipation	P_D	Ta = 25°C	0.9	0.7	0.9	W

OPERATING RANGES

Parameter	Symbol	Limits	Conditions	Unit
Supply Voltage	V_{CC}	3 to 6	V_{IL} = 0.2V, V_{IH} = V_{CC} − 0.2V, operating frequency 2.6 MHz	V
Operating Temperature	T_{OP}	−40 to +85		°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5	5.5	V
Operating Temperature	T_{OP}	−40	+25	+85	°C
"L" Input Voltage	V_{IL}	−0.3		+0.8	V
"H" Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V

DC CHARACTERISTICS

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
"L" Output Voltage	V_{OL}	I_{OL} = 4mA	V_{CC}=4.5V to 5.5V Ta=−40°C to +85°C			0.45	V
"H" Output Voltage	V_{OH}	I_{OH} = −1mA		3.7			V
Input Leak Current	I_{LI}	$0 \leq V_{IN} \leq V_{CC}$		−10		10	μA
Output Leak Current	I_{LO}	$0 \leq V_{OUT} \leq V_{CC}$		−10		10	μA
Standby Supply Current	I_{CCS}	$\overline{CS} \geq V_{CC}$ −0.2V $V_{IH} \geq V_{CC}$ − 0.2V $V_{IL} \leq 0.2V$				100	μA
Operating Supply Current	I_{CC}	t_{CLK} = 125 ns C_L = 0pF				8	mA

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■ I/O-MSM82C53-2RS/GS/JS ■

AC CHARACTERISTICS

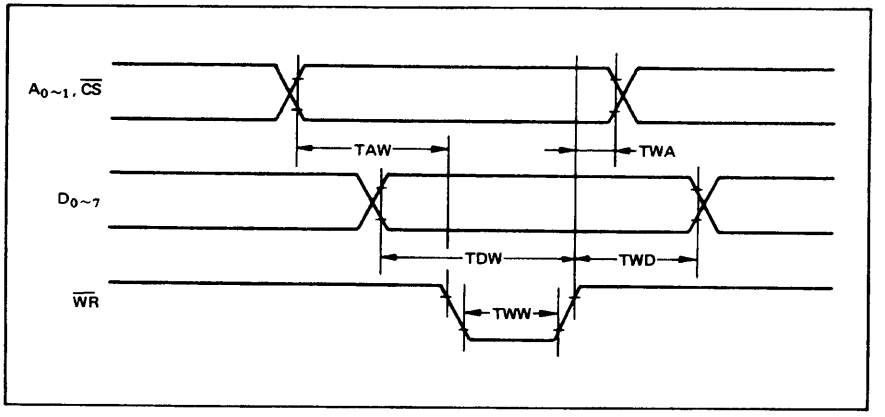
(V_{CC} = 4.5V ~ 5.5V, Ta = –40 ~ +85°C)

Parameter	Symbol	MSM82C53-2 Min.	Max.	Unit	Conditions	
Address Set-up Time before reading	TAR	30		ns	Read cycle	C_L = 150pF
Address Hold Time after reading	TRA	0		ns		
Read Pulse Width	TRR	150		ns		
Read Recovery Time	TRVR	200		ns		
Address Set-up Time before writing	TAW	0		ns	Write cycle	
Address Hold Time after writing	TWA	20		ns		
Write Pulse Width	TWW	150		ns		
Data Input Set-up Time before writing	TDW	100		ns		
Data Input Hold Time after writing	TWD	20		ns		
Write Recovery time	TRVW	200		ns		
Clock Cycle Time	TCLK	125	D.C.	ns	Clock and gate timing	
Clock "H" Pulse Width	TPWH	60		ns		
Clock "L" Pulse Width	TPWL	60		ns		
"H" Gate Pulse Width	TGW	50		ns		
"L" Gate Pulse Width	TGL	50		ns		
Gate Input Set-up Time before clock	TGS	50		ns		
Gate Input Hold Time after clock	TGH	50		ns		
Output Delay Time after reading	TRD		120	ns	Delay time	
Output Floating Delay Time after reading	TDF	5	90	ns		
Output Delay Time after gate	TODG		120	ns		
Output Delay Time after clock	TOD		150	ns		
Output Delay Time after address	TAD		180	ns		

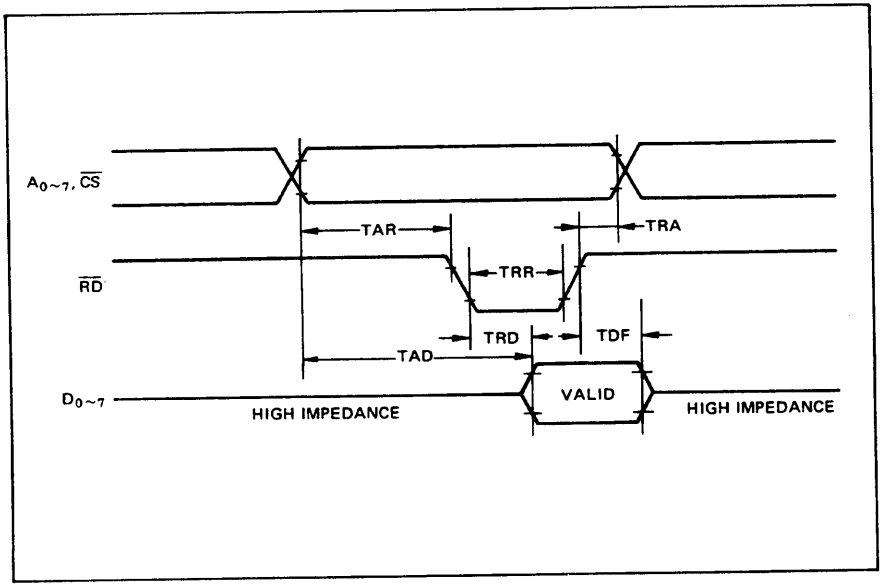
Note: Timing measured at V_L = 0.8V and V_H = 2.2V for both inputs and outputs.

TIME CHART

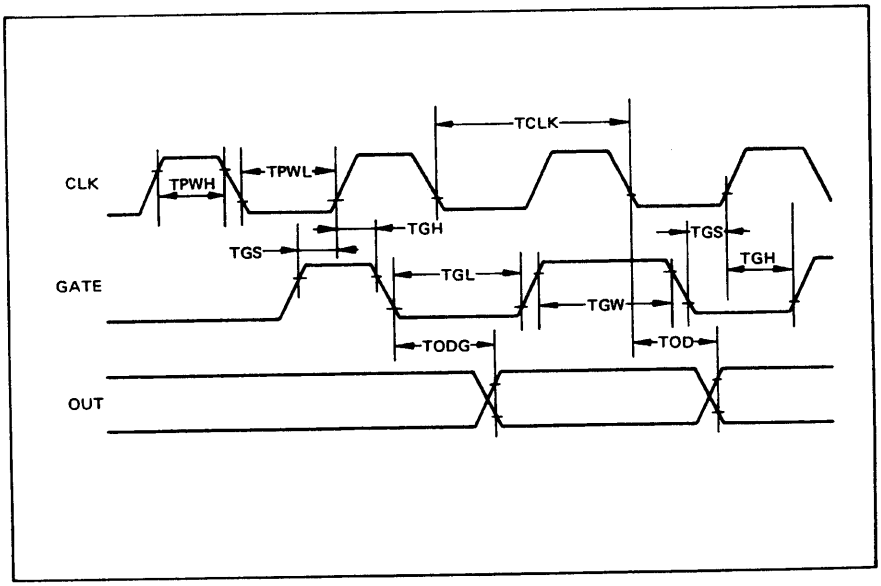
Write Timing



Read Timing



Clock & Gate Timing

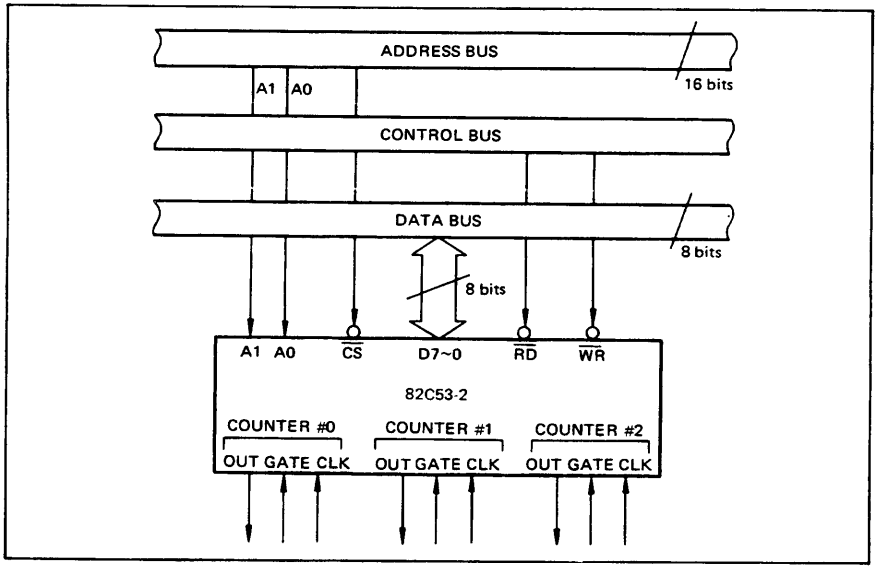


■ I/O-MSM82C53-2RS/GS/JS ■

DESCRIPTION OF PIN FUNCTIONS

Pin Symbol	Name	Input/output	Function
D7 ~ D0	Bidirectional data bus	Input/output	Three-state 8-bit bidirectional data bus used when writing control words and count values, and reading count values upon reception of $\overline{WR}$ and $\overline{RD}$ signals from CPU.
$\overline{CS}$	Chip select input	Input	Data transfer with the CPU is enabled when this pin is at low level. When at high level, the data bus (D_0 thru D_7) is switched to high impedance state where neither writing nor reading can be executed. Internal registers, however, remain unchanged.
$\overline{RD}$	Read input	Input	Data can be transferred from MSM82C53 to CPU when this pin is at low level.
$\overline{WR}$	Write input	Input	Data can be transferred from CPU to MSM82C53 when this pin is at low level.
A0, A1	Address input	Input	One of the three internal counters or the control word register is selected by A0/A1 combination. These two pins are normally connected to the two lower order bits of the address bus.
CLK0~2	Clock input	Input	Supply of three clock signals to the three counters incorporated in MSM82C53.
GATE0~2	Gate input	Input	Control of starting, interruption, and restarting of counting in the three respective counters in accordance with the set control word contents.
OUT0~2	Counter output	Output	Output of counter output waveform in accordance with the set mode and count value.

SYSTEM INTERFACING



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DESCRIPTION OF BASIC OPERATIONS

Data transfers between the internal registers and the external data bus is outlined in the following table.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	Function
0	1	0	0	0	Data bus to counter # 0 Writing
0	1	0	0	1	Data bus to counter # 1 Writing
0	1	0	1	0	Data bus to counter # 2 Writing
0	1	0	1	1	Data bus to control word register Writing
0	0	1	0	0	Data bus from counter # 0 Reading
0	0	1	0	1	Data bus from counter # 1 Reading
0	0	1	1	0	Data bus from counter # 2 Reading
0	0	1	1	1	Data bus in high impedance status
1	x	x	x	x	
0	1	1	x	x	

x denotes "not specified".

DESCRIPTION OF OPERATION

82C53 functions are selected by a control word from the CPU. In the required program sequence, the control word setting is followed by the count value setting and execution of the desired timer operation.

Control Word and Count Value Program

Each counter operation mode is set by control word programming. The control word format is outlined below.

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD
Select Counter		Read/Load		Mode			BCD

($\overline{CS}$ = 0, A0, A1 = 1,1, $\overline{RD}$ = 1, $\overline{WR}$ = 0)

- **Select Counter (SC0, SC1):** Selection of set counter

SC1	SC0	Set Contents
0	0	Counter # 0 selection
0	1	Counter # 1 selection
1	0	Counter # 2 selection
1	1	Illegal combination

- **Read/Load (RL1, RL0):** Count value Reading/Loading format setting

RL1	RL0	Set Contents
0	0	Counter Latch operation
0	1	Reading/Loading of Least Significant byte (LSB)
1	0	Reading/Loading of Most Significant byte (MSB)
1	1	Reading/Loading of LSB followed by MSB

- **Mode (M2, M1, M0):** Operation waveform mode setting

M2	M1	M0	Set Contents
0	0	0	Mode 0 (Interrupt on Terminal Count)
0	0	1	Mode 1 (Programmable One-Shot)
x	1	0	Mode 2 (Rate Generator)
x	1	1	Mode 3 (Square Wave Generator)
1	0	0	Mode 4 (Software Triggered Strobe)
1	0	1	Mode 5 (Hardware Triggered Strobe)

x denotes "not specified".

- **BCD:** Operation count mode setting

BCD	Set Contents
0	Binary Count (16-bits Binary)
1	BCD Count (4-decades Binary Coded Decimal)

After setting Read/Load, Mode, and BCD in each counter as outlined above, next set the desired count value. (In some Modes, counting is started immediately after the count value has been written). This count value setting must conform with the Read/Load format set in advance. Note that the internal counters are reset to OOOOH during control word setting. The counter value (OOOOH) can.t be read.

If the two bytes (LSB and MSB) are written at this stage (RL0 and RL1 = 1,1), take note of the following precaution.

Although the count values may be set in the three counters in any sequence after the control word has been set in each counter, count values must be set consecutively in the LSB – MSB order in any one counter.

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■ I/O-MSM82C53-2RS/GS/JS ■

- **Example of control word and count value setting**

Counter # 0: Read/Load LSB only, Mode 3, Binary count, count value 3H
Counter # 1: Read/Load MSB only, Mode 5, Binary count, count value AA00H
Counter # 2: Read/Load LSB and MSB, Mode 0, BCD count, count value 1234

```
MVI A, 1EH ┐
OUT n3     ┘ Counter #0 control word setting
MVI A, 6AH ┐
OUT n3     ┘ Counter #1 control word setting
MVI A, B1H ┐
OUT n3     ┘ Counter #2 control word setting
MVI A, 03H ┐
OUT n0     ┘ Counter #0 count value setting
MVI A, AAH ┐
OUT n1     ┘ Counter #1 count value setting
MVI A, 34H ┐
OUT n2     │ Counter #2 count value setting
MVI A, 12H │ (LSB then MSB)
OUT n2     ┘
```

Notes: n0: Counter #0 address
n1: Counter #1 address
n2: Counter #2 address
n3: Control word register address

- **The minimum and maximum count values which can be counted in each mode are listed below.**

Mode	Min.	Max.	Remarks
0	1	0	0 executes 10000H count (ditto in other modes)
1	1	0	
2	2	0	1 cannot be counted
3	2	1	1 executes 10001H count
4	1	0	
5	1	0	

Mode Definition

- **Mode 0 (terminal count)**
The counter output is set to "L" level by the mode setting. If the count value is then written in the counter with the gate input at "H" level (that is, upon completion of writing the MSB when there are two bytes), the clock input counting is started. When the terminal count is reached, the output is switched to "H" level and is maintained in this status until the control word and count value are set again.
Counting is interrupted if the gate input is switched to "L" level, and restarted when switched back to "H" level.
When Count Values are written during counting, the operation is as follows:

1-byte Read/Load.... When the new count value is written, counting is stopped immediately, and then restarted at the new count value by the next clock.

2-byte Read/Load.... When byte 1 (LSB) of the new count value is written, counting is stopped immediately. Counting is restarted at the new count value when byte 2 (MSB) is written.

- **Mode 1 (programmable one-shot)**
The counter output is switched to "H" level by the mode setting. Note that in this mode, counting is not started if only the count value is written. Since counting has to be started in this mode by using the leading edge of the gate input as a trigger, the counter output is switched to "L" level by the next clock after the gate input trigger. This "L" level status is maintained during the set count value, and is switched back to "H" level when the terminal count is reached.
Once counting has been started, there is no interruption until the terminal count is reached, even if the gate input is switched to "L" level in the meantime. And although counting continues even if a new count value is written during the counting, counting is started at the new count value if another trigger is applied by the gate input.

- **Mode 2 (rate generator)**
The counter output is switched to "H" level by the mode setting. When the gate input is at "H" level, counting is started by the next clock after the count value has been written. And if the gate input is at "L" level, counting is started by using the rising edge of the gate input as a trigger after the count value has been set.
An "L" level output pulse appears at the counter output during a single clock duration once every n clock inputs where n is the set count value. If a new count value is written during while counting is in progress, counting is started at the new count value following output of the pulse currently being counted. And if the gate input is switched to "L" level during counting, the counter output is forced to switch to "H" level, the counting being restarted by the rising edge of the gate input.

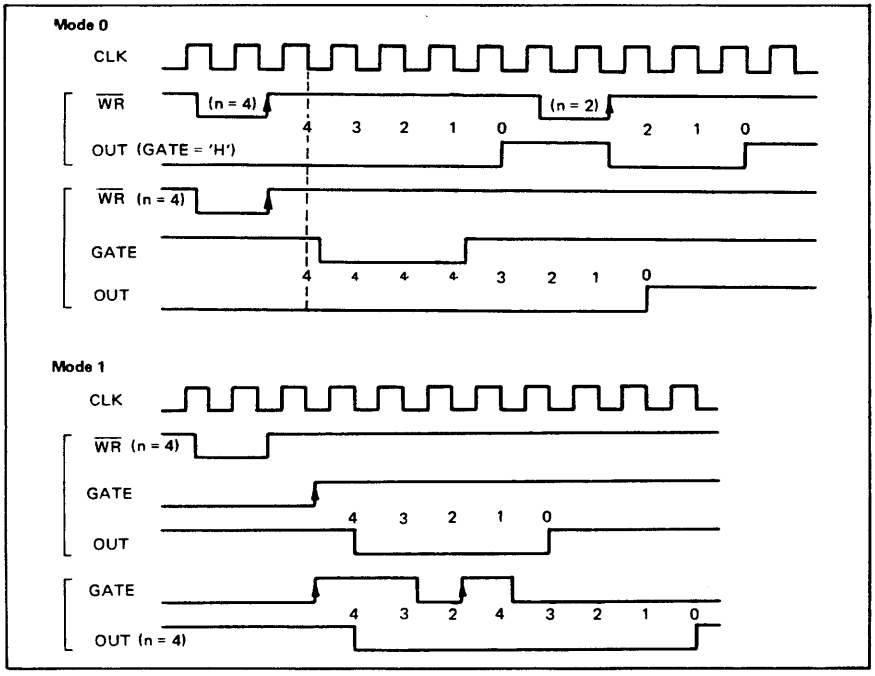
- **Mode 3 (square waveform rate generator)**
The counter output is switched to "H" level by the mode setting. Counting is started in the same way as described for mode 2 above.
The repeated square wave output appearing at the counter output contains half the number of counts as the set count value. If the set count value (n) is an odd number, the repeated square wave output consists of only (n + 1)/2 clock inputs at "H" level and (n − 1)/2 clock inputs at "L" level.
If a new count value is written during counting, the new count value is reflected immediately after the

change ("H" to "L" or "L" to "H") in the next counter output to be executed. The counting operation at the gate input is done the same as in mode 2.

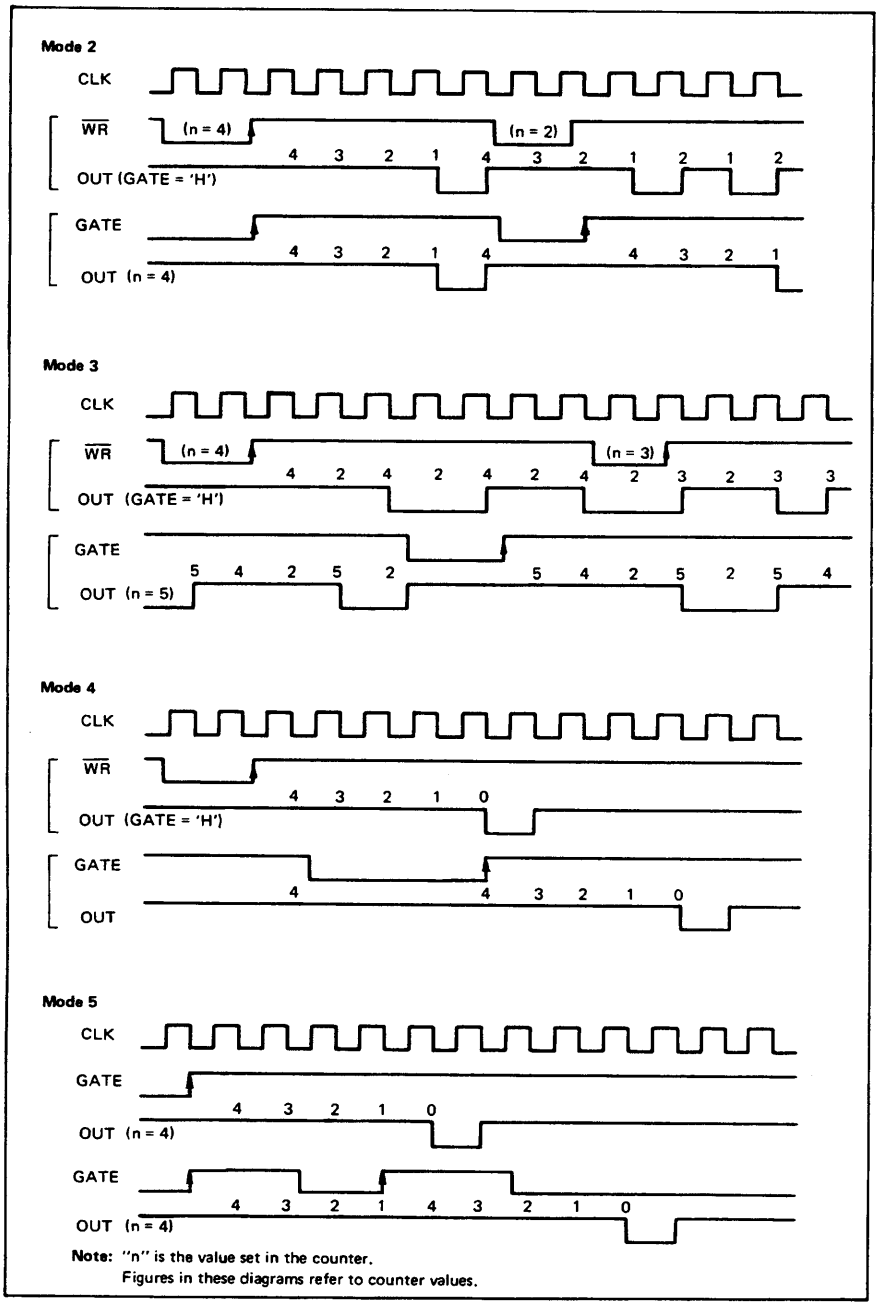
- **Mode 4 (software trigger strobe)**
  The counter output is switched to "H" level by the mode setting. Counting is started in the same way as described for mode 0. A single "L" pulse equivalent to one clock width is generated at the counter output when the terminal count is reached.
  This mode differs from 2 in that the "L" level output appears one clock earlier in mode 2, and that pulses are not repeated in mode 4. Counting is stopped when the gate input is switched to "L" level, and restarted from the set count value when switched back to "H" level.

- **Mode 5 (hardware trigger strobe)**
  The counter output is switched to "H" level by the mode setting. Counting is started, and the gate input used, in the same way as in mode 1.
  The counter output is identical to the mode 4 output.
  The various roles of the gate input signals in the above modes are summarized in the following table.

Mode \ Gate	"L" Level Falling Edge	Rising Edge	"H" Level
0	Counting not possible		Counting possible
1		(1) Start of counting (2) Retriggering	
2	(1) Counting not possible (2) Counter output forced to "H" level	Start of counting	Counting possible
3	(1) Counting not possible (2) Counter output forced to "H" level	Start of counting	Counting possible
4	Counting not possible		Counting possible
5		(1) Start of counting (2) Retriggering	



■ I/O-MSM82C53-2RS/GS/JS ■



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Reading of Counter Values

All 82C53 counting is down-counting, the counting being in steps of 2 in mode 3. Counter values can be read during counting by (1) direct reading, and (2) counter latching ("read on the fly").

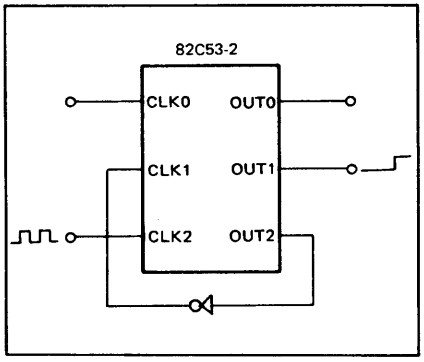
- **Direct reading**
  Counter values can be read by direct reading operations.
  Since the counter value read according to the timing of the $\overline{RD}$ and CLK signals is not guaranteed, it is necessary to stop the counting by a gate input signal, or to interrupt the clock input temporarily by an external circuit to ensure that the counter value is correctly read.

- **Counter latching**
  In this method, the counter value is latched by writing a counter latch command, thereby enabling a stable value to be read without effecting the counting in any way at all. An example of a counter latching program is given below.
  Counter latching executed for counter #1 (Read/Load 2-byte setting)

```
MVI A  0 1 0 0 x x x x
          └── Denotes counter latching

OUT n3 ──┬── Write in control word address
         │   (n3)
         └── The counter value at this point
             is latched

IN n1  ──┬── Reading of the LSB of the
         │   counter value latched from
         │   counter #1.
         └── n1: Counter #1 address

MOV B, A
IN n1  ──── Reading of MSB from counter
            #1.
MOV C, A
```

Example of Practical Application

- **82C53 used as a 32-bit counter.**



Use counter #1 and counter #2

Counter #1: mode 0, upper order 16-bit counter value

Counter #2: mode 2, lower order 16-bit counter value

This setting enables counting up to a maximum of 2^{32}

Register-Level Programming

Appendix D

This appendix describes in detail the address and function of each of the PC-DIO-96/PnP control and status registers. This appendix also includes important information about register-level programming on the PC-DIO-96/PnP along with program examples written in C and assembly language.

☞ **Note:** ***If you plan to use a programming software package such as LabWindows/CVI or NI-DAQ with your PC-DIO-96/PnP board, you need not read this appendix.***

Introduction

☞ **Note:** ***You can configure your PC-DIO-96/PnP board to use base addresses in the range of 100 to 3E0 hex. Your PC-DIO-96/PnP board occupies 16 bytes of address space and must be located on a 16-byte boundary. Therefore, valid addresses include 100, 110, 120..., 3E0 hex. The base I/O address is software configured and does not require you to manually change any settings on the board. For more information on configuring the PC-DIO-96PnP, see Chapter 2,*** *Installation and Configuration****.***

The three 8-bit ports of the 82C55A are divided into two groups of 12 signals each: group A and group B. One 8-bit control word selects the mode of operation for each group. The group A control bits configure port A (A7 through A0) and the upper 4 bits (nibble) of port C (C7 through C4). The group B control bits configure port B (B7 through B0) and the lower nibble of port C (C3 through C0). These configuration bits are defined in the *Register Description for the 82C55A* section later in this appendix. Because there are four 82C55A PPI devices on the board, they are referenced as PPI A, PPI B, PPI C, and PPI D when differentiation is required.

The three 16-bit counters of the 82C53 are accessed through individual data ports and controlled by one 8-bit control word. The control word selects how the counter data ports are accessed and what mode the

counter uses. The configuration bits are defined in the *Register Description for the 82C53* section later in this appendix.

In addition to the 82C55A devices and the 82C53 device, there are two registers that select which onboard signals are capable of generating interrupts. There are two interrupt signals from each of the four 82C55A devices and two interrupt signals from the 82C53 device. Individual enable bits select which of these 10 signals can generate interrupts. Also, a master enable signal determines whether the board can actually send a request to the host computer. The configuration bits for these registers are defined in the *Register Description for the Interrupt Control Registers* section later in this appendix.

Register Map

The following table lists the address map for the PC-DIO-96/PnP.

Table D-1. PC-DIO-96/PnP Address Map

Register Name	Offset Address (Hex)	Size	Type
82C55A Register Group			
PPI A			
PORTA Register	00	8-bit	Read-and-write
PORTB Register	01	8-bit	Read-and-write
PORTC Register	02	8-bit	Read-and-write
CNFG Register	03	8-bit	Write-only
PPI B			
PORTA Register	04	8-bit	Read-and-write
PORTB Register	05	8-bit	Read-and-write
PORTC Register	06	8-bit	Read-and-write
CNFG Register	07	8-bit	Write-only

Table D-1. PC-DIO-96/PnP Address Map (Continued)

Register Name	Offset Address (Hex)	Size	Type
PPI C			
PORTA Register	08	8-bit	Read-and-write
PORTB Register	09	8-bit	Read-and-write
PORTC Register	0A	8-bit	Read-and-write
CNFG Register	0B	8-bit	Write-only
PPI D			
PORTA Register	0C	8-bit	Read-and-write
PORTB Register	0D	8-bit	Read-and-write
PORTC Register	0E	8-bit	Read-and-write
CNFG Register	0F	8-bit	Write-only
82C53 Register Group			
PORTA Register	10	8-bit	Read-and-write
PORTB Register	11	8-bit	Read-and-write
PORTC Register	12	8-bit	Read-and-write
CNFG Register	13	8-bit	Write-only
Interrupt Control Register Group			
Register 1	14	8-bit	Write-only
Register 2	15	8-bit	Write-only

Register Descriptions

The register descriptions for the devices on the PC-DIO-96/PnP, including the 82C55A, the 82C53, and each of the interrupt control registers, are given on the pages that follow.

Register Description for the 82C55A

Figure D-1 shows the two control word formats used to completely program the 82C55A. The control word flag determines which control word format is being programmed. When the control word flag is 1, bits 6 through 0 select the I/O characteristics of the 82C55A ports. These bits also select the mode in which the ports are operating (that is, mode 0, mode 1, or mode 2). When the control word flag is 0, bits 3 through 0 select the bit set/reset format of port C.

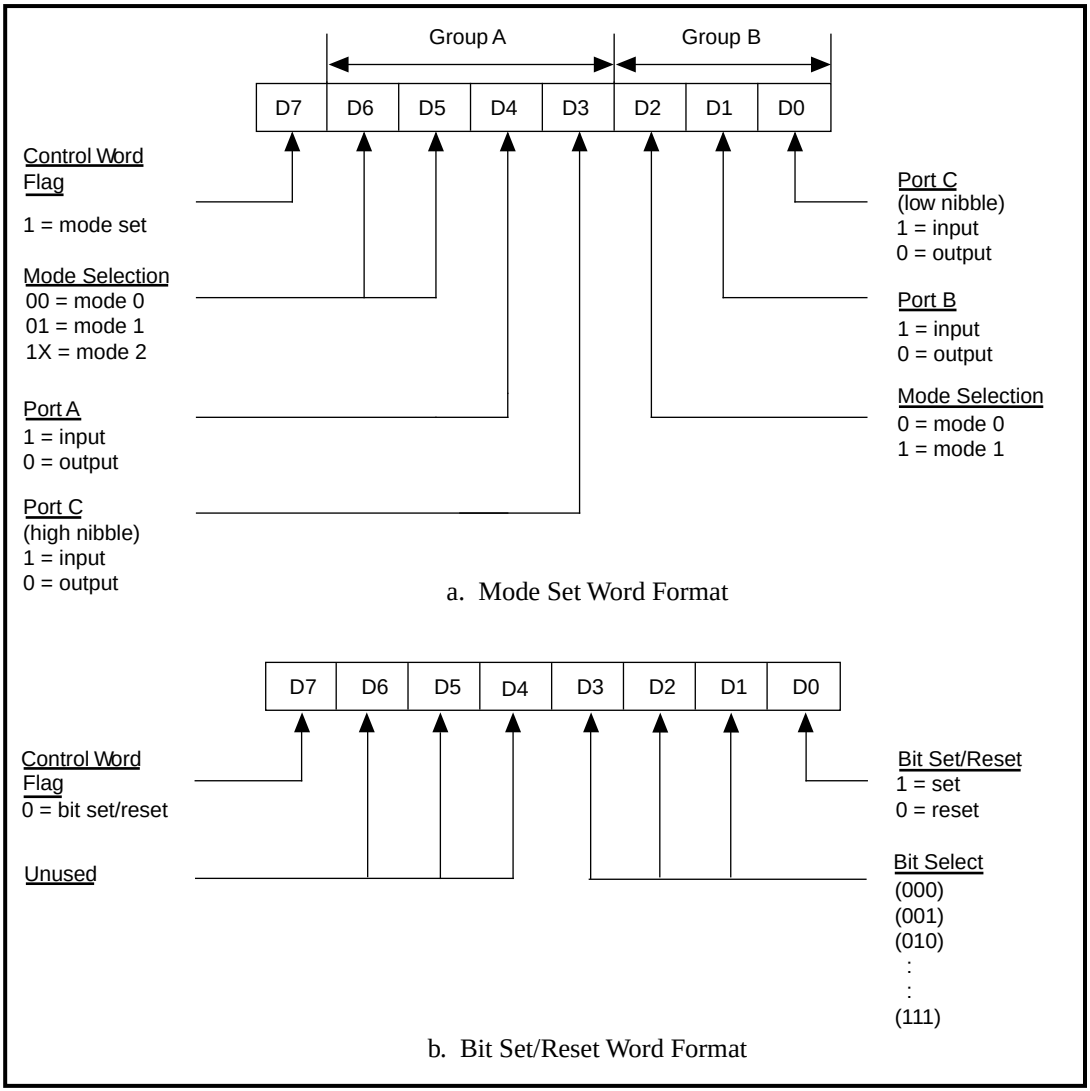


Figure D-1. Control Word Formats for the 82C55A

Warning: ***During programming, note that each time a port is configured, output ports A and C are reset to 0, and output port B is undefined.***

Table D-2 shows the control words for setting or resetting each bit in port C. Notice that bit 7 of the control word is cleared when programming the set/reset option for the bits of port C.

Table D-2. Port C Set/Reset Control Words

Bit Number	Bit Set Control Word	Bit Reset Control Word	The Bit Set or Reset in Port C
0	0xxx0001	0xxx0000	xxxxxxxb
1	0xxx0011	0xxx0010	xxxxxxbx
2	0xxx0101	0xxx0100	xxxxxbxx
3	0xxx0111	0xxx0110	xxxxbxxx
4	0xxx1001	0xxx1000	xxxbxxxx
5	0xxx1011	0xxx1010	xxbxxxxx
6	0xxx1101	0xxx1100	xbxxxxxx
7	0xxx1111	0xxx1110	bxxxxxxx

Register Description for the 82C53

Figure D-2 shows the control word format used to completely program the 82C53. Bits 7 and 6 of the control word select the counter to be programmed. Bits 5 and 4 select the mode by which the count data is written to and read from the selected counter. Bits 3, 2, and 1 select the mode for the selected counter. Bit 0 selects whether the counter counts in binary or BCD format.

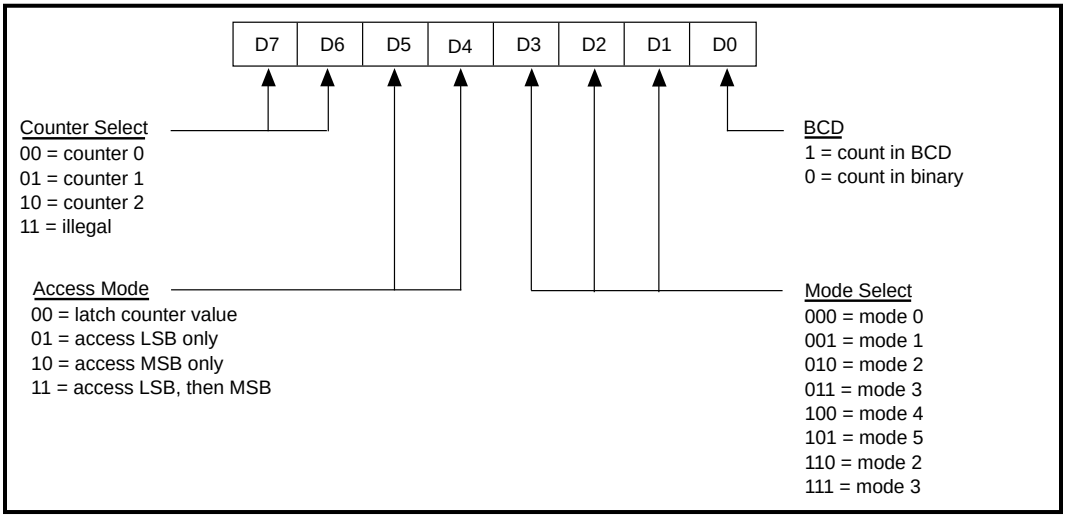


Figure D-2. Control Word Format for the 82C53

Register Description for the Interrupt Control Registers

There are two interrupt control registers on the PC-DIO-96/PnP. One of these registers has individual enable bits for the two interrupt lines from each of the 82C55A devices. The other register has a master interrupt enable bit and two bits for the timed interrupt circuitry. Of the latter two bits, one bit enables counter interrupts, while the other selects counter 0 or counter 1. The bit maps and signal definitions are listed as follows.

Interrupt Control Register 1

D7	D6	D5	D4	D3	D2	D1	D0
DIRQ1	DIRQ0	CIRQ1	CIRQ0	BIRQ1	BIRQ0	AIRQ1	AIRQ0

Bit	Name	Description
7	DIRQ1	PPI D Interrupt Request for Port B—If this bit and the INTEN bit in Interrupt Control Register 2 are both set, PPI D sends an interrupt, INTRB, to the host computer. If this bit is cleared, PPI D does not send the interrupt INTRB to the host computer, regardless of the setting of INTEN.
6	DIRQ0	PPI D Interrupt Request for Port A—If this bit and the INTEN bit in Interrupt Control Register 2 are both set, PPI D sends an interrupt, INTRA, to the host computer. If this bit is cleared, PPI D does not send the interrupt INTRA to the host computer, regardless of the setting of INTEN.
5	CIRQ1	PPI C Interrupt Request for Port B—If this bit and the INTEN bit in Interrupt Control Register 2 are both set, PPI C sends an interrupt, INTRB, to the host computer. If this bit is cleared, PPI C does not send the interrupt INTRB to the host computer, regardless of the setting of INTEN.
4	CIRQ0	PPI C Interrupt Request for Port A—If this bit and the INTEN bit in Interrupt Control Register 2 are both set, PPI C sends an interrupt, INTRA, to the host computer. If this bit is cleared, PPI C does not send the interrupt INTRA to the host computer, regardless of the setting of INTEN.
3	BIRQ1	PPI B Interrupt Request for Port B—If this bit and the INTEN bit in Interrupt Control Register 2 are both set, PPI B sends an interrupt, INTRB, to the host computer. If this bit is cleared, PPI B does not send the interrupt INTRB to the host computer, regardless of the setting of INTEN.

Bit	Name	Description (Continued)
2	BIRQ0	PPI B Interrupt Request for Port A—If this bit and the INTEN bit in Interrupt Control Register 2 are both set, PPI B sends an interrupt, INTRA, to the host computer. If this bit is cleared, PPI B does not send the interrupt INTRA to the host computer, regardless of the setting of INTEN.
1	AIRQ1	PPI A Interrupt Request for Port B—If this bit and the INTEN bit in Interrupt Control Register 2 are both set, PPI A sends an interrupt, INTRB, to the host computer. If this bit is cleared, PPI A does not send the interrupt INTRB to the host computer, regardless of the setting of INTEN.
0	AIRQ0	PPI A Interrupt Request for Port A—If this bit and the INTEN bit in Interrupt Control Register 2 are both set, PPI A sends an interrupt, INTRA, to the host computer. If this bit is cleared, PPI A does not send the interrupt INTRA to the host computer, regardless of the setting of INTEN.

Interrupt Control Register 2

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	INTEN	CTRIRQ	CTR1

Bit	Name	Description
7–3	X	Don't Care Bit.
2	INTEN	Global Interrupt Enable Bit—If this bit is set, the PC-DIO-96/PnP can interrupt the host computer. If this bit is cleared, the PnP version of this board cannot interrupt the host computer. With the non-PnP version, the interrupt line is put into high-impedance mode, so other devices can use the interrupt channel selected by jumper W1.
1	CTRIRQ	Counter Interrupt Enable Bit—If this bit is set, the 82C53 counter outputs can interrupt the host computer. If this bit is cleared, the counter outputs have no effect.
0	CTR1	Counter 1 Enable Bit—If this bit is set, the output from counter 1 of the 82C53 is connected to the interrupt request circuitry. In this mode, counter 0 of the 82C53 acts as a frequency scaler for counter 1, which generates the interrupt. If CTR1 is cleared, the output from counter 0 of the 82C53 is connected to the interrupt request circuitry. In this mode, counter 0 generates the interrupt. For more information, see the section later in this chapter on programming interrupts using the 82C53.

Programming Considerations for the 82C55A

Modes of Operation for the 82C55A

The three basic modes of operation for the 82C55A are as follows:

- Mode 0—Basic I/O
- Mode 1—Strobed I/O
- Mode 2—Bidirectional bus

The 82C55A also has a single bit set/reset feature for port C, which is programmed by the 8-bit control word. For additional information, refer to Appendix B, *OKI 82C55A Data Sheet*.

Mode 0

This mode can be used for simple input and output operations for each of the ports. No handshaking is required; data is simply written to or read from a specified port.

Mode 0 has the following features:

- Two 8-bit ports (A and B) and two 4-bit ports (upper and lower nibbles of port C).
- Any port can be input or output.
- Outputs are latched, but inputs are not latched.

Mode 1

This mode transfers data that is synchronized by handshaking signals. Ports A and B use the eight lines of port C to generate or receive the handshake signals. This mode divides the ports into two groups (group A and group B) and includes the following features:

- Each group contains one 8-bit data port (port A or port B) and one 4-bit control/data port (upper or lower nibble of port C).
- The 8-bit data ports can be either input or output, both of which are latched.
- The 4-bit ports are used for control and status of the 8-bit data ports.
- Interrupt generation and enable/disable functions are available.

Mode 2

This mode can be used for communication over a bidirectional 8-bit bus. Handshaking signals are used in a manner similar to mode 1. Mode 2 is available for use in group A only (port A and the upper nibble of port C). Other features of this mode include the following:

- One 8-bit bidirectional port (port A) and a 5-bit control/status port (port C).
- Latched inputs and outputs.
- Interrupt generation and enable/disable functions.

Single Bit Set/Reset Feature

Any of the eight bits of port C can be set or reset with one control word. This feature generates control signals for port A and port B when these ports are operating in mode 1 or mode 2.

Mode 0—Basic I/O

Mode 0 can be used for simple I/O functions (no handshaking) for each of the three ports. Each port can be assigned as an input or an output port. The 16 possible I/O configurations are shown in Table D-3. Notice that bit 7 of the control word is set when programming the mode of operation for each port.

Table D-3. Mode 0 I/O Configurations

	Control Word	Group A		Group B	
Number	**Bit 76543210**	**Port A**	**Port C[1]**	**Port B**	**Port C[2]**
0	10000000	Output	Output	Output	Output
1	10000001	Output	Output	Output	Input
2	10000010	Output	Output	Input	Output
3	10000011	Output	Output	Input	Input
4	10001000	Output	Input	Output	Output
5	10001001	Output	Input	Output	Input
6	10001010	Output	Input	Input	Output
7	10001011	Output	Input	Input	Input
8	10010000	Input	Output	Output	Output

Table D-3. Mode 0 I/O Configurations (Continued)

	Control Word	Group A		Group B	
Number	**Bit 76543210**	**Port A**	**Port C[1]**	**Port B**	**Port C[2]**
9	10010001	Input	Output	Output	Input
10	10010010	Input	Output	Input	Output
11	10010011	Input	Output	Input	Input
12	10011000	Input	Input	Output	Output
13	10011001	Input	Input	Output	Input
14	10011010	Input	Input	Input	Output
15	10011011	Input	Input	Input	Input

[1]Upper nibble of port C
[2]Lower nibble of port C

Mode 0 Programming Example

The following example shows how to configure PPI A for various combinations of mode 0 input and output. This code is strictly an example and is not intended to be used without modification in a practical situation.

```
Main() {

#define BASE_ADDRESS       0x180        /* Board located at address 180 */
#define APORTAoffset       0x00         /* Offset for PPI A, port A */
#define APORTBoffset       0x01         /* Offset for PPI A, port B */
#define APORTCoffset       0x02         /* Offset for PPI A, port C */
#define ACNFGoffset        0x03         /* Offset for PPI A, CNFG */

unsigned int porta, portb, portc, cnfg;
char valread;              /* Variable to store data read from a port */

/*  Calculate register addresses */
porta = BASE_ADDRESS + APORTAoffset;
portb = BASE_ADDRESS + APORTBoffset;
portc = BASE_ADDRESS + APORTCoffset;
cnfg  = BASE_ADDRESS + ACNFGoffset;
```

```
/* EXAMPLE 1*/

outp(cnfg,0x80);          /* Ports A, B, and C are outputs. */
outp(porta,0x12);         /* Write data to port A. */
outp(portb,0x34);         /* Write data to port B. */
outp(portc,0x56);         /* Write data to port C. */

/* EXAMPLE 2*/

outp(cnfg,0x90);          /* Port A is input; ports B and C are outputs. */
outp(portb,0x22);         /* Write data to port B. */
outp(portc,0x55);         /* Write data to port C. */
valread = inp(porta);     /* Read data from port A. */

/* EXAMPLE 3 */

outp(cnfg,0x82);          /* Ports A and C are outputs;
                             port B is an input. */

/* EXAMPLE 4 */

outp(cnfg,0x89);          /* Ports A and B are outputs;
                             port C is an input. */
}
```

Mode 1—Strobed Input

In mode 1, the digital I/O bits are divided into two groups: group A and group B. Each of these groups contains one 8-bit port and one 4-bit control/data port. The 8-bit port can be either an input or an output port, and the 4-bit port is used for control and status information for the 8-bit port. The transfer of data is synchronized by handshaking signals in the 4-bit port.

The control word written to the CNFG Register to configure port A for input in mode 1 is shown as follows. Bits PC6 and PC7 of port C can be used as extra input or output lines.

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	1/0	X	X	X

Port C bits PC6 and PC7
1 = input
0 = output

The control word written to the CNFG Register to configure port B for input in mode 1 is shown as follows. Notice that port B does not have extra input or output lines from port C.

D7	D6	D5	D4	D3	D2	D1	D0
1	X	X	X	X	1	1	X

During a mode 1 data read transfer, the status of the handshaking lines and interrupt signals can be obtained by reading port C. The port C status-word bit definitions for an input transfer are shown as follows.

Port C status-word bit definitions for input (port A and port B):

D7	D6	D5	D4	D3	D2	D1	D0
I/O	I/O	IBFA	INTEA	INTRA	INTEB	IBFB	INTRB

Bit	Name	Description
7–6	I/O	Input/Output—These bits can be used for general-purpose I/O when port A is in mode 1 input. If these bits are configured for output, the port C bit set/reset function must be used to manipulate them.
5	IBFA	Input Buffer for Port A—A high setting indicates that data has been loaded into the input latch for port A.
4	INTEA	Interrupt Enable Bit for Port A—Setting this bit enables interrupts from port A of the 82C55A. This bit is controlled by setting/resetting PC4.
3	INTRA	Interrupt Request Status for Port A—When INTEA and IBFA are high, this bit is high, indicating that an interrupt request is pending for port A.

Bit	Name	Description (Continued)
2	INTEB	Interrupt Enable Bit for Port B—Setting this bit enables interrupts from port B of the 82C55A. This bit is controlled by setting/resetting PC2.
1	IBFB	Input Buffer for Port B—A high setting indicates that data has been loaded into the input latch for port B.
0	INTRB	Interrupt Request Status for Port B—When INTEB and IBFB are high, this bit is high, indicating that an interrupt request is pending for port B.

At the digital I/O connector, port C has the following pin assignments when in mode 1 input. Notice that the status of STBA* and the status of STBB* are not included in the port C status word.

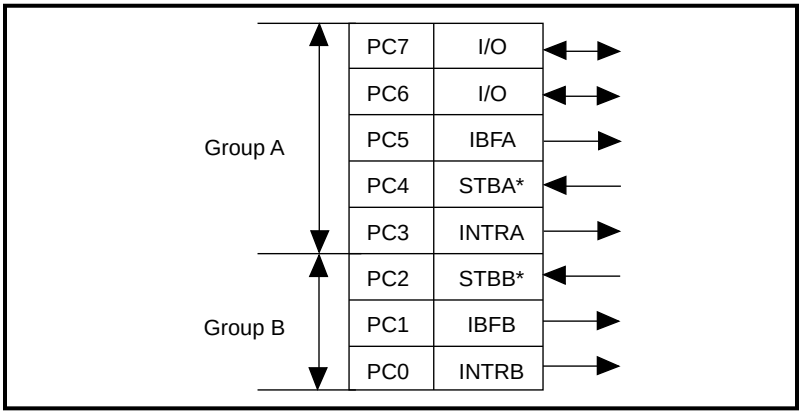


Figure D-3. Port C Pin Assignments, Mode 1 Input

Mode 1 Input Programming Example

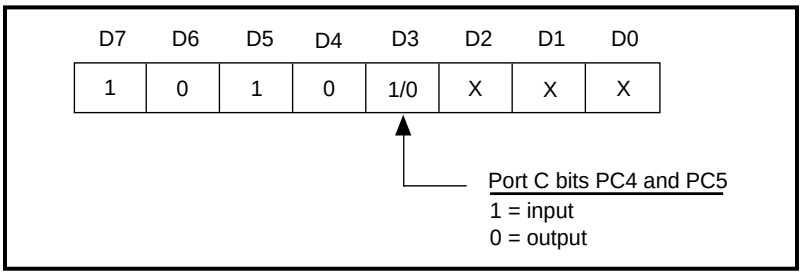
The following example shows how to configure PPI A for various combinations of mode 1 input. This code is strictly an example and is not intended to be used without modification in a practical situation.

```
Main() {
#define BASE_ADDRESS       0x180        /* Board located at address 180 */
#define APORTAoffset       0x00         /* Offset for PPI A, port A */
#define APORTBoffset       0x01         /* Offset for PPI A, port B */
#define APORTCoffset       0x02         /* Offset for PPI A, port C */
#define ACNFGoffset        0x03         /* Offset for PPI A, CNFG */
```

```
unsigned int porta, portb, portc, cnfg;
char valread;              /* Variable to store data read from a port */

/*  Calculate register addresses */

porta = BASE_ADDRESS + APORTAoffset;
portb = BASE_ADDRESS + APORTBoffset;
portc = BASE_ADDRESS + APORTCoffset;
cnfg  = BASE_ADDRESS + ACNFGoffset;

/* EXAMPLE 1–port A input */

outp(cnfg,0xB0);                        /* Port A is an input in mode 1. */
while (!(inp(portc) & 0x20));           /* Wait until IBFA is set,
                                           indicating that data has been
                                           loaded in port A. */
valread = inp(porta);                   /* Read the data from port A. */

/* EXAMPLE 2–Port B input */

outp(cnfg,0x86);                        /* Port B is an input in mode 1. */
while (!(inp(portc) & 0x02));           /* Wait until IBFB is set,
                                           indicating that data has been
                                           loaded in port B. */

valread = inp(portb);
}
```

Mode 1—Strobed Output

The control word written to the CNFG Register to configure port A for output in mode 1 is shown as follows. Bits PC4 and PC5 of port C can be used as extra input or output lines.



The control word written to the CNFG Register to configure port B for output in mode 1 is shown as follows. Notice that port B does not have extra input or output lines from port C.

D7	D6	D5	D4	D3	D2	D1	D0
1	X	X	X	X	1	0	X

During a mode 1 data write transfer, the status of the handshaking lines and interrupt signals can be obtained by reading port C. Notice that the bit definitions are different for a write and a read transfer.

Port C status-word bit definitions for output (port A and port B):

D7	D6	D5	D4	D3	D2	D1	D0
OBFA*	INTEA	I/O	I/O	INTRA	INTEB	OBFB*	INTRB

Bit	Name	Description
7	OBFA*	Output Buffer for Port A—A low setting indicates that the CPU has written data to port A.
6	INTEA	Interrupt Enable Bit for Port A—Setting this bit enables interrupts from port A of the 82C55A. This bit is controlled by setting/resetting PC6.
5–4	I/O	Input/Output—These bits can be used for general-purpose I/O when port A is in mode 1 output. If these bits are configured for output, the port C bit set/reset function must be used to manipulate them.
3	INTRA	Interrupt Request Status for Port A—When INTEA and OBFA* are high, this bit is high, indicating that an interrupt request is pending for port A.
2	INTEB	Interrupt Enable Bit for Port B—Setting this bit enables interrupts from port B of the 82C55A. This bit is controlled by setting/resetting PC2.
1	OBFB*	Output Buffer for Port B—A low setting indicates that the CPU has written data to port B.
0	INTRB	Interrupt Request Status for Port B—When INTEB and OBFB* are high, this bit is high, indicating that an interrupt request is pending for port B.

At the digital I/O connector, port C has the following pin assignments when in mode 1 output. Notice that the status of ACKA* and the status of ACKB* are not included when port C is read.

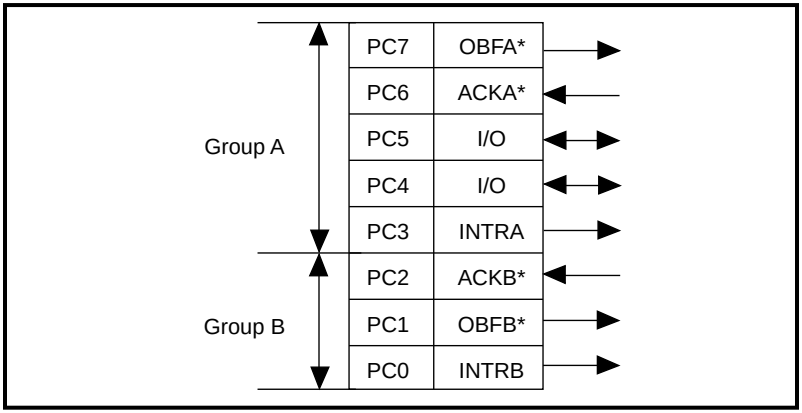


Figure D-4. Port C Pin Assignments, Mode 1 Output

Mode 1 Output Programming Example

The following example shows how to configure PPI A for various combinations of mode 1 output. This code is strictly an example and is not intended to be used without modification in a practical situation.

```
Main() {

#define BASE_ADDRESS       0x180        /* Board located at address 180 */
#define APORTAoffset       0x00         /* Offset for PPI A, port A */
#define APORTBoffset       0x01         /* Offset for PPI A, port B */
#define APORTCoffset       0x02         /* Offset for PPI A, port C */
#define ACNFGoffset        0x03         /* Offset for PPI A, CNFG */

unsigned int porta, portb, portc, cnfg;
char valread;              /* Variable to store data read from a port */

/*  Calculate register addresses */

porta = BASE_ADDRESS + APORTAoffset;
portb = BASE_ADDRESS + APORTBoffset;
portc = BASE_ADDRESS + APORTCoffset;
cnfg  = BASE_ADDRESS + ACNFGoffset;
```

```
/* EXAMPLE 1–port A output */
outp(cnfg,0xA0);                        /* Port A is an output in mode 1.*/
while (!(inp(portc) & 0x80));           /* Wait until OBFA* is set,
                                           indicating that the data last
                                           written to port A has been
                                           read.*/
outp(porta,0x12);                       /* Write data to port A. */
/* EXAMPLE 2–port B output */
outp(cnfg,0x84);                        /* Port B is an output in mode 1.*/
while (!(inp(portc) & 0x02));           /* Wait until OBFB* is set,
                                           indicating that the data last
                                           written to port B has been
                                           read.*/
outp(portb,0x34);                       /* Write the data to port B. */
}
```

Mode 2—Bidirectional Bus

Mode 2 has an 8-bit bus that can transfer both input and output data without changing the configuration. The data transfers are synchronized with handshaking lines in port C. This mode uses only port A; however, port B can be used in either mode 0 or mode 1 while port A is configured for mode 2.

The control word written to the CNFG Register to configure port A as a bidirectional data bus in mode 2 is shown as follows. If port B is configured for mode 0, then PC2, PC1, and PC0 of port C can be used as extra input or output lines.

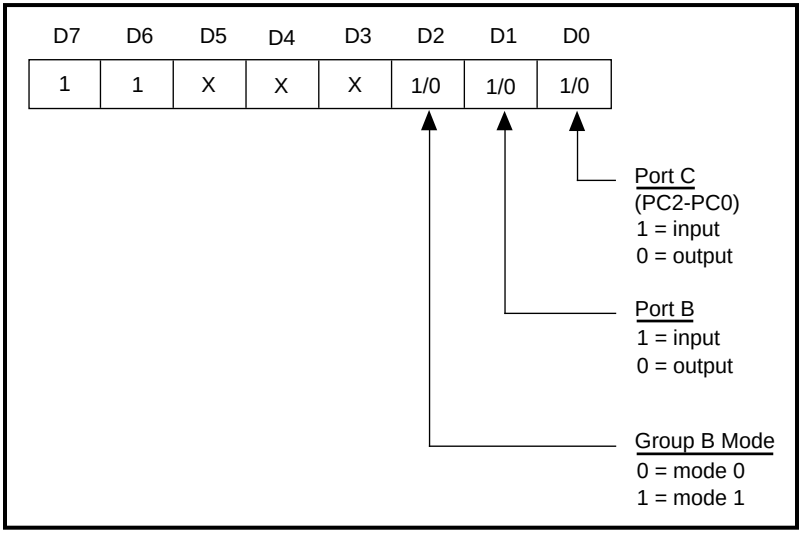


Figure D-5. Port A Configured as a Bidirectional Data Bus in Mode 2

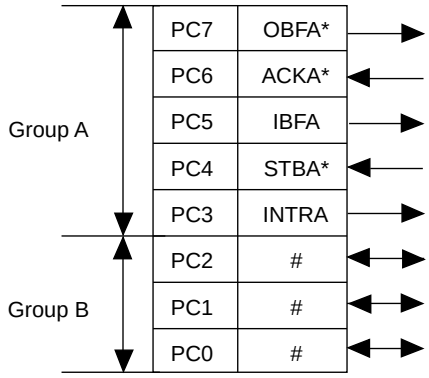
During a mode 2 data transfer, the status of the handshaking lines and interrupt signals can be obtained by reading port C. The port C status-word bit definitions for a mode 2 transfer are shown as follows.

Port C status-word bit definitions for bidirectional data path (port A only):

D7	D6	D5	D4	D3	D2	D1	D0
OBFA*	INTE1	IBFA	INTE2	INTRA	I/O	I/O	I/O

Bit	Name	Description
7	OBFA*	Output Buffer for Port A—A low setting indicates that the CPU has written data to port A.
6	INTE1	Interrupt Enable Bit for Port A Output Interrupts—Setting this bit enables output interrupts from port A of the 82C55A. This bit is controlled by setting/resetting PC6.
5	IBFA	Input Buffer for Port A—A high setting indicates that data has been loaded into the input latch of port A.
4	INTE2	Interrupt Enable Bit for Port A Input Interrupts—Setting this bit enables input interrupts from port A of the 82C55A. This bit is controlled by setting/resetting PC4.
3	INTRA	Interrupt Request Status for Port A—If INTE1 and IBFA are high, then this bit is high, indicating that an interrupt request is pending for port A input transfers. If INTE2 and OBFA* are high, then this bit is high, indicating that an interrupt request is pending for port A output transfers.
2–0	I/O	Input/Output—These bits can be used for general-purpose I/O lines if group B is configured for mode 0. If group B is configured for mode 1, refer to the bit explanations shown in the preceding mode 1 sections.

At the digital I/O connector, port C has the following pin assignments when in mode 2. Notice that the status of STBA* and the status of ACKA* are not included in the port C status word.



The three port C lines associated with group B function are based on the mode selected for group B; that is, if group B is configured for mode 0, PC2-PC0 function as general-purpose input/output, but if group B is configured for mode 1 input or output, PC2-PC0 function as handshaking lines as shown in the preceding mode 1 sections.

Figure D-6. Port C Pin Assignments, Mode 2

Mode 2 Programming Example

The following example shows how to configure PPI A for mode 2 input and output and how to use the handshaking signals to control data flow. This code is strictly an example and is not intended to be used without modification in a practical situation.

```
Main() {

#define BASE_ADDRESS       0x180        /* Board located at address 180 */
#define APORTAoffset       0x00         /* Offset for PPI A, port A */
#define APORTBoffset       0x01         /* Offset for PPI A, port B */
#define APORTCoffset       0x02         /* Offset for PPI A, port C */
#define ACNFGoffset        0x03         /* Offset for PPI A, CNFG */

unsigned int porta, portb, portc, cnfg;
char valread;              /* Variable to store data read from a port */
```

```
/*  Calculate register addresses */

porta = BASE_ADDRESS + APORTAoffset;
portb = BASE_ADDRESS + APORTBoffset;
portc = BASE_ADDRESS + APORTCoffset;
cnfg  = BASE_ADDRESS + ACNFGoffset;

/* EXAMPLE 1*/

outp(cnfg,0xC0);                        /* Port A is in mode 2. */
while (!(inp(portc) & 0x80));           /* Wait until OBFA* is set,
                                           indicating that the data last
                                           written to port A has been read.
                                           */
outp(porta,0x67);                       /* Write the data to port A. */
while (!(inp(portc) & 0x20));           /* Wait until IBFA is set,
                                           indicating that data is
                                           available in port A to be read.
                                           */
valread = inp(porta);                   /* Read data from port A. */
}
```

Interrupt Programming Examples for the 82C55A

The following examples show the process required to enable interrupts for several different operating modes. The interrupt handling routines and interrupt installation routines for the 82C55A are not included; however, sample routines for the 82C53 are included later in the appendix. These routines can be modified to function for the 82C55A. Consult your computer's technical reference manual for additional information. Also, if you generate interrupts with the PC3 or PC0 lines of the 82C55A devices, you must maintain the active high level until the interrupt service routine is entered. Otherwise, the host computer considers the interrupt a spurious interrupt and routes the request to the channel responsible for handling spurious interrupts. To prevent this problem, try using some other I/O bit to send feedback to the device generating the interrupt. In this way, the interrupting device can be signaled that the interrupt service routine has been entered. For further information on using PC3 and PC0 for interrupts, see the *Interrupt Handling* section later in this appendix.

```
Main() {

#define BASE_ADDRESS       0x180        /* Board located at address 180 */
#define APORTAoffset       0x00         /* Offset for PPI A, port A */
#define APORTBoffset       0x01         /* Offset for PPI A, port B */
#define APORTCoffset       0x02         /* Offset for PPI A, port C */
```

```
#define ACNFGoffset        0x03         /* Offset for PPI A, CNFG */
#define IREG1offset        0x14         /* Offset for Interrupt Reg. 1 */
#define IREG2offset        0x15         /* Offset for Interrupt Reg. 2 */

unsigned int porta, portb, portc, cnfg, ireg1, ireg2;
char valread;              /* Variable to store data read from a port */

/*  Calculate register addresses */

porta = BASE_ADDRESS + APORTAoffset;
portb = BASE_ADDRESS + APORTBoffset;
portc = BASE_ADDRESS + APORTCoffset;
cnfg  = BASE_ADDRESS + ACNFGoffset;
ireg1 = BASE_ADDRESS + IREG1offset;
ireg2 = BASE_ADDRESS + IREG2offset;

/* EXAMPLE 1–Set up interrupts for mode 1 input for port A. Enable the
   appropriate interrupt bits. */

outp(cnfg,0xB0);           /* Port A is an input in mode 1. */
outp(cnfg,0x09);           /* Set PC4 to enable interrupts from 82C55A. */
outp(ireg1,0x01);          /* Set AIRQ0 to enable PPI A, port A interrupts. */
outp(ireg2,0x04);          /* Set INTEN bit. */

/* EXAMPLE 2–Set up interrupts for mode 1 input for port B. Enable the
   appropriate interrupt bits. */

outp(cnfg,0x86);           /* Port B is an input in mode 1. */
outp(cnfg,0x05);           /* Set PC2 to enable interrupts from 82C55A. */
outp(ireg1,0x02);          /* Set AIRQ1 to enable PPI A, port B interrupts. */
outp(ireg2,0x04);          /* Set INTEN bit. */

/* EXAMPLE 3–Set up interrupts for mode 1 output for port A. Enable the
   appropriate interrupt bits. */

outp(cnfg,0xA0);           /* Port A is an output in mode 1. */
outp(cnfg,0x0D);           /* Set PC6 to enable interrupts from 82C55A. */
outp(ireg1,0x01);          /* Set AIRQ0 to enable PPI A, port A interrupts. */
outp(ireg2,0x04);          /* Set INTEN bit. */

/* EXAMPLE 4–Set up interrupts for mode 1 output for port B. Enable the
                              appropriate interrupt bits. */

outp(cnfg,0x84);           /* Port B is an output in mode 1. */
outp(cnfg,0x05);           /* Set PC2 to enable interrupts from 82C55A. */
outp(ireg1,0x02);          /* Set AIRQ1 to enable PPI A, port B interrupts. */
outp(ireg2,0x04);          /* Set INTEN bit. */
```

```
/* EXAMPLE 5–Set up interrupts for mode 2 output transfers. Enable the
   appropriate interrupt bits. */
outp(cnfg,0xC0);          /* Mode 2 output. */
outp(cnfg,0x0D);          /* Set PC6 to enable interrupts from 82C55A. */
outp(ireg1,0x01);         /* Set AIRQ0 to enable PPI A, port A interrupts. */
outp(ireg2,0x04);         /* Set INTEN bit. */
/* EXAMPLE 6–Set up interrupts for mode 2 input transfers. Enable the
   appropriate interrupt bits. */
outp(cnfg,0xD0);          /* Mode 2 input. */
outp(cnfg,0x09);          /* Set PC4 to enable interrupts from 82C55A. */
outp(ireg1,0x01);         /* Set AIRQ0 to enable PPI A, port A interrupts. */
outp(ireg2,0x04);         /* Set INTEN bit. */
}
```

Programming Considerations for the 82C53

A general overview of the 82C53 and how it is configured on the PC-DIO-96/PnP are presented as follows. This section also includes an in-depth example of handling interrupts generated by the 82C53.

General Information

The 82C53 contains three counter/timers, each of which can operate in one of six different modes. As the PC-DIO-96/PnP is designed, however, only counter 0 and counter 1 are configured for operation; counter 2 is not connected, nor is it available on the external I/O connector. In addition, counter 0 and counter 1 are wired to the interrupt circuitry in such a way that only four of the modes are available for use.

The source for counter 0 is a 2 MHz clock. If counter 0 is used for interrupting the host computer, configure the counter for rate generation, or mode 2. If counter 1 is used for interrupting the host computer, counter 0 is used as a frequency scaler which feeds the source input for counter 1. In this case, configure both counters for rate generation, or mode 2. To determine the time between pulses generated by counter 0, multiply the load value by 500 ns (1/(2 MHz)). To determine the time between pulses generated by counter 1, multiply the load value by the time between pulses of counter 0. A sample configuration procedure is presented in the next section.

Interrupt Programming Example for the 82C53

An in-depth example of handling interrupts generated by the 82C53 is presented as follows. The main program is presented in C, while sample interrupt routines are presented in assembly language.

```
Main() {

#define BASE_ADDRESS       0x180        /* Board located at address 180 */
#define CTR0offset         0x10         /* Offset for counter 0 */
#define CTR1offset         0x11         /* Offset for counter 1 */
#define CTRCNFGoffset      0x13         /* Offset for 82C53 CNFG   */
#define IREG1offset        0x14         /* Offset for Interrupt Reg. 1 */
#define IREG2offset        0x15         /* Offset for Interrupt Reg. 2 */

#define channel            5            /* Interrupt channel selected */

#define use_ctr1           0            /* 0 for ctr0, 1 for ctr1 */
#define ctr0_data          10000        /* Pulse every 5 msec */
#define ctr1_data          1000         /* Pulse every 5 sec */

unsigned int ctr0, ctr1, cnfg, ireg1, ireg2;

/*  Calculate register addresses */

ctr0  = BASE_ADDRESS + CTR0offset;
ctr1  = BASE_ADDRESS + CTR1offset;
cnfg  = BASE_ADDRESS + CTRCNFGoffset;
ireg1 = BASE_ADDRESS + IREG1offset;
ireg2 = BASE_ADDRESS + IREG2offset;

/* Disable interrupts */

outp(ireg1,0x00);          /* Disable all 82C55A interrupts */
outp(ireg2,0x00);          /* Disable counter interrupts */

/* Set up the counter modes--do not write out the counter load values at this
   time, as this starts the counter. */

outp(cnfg,0x34);           /* Set counter 0 to mode 2 */
if (use_ctr1) {
  outp(cnfg,0x74);         /* Set counter 1 to mode 2 */
  outp(ireg2,0x07);        /* Enable interrupts, enable counter interrupts,
                              and select counter 1's output */
  }
  else outp(ireg2, 0x06);  /* Enable interrupts, enable counter interrupts,
                              and select counter 0's output */

/* At this point, you should install your interrupt service routine using the
   interrupt channel selected. */

/* install_isr(channel,...); */
```

```
/* Now write out the counter load values for the selected counters. */

if (use_ctr1) {
  outp(ctr1, ((unsigned char) (ctr1_data & 0x00ff)));
                          /* Send the least significant byte of the counter
                             data for counter 1 */
  outp(ctr1, ((unsigned char) ((ctr1_data & 0xff00) >> 8)));
                          /* Send the most significant byte of the counter
                             data for counter 1 */
  }
outp(ctr0, ((unsigned char) (ctr0_data & 0x00ff)));
                          /* Send the least significant byte of the counter
                             data for counter 0 */
outp(ctr0, ((unsigned char) ((ctr0_data & 0xff00) >> 8)));
                          /* Send the most significant byte of the counter
                             data for counter 0 */

/* As soon as the last byte is written to counter 0, the counter begins
   counting, and the PC-DIO-96/PnP starts to interrupt the host computer. At
   this point, you can run other code.... */

/* call_foreground_code(...); */

/* When you are ready to exit your program, you should deactivate the counters
   and interrupts as shown below. */

if (use_ctr1) outp(cnfg,0x70);       /* Turn off counter 1 */
outp(cnfg,0x30);                     /* Turn off counter 0 */
outp(ireg2,0x00);                    /* Disable PC-DIO-96/PnP interrupts */

/* After you have deactivated interrupts, you must remove your interrupt
   service routine before exiting your program--do this now. */

/* remove_isr(); */
```

Sample code for the functions `install_isr()` and `remove_isr()` is presented as follows. Be sure to pass a 32-bit structure pointer to the `install_isr()` function, because the main program's data will probably be stored in a different memory segment than the one where the interrupt functions are located. In addition, if you call the installation function from a language besides C, make sure the parameters are passed in the proper order. C pushes parameters on the stack from right to left, but most other languages, most notably Pascal, push parameters from left to right. Finally, be sure to make the calls to the functions using 32-bit addresses, because all of the code assumes data is offset with respect to a 32-bit return address. The code can be modified to use 16-bit addresses by changing far to near and

decrementing all references to the base page register, bp, by two in install_isr() and remove_isr() only. *Do not* modify isr_handler().

```
; assemble this file with the following command:
;   masm /MX filename;
;   /MX preserves case sensitivity
;
;
; function prototypes:
;
;   void    install_isr(int level, isr_block_type far * isr_block);
;
;       on input, level indicates the interrupt level that is to be modified
;       on input, isr_block points to the data structure that will be used by
;           the isr_handler function
;
;   void    isr_handler(void);
;
;      the isr_handler() function will never be called from C.....
;
;   void    remove_isr(void);
;

public _install_isr, _isr_handler, _remove_isr

_DATA   segment word public 'DATA'

; declarations

ackm        equ     00020h
acks        equ     000a0h
eoi         equ     00020h
maskm       equ     00021h
masks       equ     000a1h

int_addr    dd      0
int_mask    dw      0
isrb_addr   dd      0
slave_ack   db      0
vect_num    db      0

_DATA       ends
```

```
_TEXT   segment word public 'CODE'
        assume cs:_TEXT, ss:_TEXT, ds:_DATA

; install_isr
;
; bp reg            at [bp+0]
; ret addr ofs      at [bp+2]
; ret addr seg      at [bp+4]
; level             at [bp+6]
; isr_block ofs     at [bp+8]
; isr_block seg     at [bp+10]
;

_install_isr        proc    far
             cli
             push    bp
             mov     bp,sp
             push    ax
             push    bx
             push    cx
             push    dx
             push    ds
             push    es
             mov     ax,seg _DATA
             mov     ds,ax


; save the pointer for the isr_block structure--used in isr_handler
             mov     ax,[bp+8]                  ; Get ofs into ax
             mov     word ptr isrb_addr[0],ax   ; Save address in variable
             mov     ax,[bp+10]                 ; Get seg into ax
             mov     word ptr isrb_addr[2],ax   ; Save address in variable


; set interrupt vector--save the current vector before writing out new one

             mov     ax,[bp+6]        ; Get interrupt level
             cmp     al,7             ; Check to see if it belongs to master
             ja      short slave      ;   or slave interrupt chip
             add     al,008h          ; Offset for master vector list
             jmp     short setvec     ; Go set the vector
```

```
slave:
            add     al,068h         ; Offset for slave vector list
            mov     slave_ack,1     ; Flag for slave channel
setvec:
            push    ax              ; Save vector number for later
            mov     ah,35h          ; Get current vector
            int     21h             ; Get previous int_addr in es:bx
            pop     ax              ; Restore vector number
            mov     cx,cs           ; Prep to compare current/new vectors
            mov     dx,es
            cmp     dx,cx           ; See if vector is already there
            jne     short ii_0
            cmp     bx,offset _isr_handler
            je      short ii_exit   ; Vector already installed--exit
ii_0:
            mov     vect_num,al     ; Save vector number for remove_isr
            mov     word ptr int_addr[0],bx ; Save the address
            mov     word ptr int_addr[2],es
            push    ds              ; Save the data segment
            mov     ds,cx           ; Copy cx (== cs) into ds
            mov     dx,offset _isr_handler   ; ds:dx points to new handler
            mov     ah,25h
            int     21h             ; Install the handler in the system
            pop     ds


; mask interrupt level in the interrupt controller register and store
;   the original setting of the mask bit for the selected interrupt level

            mov     cx,[bp+6]       ; Get interrupt level
            mov     bx,1            ; Generate some masks
            shl     bx,cl
            mov     cx,bx           ; cx has 1 in bit pos of int-level
            not     bx              ; bx has 0 in bit pos of int-level
            in      al,maskm        ; Get mask data from master chip
            jmp     $+2             ; Delay--wait for data transfer
            and     cl,al           ; Determine setting of mask bit
            and     al,bl           ; Enable interrupts for selected level
            out     maskm,al
            jmp     $+2             ; Delay--wait for data transfer
            in      al,masks        ; Get mask data from slave chip
            jmp     $+2             ; Delay--wait for data transfer
            and     ch,al           ; Determine setting of mask bit
```

```
            and     al,bh           ; Enable interrupts for selected level
            out     masks,al
            mov     int_mask,cx     ; Save the previous value of the mask

; restore saved registers

ii_exit:
            pop     es
            pop     ds
            pop     dx
            pop     cx
            pop     bx
            pop     ax
            pop     bp
            sti
            ret
_install_isr        endp



; remove_isr
;
; bp reg            at [bp+0]
; ret addr ofs      at [bp+2]
; ret addr seg      at [bp+4]
;

_remove_isr  proc    far
            cli
            push    ax
            push    bx
            push    cx
            push    dx
            push    ds
            push    es
            mov     ax,seg _DATA
            mov     ds,ax
```

```
; see if our vector is installed--if not, do not remove the vector

            cmp     vect_num,0      ; See if vect_num was ever set
            jz      short ri_exit   ; Our vector never installed--exit
            mov     al,vect_num     ; Get vector number
            mov     ah,35h          ; Get current vector from DOS
            int     21h             ; Get previous int_addr in es:bx
            mov     cx,cs           ; Prep to compare old/current vectors
            mov     dx,es
            cmp     dx,cx           ; See if our vector is already there
            jne     short ri_exit   ; Different vector segment--exit
            cmp     bx,offset _isr_handler
            jne     short ri_exit   ; Different vector offset--exit


; restore old mask and vector values
            mov     cx,int_mask     ; Get the old mask value
            in      al,maskm        ; Get current master mask
            jmp     $+2             ; Delay--wait for data transfer
            or      al,cl           ; OR in old mask value
            out     maskm,al        ; Send out new setting
            jmp     $+2             ; Delay--wait for data transfer
            in      al,masks        ; Get current slave mask
            jmp     $+2             ; Delay--wait for data transfer
            or      al,ch           ; OR in old mask value
            out     masks,al        ; Send out new setting
            jmp     $+2             ; Delay--wait for data transfer
            mov     al,vect_num     ; al holds interrupt level
            mov     ah,25h
            lds     dx,int_addr     ; ds:dx points to new handler
            int     21h             ; Install the old vector
```

```
; restore saved registers

ri_exit:
             pop     es
             pop     ds
             pop     dx
             pop     cx
             pop     bx
             pop     ax
             sti
             ret
_remove_isr endp



; isr_handler
;

_isr_handler proc    far
             cli
             push    ax
             push    ds


; service interrupt

             ; Your code here...
             ;    if this was not your interrupt, jump to 'ih_0'
             ;    if this was your interrupt, service it as appropriate;
             ;      the pointer for the data structure 'isr_block' is stored
             ;        at _DATA:isrb_addr; to access the structure, use the
             ;        following steps:
             ;
             ;            mov    ax,seg _DATA
             ;            mov    ds,ax
             ;            lds    si,isrb_addr
             ;
             ;        you need not use ds:si, but be sure to save any
             ;        registers you use...
```

```
; acknowledge the interrupt

ih_0:
            mov     ax,seg _DATA
            mov     ds,ax
            mov     al,eoi              ; Signify end of interrupt
            cmp     slave_ack,0       ; See if we need to acknowledge slave
            je      short ih_1          ; Jump if not
            out     acks,al             ; Send slave acknowledge
            jmp     $+2                 ; Delay--wait for data transfer
ih_1:
            out     ackm,al             ; Send master acknowledge


; restore saved registers

            pop     ds
            pop     ax
            sti
            iret
_isr_handler        endp


_TEXT       ends
            end
```

Interrupt Handling

The INTEN bit of Interrupt Register 2 must be set to enable interrupts from the PC-DIO-96/PnP. This bit must first be cleared to disable unwanted interrupts. After all sources of interrupts have been disabled or placed in an inactive state, you can set INTEN.

To interrupt the host computer using one of the 82C55A devices, program the selected 82C55A for the I/O mode desired. In mode 1, set either the INTEA or the INTEB bit to enable interrupts from port A or port B, respectively. In mode 2, set either INTE1 or INTE2 for interrupts on output or input transfers, respectively. The INTE1 and INTE2 interrupt outputs are cascaded into a single interrupt output for port A. After interrupts have been enabled from the 82C55A, set the appropriate enable bit for the selected 82C55A; for example, if you selected both mode 2 interrupts for PPI C, you would set CIRQ0 in order to interrupt the host computer.

To interrupt the host computer using one of the 82C53 counter outputs, program the counter(s) as described in the section, *Interrupt Programming Example for the 82C53*, of this chapter.

External signals can be used to interrupt the PC-DIO-96/PnP when port A or port B is in mode 0 and the low nibble of port C is configured for input. If port A is in mode 0, use PC3 to generate an interrupt; if port B is in mode 0, use PC0 to generate an interrupt. Once you have configured the selected 82C55A, you must set the corresponding interrupt enable bit in Interrupt Register 1. If you are using PC3, set xIRQ0; if you are using PC0, set xIRQ1. When the external signal becomes logic high, an interrupt request occurs. Although the host computer's interrupt-monitoring circuitry is triggered by the positive-going edge of the interrupt signal, the signal must remain high until the interrupt routine has been entered and interrupts have been masked out. Make sure your external interrupt signal meets these qualifications. To disable the external interrupt, clear the appropriate xIRQy bit or clear the INTEN bit.

Using Your PC-DIO-96 (Non-PnP) Board

Appendix E

This appendix describes the differences between the PC-DIO-96PnP and PC-DIO-96 boards, the PC-DIO-96 board configuration, and the installation of the PC-DIO-96 into your computer. Read this appendix only if you do *not* have the Plug and Play version of the board.

Differences between the PC-DIO-96PnP and the PC-DIO-96

The PC-DIO-96PnP is a Plug and Play upgrade from a legacy board, the PC-DIO-96. *Legacy* refers to the original board with switches and jumpers used to set the addresses. The original legacy board was replaced with a backwards-compatible, revised PC-DIO-96 that has the same functionality as the Plug and Play version (except for the base address and interrupt selection), but differs somewhat from the original board. The following list compares the specifications and functionality of the newer boards with the obsolete legacy board.

Table E-1. Comparison of Characteristics

Functional Changes	Legacy PC-DIO-96	Revised PC-DIO-96	PC-DIO-96PnP
Assembly number	181170B-01	183549*X*-02	183549*X*-01
I/O base address selection	Uses switches	Uses switches	Plug and Play compatible
Interrupt request selection	Uses jumpers	Uses jumpers	Plug and Play compatible
5 V supply fuse	Nonresettable	Self-resetting	Self-resetting
Power-up state	DIO lines pulled HIGH (100 kΩ)	Jumper for pull-up (factory default) or pull-down	Jumper for pull-up (factory default) or pull-down

Configuration and Installation of the PC-DIO-96

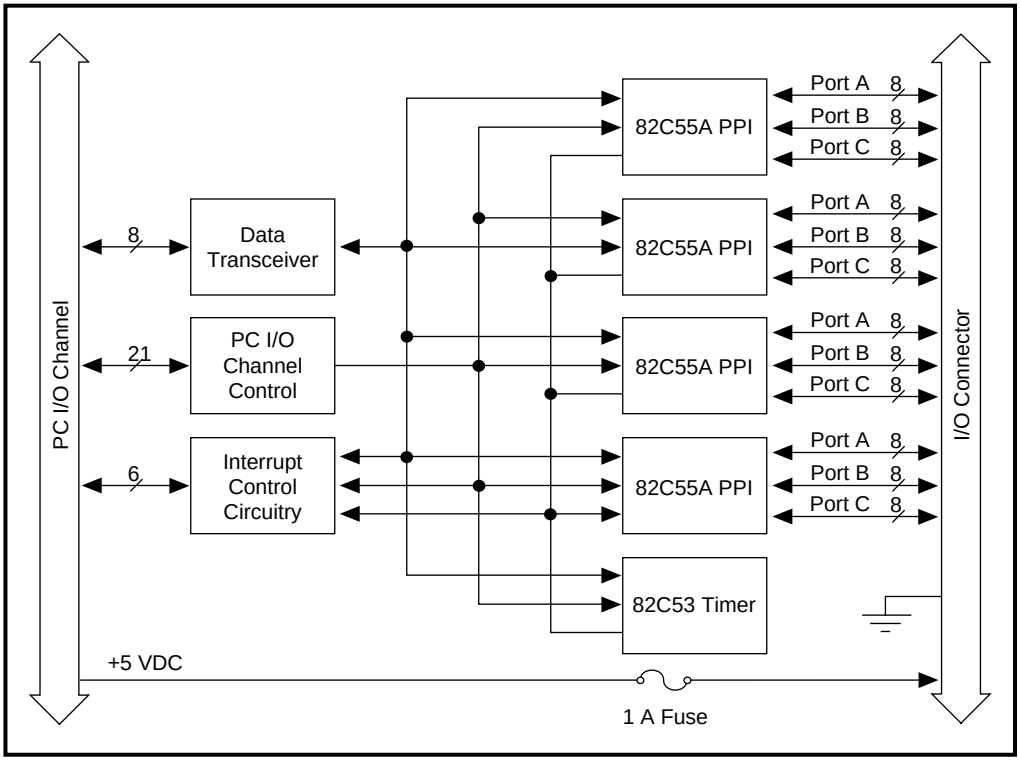
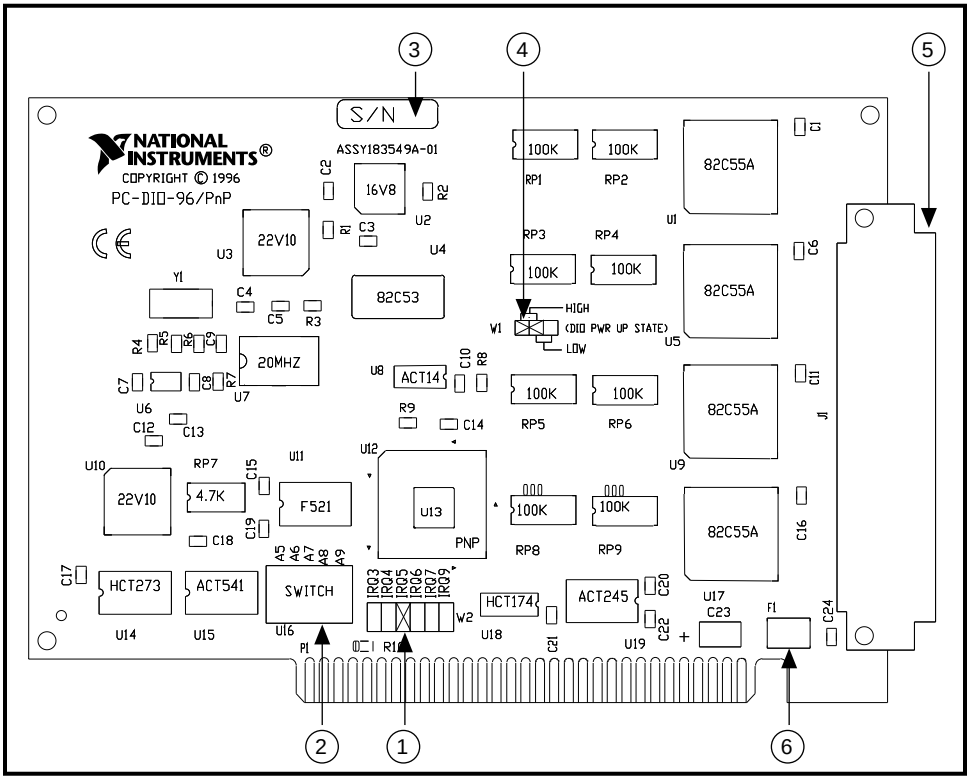


Figure E-1. PC-DIO-96 Block Diagram

The block diagram in Figure E-1 illustrates the key functional components of the PC-DIO-96 board.

Board Configuration

The PC-DIO-96 contains one jumper and one DIP switch to configure the PC bus interface settings. The DIP switch U16 sets the base I/O address. Jumper W2 selects the interrupt level. The DIP switch and jumper are shown in the parts locator diagram in Figure E-2.

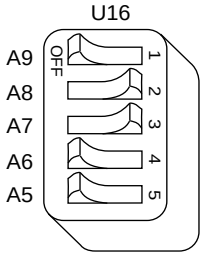


1	W2	3	Serial Number	5	J1
2	U16	4	W1	6	F1

Figure E-2. PC-DIO-96 Parts Locator Diagram

The PC-DIO-96 is configured at the factory to a base I/O address of hex 180 and to interrupt level 5. These settings (shown in Table E-2) are suitable for most systems. However, if your system has other hardware at this base I/O address or interrupt level, you need to change these settings on the PC-DIO-96 (as instructed on the following pages) or on the other hardware. Record your settings in the *PC-DIO-96/PnP Hardware and Software Configuration Form* in Appendix F, *Customer Communication*.

Table E-2. PC-DIO-96 Factory-Set Switch and Jumper Settings

PC-DIO-96 Board	Default Settings	Hardware Implementation
Base I/O Address	Hex 180 (factory setting)	
Interrupt Level	Interrupt level 5 selected (factory setting)	**W2:** Row 5

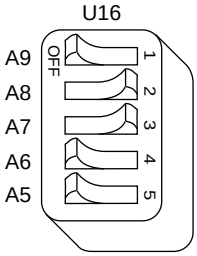
Base I/O Address Selection

An onboard switch setting determines the board base address. The address on the PC I/O channel bus is monitored by the address decoder, which is part of the I/O channel control circuitry. If the address on the bus matches the selected I/O base address of the board, the board is enabled and the corresponding register on the PC-DIO-96 is accessed.

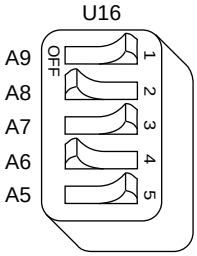
The base I/O address for the PC-DIO-96 is determined by the switches at position U16 (see Figure E-2). The switches are set at the factory for the I/O address hex 180. With this default setting, the PC-DIO-96 uses the I/O address space hex 180 through 19F.

☞ **Note:** ***Verify that this space is not already used by other equipment installed in your computer. If any equipment in your computer uses this I/O address space, you must change the base I/O address for the PC-DIO-96 or for the other device.***

Each switch in U16 corresponds to one of the address lines A9 through A5. Thus, the range for possible base I/O address settings is hex 000 through 3E0. Base I/O address values hex 000 through 0FF are reserved for system use. Base I/O values hex 100 through 3FF are available on the I/O channel. A4, A3, A2, A1, and A0 are used by the PC-DIO-96 to decode accesses to the onboard registers. On the U16 DIP switch, press the side marked OFF to select a binary value of 1 for the corresponding address bit. Press the other side of the switch to select a binary value of 0 for the corresponding address bit. Figure E-3 shows two possible switch settings. The black side indicates the side of the switch that is pushed down.



Switches Set to Default Setting (Base I/O Address Hex 180)



Switches Set to Base I/O Address Hex 2A0

Figure E-3. Example Base I/O Address Switch Settings

Table E-3 shows all possible switch settings and their corresponding address ranges.

Table E-3. Switch Settings with Corresponding Base I/O Address and Base I/O Address Space

Switch Setting					Base I/O Address (hex)	Base I/O Address Space Used (hex)
A9	A8	A7	A6	A5		
0	0	0	0	0	000	000–01F
0	0	0	0	1	020	020–03F
0	0	0	1	0	040	040–05F
0	0	0	1	1	060	060–07F
0	0	1	0	0	080	080–09F
0	0	1	0	1	0A0	0A0–0BF
0	0	1	1	0	0C0	0C0–0DF
0	0	1	1	1	0E0	0E0–0FF
0	1	0	0	0	100	100–11F
0	1	0	0	1	120	120–13F
0	1	0	1	0	140	140–15F
0	1	0	1	1	160	160–17F
0	1	1	0	0	180	180–19F
0	1	1	0	1	1A0	1A0–1BF
0	1	1	1	0	1C0	1C0–1DF
0	1	1	1	1	1E0	1E0–1FF
1	0	0	0	0	200	200–21F
1	0	0	0	1	220	220–23F
1	0	0	1	0	240	240–25F
1	0	0	1	1	260	260–27F
1	0	1	0	0	280	280–29F
1	0	1	0	1	2A0	2A0–2BF
1	0	1	1	0	2C0	2C0–2DF
1	0	1	1	1	2E0	2E0–2FF
1	1	0	0	0	300	300–31F

Table E-3. Switch Settings with Corresponding Base I/O Address and Base I/O Address Space (Continued)

Switch Setting					Base I/O Address (hex)	Base I/O Address Space Used (hex)
A9	A8	A7	A6	A5		
1	1	0	0	1	320	320–33F
1	1	0	1	0	340	340–35F
1	1	0	1	1	360	360–37F
1	1	1	0	0	380	380–39F
1	1	1	0	1	3A0	3A0–3BF
1	1	1	1	0	3C0	3C0–3DF
1	1	1	1	1	3E0	3E0–3FF
Note: ***Base I/O address values 000 through 0FF hex are reserved for system use. Base I/O address values 100 through 3FF hex are available on the I/O channel.***						

Interrupt Selection

There is one set of jumpers for interrupt selection on the PC-DIO-96 board. Use W2 for selecting the interrupt level. The location of this jumper is shown in Figure E-2.

The PC-DIO-96 board can connect to any one of six interrupt lines of the PC I/O Channel: IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, or IRQ9. Select the interrupt line by setting a jumper on W2. The default interrupt line is IRQ5. To change to another line, remove the jumper from IRQ5 and place it on the pins for another request line. Figure E-4 shows the default factory setting for IRQ5.

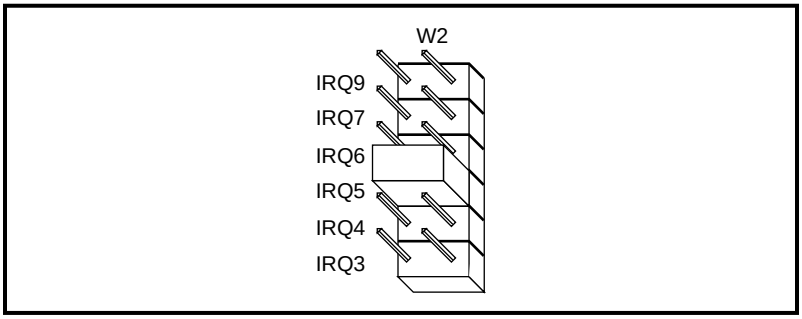


Figure E-4. Interrupt Jumper Setting for IRQ5 (Default Setting)

The PC-DIO-96 can share interrupt lines with other devices because it uses a tri-state driver to drive its selected interrupt line. For information on how to disable this driver, see Appendix D, *Register-Level Programming*.

Installation

You can install the PC-DIO-96 in any unused 8-bit, 16-bit, or 32-bit expansion slot in your computer. To optimize the board's noise performance, install the board away from the video card and leave a slot vacant on each side of the PC-DIO-96, if possible. After you make any necessary changes and verify the switch and jumper settings, record them using the *PC-DIO-96/PnP Hardware and Software Configuration Form* in Appendix F, *Customer Communication*. You are now ready to install the PC-DIO-96.

The following are general installation instructions, but consult your computer's user manual or technical reference manual for specific instructions and warnings. If you want to install this board in an EISA-class computer, you can obtain a configuration file for the board by contacting National Instruments.

1. Turn off your computer.
2. Remove the top cover or access port to the I/O channel.
3. Remove the expansion slot cover on the back panel of the computer.
4. Insert the PC-DIO-96 in an unused 8-bit, 16-bit, or 32-bit slot. It may be a tight fit, but *do not* force the board into place.
5. Screw the mounting bracket of the PC-DIO-96 to the back panel rail of the computer.

6. Visually verify the installation.
7. Replace the cover to the computer.

☞ **Note:** ***If you have an ISA-class computer and you are using a configurable software package, such as NI-DAQ, you may need to reconfigure your software to reflect any changes in jumper or switch settings. If you have an EISA-class computer, you need to update the computer's resource allocation (or configuration) table by reconfiguring your computer. See your computer's user manual for information about updating the configuration table.***

The PC-DIO-96 board is now installed and ready for operation.

Customer Communication

Appendix F

For your convenience, this appendix contains forms to help you gather the information necessary to help us solve your technical problems and a form you can use to comment on the product documentation. When you contact us, we need the information on the Technical Support Form and the configuration form, if your manual contains one, about your system configuration to answer your questions as quickly as possible.

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Up to 14,400 baud, 8 data bits, 1 stop bit, no parity

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Canada (Quebec)	514 694 8521	514 694 4399
Denmark	45 76 26 00	45 76 26 02
Finland	90 527 2321	90 502 2930
France	01 48 14 24 24	01 48 14 24 14
Germany	089 741 31 30	089 714 60 35
Hong Kong	2645 3186	2686 8505
Israel	03 5734815	03 5734816
Italy	02 413091	02 41309215
Japan	03 5472 2970	03 5472 2977
Korea	02 596 7456	02 596 7455
Mexico	95 800 010 0793	5 520 3282
Netherlands	0348 433466	0348 430673
Norway	32 84 84 00	32 84 86 00
Singapore	2265886	2265887
Spain	91 640 0085	91 640 0533
Sweden	08 730 49 70	08 730 43 70
Switzerland	056 200 51 51	056 200 51 55
Taiwan	02 377 1200	02 737 4644
U.K.	01635 523545	01635 523154

Technical Support Form

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If you are using any National Instruments hardware or software products related to this problem, include the configuration forms from their user manuals. Include additional pages if necessary.

Name _____

Company _____

Address _____

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Fax (___)_____ Phone (___) _____

Computer brand _____ Model _____ Processor _____

Operating system (include version number)_____

Clock speed _____ MHz RAM _____ MB Display adapter _____

Mouse ___yes ___no Other adapters installed _____

Hard disk capacity _____ MB Brand _____

Instruments used _____

_____

National Instruments hardware product model_____ Revision_____

Configuration _____

National Instruments software product_____ Version_____

Configuration _____

The problem is: _____

_____

_____

_____

_____

_____

List any error messages: _____

_____

_____

The following steps reproduce the problem: _____

_____

_____

_____

_____

PC-DIO-96/PnP Hardware and Software Configuration Form

Record the settings and revisions of your hardware and software on the line to the right of each item. Also fill out the hardware and software configuration forms for all modules in the chassis, all relevant DAQ boards, and all other chassis in the application. By completing these forms accurately, our applications engineers will be able to answer your questions efficiently.

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Please comment on the completeness, clarity, and organization of the manual.

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Glossary

Prefix	Meaning	Value
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}

°	degrees
Ω	ohms
%	percent
+5 V	+5 volt signal
A	amperes
ACK*	acknowledge input signal
AIRQ0	PPI A interrupt request bit for Port A
AIRQ1	PPI A interrupt request bit for Port B
APA	bidirectional data lines for Port A of PPI A
APB	bidirectional data lines for Port B of PPI A
APC	bidirectional data lines for Port B of PPI A
BCD	binary-coded decimal
BIRQ0	PPI B interrupt request bit for Port A
BIRQ1	PPI B interrupt request bit for Port B

BPA	bidirectional data lines for Port A of PPI B
BPB	bidirectional data lines for Port B of PPI B
BPC	bidirectional data lines for Port C of PPI B
C	Celsius
CIRQ0	PPI C interrupt request bit for Port A
CIRQ1	PPI C interrupt request bit for Port B
CMOS	complementary metal-oxide semiconductor
CPA	bidirectional data lines for Port A of PPI C
CPB	bidirectional data lines for Port B of PPI C
CPC	bidirectional data lines for Port C of PPI C
CTR1	counter 1 enable bit
CTRIRQ	counter interrupt enable bit
DATA	data lines at the specified port signal
DIO	digital input/output
DIRQ0	PPI D interrupt request bit for Port A
DIRQ1	PPI D interrupt request bit for Port B
DMA	direct memory access
DPA	bidirectional data lines for Port A of PPI D
DPB	bidirectional data lines for Port B of PPI D
DPC	bidirectional data lines for Port C of PPI D
EISA	Extended Industry Standard Architecture
GND	ground
hex	hexadecimal
Hz	hertz
IBF	input buffer full signal
IBFA	input buffer bit for Port A

IBFB	input buffer bit for Port B
in.	inches
INTE1	interrupt enable bit for Port A output interrupts
INTE2	interrupt enable bit for Port A input interrupts
INTEA	interrupt enable bit for Port A
INTEB	interrupt enable bit for Port B
INTEN	global interrupt enable bit
INTR	interrupt request signal
INTRA	interrupt request status bit for Port A
INTRB	interrupt request status bit for Port B
I/O	input/output or input/output bit
I_{out}	output current
ISA	Industry Standard Architecture
kbytes	1,024 bytes
LSB	least significant bit
m	meters
MB	megabytes of memory
MSB	most significant bit
OBF*	output buffer full signal
OBFA*	output buffer bit for Port A
OBFB*	output buffer bit for Port B
PnP	Plug and Play
PPI	programmable peripheral interface
RD*	read signal
R_{EXT}	external resistance
R_L	load resistance

RTSI	Real-Time System Integration
s	seconds
SCXI	Signal Conditioning eXtensions for Instrumentation
STB	strobe input signal
TTL	transistor-to-transistor logic
V	volts
VDC	volts direct current
V_{EXT}	external volt
V_{in}	volts in
V_{OH}	volts, output high
V_{OL}	volts, output low
WR*	write signal

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