DAQ

AT E Series User Manual

Multifunction I/O Boards for the PC AT

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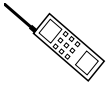

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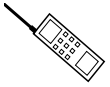

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This manual describes the electrical and mechanical aspects of each board in the AT E Series product line and contains information concerning their operation and programming. Unless otherwise noted, text applies to all boards in the AT E Series.

The AT E Series includes the following boards:

- AT-MIO-16E-1
- AT-MIO-16E-2
- AT-MIO-64E-3
- AT-MIO-16E-10
- AT-MIO-16DE-10
- AT-MIO-16XE-10
- AT-AI-16XE-10
- AT-MIO-16XE-50

The AT E Series boards are high-performance multifunction analog, digital, and timing I/O boards for the PC AT series computers. Supported functions include analog input, analog output, digital I/O, and timing I/O.

Organization of This Manual

The *AT-MIO/AI E Series User Manual* is organized as follows:

- Chapter 1, *Introduction*, describes the AT E Series boards, lists what you need to get started, describes the optional software and optional equipment, and explains how to unpack your AT E Series board.
- Chapter 2, *Installation and Configuration*, explains how to install and configure your AT E Series board.
- Chapter 3, *Hardware Overview*, presents an overview of the hardware functions on your AT E Series board.

- Chapter 4, *Signal Connections*, describes how to make input and output signal connections to your AT E Series board via the board I/O connector.
- Chapter 5, *Calibration*, discusses the calibration procedures for your AT E Series board.
- Appendix A, *Specifications*, lists the specifications of each board in the AT E Series.
- Appendix B, *Optional Cable Connector Descriptions*, describes the connectors on the optional cables for the AT E Series boards.
- Appendix C, *Common Questions*, contains a list of commonly asked questions and their answers relating to usage and special features of your AT E Series board.
- Appendix D, *Customer Communication*, contains forms you can use to request help from National Instruments or to comment on our products.
- The *Glossary* contains an alphabetical list and description of terms used in this manual, including acronyms, abbreviations, metric prefixes, mnemonics, and symbols.
- The *Index* alphabetically lists topics covered in this manual, including the page where you can find the topic.

Conventions Used in This Manual

The following conventions are used in this manual.

This icon to the left of bold italicized text denotes a note, which alerts you to important information.

This icon to the left of bold italicized text denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash.

bold Bold text denotes parameters.

bold italic Bold italic text denotes a note, caution, or warning.

italic Italic text denotes emphasis on a specific board in the AT E Series or on other important information, a cross reference, or an introduction to a key concept. This font also denotes text from which you supply the appropriate word or value, as in Windows 3.*x*.

NI-DAQ	NI-DAQ refers to the NI-DAQ software for PC compatibles unless otherwise noted.
PC	PC refers to the PC AT series computers.
SCXI	SCXI stands for Signal Conditioning eXtensions for Instrumentation and is a National Instruments product line designed to perform front-end signal conditioning for National Instruments plug-in DAQ boards.
♦	The ♦ indicates that the text following it applies only to specific AT E Series boards.
<>	Angle brackets containing numbers separated by an ellipsis represent a range of values associated with a bit, port, or signal name (for example, ACH<0..7> stands for ACH0 through ACH7).
	The *Glossary* lists abbreviations, acronyms, metric prefixes, mnemonics, symbols, and terms.

National Instruments Documentation

The *AT-MIO/AI E Series User Manual* is one piece of the documentation set for your DAQ system. You could have any of several types of manuals depending on the hardware and software in your system. Use the manuals you have as follows:

- *Getting Started with SCXI*—If you are using SCXI, this is the first manual you should read. It gives an overview of the SCXI system and contains the most commonly needed information for the modules, chassis, and software.
- Your SCXI hardware user manuals—If you are using SCXI, read these manuals next for detailed information about signal connections and module configuration. They also explain in greater detail how the module works and contain application hints.
- Your DAQ hardware user manuals—These manuals have detailed information about the DAQ hardware that plugs into or is connected to your computer. Use these manuals for hardware installation and configuration instructions, specification information about your DAQ hardware, and application hints.
- Software documentation—Examples of software documentation you may have are the LabVIEW and LabWindows™/CVI documentation sets and the NI-DAQ documentation. After you set

up your hardware system, use either the application software (LabVIEW or LabWindows/CVI) or the NI-DAQ documentation to help you write your application. If you have a large and complicated system, it is worthwhile to look through the software documentation before you configure your hardware.

- Accessory installation guides or manuals—If you are using accessory products, read the terminal block and cable assembly installation guides. They explain how to physically connect the relevant pieces of the system. Consult these guides when you are making your connections.
- *SCXI Chassis Manual*—If you are using SCXI, read this manual for maintenance information on the chassis and installation instructions.

Related Documentation

The following documents contain information you may find helpful:

- Application Note 025, *Field Wiring and Noise Considerations for Analog Signals*
- *DAQ-STC Technical Reference Manual*

Customer Communication

National Instruments wants to receive your comments on our products and manuals. We are interested in the applications you develop with our products, and we want to help if you have problems with them. To make it easy for you to contact us, this manual contains comment and configuration forms for you to complete. These forms are in Appendix D, *Customer Communication*, at the end of this manual.

Chapter 1

Introduction

This chapter describes the AT E Series boards, lists what you need to get started, describes the optional software and optional equipment, and explains how to unpack your AT E Series board.

About the AT E Series

Thank you for buying a National Instruments AT E Series board. The AT E Series boards are the first completely Plug and Play-compatible multifunction analog, digital, and timing I/O boards for the PC AT and compatible computers. This family of boards features 12-bit and 16-bit ADCs with 16 and 64 analog inputs, 12-bit and 16-bit DACs with voltage outputs, eight and 32 lines of TTL-compatible digital I/O, and two 24-bit counter/timers for timing I/O. Because the AT E Series boards have no DIP switches, jumpers, or potentiometers, they are easily configured and calibrated using software.

The AT E Series boards are the first completely switchless and jumperless data acquisition boards. This feature is made possible by the National Instruments DAQ-PnP bus interface chip that connects the board to the AT I/O bus. The DAQ-PnP implements the Plug and Play ISA Specification so that the DMA, interrupts, and base I/O addresses are all software configurable. This allows you to easily change the AT E Series board configuration without having to remove the board from your computer. The DAQ-STC makes possible such applications as buffered pulse generation, equivalent time sampling, and seamlessly changing the sampling rate.

The AT E Series boards use the National Instruments DAQ-STC system timing controller for time-related functions. The DAQ-STC consists of three timing groups that control analog input, analog output, and general-purpose counter/timer functions. These groups include a total of seven 24-bit and three 16-bit counters and a maximum timing resolution of 50 ns.

A common problem with DAQ boards is that you cannot easily synchronize several measurement functions to a common trigger or

timing event. The AT E Series boards have the Real-Time System Integration (RTSI) bus to solve this problem. The RTSI bus consists of our RTSI bus interface and a ribbon cable to route timing and trigger signals between several functions on as many as five DAQ boards in your PC.

The AT E Series boards can interface to an SCXI system so that you can acquire over 3,000 analog signals from thermocouples, RTDs, strain gauges, voltage sources, and current sources. You can also acquire or generate digital signals for communication and control. SCXI is the instrumentation front end for plug-in DAQ boards.

Detailed specifications of the AT E Series boards are in Appendix A, *Specifications*.

What You Need to Get Started

To set up and use your AT E Series board, you will need the following:

- ❑ One of the following boards:
  - AT-MIO-16E-1
  - AT-MIO-16E-2
  - AT-MIO-64E-3
  - AT-MIO-16E-10
  - AT-MIO-16DE-10
  - AT-MIO-16XE-10
  - AT-AI-16XE-10
  - AT-MIO-16XE-50
- ❑ *AT E Series User Manual*
- ❑ One of the following software packages and documentation
  - BridgeVIEW
  - ComponentWorks
  - LabVIEW for Windows
  - LabWindows/CVI for Windows
  - LookOut
  - Measure
  - NI-DAQ for PC Compatibles
  - VirtualBench
- ❑ Your computer

Software Programming Choices

There are several options to choose from when programming your National Instruments DAQ and SCXI hardware. You can use National Instruments application software, NI-DAQ, or register-level programming.

National Instruments Application Software

ComponentWorks contains tools for data acquisition and instrument control built on NI-DAQ driver software. ComponentWorks provides a higher-level programming interface for building virtual instruments through standard OLE controls and DLLs. With ComponentWorks, you can use all of the configuration tools, resource management utilities, and interactive control utilities included with NI-DAQ.

LabVIEW features interactive graphics, a state-of-the-art user interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of VIs for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW. The LabVIEW Data Acquisition VI Library is functionally equivalent to NI-DAQ software.

LabWindows/CVI features interactive graphics, state-of-the-art user interface, and uses the ANSI standard C programming language. The LabWindows/CVI Data Acquisition Library, a series of functions for using LabWindows/CVI with National Instruments DAQ hardware, is included with the NI-DAQ software kit. The LabWindows/CVI Data Acquisition Library is functionally equivalent to the NI-DAQ software.

VirtualBench features virtual instruments that combine DAQ products, software, and your computer to create a stand-alone instrument with the added benefit of the processing, display, and storage capabilities of your computer. VirtualBench instruments load and save waveform data to disk in the same forms that can be used in popular spreadsheet programs and word processors.

Using ComponentWorks, LabVIEW, LabWindows/CVI, or VirtualBench software will greatly reduce the development time for your data acquisition and control application.

NI-DAQ Driver Software

The NI-DAQ driver software is included at no charge with all National Instruments DAQ hardware. NI-DAQ is not packaged with signal conditioning or accessory products. NI-DAQ has an extensive library of functions that you can call from your application programming environment. These functions include routines for analog input (A/D conversion), buffered data acquisition (high-speed A/D conversion), analog output (D/A conversion), waveform generation (timed D/A conversion), digital I/O, counter/timer operations, SCXI, RTSI, calibration, messaging, and acquiring data to extended memory.

NI-DAQ has both high-level DAQ I/O functions for maximum ease of use and low-level DAQ I/O functions for maximum flexibility and performance. Examples of high-level functions are streaming data to disk or acquiring a certain number of data points. An example of a low-level function is writing directly to registers on the DAQ device. NI-DAQ does not sacrifice the performance of National Instruments DAQ devices because it lets multiple devices operate at their peak performance.

NI-DAQ also internally addresses many of the complex issues between the computer and the DAQ hardware such as programming interrupts and DMA controllers. NI-DAQ maintains a consistent software interface among its different versions so that you can change platforms with minimal modifications to your code. Whether you are using conventional programming languages, LabVIEW, or LabWindows/CVI, your application uses the NI-DAQ driver software, as illustrated in Figure 1-1.

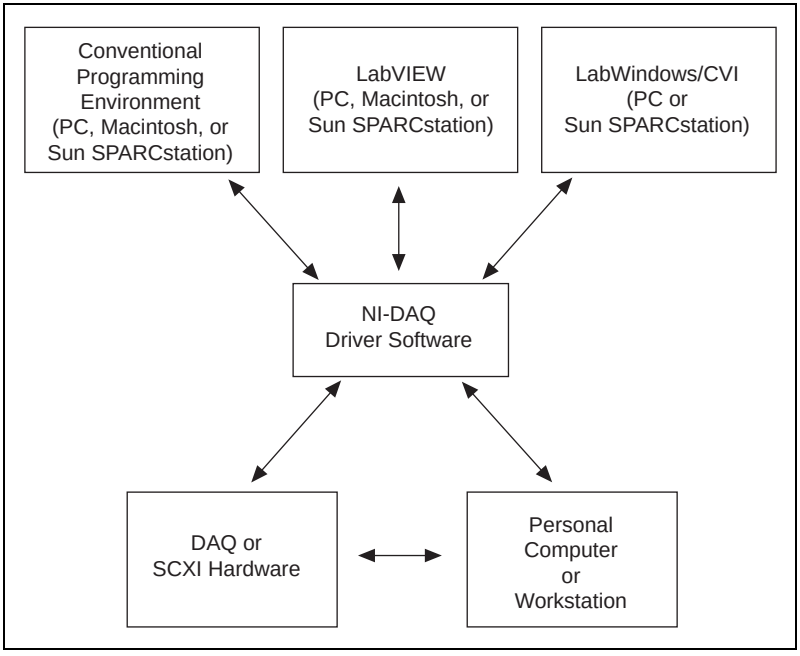


Figure 1-1. The Relationship between the Programming Environment, NI-DAQ, and Your Hardware

You can use your AT E Series board, together with other PC, AT, EISA, DAQCard, and DAQPad Series DAQ and SCXI hardware, with NI-DAQ software for PC compatibles.

Register-Level Programming

The final option for programming any National Instruments DAQ hardware is to write register-level software. Writing register-level programming software can be very time-consuming and inefficient and is not recommended for most users.

Even if you are an experienced register-level programmer, consider using NI-DAQ, LabVIEW, or LabWindows/CVI to program your National Instruments DAQ hardware. Using the NI-DAQ, LabVIEW, or LabWindows/CVI software is as easy and as flexible as register-level programming and can save weeks of development time.

Optional Equipment

National Instruments offers a variety of products to use with your AT E Series board, including cables, connector blocks, and other accessories, as follows:

- Cables and cable assemblies, shielded and ribbon
- Connector blocks, shielded and unshielded 50, 68, and 100-pin screw terminals
- Real Time System Integration (RTSI) bus cables
- Signal condition eXtension for instrumentation (SCXI) modules and accessories for isolating, amplifying, exciting, and multiplexing signals for relays and analog output. With SCXI you can condition and acquire up to 3072 channels.
- Low channel count signal conditioning modules, boards, and accessories, including conditioning for strain gauges and RTDs, simultaneous sample and hold, and relays

For more specific information about these products, refer to your National Instruments catalogue or call the office nearest you.

Custom Cabling

National Instruments offers cables and accessories for you to prototype your application or to use if you frequently change board interconnections.

If you want to develop your own cable, however, the following guidelines may be useful:

- For the analog input signals, shielded twisted-pair wires for each analog input pair yield the best results, assuming that you use differential inputs. Tie the shield for each signal pair to the ground reference at the source.
- You should route the analog lines separately from the digital lines.
- When using a cable shield, use separate shields for the analog and digital halves of the cable. Failure to do so results in noise coupling into the analog signals from transient digital signals.

The following list gives recommended part numbers for connectors that mate to the I/O connector on your AT E Series board.

Mating connectors and a backshell kit for making custom 68-pin cables are available from National Instruments (part number 776832-01).

- AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-16E-10, AT-MIO-16XE-10, AT-AI-16XE-10, and the AT-MIO-16XE-50

  Honda 68-position, solder cup, female connector (part number PCS-E68FS)

  Honda backshell (part number PCS-E68LKPA)

- AT-MIO-64E-3 and AT-MIO-16DE-10

  AMP 100-position IDC male connector (part number 1-750913-9)

  AMP backshell,.50 max O.D. cable (part number 749081-1)

  AMP backshell,.55 max O.D. cable, (part number 749854-1)

Unpacking

Your AT E Series board is shipped in an antistatic package to prevent electrostatic damage to the board. Electrostatic discharge can damage several components on the board. To avoid such damage in handling the board, take the following precautions:

- Ground yourself via a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of your computer chassis before removing the board from the package.
- Remove the board from the package and inspect the board for loose components or any other sign of damage. Notify National Instruments if the board appears damaged in any way. *Do not* install a damaged board into your computer.
- *Never* touch the exposed pins of connectors.

Installation and Configuration

Chapter 2

This chapter explains how to install and configure your AT E Series board.

Software Installation

You may need to install your software before you install your AT E Series board. Refer to the appropriate release notes indicated below for specific instructions on the software installation sequence.

If you are using NI-DAQ, refer to the *NI-DAQ Release Notes*. Find the installation section for your operating system and follow the instructions given there.

If you are using LabVIEW, refer to your LabVIEW release notes. After you have installed LabVIEW, refer to the NI-DAQ release notes and follow the instructions given there for your operating system and LabVIEW.

If you are using LabWindows/CVI, refer to your LabWindows/CVI release notes. After you have installed LabWindows/CVI, refer to your NI-DAQ release notes and follow the instructions given there for your operating system and LabWindows/CVI.

If you are using other National Instruments application software, refer to the appropriate release notes and follow the instructions given there for your operating system and application software.

If you are a register-level programmer, refer to the *AT-MIO E Series Register-Level Programmer Manual* and the *DAQ-STC Technical Reference Manual* for software configuration information.

Hardware Installation

You can install an AT E Series board in any available expansion slot in your PC. However, to achieve best noise performance, you should leave as much room as possible between the AT E Series board and other boards and hardware. The following are general installation instructions, but consult your PC user manual or technical reference manual for specific instructions and warnings.

1. Write down the AT E Series board serial number in the *AT E Series Hardware and Software Configuration Form* in Appendix D, *Customer Communication*, at the back of this manual. You will need this serial number when you install and configure your software.
2. Turn off and unplug your computer.
3. Remove the top cover or access port to the I/O channel.
4. Remove the expansion slot cover on the back panel of the computer.
5. Insert the AT E Series board into an EISA or 16-bit ISA slot. It may be a tight fit, but *do not force* the board into place.
6. Screw the mounting bracket of the AT E Series board to the back panel rail of the computer.
7. Check the installation.
8. Replace the cover.
9. Plug in and turn on your computer.

The AT E Series board is installed. You are now ready to install and configure your software.

Board Configuration

Due to the DAQ-PnP features, the AT E Series boards are completely software configurable. Two types of configuration must be performed on the AT E Series boards—bus-related configuration and data acquisition-related configuration. Bus-related configuration includes setting the base I/O address, DMA channels, and interrupt channels. Data acquisition-related configuration, explained in the next chapter, includes such settings as analog input polarity and range, analog output reference source, and other settings. For more information about data acquisition-related configuration, refer to your NI-DAQ user manual.

Bus Interface

The AT E Series boards work in either a Plug and Play mode or a switchless mode. These modes dictate how the base I/O address, DMA channels, and interrupt channels are determined and assigned to the board.

Plug and Play

The AT E Series boards are fully compatible with the industry-standard Plug and Play ISA specification. A Plug and Play system arbitrates and assigns resources through software, freeing you from manually setting switches and jumpers. These resources include the board base I/O address, DMA channels, and interrupt channels. Each AT E Series board is configured at the factory to request these resources from the Plug and Play Configuration Manager.

The Configuration Manager receives all of the resource requests at start up, compares the available resources to those requested, and assigns the available resources as efficiently as possible to the Plug and Play boards. Application software can query the Configuration Manager to determine the resources assigned to each board without your involvement. The Plug and Play software is installed as a device driver or as an integral component of the computer BIOS.

Switchless Data Acquisition

You can use an AT E Series board in a non-Plug and Play system as a switchless DAQ board. A non-Plug and Play system is a system in which the Configuration Manager has not been installed and which does not contain any non-National Instruments Plug and Play products. You use a configuration utility to enter the base address, DMA, and interrupt selections, and the application software assigns them to the board.

☞ **Note:** ***Avoid resource conflicts with non-National Instruments boards. For example, do not configure two boards for the same base address.***

Base I/O Address Selection

The AT E Series boards can be configured to use base addresses in the range of 20 to FFE0 hex. Each AT E Series board occupies 32 bytes of address space and must be located on a 32-byte boundary. Therefore, valid addresses include 100, 120, 140,..., 3C0, 3E0 hex. This selection is software configured and does not require you to manually change any settings on the board.

DMA Channel Selection

The AT E Series boards can achieve high transfer rates by using up to three 16-bit DMA channels. You can use these DMA channels for data transfers with the analog input, analog output, and general-purpose counter sections of the board. The AT E Series boards can use only 16-bit DMA channels, which correspond to channels 5, 6, and 7 in an ISA computer and channels 0, 1, 2, 3, 5, 6, and 7 in an EISA computer. These selections are all software configured and do not require you to manually change any settings on the board.

Interrupt Channel Selection

The AT E Series boards can increase bus efficiency by using an interrupt channel. You can use an interrupt channel for event notification without the use of polling techniques. AT E Series boards can use interrupt channels 3, 4, 5, 7, 10, 11, 12, and 15. These selections are all software configured and do not require you to manually change any settings on the board. The following tables provide information concerning possible conflicts when configuring your AT E Series board.

Table 2-1. PC AT I/O Address Map

I/O Address Range (Hex)	Device
100 to 1EF	—
1F0 to 1F8	IBM PC AT Fixed Disk
200 to 20F	PC and PC AT Game Controller, reserved
210 to 213	PC-DIO-24 – default
218 to 21F	—
220 to 23F	Previous generation of AT-MIO boards – default
240 to 25F	AT-DIO-32F – default
260 to 27F	Lab-PC/PC+ – default
278 to 28F	AT Parallel Printer Port 2 (LPT2)

Table 2-1. PC AT I/O Address Map (Continued)

I/O Address Range (Hex)	Device
279	Reserved for Plug and Play operation
280 to 29F	WD EtherCard+ – default
2A0 to 2BF	—
2E2 to 2F7	—
2F8 to 2FF	PC, AT Serial Port 2 (COM2)
300 to 30F	3Com EtherLink – default
310 to 31F	—
320 to 32F	ICM PC/XT Fixed Disk Controller
330 to 35F	—
360 to 363	PC Network (low address)
364 to 367	Reserved
368 to 36B	PC Network (high address)
36C to 36F	Reserved
370 to 366	PC, AT Parallel Printer Port 1 (LPT1)
380 to 38C	SDLC Communications
380 to 389	Bisynchronous (BSC) Communications (alternate)
390 to 393	Cluster Adapter 0
394 to 39F	—
3A0 to 3A9	BSC Communications (primary)
3AA to 3AF	—

Table 2-1. PC AT I/O Address Map (Continued)

I/O Address Range (Hex)	Device
3B0 to 3BF	Monochrome Display/Parallel Printer Adapter 0
3C0 to 3CF	Enhanced Graphics Adapter, VGA
3D0 to 3DF	Color/Graphics Monitor Adapter, VGA
3E0 to 3EF	—
3F0 to 3F7	Diskette Controller
3F8 to 3FF	Serial Port 1 (COM1)
A79	Reserved for Plug and Play operation

Table 2-2. PC AT Interrupt Assignment Map

IRQ	Device
15	Available
14	Fixed Disk Controller
13	Coprocessor
12	AT-DIO-32F – default
11	AT-DIO-32F – default
10	AT-MIO-16 – default
9	PC Network – default PC Network Alternate – default
8	Real Time Clock
7	Parallel Port 1 (LPT1)
6	Diskette Drive Controller Fixed Disk and Diskette Drive Controller

Table 2-2. PC AT Interrupt Assignment Map (Continued)

IRQ	Device
5	Parallel Port 2 (LPT2) PC-DIO-24 – default Lab-PC/PC+ – default
4	Serial Port 1 (COM1) BSC, BSC Alternate
3	Serial Port 2 (COM2) BSC, BSC Alternate Cluster (primary) PC Network, PC Network Alternate WD EtherCard+ – default 3Com EtherLink – default
2	IRQ 8-15 Chain (from interrupt controller 2)
1	Keyboard Controller Output Buffer Full
0	Timer Channel 0 Output

Table 2-3. PC AT 16-bit DMA Channel Assignment Map

Channel	Device
7	AT-MIO-16 series – default
6	AT-MIO-16 series – default AT-DIO-32F – default
5	AT-DIO-32F – default
4	Cascade for DMA Controller #1 (channels 0 through 3)

☞ **Note:** ***EISA computers also have channels 0–3 available as 16-bit DMA channels.***

Chapter 3

Hardware Overview

This chapter presents an overview of the hardware functions on your AT E Series board.

Figure 3-1 shows the block diagram for the AT-MIO-16E-1 and AT-MIO-16E-2.

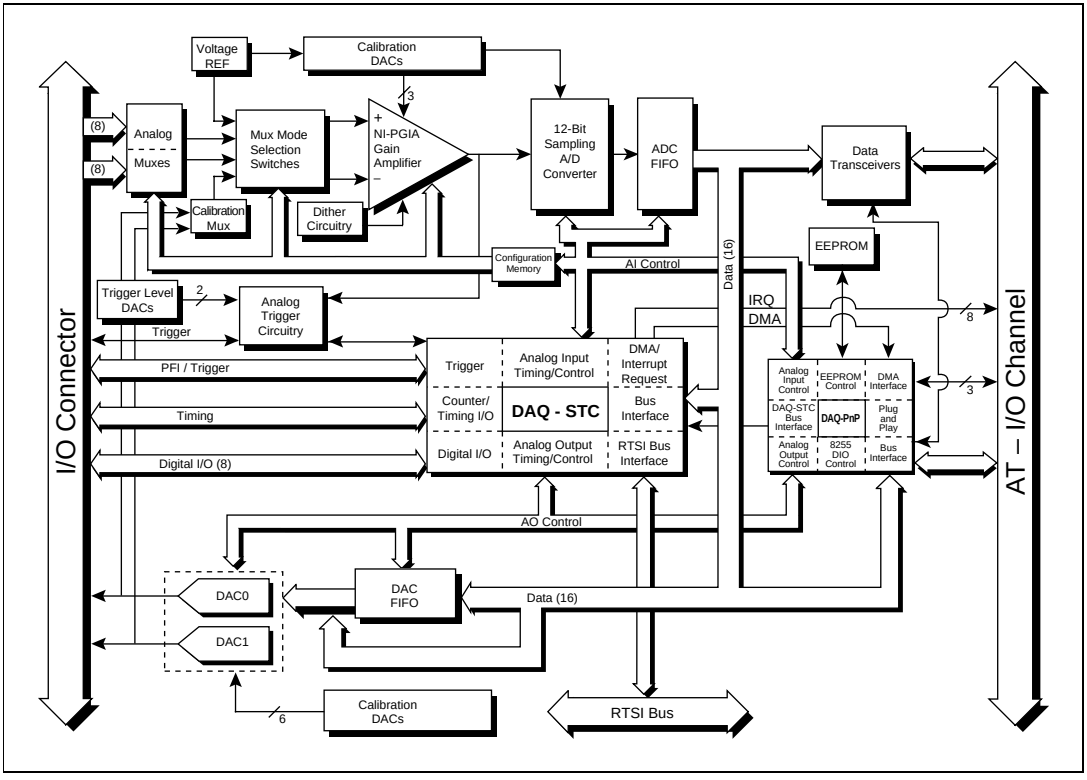


Figure 3-1. AT-MIO-16E-1 and AT-MIO-16E-2 Block Diagram

Figure 3-2 shows the block diagram for the AT-MIO-64E-3.

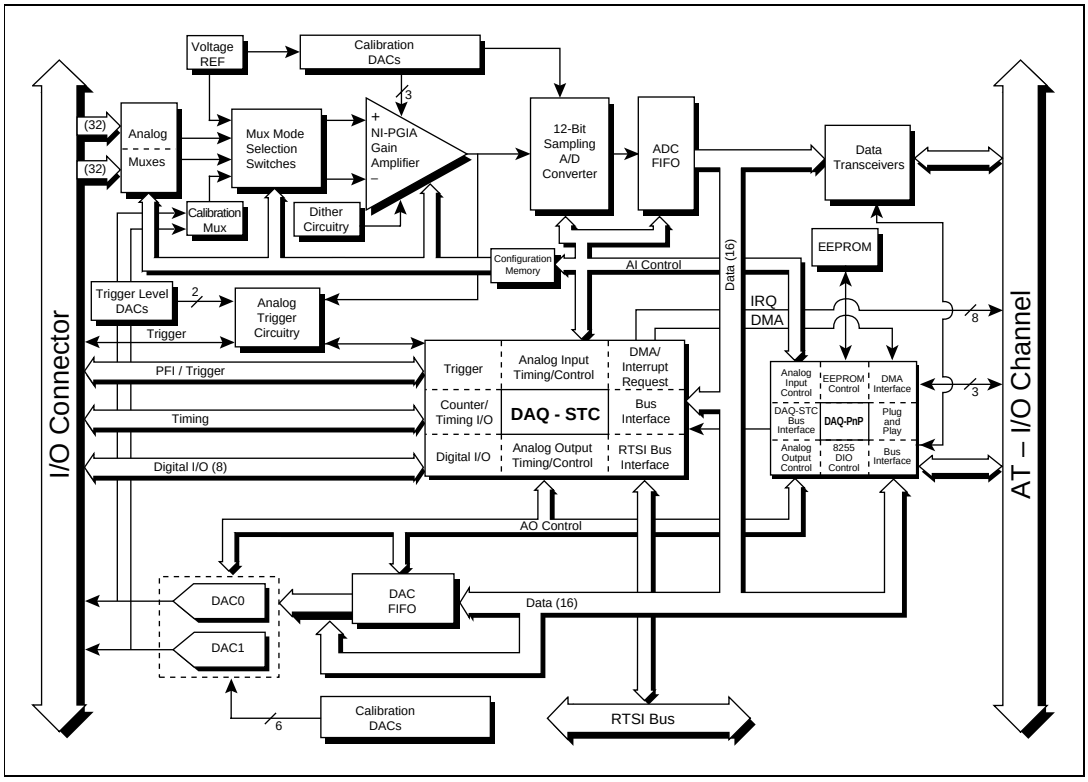


Figure 3-2. AT-MIO-64E-3 Block Diagram

Figure 3-3 shows the block diagram for the AT-MIO-16E-10 and AT-MIO-16DE-10.

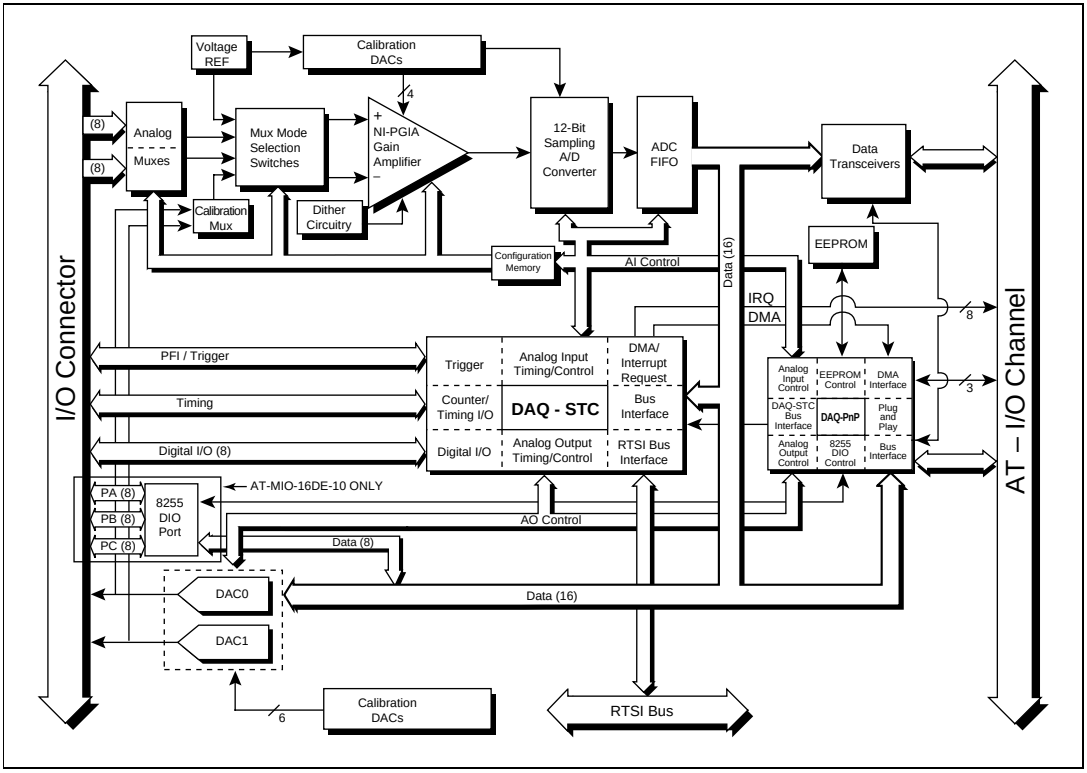


Figure 3-3. AT-MIO-16E-10 and AT-MIO-16DE-10 Block Diagram

The primary differences between the AT-MIO-16E-10 and the AT-MIO-16DE-10 are in the 8255 DIO port, which is not present on the AT-MIO-16E-10, and the I/O connector.

Figure 3-4 shows a block diagram for the AT-MIO-16XE-10.

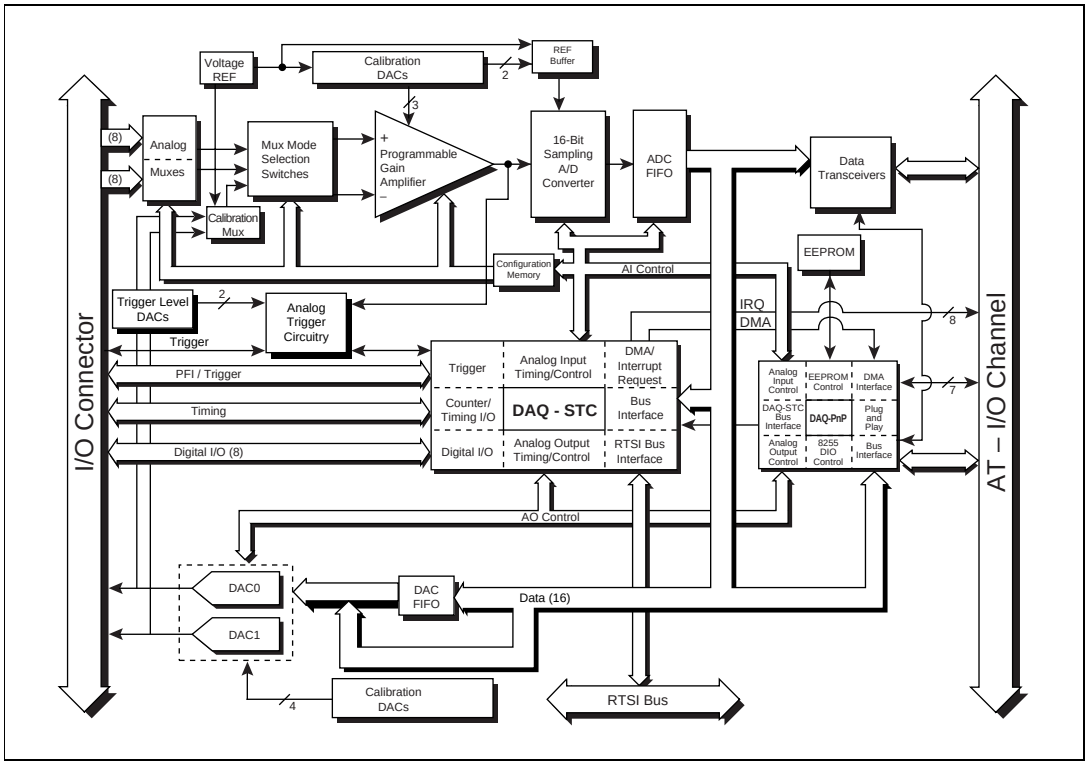


Figure 3-4. AT-MIO-16XE-10 Block Diagram

Figure 3-5 shows a block diagram for the AT-AI-16XE-10.

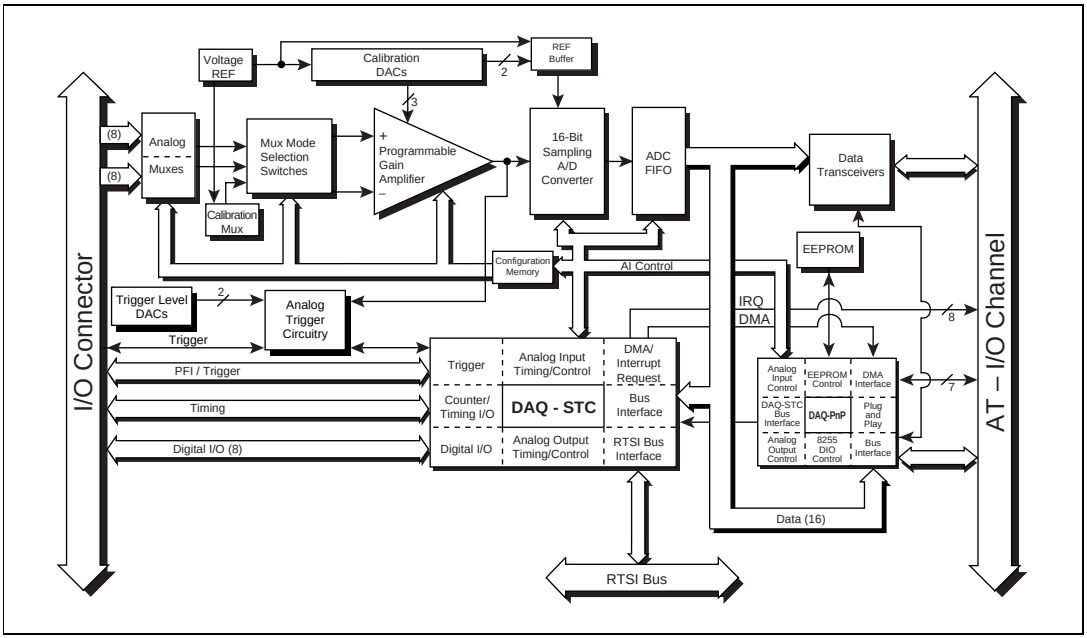


Figure 3-5. AT-AI-16XE-10 Block Diagram

Figure 3-6 shows a block diagram for the AT-MIO-16XE-50.

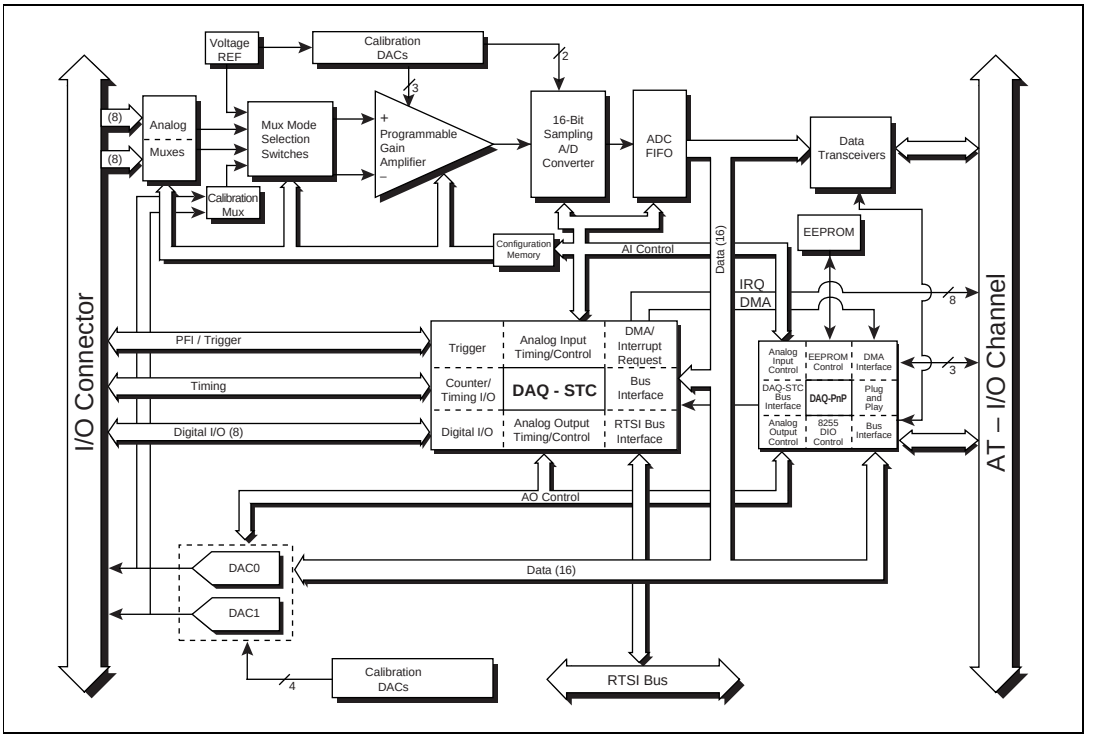


Figure 3-6. AT-MIO-16XE-50 Block Diagram

Analog Input

The analog input section of each AT E Series board is software configurable. You can select different analog input configurations through application software designed to control the AT E Series boards. The following sections describe in detail each of the analog input categories.

Input Mode

The AT E Series boards have three different input modes—nonreferenced single-ended (NRSE) input, referenced single-ended (RSE) input, and differential (DIFF) input. The single-ended input configurations use up to 16 channels (64 channels on the AT-MIO-64E-3). The DIFF input configuration uses up to eight

channels (32 channels on the AT-MIO-64E-3). Input modes are programmed on a per channel basis for multimode scanning. For example, you can configure the circuitry to scan 12 channels—four differentially configured channels and eight single-ended channels. Table 3-1 describes the three input configurations.

Table 3-1. Available Input Configurations for the AT E Series

Configuration	Description
DIFF	A channel configured in DIFF mode uses two analog channel input lines. One line connects to the positive input of the board programmable gain instrumentation amplifier (PGIA), and the other connects to the negative input of the PGIA.
RSE	A channel configured in RSE mode uses one analog channel input line, which connects to the positive input of the PGIA. The negative input of the PGIA is internally tied to analog input ground (AIGND).
NRSE	A channel configured in NRSE mode uses one analog channel input line, which connects to the positive input of the PGIA. The negative input of the PGIA connects to the analog input sense (AISENSE) input.

For more information about the three types of input configuration, refer to the *Analog Input Signal Connections* section in Chapter 4, *Signal Connections*, which contains diagrams showing the signal paths for the three configurations.

Input Polarity and Input Range

- AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-64E-3, AT-MIO-16E-10, and AT-MIO-16DE-10

  These boards have two input polarities—unipolar and bipolar. Unipolar input means that the input voltage range is between 0 and V_{ref}, where V_{ref} is a positive reference voltage. Bipolar input means that the input voltage range is between $-V_{ref}/2$ and $+V_{ref}/2$. The AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-64E-3, AT-MIO-16E-10, and AT-MIO-16DE-10 have a unipolar input range of 10 V (0 to 10 V) and a bipolar input range of 10 V (±5 V). You can program polarity and

range settings on a per channel basis so that you can configure each input channel uniquely.

The software-programmable gain on these boards increases their overall flexibility by matching the input signal ranges to those that the ADC can accommodate. The AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-64E-3, AT-MIO-16E-10, and AT-MIO-16DE-10 have gains of 0.5, 1, 2, 5, 10, 20, 50, and 100 and are suited for a wide variety of signal levels. With the proper gain setting, you can use the full resolution of the ADC to measure the input signal. Table 3-2 shows the overall input range and precision according to the input range configuration and gain used.

Table 3-2. Actual Range and Measurement Precision

Range Configuration	Gain	Actual Input Range	Precision[1]
0 to +10 V	1.0	0 to +10 V	2.44 mV
	2.0	0 to +5 V	1.22 mV
	5.0	0 to +2 V	488.28 µV
	10.0	0 to +1 V	244.14 µV
	20.0	0 to +500 mV	122.07 µV
	50.0	0 to +200 mV	48.83 µV
	100.0	0 to +100 mV	24.41 µV
–5 to +5 V	0.5	–10 to +10 V	4.88 mV
	1.0	–5 to +5 V	2.44 mV
	2.0	–2.5 to +2.5 V	1.22 mV
	5.0	–1 to +1 V	488.28 µV
	10.0	–500 to +500 mV	244.14 µV
	20.0	–250 to +250 mV	122.07 µV
	50.0	–100 to +100 mV	48.83 µV
	100.0	–50 to +50 mV	24.41 µV

[1] The value of 1 LSB of the 12-bit ADC; that is, the voltage increment corresponding to a change of one count in the ADC 12-bit count.

Note: See Appendix A, *Specifications*, for absolute maximum ratings.

- AT-MIO-16XE-10, AT-AI-16XE-10, AT-MIO-16XE-50

These boards have two input polarities—unipolar and bipolar. Unipolar input means that the input voltage range is between 0 and V_{ref}, where V_{ref} is a positive reference voltage. Bipolar input means that the input

voltage range is between $-V_{ref}$ and $+V_{ref}$. The AT-MIO-16XE-10, AT-AI-16XE-10, and AT-MIO-16XE-50 have a unipolar input range of 10 V (0 to 10 V) and a bipolar input range of 20 V (±10 V). You can program polarity and range settings on a per channel basis so that you can configure each input channel uniquely.

☞ **Note:** ***You can calibrate your AT-MIO-16XE-10, AT-AI-16XE-10, and AT-MIO-16XE-50 analog input circuitry for either a unipolar or bipolar polarity. If you mix unipolar and bipolar channels in your scan list and you are using NI-DAQ, then NI-DAQ will load the calibration constants appropriate to the polarity for which analog input channel 0 is configured.***

The software-programmable gain on these boards increases their overall flexibility by matching the input signal ranges to those that the ADC can accommodate. The AT-MIO-16XE-10 and AT-AI-16XE-10 have gains of 1, 2, 5, 10, 20, 50, and 100 and the AT-MIO-16XE-50 has gains of 1, 2, 10, and 100. These gains are suited for a wide variety of signal levels. With the proper gain setting, you can use the full resolution of the ADC to measure the input signal. Table 3-3 shows the overall input range and precision according to the input range configuration and gain used.

Table 3-3. Actual Range and Measurement Precision, AT-MIO-16XE-10, AT-AI-16XE-10, and AT-MIO-16XE-50

Range Configuration	Gain	Actual Input Range	Precision[1]
0 to +10 V	1.0	0 to +10 V	152.59 µV
	2.0	0 to +5 V	76.29 µV
	5.0[2]	0 to +2 V	30.52 µV
	10.0	0 to +1 V	15.26 µV
	20.0[2]	0 to +500 mV	.63 µV
	50.0[2]	0 to +200 mV	3.05 µV
	100.0	0 to 100 mV	1.53 µV

Table 3-3. Actual Range and Measurement Precision, AT-MIO-16XE-10, AT-AI-16XE-10, and AT-MIO-16XE-50 (Continued)

Range Configuration	Gain	Actual Input Range	Precision[1]
–10 to +10 V	1.0	–10 to +10 V	305.18 µV
	2.0	–5 to +5 V	152.59 µV
	5.0[2]	–2 to +2 V	61.04 µV
	10.0	–1 to +1 V	30.52 µV
	20.0[2]	–500 to +500 mV	15.26 µV
	50.0[2]	–200 to +200 mV	6.10 µV
	100.0	–100 to +100 mV	3.05 µV

[1] The value of 1 LSB of the 16-bit ADC; that is, the voltage increment corresponding to a change of one count in the ADC 16-bit count.

[2] AT-MIO-16XE-10 and AT-AI-16XE-10 only

Note: See Appendix A, *Specifications*, for absolute maximum ratings.

Considerations for Selecting Input Ranges

Which input polarity and range you select depends on the expected range of the incoming signal. A large input range can accommodate a large signal variation but reduces the voltage resolution. Choosing a smaller input range improves the voltage resolution but may result in the input signal going out of range. For best results, you should match the input range as closely as possible to the expected range of the input signal. For example, if you are certain the input signal will not be negative (below 0 V), unipolar input polarity is best. However, if the signal is negative or equal to zero, inaccurate readings will occur if you use unipolar input polarity.

Dither

When you enable dither, you add approximately 0.5 LSB rms of white Gaussian noise to the signal to be converted by the ADC. This addition is useful for applications involving averaging to increase the resolution of your AT E Series board, as in calibration or spectral analysis. In such applications, noise modulation is decreased and differential linearity is improved by the addition of the dither. When taking DC measurements, such as when checking the board calibration, you should enable dither and average about 1,000 points to take a single reading. This process removes the effects of quantization and reduces measurement noise, resulting in improved resolution. For high-speed applications not

involving averaging or spectral analysis, you may want to disable the dither to reduce noise. You enable and disable the dither circuitry through software.

Figure 3-7 illustrates the effect of dither on signal acquisition. Figure 3-7a shows a small (±4 LSB) sine wave acquired with dither off. The quantization of the ADC is clearly visible. Figure 3-7b shows what happens when 50 such acquisitions are averaged together; quantization is still plainly visible. In Figure 3-7c, the sine wave is acquired with dither on. There is a considerable amount of noise visible. But averaging about 50 such acquisitions, as shown in Figure 3-7d, eliminates both the added noise and the effects of quantization. Dither has the effect of forcing quantization noise to become a zero-mean random variable rather than a deterministic function of the input signal.

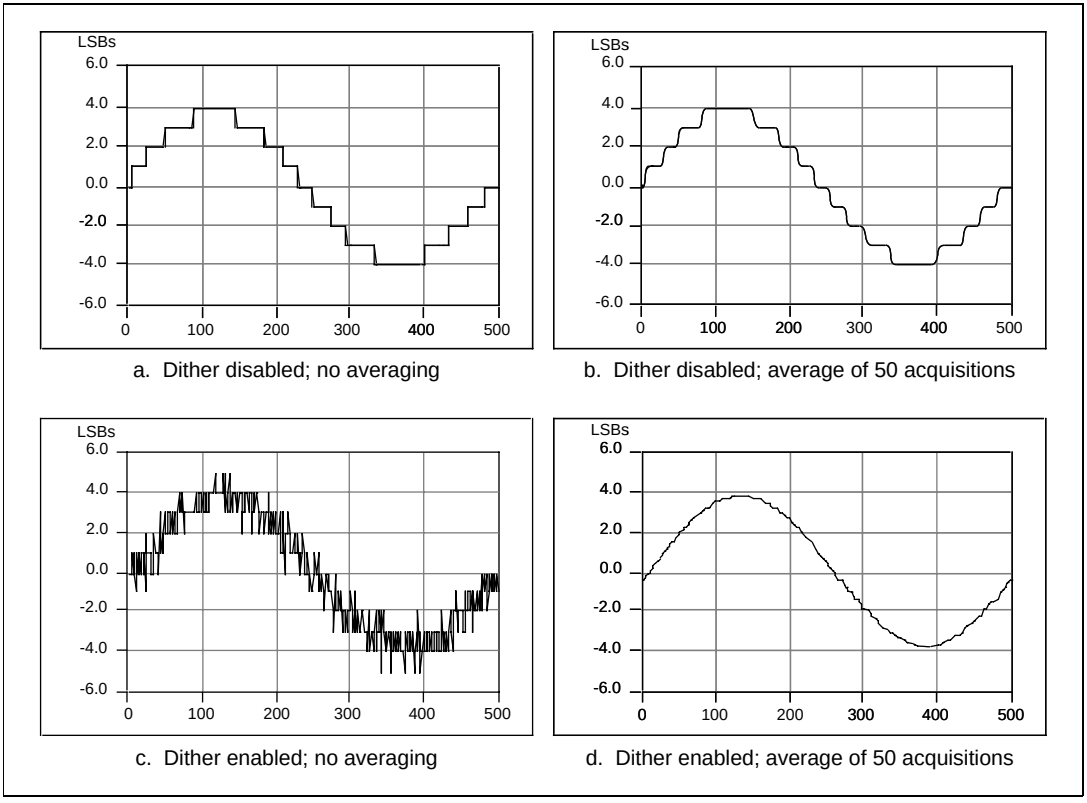


Figure 3-7. Dither

You cannot disable dither on the AT-MIO-16XE-10, AT-AI-16XE-10, or AT-MIO-16XE-50. This is because the resolution of the ADC is so fine that the ADC and the PGIA inherently produce almost 0.5 LSB rms of noise. This is equivalent to having a dither circuit that is always enabled.

Multiple-Channel Scanning Considerations

All of the AT E Series boards can scan multiple channels at the same maximum rate as their single-channel rate; however, you should pay careful attention to the settling times for each of the boards. The settling time for most of the AT E Series boards is independent of the selected gain, even at the maximum sampling rate. The settling time for the high channel count and very high-speed boards is gain dependent, which can affect the useful sampling rate for a given gain. No extra settling time is necessary between channels as long as the gain is constant and source impedances are low. Refer to Appendix A, *Specifications*, for a complete listing of settling times for each of the AT E Series boards.

When scanning among channels at various gains, the settling times may increase. When the PGIA switches to a higher gain, the signal on the previous channel may be well outside the new, smaller range. For instance, suppose a 4 V signal is connected to channel 0 and a 1 mV signal is connected to channel 1, and suppose the PGIA is programmed to apply a gain of one to channel 0 and a gain of 100 to channel 1. When the multiplexer switches to channel 1 and the PGIA switches to a gain of 100, the new full-scale range is 100 mV (if the ADC is in unipolar mode).

The approximately 4 V step from 4 V to 1 mV is 4,000% of the new full-scale range. For a 12-bit board to settle within 0.012% (120 ppm or 1/2 LSB) of the 100 mV full-scale range on channel 1, the input circuitry has to settle to within 0.0003% (3 ppm or 1/80 LSB) of the 4 V step. It may take as long as 100 µs for the circuitry to settle this much. For a 16-bit board to settle within 0.0015% (15 ppm or 1 LSB) of the 100 mV full-scale range on channel 1, the input circuitry has to settle within 0.00004% (0.4 ppm or 1/400 LSB) of the 4 V step. It may take as long as 200 µs for the circuitry to settle this much. In general, this extra settling time is not needed when the PGIA is switching to a lower gain.

Settling times can also increase when scanning high-impedance signals due to a phenomenon called *charge injection*, where the analog input multiplexer injects a small amount of charge into each signal source

when that source is selected. If the impedance of the source is not low enough, the effect of the charge—a voltage error—will not have decayed by the time the ADC samples the signal. For this reason, you should keep source impedances under 1 kΩ to perform high-speed scanning.

Due to the previously described limitations of settling times resulting from these conditions, multiple-channel scanning is not recommended unless sampling rates are low enough or it is necessary to sample several signals as nearly simultaneously as possible. The data is much more accurate and channel-to-channel independent if you acquire data from each channel independently (for example, 100 points from channel 0, then 100 points from channel 1, then 100 points from channel 2, and so on).

Analog Output

- AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-64E-3, AT-MIO-16E-10, AT-MIO-16DE-10

  The AT E Series boards supply two channels of analog output voltage at the I/O connector. You can select the reference and range for the analog output circuitry through software. The reference can be either internal or external, whereas the range can be either bipolar or unipolar.

- AT-MIO-16XE-50

  The AT-MIO-16XE-50 supplies two channels of analog output voltage at the I/O connector. The range is fixed at bipolar ±10 V.

- AT-MIO-16XE-10

  The AT-MIO-16XE-10 supplies two channels of analog output voltage at the I/O connector. The range is software selectable between unipolar (0 to 10 V) and bipolar (±10 V).

Analog Output Reference Selection

- AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-64E-3, AT-MIO-16E-10, AT-MIO-16DE-10 only

  You can connect each D/A converter (DAC) to the AT E Series board internal reference of 10 V or to the external reference signal connected

to the external reference (EXTREF) pin on the I/O connector. This signal applied to EXTREF should be between –10 and +10 V. You do not need to configure both channels for the same mode.

Analog Output Polarity Selection

- AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-64E-3, AT-MIO-16E-10, AT-MIO-16DE-10 only

  You can configure each analog output channel for either unipolar or bipolar output. A unipolar configuration has a range of 0 to V_{ref} at the analog output. A bipolar configuration has a range of $-V_{ref}$ to $+V_{ref}$ at the analog output. V_{ref} is the voltage reference used by the DACs in the analog output circuitry and can be either the +10 V onboard reference or an externally supplied reference between –10 and +10 V. You do not need to configure both channels for the same range.

  Selecting a bipolar range for a particular DAC means that any data written to that DAC will be interpreted as two's complement format. In two's complement mode, data values written to the analog output channel can be either positive or negative. If you select unipolar range, data is interpreted in straight binary format. In straight binary mode, data values written to the analog output channel range must be positive.

- AT-MIO-16XE-10

  You can configure each analog output channel for either unipolar or bipolar output. A unipolar configuration has a range of 0 to 10 V at the analog output. A bipolar configuration has a range of –10 to +10 V at the analog output. You do not need to configure both channels for the same range.

Analog Output Reglitch Selection

- AT-MIO-16E-1, AT-MIO-16E-2, and AT-MIO-64E-3 only

  In normal operation, a DAC output will glitch whenever it is updated with a new value. The glitch energy differs from code to code and appears as distortion in the frequency spectrum. Each analog output of the AT-MIO-16E-1, AT-MIO-16E-2, and AT-MIO-64E-3 contains a reglitch circuit that generates uniform glitch energy at every code rather than large glitches at the major code transitions. This uniform glitch energy appears as a multiple of the update rate in the frequency spectrum. Notice that this reglitch circuit *does not* eliminate the

glitches; it only makes them more uniform in size. Reglitching is normally disabled at startup and can be independently enabled for each channel through software.

Analog Trigger

- AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-64E-3, AT-MIO-16XE-10, and AT-AI-16XE-10 only

  In addition to supporting internal software triggering and external digital triggering to initiate a data acquisition sequence, the AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-64E-3, AT-MIO-16XE-10, and AT-AI-16XE-10 also support analog triggering. You can configure the analog trigger circuitry to accept either a direct analog input from the PFI0/TRIG1 pin on the I/O connector or a postgain signal from the output of the PGIA, as shown in Figure 3-8. The trigger-level range for the direct analog channel is ±10 V in 78 mV steps for the AT-MIO-16E-1, AT-MIO-16E-2, and AT-MIO-64E-3, and ±10 V in 4.9 mV steps for the AT-MIO-16XE-10 and AT-AI-16XE-10. The range for the post-PGIA trigger selection is simply the full-scale range of the selected channel, and the resolution is that range divided by 256 for the AT-MIO-16E-1, AT-MIO-16E-2, and AT-MIO-64E-3, and divided by 4,096 for the AT-MIO-16XE-10 and AT-AI-16XE-10.

☞ **Note:** ***The PFI0/TRIG1 pin is a high-impedance input. Therefore, it is susceptible to cross-talk from adjacent pins, which can result in false triggering when the pin is left unconnected. To avoid false triggering, make sure this pin is connected to a low-impedance signal source (less than 10 kΩ source impedance) if you plan to enable this input via software.***

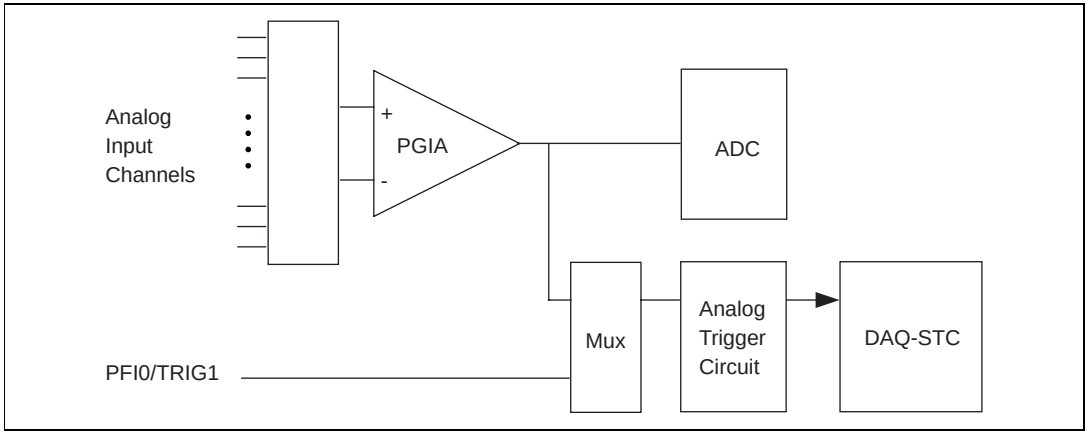


Figure 3-8. Analog Trigger Block Diagram

There are five analog triggering modes available, as shown in Figures 3-9 through 3-13. You can set **lowValue** and **highValue** independently in software.

In below-low-level analog triggering mode, the trigger is generated when the signal value is less than **lowValue**. **HighValue** is unused.

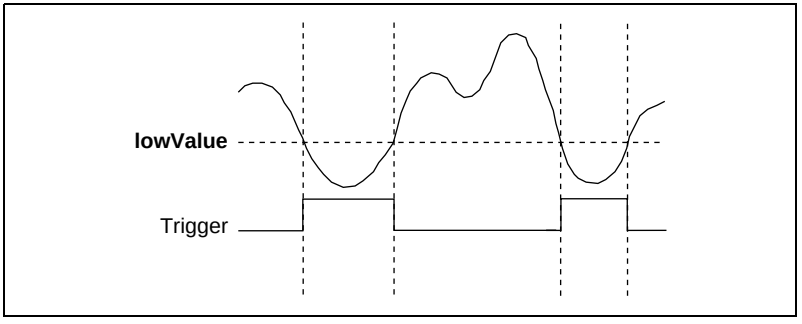


Figure 3-9. Below-Low-Level Analog Triggering Mode

In above-high-level analog triggering mode, the trigger is generated when the signal value is greater than **highValue**. **LowValue** is unused.

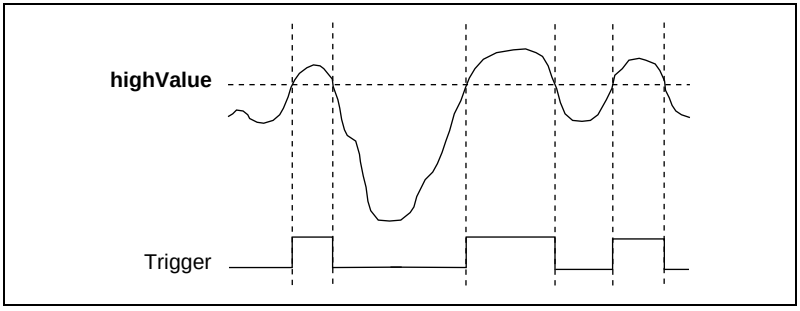


Figure 3-10. Above-High-Level Analog Triggering Mode

In inside-region analog triggering mode, the trigger is generated when the signal value is between the **lowValue** and the **highValue.**

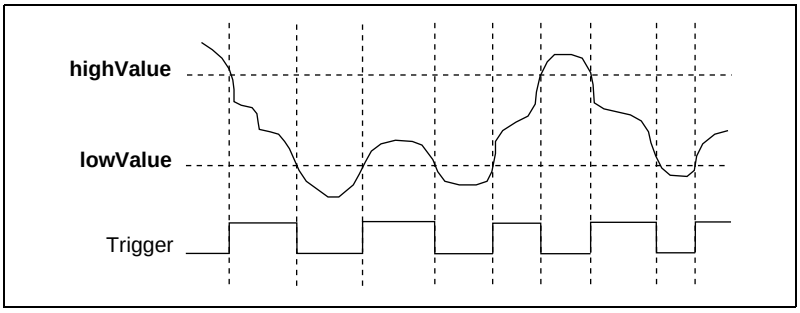


Figure 3-11. Inside-Region Analog Triggering Mode

In high-hysteresis analog triggering mode, the trigger is generated when the signal value is greater than **highValue**, with the hysteresis specified by **lowValue**.

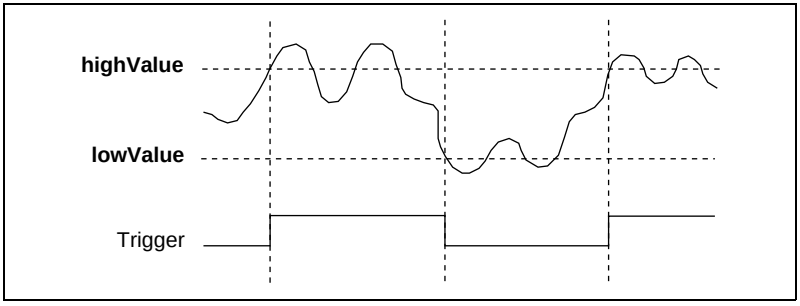


Figure 3-12. High-Hysteresis Analog Triggering Mode

In low-hysteresis analog triggering mode, the trigger is generated when the signal value is less than **lowValue**, with the hysteresis specified by **highValue.**

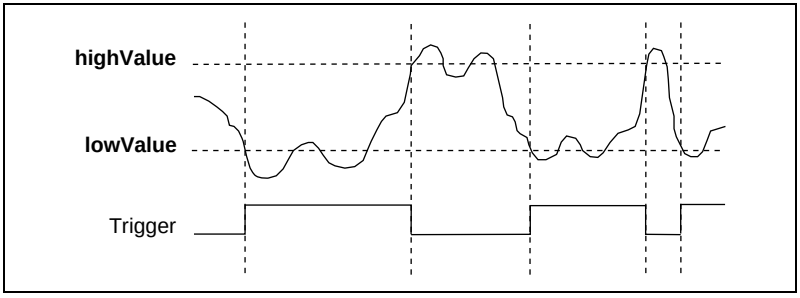


Figure 3-13. Low-Hysteresis Analog Triggering Mode

The analog trigger circuit generates an internal digital trigger based on the analog input signal and the user-defined trigger levels. This digital trigger can be used by any of the timing sections of the DAQ-STC, including the analog input, analog output, and general-purpose counter/timer sections. For example, the analog input section can be configured to acquire *n* scans after the analog input signal crosses a specific threshold. As another example, the analog output section can be configured to update its outputs whenever the analog input signal crosses a specific threshold.

Digital I/O

The AT E Series boards contain eight lines of digital I/O for general-purpose use. You can individually configure each line through software for either input or output. The AT-MIO-16DE-10 has 24 additional DIO lines, configured as three 8-bit ports: PA<0..7>, PB<0..7>, and PC<0..7>. You can configure each port for both input and output in various combinations, with some handshaking capabilities. At system startup and reset, the digital I/O ports are all high impedance.

The hardware up/down control for general-purpose counters 0 and 1 are connected onboard to DIO6 and DIO7, respectively. Thus, you can use DIO6 and DIO7 to control the general-purpose counters. The up/down control signals are input only and do not affect the operation of the DIO lines.

Timing Signal Routing

The DAQ-STC provides a very flexible interface for connecting timing signals to other boards or external circuitry. Your AT E Series board uses the RTSI bus for interconnecting timing signals between boards and the Programmable Function Input (PFI) pins on the I/O connector for connecting to external circuitry. These connections are designed to enable the AT E Series board to both control and be controlled by other boards and circuits.

There are a total of 13 timing signals internal to the DAQ-STC that can be controlled by an external source. These timing signals can also be controlled by signals generated internally to the DAQ-STC, and these selections are fully software configurable. For example, the signal routing multiplexer for controlling the CONVERT* signal is shown in Figure 3-14.

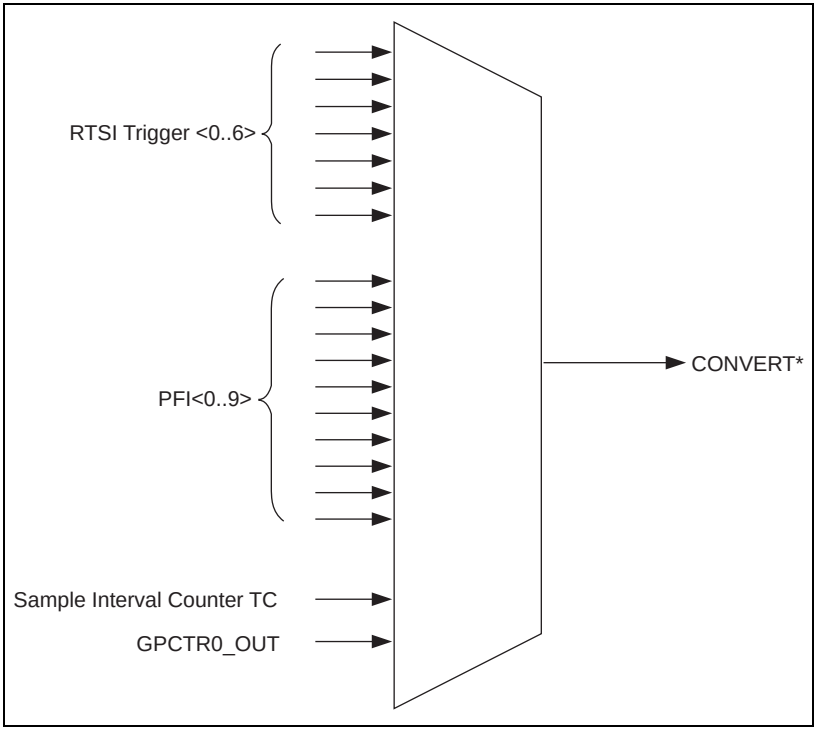


Figure 3-14. CONVERT* Signal Routing

This figure shows that CONVERT* can be generated from a number of sources, including the external signals RTSI<0..6> and PFI<0..9> and the internal signals Sample Interval Counter TC and GPCTR0_OUT.

Many of these timing signals are also available as outputs on the RTSI pins, as indicated in the *RTSI Triggers* section later in this chapter, and on the PFI pins, as indicated in Chapter 4, *Signal Connections*.

Programmable Function Inputs

The 10 PFIs are connected to the signal routing multiplexer for each timing signal, and software can select one of the PFIs as the external source for a given timing signal. It is important to note that any of the PFIs can be used as an input by any of the timing signals and that multiple timing signals can use the same PFI simultaneously. This flexible routing scheme reduces the need to change physical connections to the I/O connector for different applications.

You can also individually enable each of the PFI pins to output a specific internal timing signal. For example, if you need the UPDATE* signal as an output on the I/O connector, software can turn on the output driver for the PFI5/UPDATE* pin.

Board and RTSI Clocks

Many functions performed by the AT E Series boards require a frequency timebase to generate the necessary timing signals for controlling A/D conversions, DAC updates, or general-purpose signals at the I/O connector.

An AT E Series board can use either its internal 20 MHz timebase or a timebase received over the RTSI bus. In addition, if you configure the board to use the internal timebase, you can also program the board to drive its internal timebase over the RTSI bus to another board that is programmed to receive this timebase signal. This clock source, whether local or from the RTSI bus, is used directly by the board as the primary frequency source. The default configuration at startup is to use the internal timebase without driving the RTSI bus timebase signal. You select this timebase through software.

RTSI Triggers

The seven RTSI trigger lines on the RTSI bus provide a very flexible interconnection scheme for any AT E Series board sharing the RTSI bus. These bidirectional lines can drive any of eight timing signals onto the RTSI bus and can receive any of these timing signals. This signal connection scheme is shown in Figure 3-15.

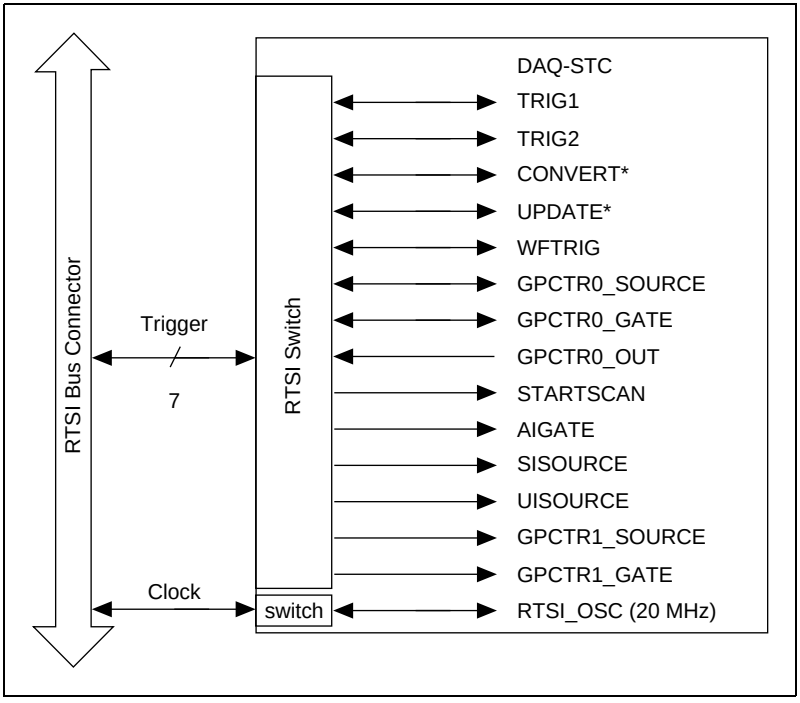


Figure 3-15. RTSI Bus Signal Connection

Refer to the *Timing Connections* section of Chapter 4, *Signal Connections*, for a description of the signals shown in Figure 3-15.

Chapter 4

Signal Connections

This chapter describes how to make input and output signal connections to your AT E Series board via the board I/O connector.

The I/O connector for the AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-16E-10, AT-MIO-16XE-10, AT-AI-16XE-10, and AT-MIO-16XE-50 has 68 pins that you can connect to 68-pin accessories with the SH6868 shielded cable or the R6868 ribbon cable. With the SH6850 shielded cable or R6850 ribbon cable, you can connect your board to 50-pin signal conditioning modules and terminal blocks.

The I/O connector for the AT-MIO-64E-3 and AT-MIO-16DE-10 has 100 pins that you can connect to 100-pin accessories with the SH100100 shielded cable. With the SH1006868 shielded cable you can connect your board to 68-pin accessories, and with the R1005050 ribbon cable you can connect your board to 50-pin accessories.

I/O Connector

Figure 4-1 shows the pin assignments for the 68-pin I/O connector on the AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-16E-10, AT-MIO-16XE-10, AT-AI-16XE-10, and AT-MIO-16XE-50. Figure 4-2 shows the pin assignments for the 100-pin I/O connector on the AT-MIO-64E-3. Figure 4-3 shows the pin assignments for the 100-pin I/O connector on the AT-MIO-16DE-10. Refer to Appendix B, *Optional Cable Connector Descriptions*, for the pin assignments for the 50-pin connectors. A signal description follows the connector pinouts.

⚠ **Caution:** ***Connections that exceed any of the maximum ratings of input or output signals on the AT E Series boards can damage the AT E Series board and the PC. Maximum input ratings for each signal are given in Tables 4-2 through 4-5 in the*** *Protection* ***column. National Instruments is NOT liable for any damages resulting from such signal connections.***

ACH8	34	68	ACH0
ACH1	33	67	AIGND
AIGND	32	66	ACH9
ACH10	31	65	ACH2
ACH3	30	64	AIGND
AIGND	29	63	ACH11
ACH4	28	62	AISENSE
AIGND	27	61	ACH12
ACH13	26	60	ACH5
ACH6	25	59	AIGND
AIGND	24	58	ACH14
ACH15	23	57	ACH7
DAC0OUT[1]	22	56	AIGND
DAC1OUT[1]	21	55	AOGND
EXTREF[2]	20	54	AOGND
DIO4	19	53	DGND
DGND	18	52	DIO0
DIO1	17	51	DIO5
DIO6	16	50	DGND
DGND	15	49	DIO2
+5 V	14	48	DIO7
DGND	13	47	DIO3
DGND	12	46	SCANCLK
PFI0/TRIG1	11	45	EXTSTROBE*
PFI1/TRIG2	10	44	DGND
DGND	9	43	PFI2/CONVERT*
+5 V	8	42	PFI3/GPCTR1_SOURCE
DGND	7	41	PFI4/GPCTR1_GATE
PFI5/UPDATE*	6	40	GPCTR1_OUT
PFI6/WFTRIG	5	39	DGND
DGND	4	38	PFI7/STARTSCAN
PFI9/GPCTR0_GATE	3	37	PFI8/GPCTR0_SOURCE
GPCTR0_OUT	2	36	DGND
FREQ_OUT	1	35	DGND

[1] Not available on AT-AI-16XE-10

[2] Not available on AT-MIO-16XE-10, AT-AI-16XE-10, or AT-MIO-16XE-50

Figure 4-1. I/O Connector Pin Assignment for the AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-16E-10, AT-MIO-16XE-10, AT-AI-16XE-10, and AT-MIO-16XE-50

AIGND	1	51	ACH16
AIGND	2	52	ACH24
ACH0	3	53	ACH17
ACH8	4	54	ACH25
ACH1	5	55	ACH18
ACH9	6	56	ACH26
ACH2	7	57	ACH19
ACH10	8	58	ACH27
ACH3	9	59	ACH20
ACH11	10	60	ACH28
ACH4	11	61	ACH21
ACH12	12	62	ACH29
ACH5	13	63	ACH22
ACH13	14	64	ACH30
ACH6	15	65	ACH23
ACH14	16	66	ACH31
ACH7	17	67	ACH32
ACH15	18	68	ACH40
AISENSE	19	69	ACH33
DAC0OUT	20	70	ACH41
DAC1OUT	21	71	ACH34
EXTREF	22	72	ACH42
AOGND	23	73	ACH35
DGND	24	74	ACH43
DIO0	25	75	AISENSE2
DIO4	26	76	AIGND
DIO1	27	77	ACH36
DIO5	28	78	ACH44
DIO2	29	79	ACH37
DIO6	30	80	ACH45
DIO3	31	81	ACH38
DIO7	32	82	ACH46
DGND	33	83	ACH39
+5 V	34	84	ACH47
+5 V	35	85	ACH48
SCANCLK	36	86	ACH56
EXTSTROBE*	37	87	ACH49
PFI0/TRIG1	38	88	ACH57
PFI1/TRIG2	39	89	ACH50
PFI2/CONVERT*	40	90	ACH58
PFI3/GPCTR1_SOURCE	41	91	ACH51
PFI4/GPCTR1_GATE	42	92	ACH59
GPCTR1_OUT	43	93	ACH52
PFI5/UPDATE*	44	94	ACH60
PFI6/WFTRIG	45	95	ACH53
PFI7/STARTSCAN	46	96	ACH61
PFI8/GPCTR0_SOURCE	47	97	ACH54
PFI9/GPCTR0_GATE	48	98	ACH62
GPCTR0_OUT	49	99	ACH55
FREQ_OUT	50	100	ACH63

Figure 4-2. I/O Connector Pin Assignment for the AT-MIO-64E-3

AIGND	1	51	PC7
AIGND	2	52	GND
ACH0	3	53	PC6
ACH8	4	54	GND
ACH1	5	55	PC5
ACH9	6	56	GND
ACH2	7	57	PC4
ACH10	8	58	GND
ACH3	9	59	PC3
ACH11	10	60	GND
ACH4	11	61	PC2
ACH12	12	62	GND
ACH5	13	63	PC1
ACH13	14	64	GND
ACH6	15	65	PC0
ACH14	16	66	GND
ACH7	17	67	PB7
ACH15	18	68	GND
AISENSE	19	69	PB6
DAC0OUT	20	70	GND
DAC1OUT	21	71	PB5
EXTREF	22	72	GND
AOGND	23	73	PB4
DGND	24	74	GND
DIO0	25	75	PB3
DIO4	26	76	GND
DIO1	27	77	PB2
DIO5	28	78	GND
DIO2	29	79	PB1
DIO6	30	80	GND
DIO3	31	81	PB0
DIO7	32	82	GND
DGND	33	83	PA7
+5 V	34	84	GND
+5 V	35	85	PA6
SCANCLK	36	86	GND
EXTSTROBE*	37	87	PA5
PFI0/TRIG1	38	88	GND
PFI1/TRIG2	39	89	PA4
PFI2/CONVERT*	40	90	GND
PFI3/GPCTR1_SOURCE	41	91	PA3
PFI4/GPCTR1_GATE	42	92	GND
GPCTR1_OUT	43	93	PA2
PFI5/UPDATE*	44	94	GND
PFI6/WFTRIG	45	95	PA1
PFI7/STARTSCAN	46	96	GND
PFI8/GPCTR0_SOURCE	47	97	PA0
PFI9/GPCTR0_GATE	48	98	GND
GPCTR0_OUT	49	99	+5 V
FREQ_OUT	50	100	GND

Figure 4-3. I/O Connector Pin Assignment for the AT-MIO-16DE-10

I/O Connector Signal Descriptions

Table 4-1. I/O Signal Summary, AT E Series

Signal Name	Reference	Direction	Description
AIGND	—	—	Analog Input Ground—These pins are the reference point for single-ended measurements and the bias current return point for differential measurements. All three ground references—AIGND, AOGND, and DGND—are connected together on your AT E Series board.
ACH<0..15>	AIGND	Input	Analog Input Channels 0 through 15—Each channel pair, ACH<*i*, *i*+8> (*i* = 0..7), can be configured as either one differential input or two single-ended inputs.
ACH<16..63>	AIGND	Input	Analog Input Channels 16 through 63 (AT-MIO-64E-3 only)—Each channel pair, ACH<*i*, *i*+8> (*i* = 16..23, 32..39, 48..55), can be configured as either one differential input or two single-ended inputs.
AISENSE	AIGND	Input	Analog Input Sense—This pin serves as the reference node for any of channels ACH <0..15> in NRSE configuration.
AISENSE2	AIGND	Input	Analog Input Sense (AT-MIO-64E-3 only)—This pin serves as the reference node for any of channels ACH <16..63> in NRSE configuration.
DAC0OUT	AOGND	Output	Analog Channel 0 Output—This pin supplies the voltage output of analog output channel 0. This pin is *not* available on the AT-AI-16XE-10.
DAC1OUT	AOGND	Output	Analog Channel 1 Output—This pin supplies the voltage output of analog output channel 1. This pin is *not* available on the AT-AI-16XE-10.
EXTREF	AOGND	Input	External Reference—This is the external reference input for the analog output circuitry. This pin is *not* available on the AT-MIO-16XE-10, AT-AI-16XE-10, or AT-MIO-16XE-50.
AOGND	—	—	Analog Output Ground—The analog output voltages are referenced to this node. All three ground references—AIGND, AOGND, and DGND—are connected together on your AT E Series board.

Table 4-1. I/O Signal Summary, AT E Series (Continued)

Signal Name	Reference	Direction	Description
DGND	—	—	Digital Ground—This pin supplies the reference for the digital signals at the I/O connector as well as the +5 VDC supply. All three ground references—AIGND, AOGND, and DGND—are connected together on your AT E Series board.
DIO<0..7>	DGND	Input or Output	Digital I/O signals—DIO6 and 7 can control the up/down signal of general-purpose counters 0 and 1, respectively.
PA<0..7>	DGND	Input or Output	Port A—These pins are port A of the extra digital I/O signals on the AT-MIO-16DE-10.
PB<0..7>	DGND	Input or Output	Port B—These pins are port B of the extra digital I/O signals on the AT-MIO-16DE-10.
PC<0..7>	DGND	Input or Output	Port C—These pins are port C of the extra digital I/O signals on the AT-MIO-16DE-10.
+5 V	DGND	Output	+5 VDC Source—These pins are fused for up to 1 A of +5 V supply. The fuse is self-respecting.
SCANCLK	DGND	Output	Scan Clock—This pin pulses once for each A/D conversion in the scanning modes when enabled. The low-to-high edge indicates when the input signal can be removed from the input or switched to another signal.
EXTSTROBE*	DGND	Output	External Strobe—This output can be toggled under software control to latch signals or trigger events on external devices.
PFI0/TRIG1	DGND	Input	PFI0/Trigger 1—As an input, this is either one of the Programmable Function Inputs (PFIs) or the source for the hardware analog trigger. PFI signals are explained in the *Timing Connections* section later in this chapter. The hardware analog trigger is explained in the *Analog Trigger* section in Chapter 2. Analog trigger is available only on the AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-16XE-10, AT-AI-16XE-10, and the AT-MIO-64E-3.
		Output	As an output, this is the TRIG1 signal. In posttrigger data acquisition sequences, a low-to-high transition indicates the initiation of the acquisition sequence. In pretrigger applications, a low-to-high transition indicates the initiation of the pretrigger conversions.

Table 4-1. I/O Signal Summary, AT E Series (Continued)

Signal Name	Reference	Direction	Description
PFI1/TRIG2	DGND	Input	PFI1/Trigger 2—As an input, this is one of the PFIs.
		Output	As an output, this is the TRIG2 signal. In pretrigger applications, a low-to-high transition indicates the initiation of the posttrigger conversions. TRIG2 is not used in posttrigger applications.
PFI2/CONVERT*	DGND	Input	PFI2/Convert—As an input, this is one of the PFIs.
		Output	As an output, this is the CONVERT* signal. A high-to-low edge on CONVERT* indicates that an A/D conversion is occurring.
PFI3/GPCTR1_SOURCE	DGND	Input	PFI3/Counter 1 Source—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR1_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 1.
PFI4/GPCTR1_GATE	DGND	Input	PFI4/Counter 1 Gate—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR1_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 1.
GPCTR1_OUT	DGND	Output	Counter 1 Output—This output is from the general-purpose counter 1 output.
PFI5/UPDATE*	DGND	Input	PFI5/Update—As an input, this is one of the PFIs.
		Output	As an output, this is the UPDATE* signal. A high-to-low edge on UPDATE* indicates that the analog output primary group is being updated.
PFI6/WFTRIG	DGND	Input	PFI6/Waveform Trigger—As an input, this is one of the PFIs.
		Output	As an output, this is the WFTRIG signal. In timed analog output sequences, a low-to-high transition indicates the initiation of the waveform generation.

Table 4-1. I/O Signal Summary, AT E Series (Continued)

Signal Name	Reference	Direction	Description
PFI7/STARTSCAN	DGND	Input	PFI7/Start of Scan—As an input, this is one of the PFIs.
		Output	As an output, this is the STARTSCAN signal. This pin pulses once at the start of each analog input scan in the interval scan. A low-to-high transition indicates the start of the scan.
PFI8/GPCTR0_SOURCE	DGND	Input	PFI8/Counter 0 Source—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR0_SOURCE signal. This signal reflects the actual source connected to the general-purpose counter 0.
PFI9/GPCTR0_GATE	DGND	Input	PFI9/Counter 0 Gate—As an input, this is one of the PFIs.
		Output	As an output, this is the GPCTR0_GATE signal. This signal reflects the actual gate signal connected to the general-purpose counter 0.
GPCTR0_OUT	DGND	Output	Counter 0 Output—This output is from the general-purpose counter 0 output.
FREQ_OUT	DGND	Output	Frequency Output—This output is from the frequency generator output.

Table 4-2 shows the I/O signal summary for the AT-MIO-16E-1, AT-MIO-16E-2 and AT-MIO-64E-3.

Table 4-2. I/O Signal Summary, AT-MIO-16E-1, AT-MIO-16E-2, and AT-MIO-64E-3

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
ACH<0..63>	AI	100 GΩ in parallel with 100 pF	25/15	—	—	—	±200 pA
AISENSE, AISENSE2	AI	100 GΩ in parallel with 100 pF	25/15	—	—	—	±200 pA
AIGND	AO	—	—	—	—	—	—

Table 4-2. I/O Signal Summary, AT-MIO-16E-1, AT-MIO-16E-2, and AT-MIO-64E-3 (Continued)

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
DAC0OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at –10	20 V/µs	—
DAC1OUT	AO	0.1Ω	Short-circuit to ground	5 at 10	5 at –10	20 V/µs	—
EXTREF	AI	10 kΩ	25/15	—	—	—	—
AOGND	AO	—	—	—	—	—	—
DGND	DO	—	—	—	—	—	—
VCC	DO	0.1Ω	Short-circuit to ground	1A	—	—	—
DIO<0..7>	DIO	—	V_{cc} +0.5	13 at (V_{cc} -0.4)	24 at 0.4	1.1	50 kΩ pu[1]
SCANCLK	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
EXTSTROBE*	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI0/TRIG1	ADIO	10 kΩ	V_{cc} +0.5/±35	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu[2]
PFI1/TRIG2	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI2/CONVERT*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI3/GPCTR1_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI4/GPCTR1_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR1_OUT	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI5/UPDATE*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI6/WFTRIG	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI7/STARTSCAN	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI8/GPCTR0_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI9/GPCTR0_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu

Table 4-2. I/O Signal Summary, AT-MIO-16E-1, AT-MIO-16E-2, and AT-MIO-64E-3 (Continued)

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
GPCTR0_OUT	DO	—	—	3.5 at (V_{CC} -0.4)	5 at 0.4	1.5	50 kΩ pu
FREQ_OUT	DO	—	—	3.5 at (V_{CC}-0.4)	5 at 0.4	1.5	50 kΩ pu

[1]DIO <6..7> are also pulled down with a 50 kΩ resistor.
AI = Analog InputDIO = Digital Input/Outputpu = pullup
AO = Analog OutputDO = Digital OutputADIO = Analog/Digital Input/Output

[2]Also pulled down with a 10 kΩ resistor.

The tolerance on the 50 kΩ pullup and pulldown resistors is very large. Actual value may range between 17 kΩ and 100 kΩ.

Table 4-3 shows the I/O signal summary for the AT-MIO-16E-10 and AT-MIO-16DE-10.

Table 4-3. I/O Signal Summary, AT-MIO-16E-10 and AT-MIO-16DE-10

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
ACH<0..15>	AI	100 GΩ in parallel with 50 pF	35/25	—	—	—	±200 pA
AISENSE	AI	100 GΩ in parallel with 50 pF	35/25	—	—	—	±200 pA
AIGND	AO	—	—	—	—	—	—
DAC0OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at -10	15 V/µs	—
DAC1OUT	AO	0.1Ω	Short-circuit to ground	5 at 10	5 at -10	15 V/µs	—
EXTREF	AI	10 kΩ	35/25	—	—	—	—
AOGND	AO	—	—	—	—	—	—
DGND	DO	—	—	—	—	—	—

Table 4-3. I/O Signal Summary, AT-MIO-16E-10 and AT-MIO-16DE-10 (Continued)

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
VCC	DO	0.1Ω	Short-circuit to ground	1A	—	—	—
DIO<0..7>	DIO	—	V_{cc} +0.5	13 at (V_{cc} -0.4)	24 at 0.4	1.1	50 kΩ pu[1]
PA<0..7>	DIO	—	V_{cc} +0.5	2.5 at 3.9	2.5 at 0.4	5	100 kΩ pu
PB<0..7>	DIO	—	V_{cc} +0.5	2.5 at 3.9	2.5 at 0.4	5	100 kΩ pu
PC<0..7>	DIO	—	V_{cc} +0.5	2.5 at 3.9	2.5 at 0.4	5	100 kΩ pu
SCANCLK	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
EXTSTROBE*	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI0/TRIG1	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI1/TRIG2	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI2/CONVERT*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI3/GPCTR1_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI4/GPCTR1_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR1_OUT	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI5/UPDATE*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI6/WFTRIG	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI7/STARTSCAN	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI8/GPCTR0_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI9/GPCTR0_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc}-0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR0_OUT	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
FREQ_OUT	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu

[1]DIO <6..7> are also pulled down with a 50 kΩ resistor.
AI = Analog Input DIO = Digital Input/Output pu = pullup
AO = Analog Output DO = Digital Output

The tolerance on the 50 kΩ pullup and pulldown resistors is very large. Actual value may range between 17 kΩ and 100 kΩ.

Table 4-4 shows the I/O signal summary for the AT-MIO-16XE-10 and AT-AI-16XE-10.

Table 4-4. I/O Signal Summary, AT-MIO-16XE-10 and AT-AI-16XE-10

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
ACH<0..15>	AI	100 GΩ in parallel with 100 pF	25/15	—	—	—	±1 nA
AISENSE	AI	100 GΩ in parallel with 100 pF	25/15	—	—	—	±1 nA
AIGND	AO	—	—	—	—	—	—
DAC0OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at -10	5 V/µs	—
DAC1OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at -10	5 V/µs	—
AOGND	AO	—	—	—	—	—	—
DGND	DO	—	—	—	—	—	—
VCC	DO	0.1 Ω	Short-circuit to ground	1A	—	—	—
DIO<0..7>	DIO	—	V_{cc} +0.5	13 at (V_{cc} -0.4)	24 at 0.4	1.1	50 kΩ pu
SCANCLK	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
EXTSTROBE*	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI0/TRIG1	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	4.75 kΩ pu
PFI1/TRIG2	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI2/CONVERT*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI3/GPCTR1_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI4/GPCTR1_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR1_OUT	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu

Table 4-4. I/O Signal Summary, AT-MIO-16XE-10 and AT-AI-16XE-10 (Continued)

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
PFI5/UPDATE*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI6/WFTRIG	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI7/STARTSCAN	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI8/GPCTR0_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI9/GPCTR0_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR0_OUT	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
FREQ_OUT	DO	—	—	3.5 at (V_{cc}-0.4)	5 at 0.4	1.5	50 kΩ pu

AI = Analog Input DIO = Digital Input/Output pu = pullup
AO = Analog Output DO = Digital Output

The tolerance on the 50 kΩ pullup and pulldown resistors is very large. Actual value may range between 17 kΩ and 100 kΩ.

Table 4-5 shows the I/O signal summary for the AT-MIO-16XE-50.

Table 4-5. I/O Signal Summary, AT-MIO-16XE-50

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
ACH<0..15>	AI	20 GΩ in parallel with 100 pF	25/15	—	—	—	±3 nA
AISENSE	AI	20 GΩ in parallel with 100 pF	25/15	—	—	—	±3 nA
AIGND	AO	—	—	—	—	—	—
DAC0OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at -10	2 V/µs	—
DAC1OUT	AO	0.1 Ω	Short-circuit to ground	5 at 10	5 at -10	2 V/µs	—

Table 4-5. I/O Signal Summary, AT-MIO-16XE-50 (Continued)

Signal Name	Drive	Impedance Input/ Output	Protection (Volts) On/Off	Source (mA at V)	Sink (mA at V)	Rise Time (ns)	Bias
AOGND	AO	—	—	—	—	—	—
DGND	DO	—	—	—	—	—	—
VCC	DO	0.1 Ω	Short-circuit to ground	1A	—	—	—
DIO<0..7>	DIO	—	V_{cc} +0.5	13 at (V_{cc} -0.4)	24 at 0.4	1.1	50 kΩ pu[1]
SCANCLK	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
EXTSTROBE*	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI0/TRIG1	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI1/TRIG2	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI2/CONVERT*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI3/GPCTR1_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI4/GPCTR1_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR1_OUT	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI5/UPDATE*	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI6/WFTRIG	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI7/STARTSCAN	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI8/GPCTR0_SOURCE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
PFI9/GPCTR0_GATE	DIO	—	V_{cc} +0.5	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
GPCTR0_OUT	DO	—	—	3.5 at (V_{cc} -0.4)	5 at 0.4	1.5	50 kΩ pu
FREQ_OUT	DO	—	—	3.5 at (V_{cc}-0.4)	5 at 0.4	1.5	50 kΩ pu

[1]DIO <6..7> are also pulled down with a 50 kΩ resistor.
AI = Analog Input DIO = Digital Input/Output pu = pullup
AO = Analog Output DO = Digital Output

The tolerance on the 50 kΩ pullup and pulldown resistors is very large. Actual value may range between 17 kΩ and 100 kΩ.

Analog Input Signal Connections

- AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-16E-10, AT-MIO-16DE-10, AT-MIO-16XE-10, AT-AI-16XE-10, AT-MIO-16XE-50

  The analog input signals are ACH<0..15>, AISENSE, and AIGND. The ACH<0..15> signals are tied to the 16 analog input channels of your AT E Series board. In single-ended mode, signals connected to ACH<0..15> are routed to the positive input of the board PGIA. In differential mode, signals connected to ACH<0..7> are routed to the positive input of the PGIA, and signals connected to ACH<8..15> are routed to the negative input of the PGIA.

- AT-MIO-64E-3

  The analog input signals are ACH<0..63>, AISENSE, AISENSE2, and AIGND. The ACH<0..63> signals are tied to the 64 analog input channels of the AT-MIO-64E-3. In single-ended mode, signals connected to ACH<0..63> are routed to the positive input of the AT-MIO-64E-3 PGIA. In differential mode, signals connected to ACH<0..7, 16..23, 32..39, 48..55> are routed to the positive input of the PGIA, and signals connected to ACH<8..15, 24..31, 40..47, 56..63> are routed to the negative input of the PGIA.

Caution: ***Exceeding the differential and common-mode input ranges distorts your input signals. Exceeding the maximum input voltage rating can damage the AT E Series board and the PC. National Instruments is NOT liable for any damages resulting from such signal connections. The maximum input voltage ratings are listed in Tables 4-2 through 4-5 in the*** *Protection* ***column.***

In NRSE mode, the AISENSE and AISENSE2 signals are connected internally to the negative input of the AT E Series board PGIA when their corresponding channels are selected. In DIFF and RSE modes, these signals are left unconnected.

AIGND is an analog input common signal that is routed directly to the ground tie point on the AT E Series boards. You can use this signal for a general analog ground tie point to your AT E Series board if necessary.

Connection of analog input signals to your AT E Series board depends on the configuration of the analog input channels you are using and the

type of input signal source. With the different configurations, you can use the PGIA in different ways. Figure 4-4 shows a diagram of your AT E Series board PGIA.

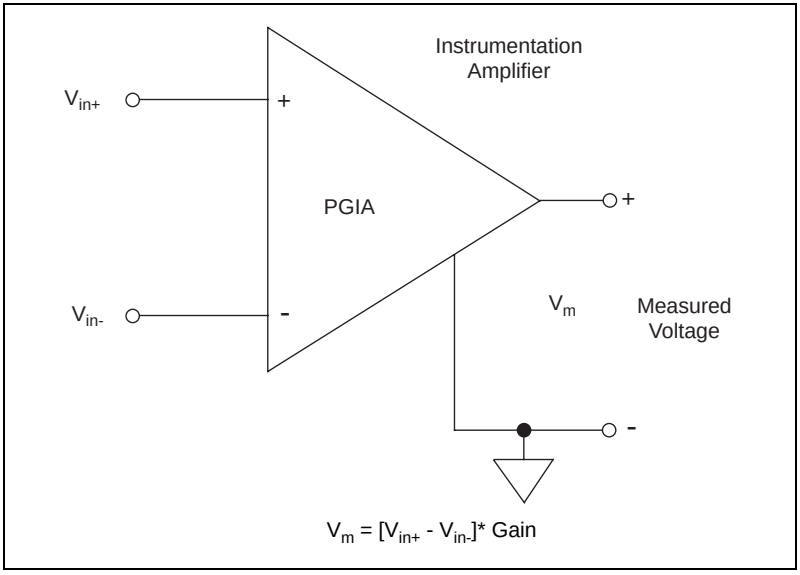


Figure 4-4. AT E Series PGIA

The PGIA applies gain and common-mode voltage rejection and presents high input impedance to the analog input signals connected to your AT E Series board. Signals are routed to the positive and negative inputs of the PGIA through input multiplexers on the board. The PGIA converts two input signals to a signal that is the difference between the two input signals multiplied by the gain setting of the amplifier. The amplifier output voltage is referenced to the ground for the board. Your AT E Series board A/D converter (ADC) measures this output voltage when it performs A/D conversions.

You must reference all signals to ground either at the source device or at the board. If you have a floating source, you should reference the signal to ground by using the RSE input mode or the DIFF input configuration with bias resistors. See the *Differential Connections for Nonreferenced or Floating Signal Sources* section later in this chapter. If you have a grounded source, you should not reference the signal to AIGND. You can avoid this reference by using DIFF or NRSE input configurations.

Types of Signal Sources

When configuring the input channels and making signal connections, you must first determine whether the signal sources are floating or ground-referenced. The following sections describe these two types of signals.

Floating Signal Sources

A floating signal source is one that is not connected in any way to the building ground system but, rather, has an isolated ground-reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolator outputs, and isolation amplifiers. An instrument or device that has an isolated output is a floating signal source. You must tie the ground reference of a floating signal to your AT E Series board analog input ground to establish a local or onboard reference for the signal. Otherwise, the measured input signal varies as the source floats out of the common-mode input range.

Ground-Referenced Signal Sources

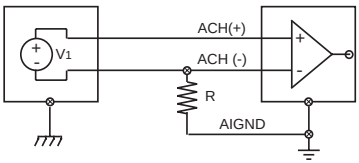
A ground-referenced signal source is one that is connected in some way to the building system ground and is, therefore, already connected to a common ground point with respect to the AT E Series board, assuming that the PC is plugged into the same power system. Nonisolated outputs of instruments and devices that plug into the building power system fall into this category.

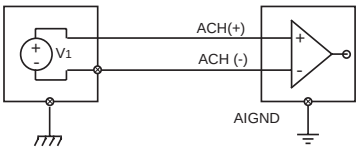
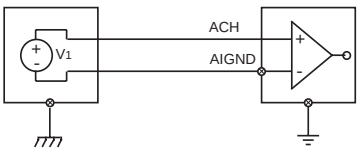
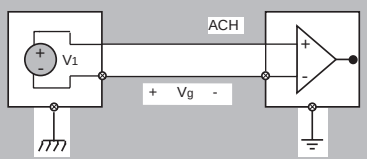
The difference in ground potential between two instruments connected to the same building power system is typically between 1 and 100 mV but can be much higher if power distribution circuits are not properly connected. If a grounded signal source is improperly measured, this difference may appear as an error in the measurement. The connection instructions for grounded signal sources are designed to eliminate this ground potential difference from the measured signal.

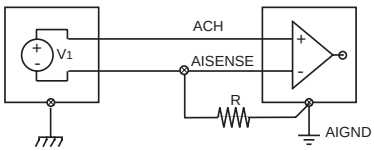
Input Configurations

You can configure your AT E Series board for one of three input modes—NRSE, RSE, or DIFF. The following sections discuss the use of single-ended and differential measurements and considerations for measuring both floating and ground-referenced signal sources.

Figure 4-5 summarizes the recommended input configuration for both types of signal sources.

<table>
<tr><th rowspan="2">Input</th><th colspan="2">Signal Source Type</th></tr>
<tr><th>Floating Signal Source
(Not Connected to Building Ground)</th><th>Grounded Signal Source</th></tr>
<tr><td></td><td>Examples
• Ungrounded Thermocouples
• Signal conditioning with isolated outputs
• Battery devices</td><td>Examples
• Plug-in instruments with nonisolated outputs</td></tr>
<tr><td>Differential (DIFF)</td><td> 

See text for information on bias resistors.</td><td> 
</td></tr>
<tr><td>Single-Ended — Ground Referenced (RSE)</td><td> 
</td><td>NOT RECOMMENDED
 

Ground-loop losses, V_g, are added to measured signal</td></tr>
<tr><td>Single-Ended — Nonreferenced (NRSE)</td><td> 

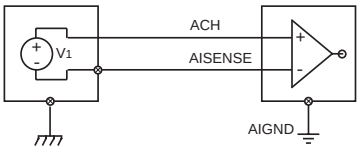
See text for information on bias resistors.</td><td> 
</td></tr>
</table>

Figure 4-5. Summary of Analog Input Connections

Differential Connection Considerations (DIFF Input Configuration)

A differential connection is one in which the AT E Series board analog input signal has its own reference signal or signal return path. These connections are available when the selected channel is configured in DIFF input mode. The input signal is tied to the positive input of the PGIA, and its reference signal, or return, is tied to the negative input of the PGIA.

When you configure a channel for differential input, each signal uses two multiplexer inputs—one for the signal and one for its reference signal. Therefore, with a differential configuration for every channel, up to eight analog input channels are available (up to 32 channels on the AT-MIO-64E-3).

You should use differential input connections for any channel that meets any of the following conditions:

- The input signal is low level (less than 1 V).
- The leads connecting the signal to the AT E Series board are greater than 10 ft (3 m).
- The input signal requires a separate ground-reference point or return signal.
- The signal leads travel through noisy environments.

Differential signal connections reduce picked-up noise and increase common-mode noise rejection. Differential signal connections also allow input signals to float within the common-mode limits of the PGIA.

Differential Connections for Ground-Referenced Signal Sources

Figure 4-6 shows how to connect a ground-referenced signal source to an AT E Series board channel configured in DIFF input mode.

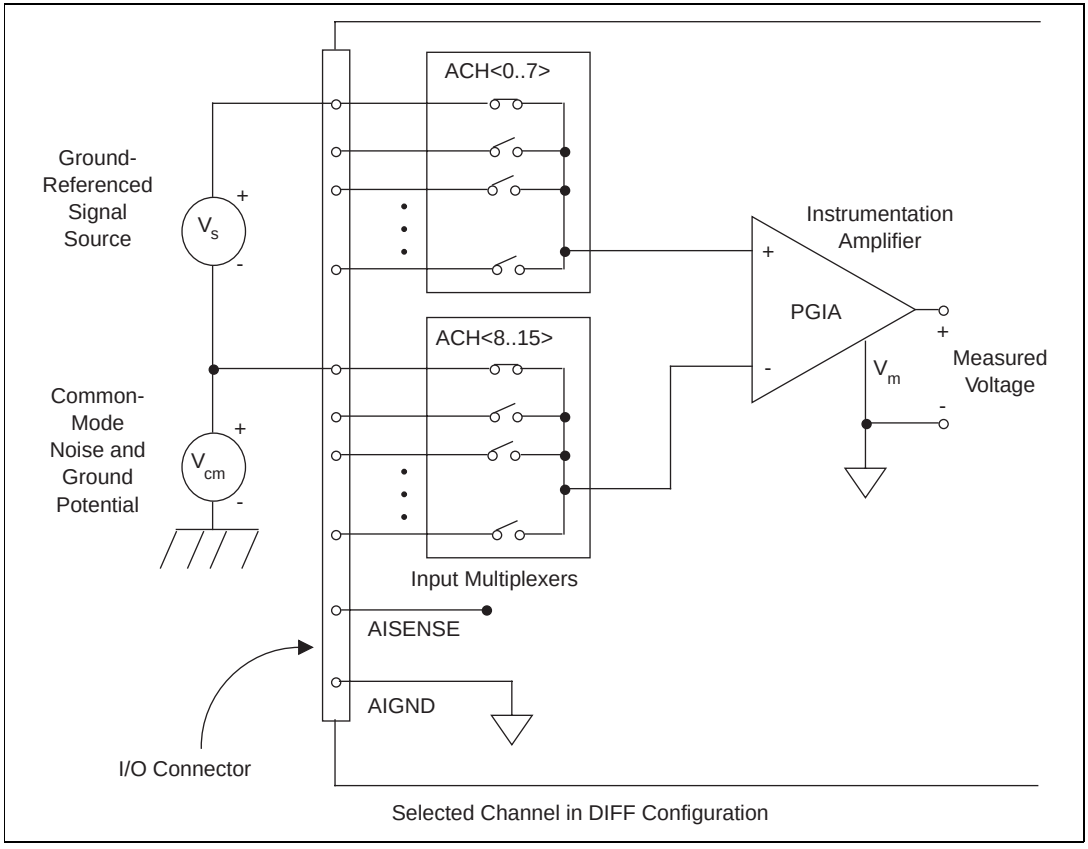


Figure 4-6. Differential Input Connections for Ground-Referenced Signals

With this type of connection, the PGIA rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the AT E Series board ground, shown as V_{cm} in Figure 4-6.

Differential Connections for Nonreferenced or Floating Signal Sources

Figure 4-7 shows how to connect a floating signal source to an AT E Series board channel configured in DIFF input mode.

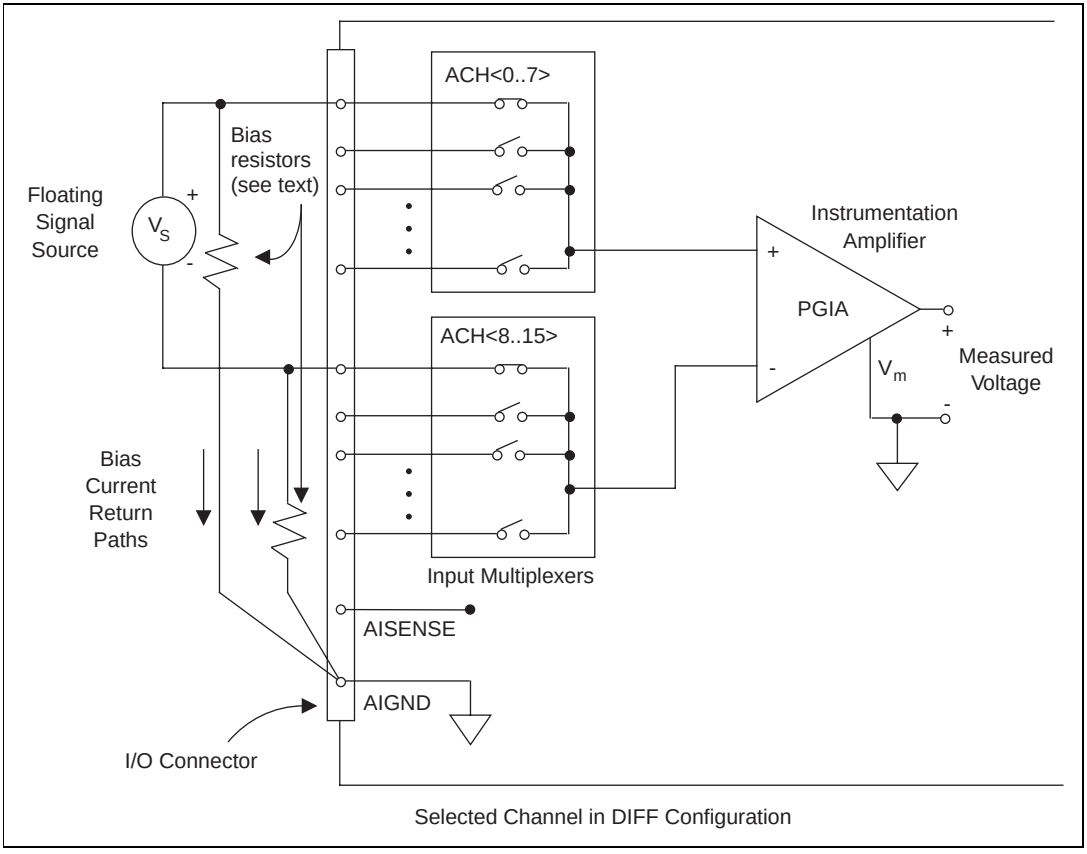


Figure 4-7. Differential Input Connections for Nonreferenced Signals

Figure 4-7 shows two bias resistors connected in parallel with the signal leads of a floating signal source. If you do not use the resistors and the source is truly floating, the source is not likely to remain within the common-mode signal range of the PGIA, and the PGIA will saturate, causing erroneous readings. You must reference the source to AIGND. The easiest way is simply to connect the positive side of the signal to the positive input of the PGIA and connect the negative side of the signal to AIGND as well as to the negative input of the PGIA, without

any resistors at all. This connection works well for DC-coupled sources with low source impedance (less than 100 Ω).

However, for larger source impedances, this connection leaves the differential signal path significantly out of balance. Noise that couples electrostatically onto the positive line does not couple onto the negative line because it is connected to ground. Hence, this noise appears as a differential-mode signal instead of a common-mode signal, and so the PGIA does not reject it. In this case, instead of directly connecting the negative line to AIGND, connect it to AIGND through a resistor that is about 100 times the equivalent source impedance. The resistor puts the signal path nearly in balance, so that about the same amount of noise couples onto both connections, yielding better rejection of electrostatically coupled noise. Also, this configuration does not load down the source (other than the very high input impedance of the PGIA).

You can fully balance the signal path by connecting another resistor of the same value between the positive input and AIGND, as shown in Figure 4-7. This fully balanced configuration offers slightly better noise rejection but has the disadvantage of loading the source down with the series combination (sum) of the two resistors. If, for example, the source impedance is 2 kΩ and each of the two resistors is 100 kΩ, the resistors load down the source with 200 kΩ and produce a –1% gain error.

Both inputs of the PGIA require a DC path to ground in order for the PGIA to work. If the source is AC coupled (capacitively coupled), the PGIA needs a resistor between the positive input and AIGND. If the source has low impedance, choose a resistor that is large enough not to significantly load the source but small enough not to produce significant input offset voltage as a result of input bias current (typically 100 kΩ to 1 MΩ). In this case, you can tie the negative input directly to AIGND. If the source has high output impedance, you should balance the signal path as previously described using the same value resistor on both the positive and negative inputs; you should be aware that there is some gain error from loading down the source.

Single-Ended Connection Considerations

A single-ended connection is one in which the AT E Series board analog input signal is referenced to a ground that can be shared with other input signals. The input signal is tied to the positive input of the PGIA, and the ground is tied to the negative input of the PGIA.

When every channel is configured for single-ended input, up to 16 analog input channels are available (up to 64 channels on the AT-MIO-64E-3).

You can use single-ended input connections for any input signal that meets the following conditions:

- The input signal is high level (greater than 1 V).
- The leads connecting the signal to the AT E Series board are less than 10 ft (3 m).
- The input signal can share a common reference point with other signals.

DIFF input connections are recommended for greater signal integrity for any input signal that does not meet the preceding conditions.

You can software configure the AT E Series board channels for two different types of single-ended connections—RSE configuration and NRSE configuration. The RSE configuration is used for floating signal sources; in this case, the AT E Series board provides the reference ground point for the external signal. The NRSE input configuration is used for ground-referenced signal sources; in this case, the external signal supplies its own reference ground point and the AT E Series board should not supply one.

In single-ended configurations, more electrostatic and magnetic noise couples into the signal connections than in differential configurations. The coupling is the result of differences in the signal path. Magnetic coupling is proportional to the area between the two signal conductors. Electrical coupling is a function of how much the electric field differs between the two conductors.

Single-Ended Connections for Floating Signal Sources (RSE Configuration)

Figure 4-8 shows how to connect a floating signal source to an AT E Series board channel configured for RSE mode.

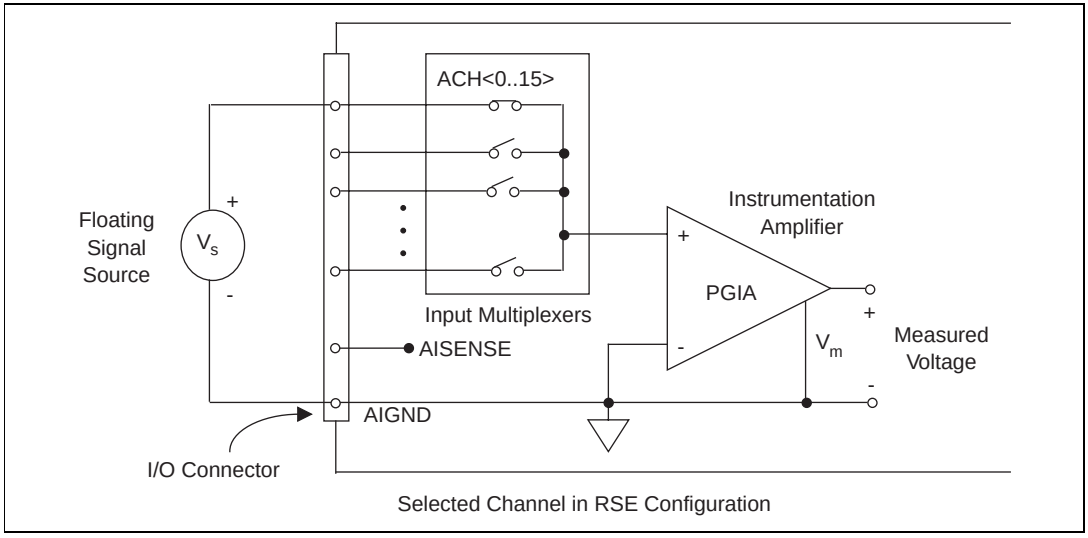


Figure 4-8. Single-Ended Input Connections for Nonreferenced or Floating Signals

Single-Ended Connections for Grounded Signal Sources (NRSE Configuration)

To measure a grounded signal source with a single-ended configuration, you must configure your AT E Series board in the NRSE input configuration. The signal is then connected to the positive input of the AT E Series PGIA, and the signal local ground reference is connected to the negative input of the PGIA. The ground point of the signal should, therefore, be connected to the AISENSE pin. Any potential difference between the AT E Series ground and the signal ground appears as a common-mode signal at both the positive and negative inputs of the PGIA, and this difference is rejected by the amplifier. If the input circuitry of an AT E Series board were referenced to ground, in this situation as in the RSE input configuration, this difference in ground potentials would appear as an error in the measured voltage.

Figure 4-9 shows how to connect a grounded signal source to an AT E Series board channel configured for NRSE mode.

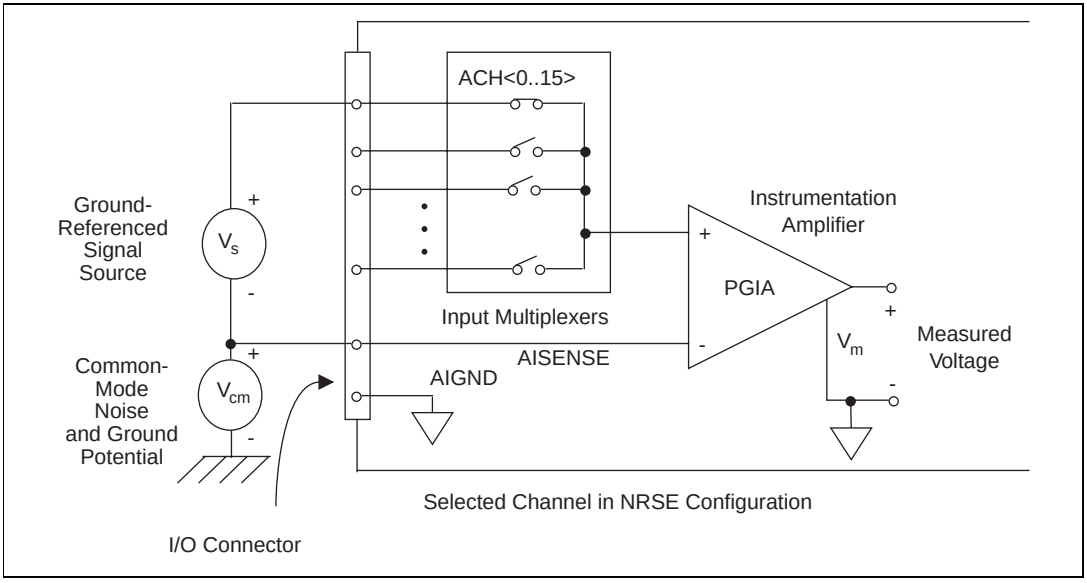


Figure 4-9. Single-Ended Input Connections for Ground-Referenced Signal

Common-Mode Signal Rejection Considerations

Figures 4-6 and 4-9 show connections for signal sources that are already referenced to some ground point with respect to the AT E Series board. In these cases, the PGIA can reject any voltage caused by ground potential differences between the signal source and the board. In addition, with differential input connections, the PGIA can reject common-mode noise pickup in the leads connecting the signal sources to the board. The PGIA can reject common-mode signals as long as V^+_{in} and $V-_{in}$ are both within ±11 V of AIGND. The AT-MIO-16XE-50 has the additional restriction that (V^+_{in} + $V-_{in}$) added to the gain times (V^+_{in} – $V-_{in}$) must be within ±26 V of AIGND. At gains of 10 and 100, this is roughly equivalent to restricting the two input voltages to within ±8 V of AIGND.

Analog Output Signal Connections

The analog output signals are DAC0OUT, DAC1OUT, EXTREF, and AOGND.

☞ **Note:** ***DAC0OUT and DAC1OUT are not available on the AT-AI-16XE-10. EXTREF is not available on the AT-MIO-16XE-10, AT-AI-16XE-10, or AT-MIO-16XE-50.***

DAC0OUT is the voltage output signal for analog output channel 0. DAC1OUT is the voltage output signal for analog output channel 1.

EXTREF is the external reference input for both analog output channels. You must configure each analog output channel individually for external reference selection in order for the signal applied at the external reference input to be used by that channel. If you do not specify an external reference, the channel will use the internal reference.

☞ **Note:** ***You cannot use an external analog output reference with the AT-MIO-16XE-10, AT-AI-16XE-10, or AT-MIO-16XE-50.***

Analog output configuration options are explained in the *Analog Output* section in Chapter 3, *Hardware Overview*. The following ranges and ratings apply to the EXTREF input:

- Usable input voltage range: ±11 V peak with respect to AOGND
- Absolute maximum ratings: ±15 V peak with respect to AOGND

AOGND is the ground reference signal for both analog output channels and the external reference signal.

Figure 4-10 shows how to make analog output connections and the external reference input connection to your AT E Series board.

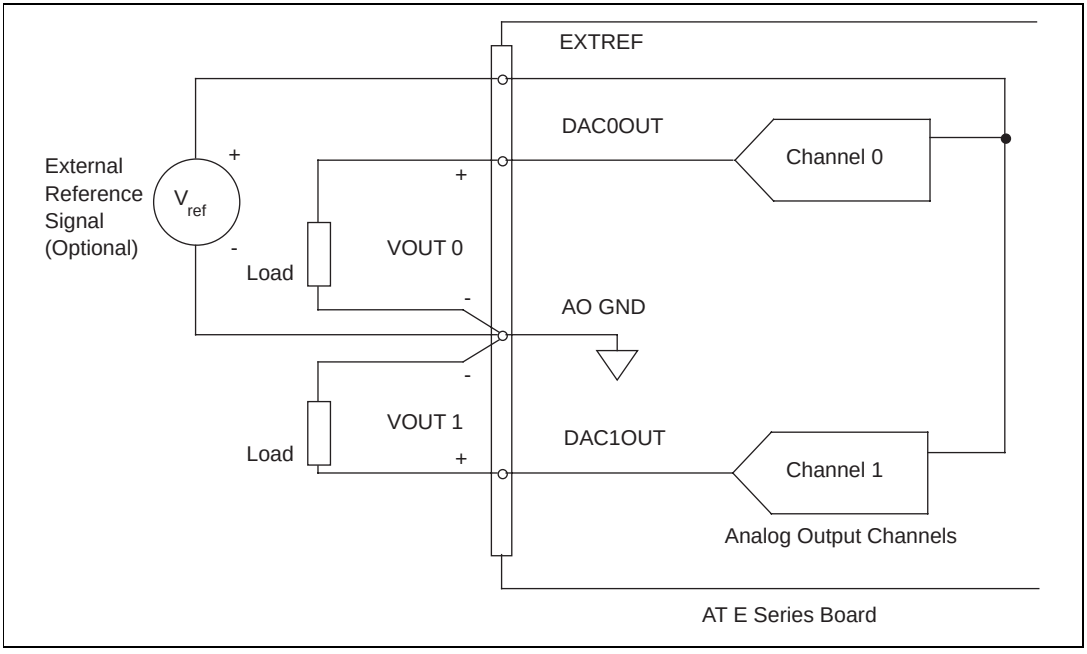


Figure 4-10. Analog Output Connections

The external reference signal can be either a DC or an AC signal. The board multiplies this reference signal by the DAC code (divided by the full-scale DAC code) to generate the output voltage.

Digital I/O Signal Connections

The digital I/O signals are DIO<0..7> and DGND. DIO<0..7> are the signals making up the DIO port, and DGND is the ground reference signal for the DIO port. You can program all lines individually to be inputs or outputs. The AT-MIO-16DE-10 has 24 additional DIO lines, configured as three 8-bit ports: PA<0..7>, PB<0..7>, and PC<0..7>. You can configure each port for both input and output in various combinations, with some handshaking capabilities.

Caution: ***Exceeding the maximum input voltage ratings, which are listed in Tables 4-2 through 4-5, can damage the AT E Series board and the PC. National Instruments is NOT liable for any damages resulting from such signal connections.***

Figure 4-11 shows signal connections for three typical digital I/O applications.

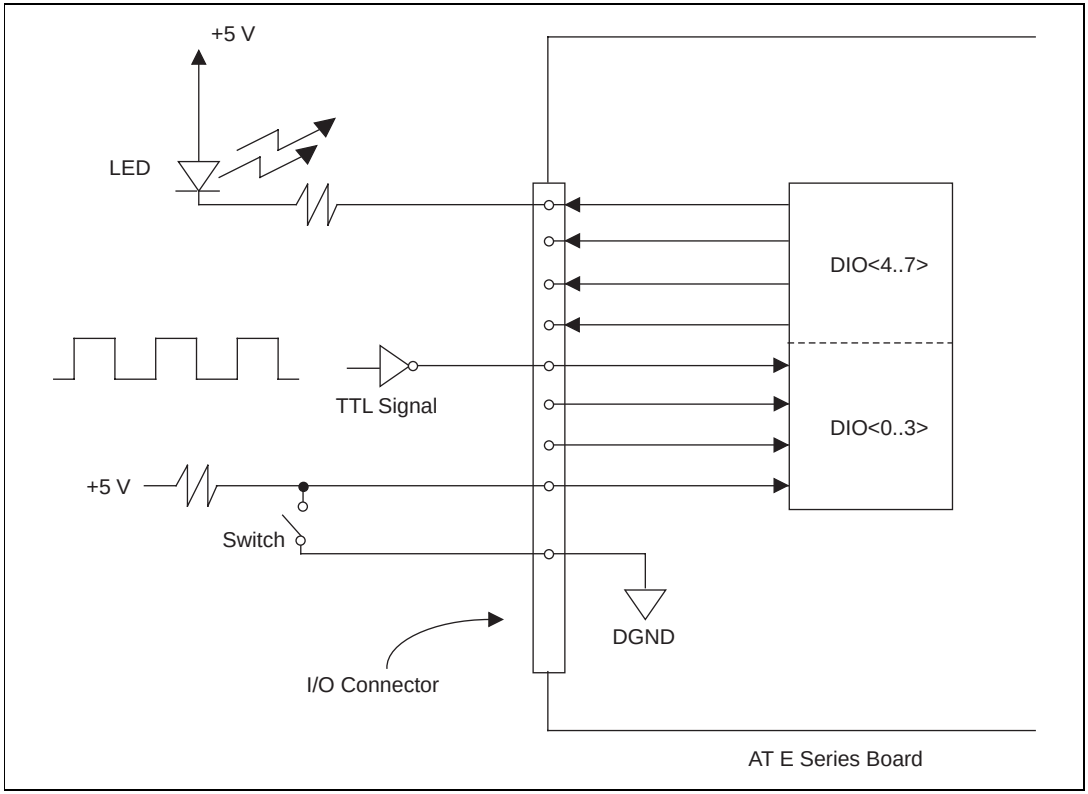


Figure 4-11. Digital I/O Connections

Figure 4-11 shows DIO<0..3> configured for digital input and DIO<4..7> configured for digital output. Digital input applications include receiving TTL signals and sensing external device states such as the state of the switch shown in the figure. Digital output applications include sending TTL signals and driving external devices such as the LED shown in the figure.

Power Connections

Two pins on the I/0 connector supply +5 V from the PC power supply via a self-resetting fuse. The fuse will reset automatically within a few seconds after the overcurrent condition is removed. These pins are referenced to DGND and can be used to power external digital circuitry. The combined total power rating for both pins should be between +4.65 VDC to +5.25 VDC at 1 A.

Caution: ***Under no circumstances should you connect these +5 V power pins directly to analog or digital ground or to any other voltage source on the AT E Series board or any other device. Doing so can damage the AT E Series board and the PC. National Instruments is NOT liable for damages resulting from such a connection.***

Timing Connections

Caution: ***Exceeding the maximum input voltage ratings, which are listed in Tables 4-2 through 4-5, can damage the AT E Series board and the PC. National Instruments is NOT liable for any damages resulting from such signal connections.***

All external control over the timing of your AT E Series board is routed through the 10 programmable function inputs labeled PFI0 through PFI9. These signals are explained in detail in the next section, *Programmable Function Input Connections*. These PFIs are bidirectional; as outputs they are not programmable and reflect the state of many data acquisition, waveform generation, and general-purpose timing signals. There are five other dedicated outputs for the remainder of the timing signals. As inputs, the PFI signals are programmable and can control any data acquisition, waveform generation, and general-purpose timing signals.

The data acquisition signals are explained in the *Data Acquisition Timing Connections* section later in this chapter. The waveform generation signals are explained in the *Waveform Generation Timing Connections* section later in this chapter. The general-purpose timing signals are explained in the *General-Purpose Timing Signal Connections* section later in this chapter.

All digital timing connections are referenced to DGND. This reference is demonstrated in Figure 4-12, which shows how to connect an

external TRIG1 source and an external CONVERT* source to two of the AT E Series board PFI pins.

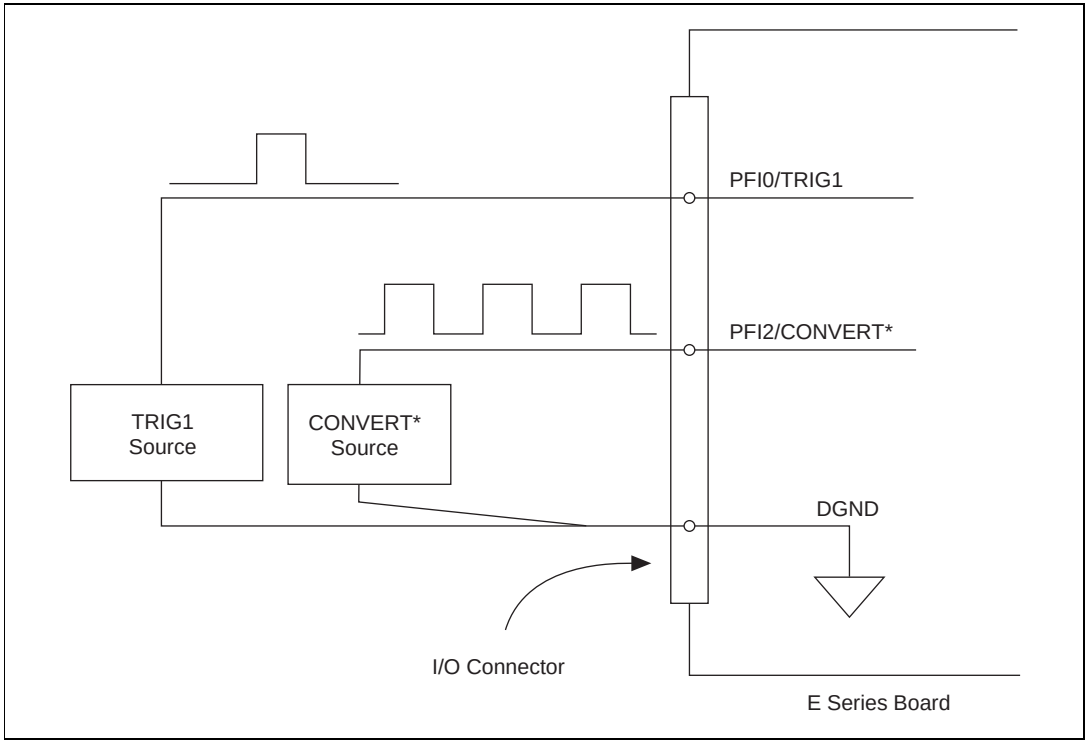


Figure 4-12. Timing I/O Connections

Programmable Function Input Connections

There are a total of 13 internal timing signals that you can externally control from the PFI pins. The source for each of these signals is software selectable from any of the PFIs when you want external control. This flexible routing scheme reduces the need to change the physical wiring to the board I/O connector for different applications requiring alternative wiring.

You can individually enable each of the PFI pins to output a specific internal timing signal. For example, if you need the CONVERT* signal as an output on the I/O connector, software can turn on the output driver for the PFI2/CONVERT* pin. You must be careful not to drive a PFI signal externally when it is configured as an output.

As an input, you can individually configure each PFI for edge or level detection and for polarity selection, as well. You can use the polarity selection for any of the 13 timing signals, but the edge or level detection will depend upon the particular timing signal being controlled. The detection requirements for each timing signal are listed within the section that discusses that individual signal.

In edge-detection mode, the minimum pulse width required is 10 ns. This applies for both rising-edge and falling-edge polarity settings. There is no maximum pulse-width requirement in edge-detect mode.

In level-detection mode, there are no minimum or maximum pulse-width requirements imposed by the PFIs themselves, but there may be limits imposed by the particular timing signal being controlled. These requirements are listed later in this chapter.

Data Acquisition Timing Connections

The data acquisition timing signals are SCANCLK, EXTSTROBE*, TRIG1, TRIG2, STARTSCAN, CONVERT*, AIGATE, and SISOURCE.

Posttriggered data acquisition allows you to view only data that is acquired after a trigger event is received. A typical posttriggered data acquisition sequence is shown in Figure 4-13. Pretriggered data acquisition allows you to view data that is acquired before the trigger of interest in addition to data acquired after the trigger. Figure 4-14 shows a typical pretriggered data acquisition sequence. The description for each signal shown in these figures is included later in this chapter.

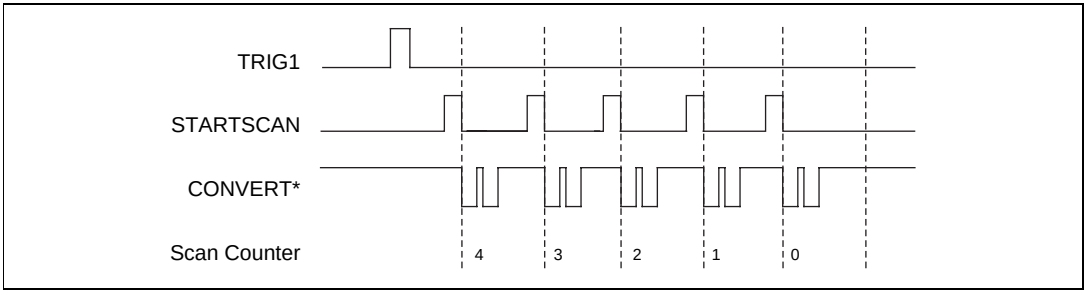


Figure 4-13. Typical Posttriggered Acquisition

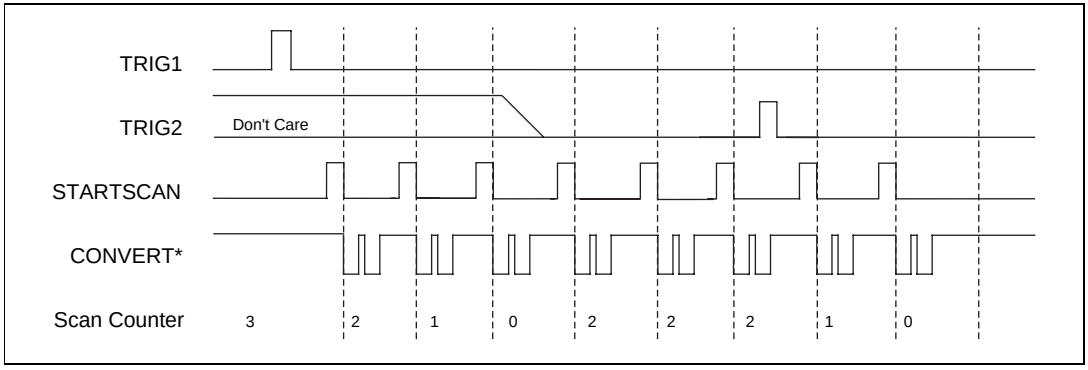


Figure 4-14. Typical Pretriggered Acquisition

SCANCLK Signal

SCANCLK is an output-only signal that generates a pulse with the leading edge occurring approximately 50 to 100 ns after an A/D conversion begins. The polarity of this output is software selectable but is typically configured so that a low-to-high leading edge can clock external analog input multiplexers indicating when the input signal has been sampled and can be removed. This signal has a 400 to 500 ns pulse width and is software enabled. Figure 4-15 shows the timing for the SCANCLK signal.

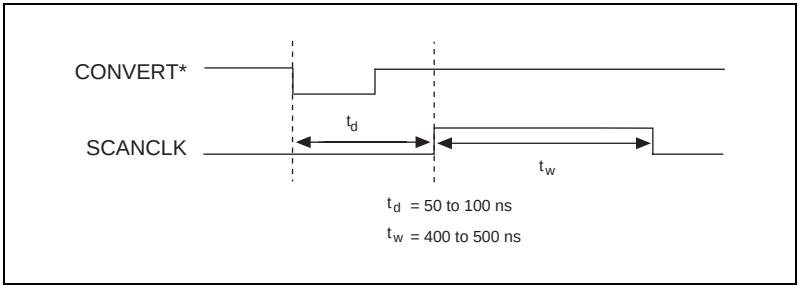


Figure 4-15. SCANCLK Signal Timing

EXTSTROBE* Signal

EXTSTROBE* is an output-only signal that generates either a single pulse or a sequence of eight pulses in the hardware-strobe mode. An external device can use this signal to latch signals or to trigger events. In the single-pulse mode, software controls the level of the EXTSTROBE* signal. A 10 µs and a 1.2 µs clock are available for generating a sequence of eight pulses in the hardware-strobe mode. Figure 4-16 shows the timing for the hardware-strobe mode EXTSTROBE* signal.

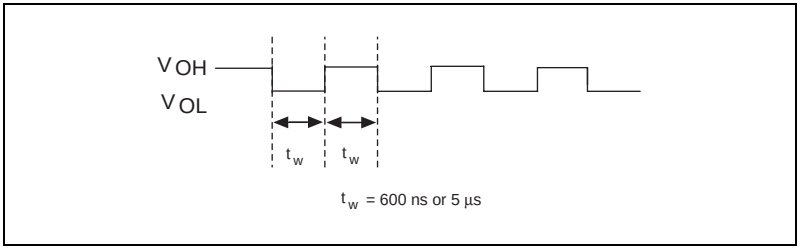


Figure 4-16. EXTSTROBE* Signal Timing

TRIG1 Signal

Any PFI pin can externally input the TRIG1 signal, which is available as an output on the PFI0/TRIG1 pin.

Refer to Figures 4-13 and 4-14 for the relationship of TRIG1 to the data acquisition sequence.

As an input, the TRIG1 signal is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG1 and configure the polarity selection for either rising or falling edge. The selected edge of the TRIG1 signal starts the data acquisition sequence for both posttriggered and pretriggered acquisitions. The AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-16XE-10, AT-AI-16XE-10, and AT-MIO-64E-3 support analog triggering on the PFI0/TRIG1 pin. See Chapter 3, *Hardware Overview*, for more information on analog triggering.

As an output, the TRIG1 signal reflects the action that initiates a data acquisition sequence. This is true even if the acquisition is being externally triggered by another PFI. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.

Figures 4-17 and 4-18 show the input and output timing requirements for the TRIG1 signal.

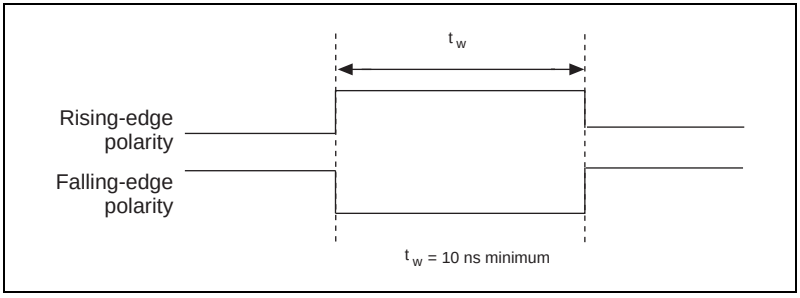


Figure 4-17. TRIG1 Input Signal Timing

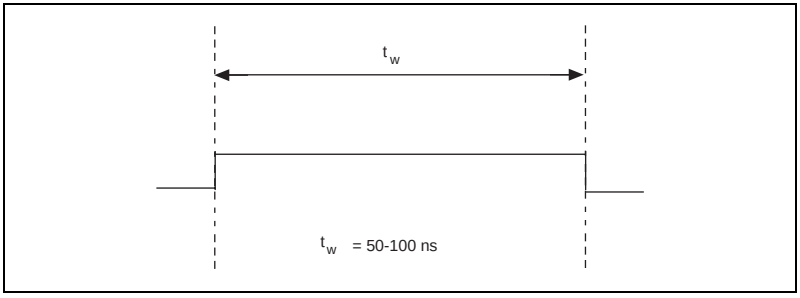


Figure 4-18. TRIG1 Output Signal Timing

The board also uses the TRIG1 signal to initiate pretriggered data acquisition operations. In most pretriggered applications, the TRIG1 signal is generated by a software trigger. Refer to the TRIG2 signal description for a complete description of the use of TRIG1 and TRIG2 in a pretriggered data acquisition operation.

TRIG2 Signal

Any PFI pin can externally input the TRIG2 signal, which is available as an output on the PFI1/TRIG2 pin.

Refer to Figure 4-13 for the relationship of TRIG2 to the data acquisition sequence.

As an input, the TRIG2 signal is configured in the edge-detection mode. You can select any PFI pin as the source for TRIG2 and configure the polarity selection for either rising or falling edge. The selected edge of the TRIG2 signal initiates the posttriggered phase of a pretriggered

acquisition sequence. In pretriggered mode, the TRIG1 signal initiates the data acquisition. The scan counter indicates the minimum number of scans before TRIG2 can be recognized. After the scan counter decrements to zero, it is loaded with the number of posttrigger scans to acquire while the acquisition continues. The board ignores the TRIG2 signal if it is asserted prior to the scan counter decrementing to zero. After the selected edge of TRIG2 is received, the board will acquire a fixed number of scans and the acquisition will stop. This mode acquires data both before and after receiving TRIG2.

As an output, the TRIG2 signal reflects the posttrigger in a pretriggered acquisition sequence. This is true even if the acquisition is being externally triggered by another PFI. The TRIG2 signal is not used in posttriggered data acquisition. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.

Figures 4-19 and 4-20 show the input and output timing requirements for the TRIG2 signal.

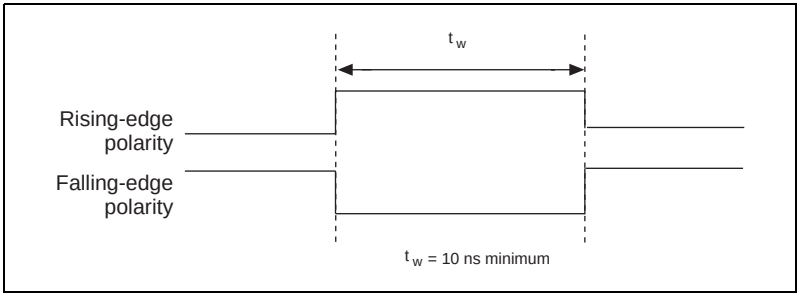


Figure 4-19. TRIG2 Input Signal Timing

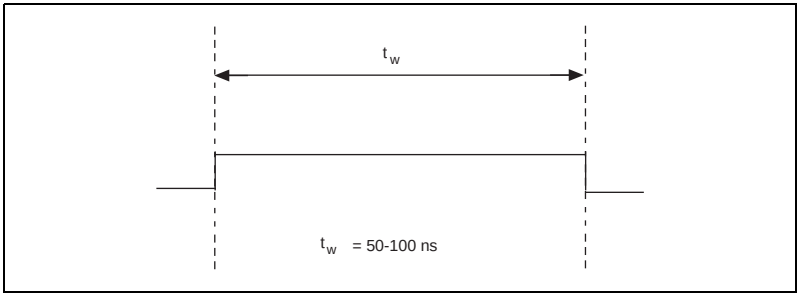


Figure 4-20. TRIG2 Output Signal Timing

STARTSCAN Signal

Any PFI pin can externally input the STARTSCAN signal, which is available as an output on the PFI7/STARTSCAN pin.

Refer to Figures 4-13 and 4-14 for the relationship of STARTSCAN to the data acquisition sequence.

As an input, the STARTSCAN signal is configured in the edge-detection mode. You can select any PFI pin as the source for STARTSCAN and configure the polarity selection for either rising or falling edge. The selected edge of the STARTSCAN signal initiates a scan. The sample interval counter is started if you select internally triggered CONVERT*.

As an output, the STARTSCAN signal reflects the actual start pulse that initiates a scan. This is true even if the starts are being externally triggered by another PFI. You have two output options. The first is an active high pulse with a pulse width of 50 to 100 ns, which indicates the start of the scan. The second action is an active high pulse that terminates at the start of the last conversion in the scan, which indicates a scan in progress. STARTSCAN will be deserted t_{off} after the last conversion in the scan is initiated. This output is set to tri-state at startup.

Figures 4-21 and 4-22 show the input and output timing requirements for the STARTSCAN signal

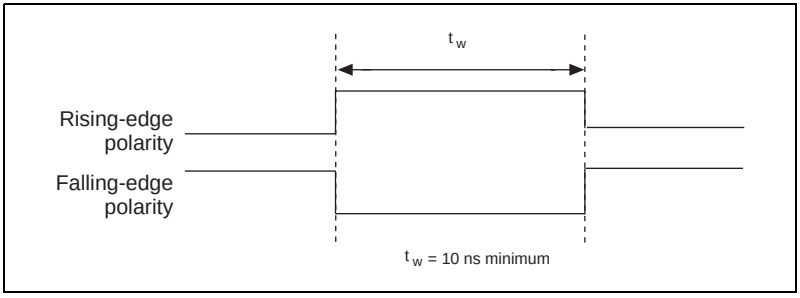


Figure 4-21. STARTSCAN Input Signal Timing

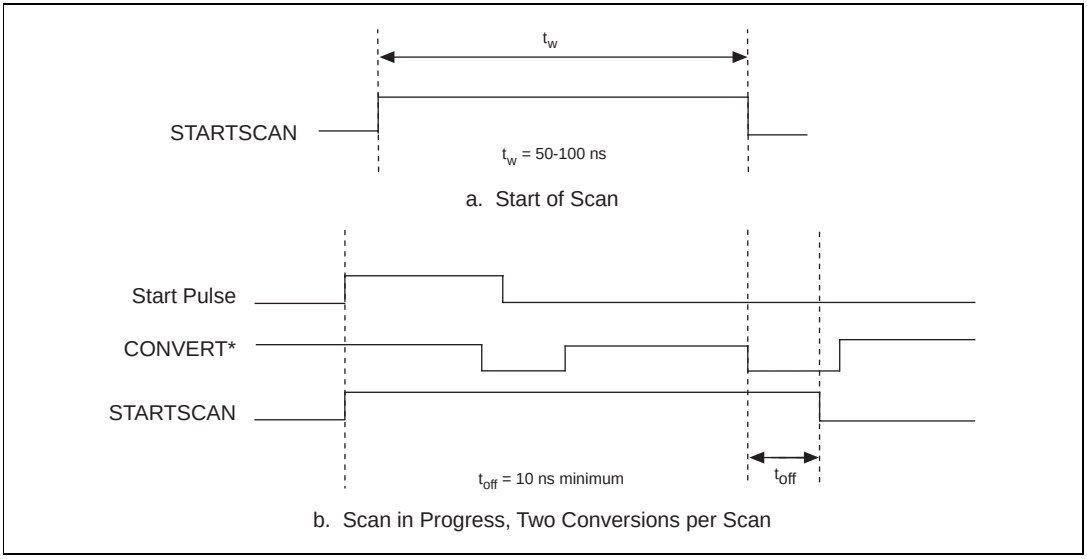


Figure 4-22. STARTSCAN Output Signal Timing

The CONVERT* pulses are masked off until the board generates the STARTSCAN signal. If you are using internally generated conversions, the first CONVERT* will appear when the onboard sample interval counter reaches zero. If you select an external CONVERT*, the first external pulse after STARTSCAN will generate a conversion. The STARTSCAN pulses should be separated by at least one scan period.

A counter on your AT E Series board internally generates the STARTSCAN signal unless you select some external source. This counter is started by the TRIG1 signal and is stopped either by software or by the sample counter.

Scans generated by either an internal or external STARTSCAN signal are inhibited unless they occur within a data acquisition sequence. Scans occurring within a data acquisition sequence may be gated by either the hardware (AIGATE) signal or software command register gate.

CONVERT* Signal

Any PFI pin can externally input the CONVERT* signal, which is available as an output on the PFI2/CONVERT* pin.

Refer to Figures 4-13 and 4-14 for the relationship of CONVERT* to the data acquisition sequence.

As an input, the CONVERT* signal is configured in the edge-detection mode. You can select any PFI pin as the source for CONVERT* and configure the polarity selection for either rising or falling edge. The selected edge of the CONVERT* signal initiates an A/D conversion.

As an output, the CONVERT* signal reflects the actual convert pulse that is connected to the ADC. This is true even if the conversions are being externally generated by another PFI. The output is an active low pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.

Figures 4-23 and 4-24 show the input and output timing requirements for the CONVERT* signal.

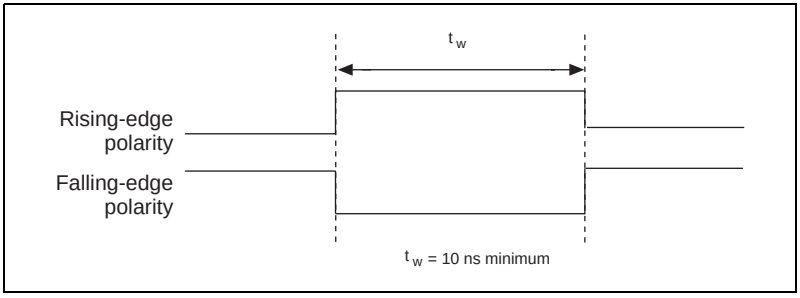


Figure 4-23. CONVERT* Input Signal Timing

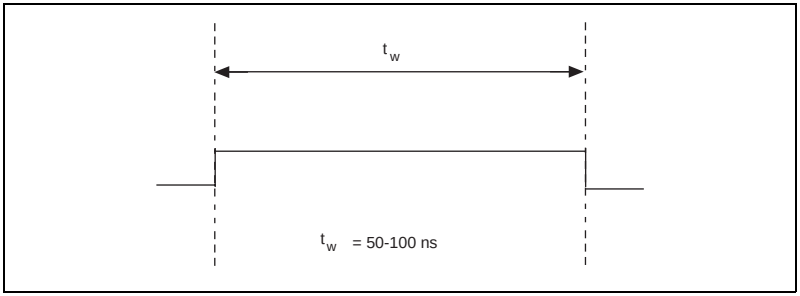


Figure 4-24. CONVERT* Output Signal Timing

The ADC switches to hold mode within 60 ns of the selected edge. This hold-mode delay time is a function of temperature and does not vary from one conversion to the next. Separate the CONVERT* pulses by at least one conversion period.

The sample interval counter on the AT E Series board normally generates the CONVERT* signal unless you select some external source. The counter is started by the STARTSCAN signal and continues to count down and reload itself until the scan is finished. It then reloads itself in readiness for the next STARTSCAN pulse.

A/D conversions generated by either an internal or external CONVERT* signal are inhibited unless they occur within a data acquisition sequence. Scans occurring within a data acquisition sequence may be gated by either the hardware (AIGATE) signal or software command register gate.

AIGATE Signal

Any PFI pin can externally input the AIGATE signal, which is not available as an output on the I/O connector. The AIGATE signal can mask off scans in a data acquisition sequence. You can configure the PFI pin you select as the source for the AIGATE signal in either the level-detection or edge-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

In the level-detection mode if AIGATE is active, the STARTSCAN signal is masked off and no scans can occur. In the edge-detection mode, the first active edge disables the STARTSCAN signal, and the second active edge enables STARTSCAN.

The AIGATE signal can neither stop a scan in progress nor continue a previously gated-off scan; in other words, once a scan has started, AIGATE does not gate off conversions until the beginning of the next scan and, conversely, if conversions are being gated off, AIGATE does not gate them back on until the beginning of the next scan.

SISOURCE Signal

Any PFI pin can externally input the SISOURCE signal, which is not available as an output on the I/O connector. The onboard scan interval counter uses the SISOURCE signal as a clock to time the generation of the STARTSCAN signal. You must configure the PFI pin you select as the source for the SISOURCE signal in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low.

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase generates the SISOURCE signal unless you select some external source. Figure 4-25 shows the timing requirements for the SISOURCE signal.

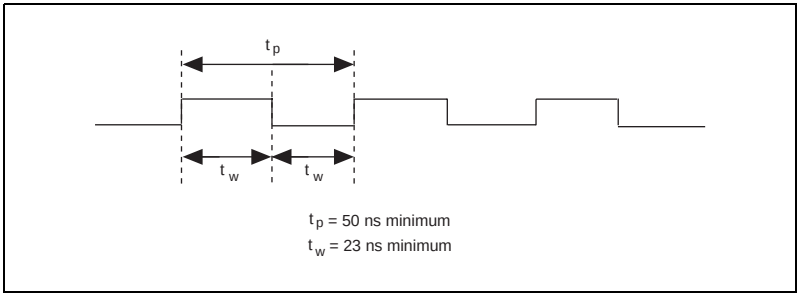


Figure 4-25. SISOURCE Signal Timing

Waveform Generation Timing Connections

The analog group defined for your AT E Series board is controlled by WFTRIG, UPDATE*, and UISOURCE.

WFTRIG Signal

Any PFI pin can externally input the WFTRIG signal, which is available as an output on the PFI6/WFTRIG pin.

As an input, the WFTRIG signal is configured in the edge-detection mode. You can select any PFI pin as the source for WFTRIG and configure the polarity selection for either rising or falling edge. The selected edge of the WFTRIG signal starts the waveform generation for the DACs. The update interval (UI) counter is started if you select internally generated UPDATE*.

As an output, the WFTRIG signal reflects the trigger that initiates waveform generation. This is true even if the waveform generation is being externally triggered by another PFI. The output is an active high pulse with a pulse width of 50 to 100 ns. This output is set to tri-state at startup.

Figures 4-26 and 4-27 show the input and output timing requirements for the WFTRIG signal.

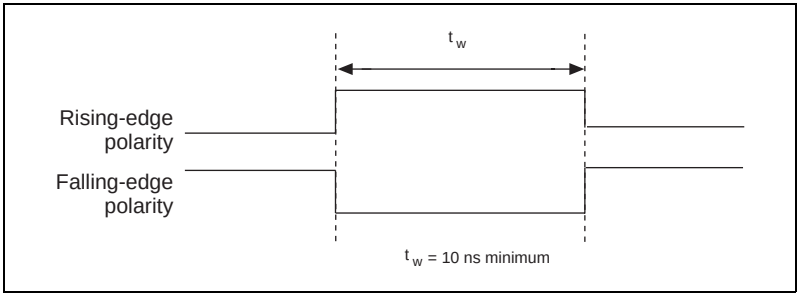


Figure 4-26. WFTRIG Input Signal Timing

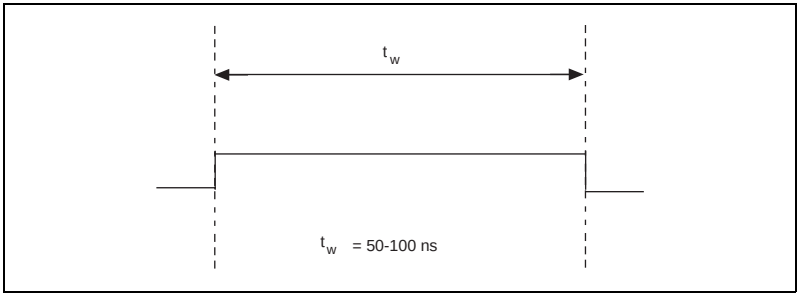


Figure 4-27. WFTRIG Output Signal Timing

UPDATE* Signal

Any PFI pin can externally input the UPDATE* signal, which is available as an output on the PFI5/UPDATE* pin.

As an input, the UPDATE* signal is configured in the edge-detection mode. You can select any PFI pin as the source for UPDATE* and configure the polarity selection for either rising or falling edge. The selected edge of the UPDATE* signal updates the outputs of the DACs. In order to use UPDATE*, you must set the DACs to posted-update mode.

As an output, the UPDATE* signal reflects the actual update pulse that is connected to the DACs. This is true even if the updates are being externally generated by another PFI. The output is an active low pulse with a pulse width of 300 to 350 ns. This output is set to tri-state at startup.

When using an external UPDATE signal, you must apply at least one more external update pulse than the number of points that you want to generate. This is necessary for proper hardware operation, otherwise the board will not indicate that the waveform generation is complete.

Figures 4-28 and 4-29 show the input and output timing requirements for the UPDATE* signal.

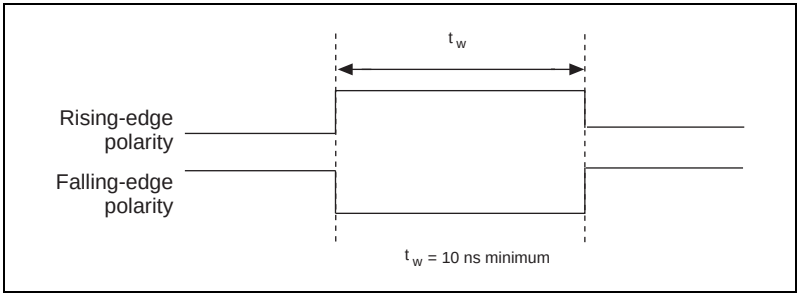


Figure 4-28. UPDATE* Input Signal Timing

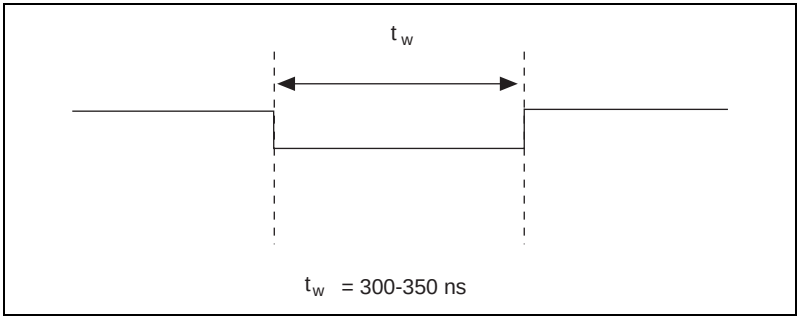


Figure 4-29. UPDATE* Output Signal Timing

The DACs are updated within 100 ns of the leading edge. Separate the UPDATE* pulses with enough time that new data can be written to the DAC latches.

The AT E Series board UI counter normally generates the UPDATE* signal unless you select some external source. The UI counter is started by the WFTRIG signal and can be stopped by software or the internal Buffer Counter.

D/A conversions generated by either an internal or external UPDATE* signal do not occur when gated by the software command register gate.

UISOURCE Signal

Any PFI pin can externally input the UISOURCE signal, which is not available as an output on the I/O connector. The UI counter uses the UISOURCE signal as a clock to time the generation of the UPDATE* signal. You must configure the PFI pin you select as the source for the UISOURCE signal in the level-detection mode. You can configure the polarity selection for the PFI pin for either active high or active low. Figure 4-30 shows the timing requirements for the UISOURCE signal.

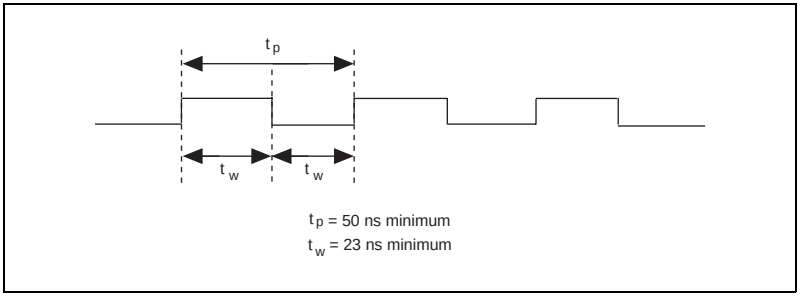


Figure 4-30. UISOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

Either the 20 MHz or 100 kHz internal timebase normally generates the UISOURCE signal unless you select some external source.

General-Purpose Timing Signal Connections

The general-purpose timing signals are GPCTR0_SOURCE, GPCTR0_GATE, GPCTR0_OUT, GPCTR0_UP_DOWN, GPCTR1_SOURCE, GPCTR1_GATE, GPCTR1_OUT, GPCTR1_UP_DOWN, and FREQ_OUT.

GPCTR0_SOURCE Signal

Any PFI pin can externally input the GPCTR0_SOURCE signal, which is available as an output on the PFI8/GPCTR0_SOURCE pin.

As an input, the GPCTR0_SOURCE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, the GPCTR0_SOURCE signal reflects the actual clock connected to general-purpose counter 0. This is true even if another PFI is externally inputting the source clock. This output is set to tri-state at startup.

Figure 4-31 shows the timing requirements for the GPCTR0_SOURCE signal.

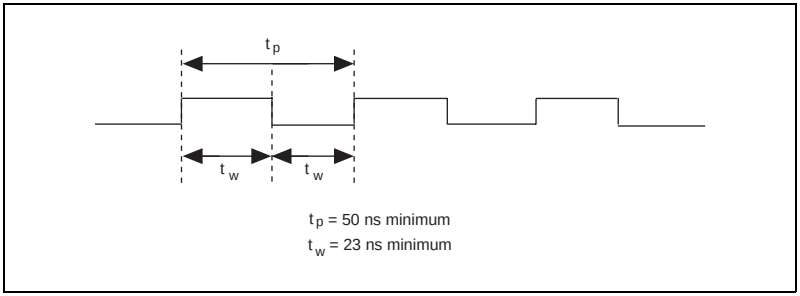


Figure 4-31. GPCTR0_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 23 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates the GPCTR0_SOURCE signal unless you select some external source.

GPCTR0_GATE Signal

Any PFI pin can externally input the GPCTR0_GATE signal, which is available as an output on the PFI9/GPCTR0_GATE pin.

As an input, the GPCTR0_GATE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR0_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform actions such as starting and stopping the counter, generating interrupts, saving the counter contents, and so on.

As an output, the GPCTR0_GATE signal reflects the actual gate signal connected to general-purpose counter 0. This is true even if the gate is being externally generated by another PFI. This output is set to tri-state at startup.

Figure 4-32 shows the timing requirements for the GPCTR0_GATE signal.

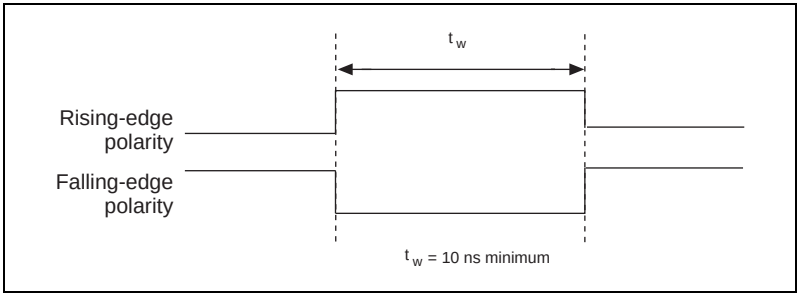


Figure 4-32. GPCTR0_GATE Signal Timing in Edge-Detection Mode

GPCTR0_OUT Signal

This signal is available only as an output on the GPCTR0_OUT pin. The GPCTR0_OUT signal reflects the terminal count (TC) of general-purpose counter 0. You have two software-selectable output options— pulse on TC and toggle output polarity on TC. The output polarity is software selectable for both options. This output is set to tri-state at startup. Figure 4-33 shows the timing of the GPCTR0_OUT signal.

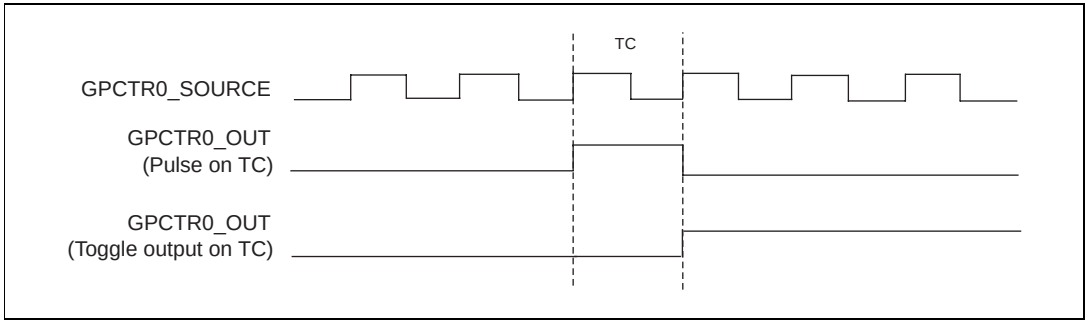


Figure 4-33. GPCTR0_OUT Signal Timing

GPCTR0_UP_DOWN Signal

This signal can be externally input on the DIO6 pin and is not available as an output on the I/O connector. The general-purpose counter 0 will count down when this pin is at a logic low and count up when it is at a logic high. You can disable this input so that software can control the up-down functionality and leave the DIO6 pin free for general use.

GPCTR1_SOURCE Signal

Any PFI pin can externally input the GPCTR1_SOURCE signal, which is available as an output on the PFI3/GPCTR1_SOURCE pin.

As an input, the GPCTR1_SOURCE signal is configured in the edge-detection mode. You can select any PFI pin as the source for GPCTR1_SOURCE and configure the polarity selection for either rising or falling edge.

As an output, the GPCTR1_SOURCE monitors the actual clock connected to general-purpose counter 1. This is true even if the source clock is being externally generated by another PFI. This output is set to tri-state at startup.

Figure 4-34 shows the timing requirements for the GPCTR1_SOURCE signal.

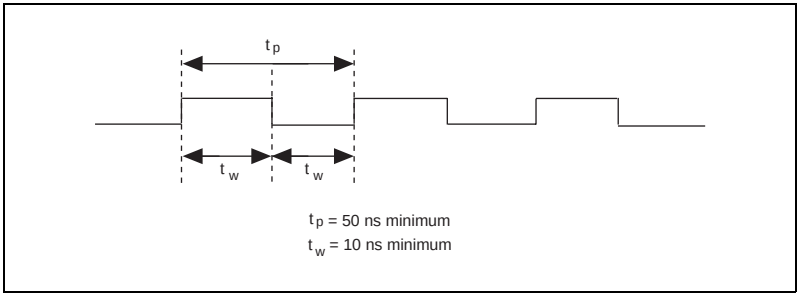


Figure 4-34. GPCTR1_SOURCE Signal Timing

The maximum allowed frequency is 20 MHz, with a minimum pulse width of 10 ns high or low. There is no minimum frequency limitation.

The 20 MHz or 100 kHz timebase normally generates the GPCTR1_SOURCE unless you select some external source.

GPCTR1_GATE Signal

Any PFI pin can externally input the GPCTR1_GATE signal, which is available as an output on the PFI4/GPCTR1_GATE pin.

As an input, the GPCTR1_GATE signal is configured in edge-detection mode. You can select any PFI pin as the source for GPCTR1_GATE and configure the polarity selection for either rising or falling edge. You can use the gate signal in a variety of different applications to perform such

actions as starting and stopping the counter, generating interrupts, saving the counter contents, and so on.

As an output, the GPCTR1_GATE signal monitors the actual gate signal connected to general-purpose counter 1. This is true even if the gate is being externally generated by another PFI. This output is set to tri-state at startup.

Figure 4-35 shows the timing requirements for the GPCTR1_GATE signal.

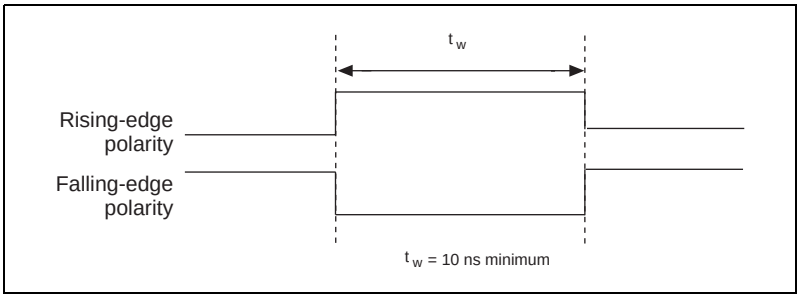


Figure 4-35. GPCTR1_GATE Signal Timing in Edge-Detection Mode

GPCTR1_OUT Signal

This signal is available only as an output on the GPCTR1_OUT pin. The GPCTR1_OUT signal monitors the TC board general-purpose counter 1. You have two software-selectable output options—pulse on TC and toggle output polarity on TC. The output polarity is software selectable for both options. This output is set to tri-state at startup. Figure 4-36 shows the timing requirements for the GPCTR1_OUT signal.

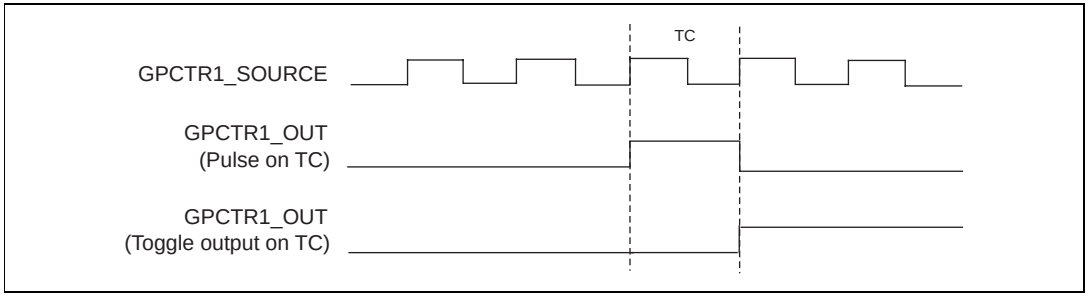
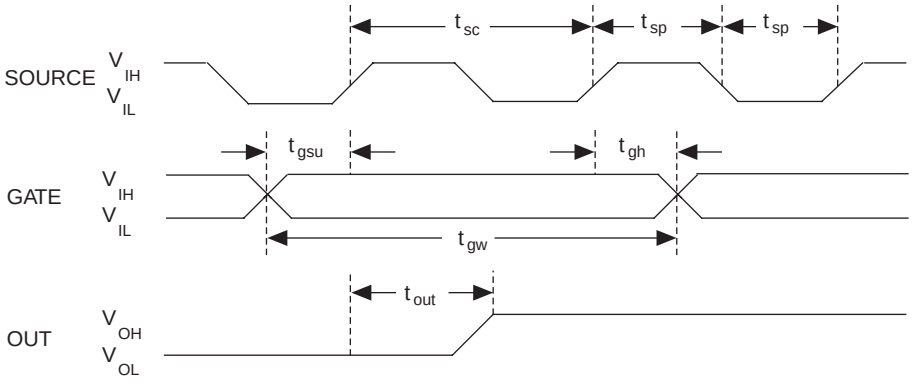


Figure 4-36. GPCTR1_OUT Signal Timing

GPCTR1_UP_DOWN Signal

This signal can be externally input on the DIO7 pin and is not available as an output on the I/O connector. General-purpose counter 1 counts down when this pin is at a logic low and counts up at a logic high. This input can be disabled so that software can control the up-down functionality and leave the DIO7 pin free for general use. Figure 4-37 shows the timing requirements for the GATE and SOURCE input signals and the timing specifications for the OUT output signals of your AT E Series board.



Source Clock Period	t_{sc}	50 ns minimum
Source Pulse Width	t_{sp}	23 ns minimum
Gate Setup Time	t_{gsu}	10 ns minimum
Gate Hold Time	t_{gh}	0 ns minimum
Gate Pulse Width	t_{gw}	10 ns minimum
Output Delay Time	t_{out}	80 ns maximum

Figure 4-37. GPCTR Timing Summary

The GATE and OUT signal transitions shown in Figure 4-37 are referenced to the rising edge of the SOURCE signal. This timing diagram assumes that the counters are programmed to count rising edges. The same timing diagram, but with the source signal inverted and referenced to the falling edge of the source signal, would apply when the counter is programmed to count falling edges.

The GATE input timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated signals on your AT E Series board. Figure 4-37 shows the GATE signal referenced to the rising edge of a source signal. The gate must be valid (either high or

low) for at least 10 ns before the rising or falling edge of a source signal for the gate to take effect at that source edge, as shown by t_{gsu} and t_{gh} in Figure 4-37. The gate signal is not required to be held after the active edge of the source signal.

If an internal timebase clock is used, the gate signal cannot be synchronized with the clock. In this case, gates applied close to a source edge take effect either on that source edge or on the next one. This arrangement results in an uncertainty of one source clock period with respect to unsynchronized gating sources.

The OUT output timing parameters are referenced to the signal at the SOURCE input or to one of the internally generated clock signals on the AT E Series boards. Figure 4-37 shows the OUT signal referenced to the rising edge of a source signal. Any OUT signal state changes occur within 80 ns after the rising or falling edge of the source signal.

FREQ_OUT Signal

This signal is available only as an output on the FREQ_OUT pin. The FREQ_OUT signal is the output of the AT E Series board frequency generator. The frequency generator is a 4-bit counter that can divide its input clock by the numbers 1 through 16. The input clock of the frequency generator is software selectable from the internal 10 MHz and 100 kHz timebases. The output polarity is software selectable. This output is set to tri-state at startup.

Timing Specifications for Digital I/O Ports A, B, and C

- AT-MIO-16DE-10 only

In addition to its function as a digital I/O port, digital port C, PC<0..7>, can also be used for handshaking when performing data transfers with ports A and B. The signals assigned to port C depend on the mode in which it is programmed. In mode 0, port C is considered two 4-bit I/O ports. In modes 1 and 2, port C is used for status and handshaking signals with two or three additional I/O bits. Table 4-6 summarizes the signal assignments of port C for each programmable mode.

Table 4-6. Port C Signal Assignments

Programming Mode	Group A					Group B		
	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Mode 0	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
Mode 1 Input	I/O	I/O	IBF_A	STB_A*	$INTR_A$	STB_B*	$IBFB_B$	$INTR_B$
Mode 1 Output	OBF_A*	ACK_A*	I/O	I/O	$INTR_A$	ACK_B*	OBF_B*	$INTR_B$
Mode 2	OBF_A*	ACK_A*	IBF_A	STB_A*	$INTR_A$	I/O	I/O	I/O

* Indicates that the signal is active low.

This section lists the timing specifications for handshaking with the AT-MIO-16DE-10 port C circuitry. The handshaking lines STB* and IBF synchronize input transfers. The handshaking lines OBF* and ACK* synchronize output transfers.

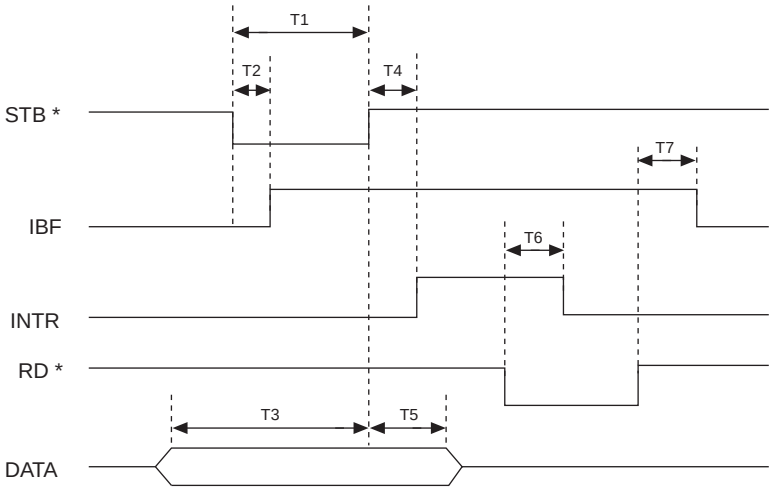
Table 4-7 summarizes the port C signals used in the timing diagrams that follow.

Table 4-7. Port C Signal Descriptions

Name	Type	Description
STB*	input	Strobe Input—A low signal on this handshaking line loads data into the input latch.
IBF	output	Input Buffer Full—A high signal on this handshaking line indicates that data has been loaded into the input latch. This is an input acknowledge signal.
ACK*	input	Acknowledge Input—A low signal on this handshaking line indicates that the data written from the selected port has been accepted. This signal is a response from the external device that it has received the data from the AT-MIO-16DE-10.
OBF*	output	Output Buffer Full—A low signal on this handshaking line indicates that data has been written from the selected port.
INTR	output	Interrupt Request—This signal becomes high to request service during a data transfer. The appropriate interrupt enable bits must be set to generate this signal and to allow it to interrupt your computer.
RD*	internal	Read Signal—This signal is the read signal generated by the host computer.
WR*	internal	Write Signal—This signal is the write signal generated by the host computer.
DATA	input or output	Data Lines at the Selected Port (PA or PB)—This signal indicates when the data on the data lines at a selected port is or should be available.

Mode 1 Input Timing

Figure 4-38 details the timing specifications for an input transfer in Mode 1.



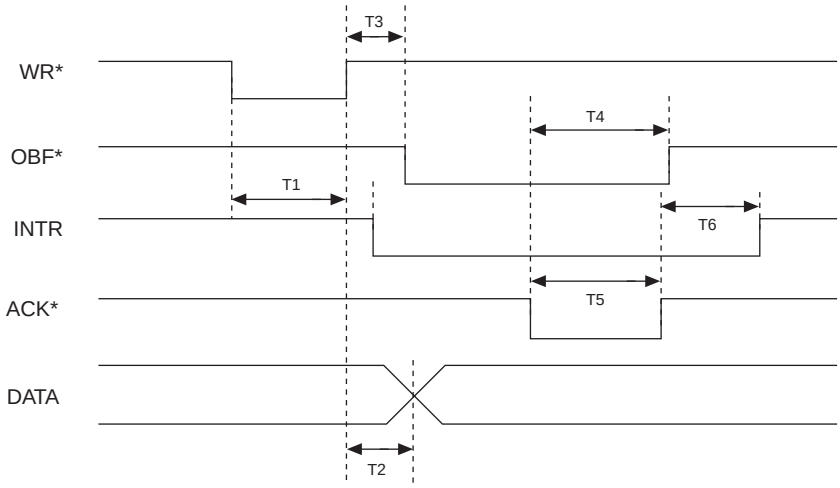
Name	Description	Minimum	Maximum
T1	STB* Pulse Width	100	—
T2	STB* = 0 to IBF = 1	—	150
T3	Data before STB* = 1	20	—
T4	STB* = 1 to INTR = 1	—	150
T5	Data after STB* = 1	50	—
T6	RD* = 0 to INTR = 0	—	200
T7	RD* = 1 to IBF = 0	—	150

All timing values are in nanoseconds.

Figure 4-38. Mode 1 Input Timing

Mode 1 Output Timing

Figure 4-39 details the timing specifications for an output transfer in Mode 1.



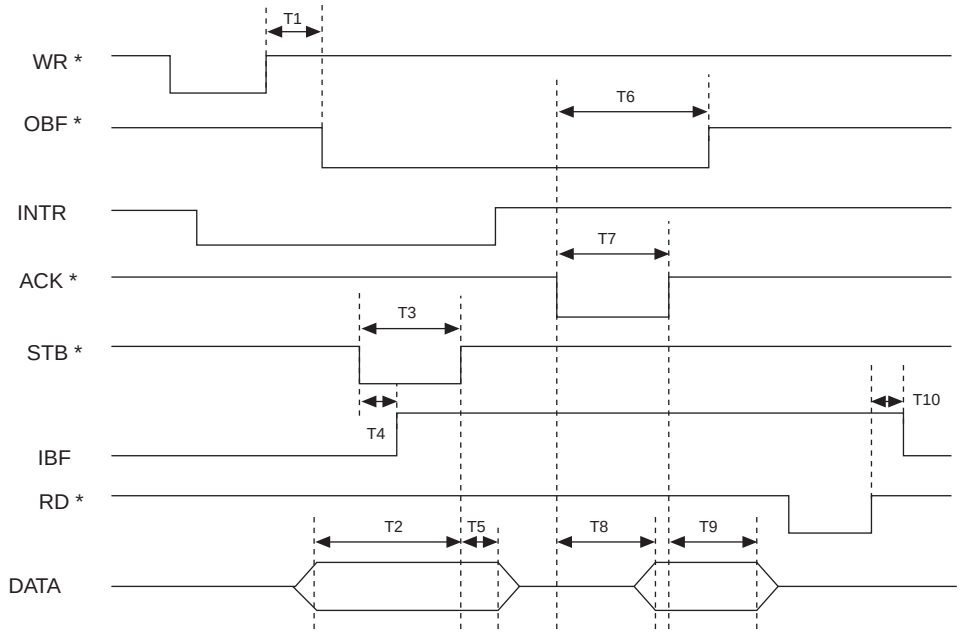
Name	Description	Minimum	Maximum
T1	WR* = 0 to INTR = 0	—	250
T2	WR* = 1 to Output	—	200
T3	WR* = 1 to OBF* = 0	—	150
T4	ACK* = 0 to OBF* = 1	—	150
T5	ACK* Pulse Width	100	—
T6	ACK* = 1 to INTR = 1	—	150

All timing values are in nanoseconds.

Figure 4-39. Mode 1 Output Timing

Mode 2 Bidirectional Timing

Figure 4-40 details the timing specifications for bidirectional transfers in Mode 2.



Name	Description	Minimum	Maximum
T1	WR* = 1 to OBF* = 0	—	150
T2	Data before STB* = 1	20	—
T3	STB* Pulse Width	100	—
T4	STB* = 0 to IBF = 1	—	150
T5	Data after STB* = 1	50	—
T6	ACK* = 0 to OBF = 1	—	150
T7	ACK* Pulse Width	100	—
T8	ACK* = 0 to Output	—	150
T9	ACK* = 1 to Output Float	20	250
T10	RD* = 1 to IBF = 0	—	150

All timing values are in nanoseconds. .

Figure 4-40. Mode 2 Bidirectional Timing

Field Wiring Considerations

Environmental noise can seriously affect the accuracy of measurements made with your AT E Series board if you do not take proper care when running signal wires between signal sources and the board. The following recommendations apply mainly to analog input signal routing to the board, although they also apply to signal routing in general.

You can minimize noise pickup and maximize measurement accuracy by taking the following precautions:

- Use differential analog input connections to reject common-mode noise.
- Use individually shielded, twisted-pair wires to connect analog input signals to the board. With this type of wire, the signals attached to the CH+ and CH– inputs are twisted together and then covered with a shield. You then connect this shield only at one point to the signal source ground. This kind of connection is required for signals traveling through areas with large magnetic fields or high electromagnetic interference.
- Route signals to the board carefully. Keep cabling away from noise sources. The most common noise source in a PC data acquisition system is the video monitor. Separate the monitor from the analog signals as much as possible.

The following recommendations apply for all signal connections to your AT E Series board:

- Separate AT E Series board signal lines from high-current or high-voltage lines. These lines are capable of inducing currents in or voltages on the AT E Series board signal lines if they run in parallel paths at a close distance. To reduce the magnetic coupling between lines, separate them by a reasonable distance if they run in parallel, or run the lines at right angles to each other.
- Do not run signal lines through conduits that also contain power lines.
- Protect signal lines from magnetic fields caused by electric motors, welding equipment, breakers, or transformers by running them through special metal conduits.

For more information, refer to the application note, *Field Wiring and Noise Consideration for Analog Signals*, available from National Instruments.

Chapter 5

Calibration

This chapter discusses the calibration procedures for your AT E Series board. If you are using the NI-DAQ device driver, that software includes calibration functions for performing all of the steps in the calibration process.

Calibration refers to the process of minimizing measurement and output voltage errors by making small circuit adjustments. On the AT E Series boards, these adjustments take the form of writing values to onboard calibration DACs (CalDACs).

Some form of board calibration is required for all but the most forgiving applications. If no board calibration were performed, your signals and measurements could have very large offset, gain, and linearity errors.

Three levels of calibration are available to you, and these are described in this chapter. The first level is the fastest, easiest, and least accurate, whereas the last level is the slowest, most difficult, and most accurate.

Loading Calibration Constants

Your AT E Series board is factory calibrated before shipment at approximately 25° C to the levels indicated in Appendix A, *Specifications*. The associated calibration constants—the values that were written to the CalDACs to achieve calibration in the factory—are stored in the onboard nonvolatile memory (EEPROM). Because the CalDACs have no memory capability, they do not retain calibration information when the board is unpowered. Loading calibration constants refers to the process of loading the CalDACs with the values stored in the EEPROM. NI-DAQ software determines when this is necessary and does it automatically. If you are not using NI-DAQ, you must load these values yourself.

In the EEPROM there is a user-modifiable calibration area in addition to the permanent factory calibration area. This means that you can load the CalDACs with values either from the original factory calibration or from a calibration that you subsequently performed.

This method of calibration is not very accurate because it does not take into account the fact that the board measurement and output voltage errors can vary with time and temperature. It is better to self-calibrate when the board is installed in the environment in which it will be used.

Self-Calibration

Your AT E Series board can measure and correct for almost all of its calibration-related errors without any external signal connections. Your National Instruments software provides a self-calibration method you can use. This self-calibration process, which generally takes less than a minute, is the preferred method of assuring accuracy in your application. You should initiate self-calibration to ensure that the effects of any offset, gain, and linearity drifts, particularly those due to warmup, are minimized.

Immediately after self-calibration, the only significant residual calibration error could be gain error due to time or temperature drift of the onboard voltage reference. This error is addressed by external calibration, which is discussed in the following section. If you are interested primarily in relative measurements, you can ignore a small amount of gain error, and self-calibration should be sufficient.

External Calibration

Your AT E Series board has an onboard calibration reference to ensure the accuracy of self-calibration. Its specifications are listed in Appendix A, *Specifications*. The reference voltage is measured at the factory and stored in the EEPROM for subsequent self-calibrations. This voltage is stable enough for most applications, but if you are using your board at an extreme temperature or if the onboard reference has not been measured for a year or more, you may wish to externally calibrate your board.

An external calibration refers to calibrating your board with a known external reference rather than relying on the onboard reference. Redetermining the value of the onboard reference is part of this process and the results can be saved in the EEPROM, so you should not have to perform an external calibration very often. You can externally calibrate your board by calling the NI-DAQ calibration function.

To externally calibrate your board, be sure to use a very accurate external reference. The reference should be several times more accurate than the board itself. For example, to calibrate a 12-bit board, the external reference should be at least ±0.005% (±50 ppm) accurate. To calibrate a 16-bit board, the external reference should be at least ±0.001% (±10 ppm) accurate.

Other Considerations

The CalDACs adjust the gain error of each analog output channel by adjusting the value of the reference voltage supplied to that channel. This calibration mechanism is designed to work only with the internal 10 V reference. Thus, in general, it is not possible to calibrate the analog output gain error when using an external reference. In this case, it is advisable to account for the nominal gain error of the analog output channel either in software or with external hardware. See Appendix A, *Specifications*, for analog output gain error information.

Specifications

Appendix A

This appendix lists the specifications of each board in the AT E Series. These specifications are typical at 25° C unless otherwise noted.

AT-MIO-16E-1, AT-MIO-16E-2 and AT-MIO-64E-3

Analog Input

Input Characteristics

Number of channels

AT-MIO-16E-1, AT-MIO-16E-2 ..... 16 single-ended or 8 differential (software selectable)

AT-MIO-64E-3 ..... 64 single-ended or 32 differential (software selectable)

Type of ADC ..... Successive approximation

Resolution ..... 12 bits, 1 in 4,096

Max sampling rate

AT-MIO-16E-1 ..... 1.25 MS/s guaranteed

AT-MIO-16E-2, AT-MIO-64E-3 ..... 500 kS/s guaranteed

Throughput to system memory

EISA machines ..... 1.0–1.25 MS/s

ISA machines ..... 600–900 kS/s

Input signal ranges

Board Gain (Software Selectable)	Board Range (Software Selectable)	
	Bipolar	Unipolar
0.5	±10 V	—
1	±5 V	0 to 10 V
2	±2.5 V	0 to 5 V
5	±1 V	0 to 2 V
10	±500 mV	0 to 1 V
20	±250 mV	0 to 500 mV
50	±100 mV	0 to 200 mV
100	±50 mV	0 to 100 mV

Input coupling ..... DC

Max working voltage
(signal + common mode)..... Each input should remain within ±11 V of ground

Overvoltage protection ..... ±25 V powered on, ± 15 V powered off

Inputs protected ..... ACH<0..63>, AISENSE, AISENSE2

FIFO buffer size

AT-MIO-16E-1..... 8,192 samples

AT-MIO-16E-2,
AT-MIO-64E-3..... 2,048 samples

Data transfers ..... DMA, interrupts, programmed I/O

DMA modes .....Single transfer, demand transfer

Configuration memory size.....512 words

Transfer Characteristics

Relative accuracy .....±0.5 LSB typ dithered,
±1.5 LSB max undithered

DNL.....±0.5 LSB typ, ±1.0 LSB max

No missing codes.....12 bits, guaranteed

Offset error

- Pregain error after calibration.....±12 µV max
- Pregain error before calibration....±2.5 mV max
- Postgain error after calibration.....±0.5 mV max
- Postgain error before calibration ..±100 mV max

Gain error (relative to calibration reference)

- After calibration (gain = 1).....±0.02% of reading max
- Before calibration.....±2.5% of reading max
  - Gain ≠ 1 with gain error adjusted to 0 at gain = 1.....±0.02% of reading max

Amplifier Characteristics

Input impedance

- Normal powered on.....100 GΩ in parallel with 100 pF
- Powered off.....820 Ω min
- Overload .....820 Ω min

Input bias current.....±200 pA

Input offset current .....±100 pA

CMRR, DC to 60 Hz

- Gain = 0.5 .....95 dB
- Gain = 1 .....100 dB
- Gain ≥ 2 .....106 dB

Dynamic Characteristics

Bandwidth

	Small signal (–3dB)	Large signal (1% THD)
AT-MIO-16E-1	1.6 MHz	1 MHz
AT-MIO-16E-2, AT-MIO-64E-3	1 MHz	300 kHz

Setting time for full-scale step

		Accuracy		
	Gain	±0.012% (±0.5 LSB)	±0.024% (±1 LSB)	±0.098% (±4 LSB)
AT-MIO-16E-1	0.5	2 µs typ 3 µs max	1.5 µs typ 2 µs max	1.5 µs typ 2 µs max
	1	2 µs typ 3 µs max	1.5 µs typ 2 µs max	1.3 µs typ 1.5 µs max
	2 to 50	2 µs typ 3 µs max	1.5 µs typ 2 µs max	0.9 µs typ 1 µs max
	100	2 µs typ 3 µs max	1.5 µs typ 2 µs max	1 µs typ 1.5 µs max
AT-MIO-16E-2	All	2 µs typ 4 µs max	1.9 µs typ 2 µs max	1.8 µs typ 2 µs max
AT-MIO-64E-3	All	3 µs typ 5 µs max	2 µs typ 3 µs max	1.8 µs typ 2 µs max

System noise (LSBrms) (not including quantization)

	Gain	Noise, dither off	Noise, dither on
AT-MIO-16E-1	0.5 to 10	0.25	0.5
	20	0.4	0.6
	50	0.5	0.7
	100	0.8	0.9
AT-MIO-16E-2, AT-MIO-64E-3	0.5 to 20	0.15	0.5
	50	0.3	0.6
	100	0.5	0.7

Crosstalk.....–80 dB, DC to 100 kHz

Stability

Offset temperature coefficient

Pregain.....±5 µV/° C

Postgain .....±240 µV/° C

Gain temperature coefficient.....±20 ppm/° C

Analog Output

Output Characteristics

Number of channels .....2 voltage

Resolution.....12 bits, 1 in 4,096

Max update rate

FIFO mode waveform generation

Internally timed .....1 MS/s per channel

Externally timed .....950 kS/s per channel

Non-FIFO mode waveform generation

1 channel ..... 600–950 kS/s (system dependent)

2 channel ..... 300–625 kS/s (system dependent)

Type of DAC..... Double buffered, multiplying

FIFO buffer size ..... 2,048 samples

Data transfers ..... DMA, interrupts, programmed I/O

DMA modes..... Single transfer, demand transfer

Transfer Characteristics

Relative accuracy (INL)

After calibration ..... ±0.3 LSB typ, ±0.5 LSB max

Before calibration..... ±4 LSB max

DNL

After calibration ..... ±0.3 LSB typ, ±1.0 LSB max

Before calibration..... ±3 LSB max

Monotonicity..... 12 bits, guaranteed after calibration

Offset error

After calibration ..... ±1.0 mV max

Before calibration..... ±200 mV max

Gain error (relative to internal reference)

After calibration ..... ±0.01% of output max

Before calibration..... ±0.5% of output max

Gain error

(relative to external reference) ..... +0% to +0.5% of output max, not adjustable

Voltage Output

Ranges .....±10 V, 0 to 10 V, ±EXTREF, 0 to EXTREF (software selectable)

Output coupling .....DC

Output impedance .....0.1 Ω max

Current drive.....±5 mA max

Protection .....Short-circuit to ground

Power-on state .....0 V

External reference input

- Range .....±11 V
- Overvoltage protection .....±25 V powered on, ±15 V powered off
- Input impedance .....10 kΩ
- Bandwidth (–3 dB) .....1 MHz

Dynamic Characteristics

Settling time for full-scale step .....3 µs to ±0.5 LSB accuracy

Slew rate .....20 V/µs

Noise .....200 µVrms, DC to 1 MHz

Glitch energy (at midscale transition)

- Magnitude
  - Reglitching disabled .....±200 mV
  - Reglitching enabled .....±30 mV
- Duration .....1.5 µs

Stability

Offset temperature coefficient.....±50 µV/° C

Gain temperature coefficient

- Internal reference .....±25 ppm/° C

External reference ..... ±25 ppm/° C

Digital I/O

Number of channels ..... 8 input/output

Compatibility ..... TTL/CMOS

Digital logic levels

Level	Min	Max
Input low voltage	0 V	0.8 V
Input high voltage	2 V	5 V
Input low current (V_{in} = 0 V)	—	–320 µA
Input high current (V_{in} = 5 V)	—	10 µA
Output low voltage (I_{OL} = 24 mA)	—	0.4 V
Output high voltage (I_{OH} = 13 mA)	4.35 V	—

Power-on state..... Input (High-Z)

Data transfers ..... Programmed I/O

Timing I/O

Number of channels ..... 2 up/down counter/timers,
1 frequency scaler

Resolution

Counter/timers..... 24 bits

Frequency scalers ..... 4 bits

Compatibility ..... TTL/CMOS

Base clocks available

Counter/timers..... 20 MHz, 100 kHz

Frequency scalers ..... 10 MHz, 100 kHz

Base clock accuracy.....±0.01%

Max source frequency.....20 MHz

Min source pulse duration.....10 ns in edge-detect mode

Min gate pulse duration .....10 ns in edge-detect mode

Data transfers.....DMA, interrupts, programmed I/O

DMA modes .....Single transfer

Triggers

Analog Trigger

Source.....ACH<0..63>, PFI0/TRIG1

Level.....± full-scale, internal; ±10 V, external

Slope.....Positive or negative (software selectable)

Resolution.....8 bits, 1 in 256

Hysteresis .....Programmable

Bandwidth (–3 dB).....1.5 MHz internal, 7 MHz external

External input (PFI0/TRIG1)

- Impedance.....10 kΩ
- Coupling .....DC
- Protection.....–0.5 to Vcc + 0.5 V when configured as a digital signal

  ±35 V when configured as an analog trigger signal or disabled

  ±35 V powered off

Digital Trigger

Compatibility ..... TTL

Response ..... Rising or falling edge

Pulse width..... 10 ns min

RTSI

Trigger lines..... 7

Calibration

Recommended warm-up time ..... 15 min

Calibration interval ..... 1 year

External calibration reference ..... >6 and <10 V

Onboard calibration reference

- Level ..... 5.000 V (±2.5 mV) (actual value stored in EEPROM)
- Temperature coefficient..... ±5 ppm/° C max
- Long-term stability ..... ±15 ppm/ $\sqrt{1,000h}$

Bus Interface

Type ..... Slave

Power Requirement

+5 VDC (±5%)..... 1.0 A

Power available at I/O connector..... +4.65 VDC to +5.25 VDC at 1 A

Physical

Dimensions
(not including connectors) .....33.8 by 9.9 cm (13.3 by 3.9 in.)

I/O connector

AT-MIO-16E-1,
AT-MIO-16E-2 .....68-pin male SCSI-II type
AT-MIO-64E-3 .....100-pin female 0.050 D-type

Environment

Operating temperature .....0° to 55° C

Storage temperature .....–55° to 150° C

Relative humidity .....5% to 90% noncondensing

AT-MIO-16E-10 and AT-MIO-16DE-10

Analog Input

Input Characteristics

Number of channels ..... 16 single-ended or 8 differential, software selectable

Type of ADC..... Successive approximation

Resolution ..... 12 bits, 1 in 4,096

Max sampling rate..... 100 kS/s guaranteed

Input signal ranges

Board Gain (Software Selectable)	Board Range (Software Selectable)	
	±5 V	0–10 V
0.5	±10 V	—
1	±5 V	0 to 10 V
2	±2.5 V	0 to 5 V
5	±1 V	0 to 2 V
10	±500 mV	0 to 1 V
20	±250 mV	0 to 500 mV
50	±100 mV	0 to 200 mV
100	±50 mV	0 to 100 mV

Input coupling.....DC

Max working voltage

(signal + common mode).....Each input should remain within ±11 V of ground

Overvoltage protection.....±35 V powered on, ±25 V powered off

Inputs protected.....ACH<0..15>, AISENSE

FIFO buffer size.....512 samples

Data transfers.....DMA, interrupts, programmed I/O

DMA modes .....Single transfer, demand transfer

Configuration memory size.....512 words

Transfer Characteristics

Relative accuracy .....±0.2 LSB typ dithered, ±1.5 LSB max undithered

DNL.....±0.2 LSB typ, ±1.0 LSB max

No missing codes.....12 bits, guaranteed

Offset error

Pregain error after calibration.....±2 µV max

Pregain error before calibration....±24 mV max

Postgain error after calibration.....±0.5 mV max

Postgain error before calibration ..±100 mV max

Gain error (relative to calibration reference)

After calibration (Gain = 1).....±0.01% of reading max

Before calibration.....±2.0% of reading max

Gain ≠ 1 with gain error

adjusted to 0 at gain = 1 .....±0.05% of reading max

Amplifier Characteristics

Input impedance

Normal powered on ..... 100 GΩ in parallel with 50 pF

Powered off ..... 3 kΩ min

Overload..... 3 kΩ min

Input bias current ..... ±200 pA

Input offset current..... ±100 pA

CMRR (all input ranges) ..... 90 dB, DC to 60 Hz

Dynamic Characteristics

Bandwidth

Small signal (–3 dB)..... 150 kHz

Large signal (1% THD) ..... 120 kHz

Settling time for full-scale step ..... 10 µs max to ±0.5 LSB accuracy

System noise (not including quantization)

Gain	Noise, Dither Off	Noise, Dither On
0.5 to 10	0.07 LSB rms	0.5
20	0.12 LSB rms	0.5
50	0.25 LSB rms	0.6
100	0.5 LSB rms	0.7

Crosstalk ..... –70 dB, DC to 100 kHz

Stability

Offset temperature coefficient

Pregain.....±15 µV/° C

Postgain .....±240 µV/° C

Gain temperature coefficient.....±20 ppm/° C

Analog Output

Output Characteristics

Number of channels .....2 voltage

Resolution.....12 bits, 1 in 4,096

Max update rate .....100 kS/s

Type of DAC .....Double buffered, multiplying

FIFO buffer size .....None

Data transfers.....DMA, interrupts, programmed I/O

DMA modes .....Single transfer

Transfer Characteristics

Relative accuracy (INL)

- After calibration ..... ±0.3 LSB typ, ±0.5 LSB max
- Before calibration ..... ±4 LSB max

DNL

- After calibration ..... ±0.3 LSB typ, ±1.0 LSB max
- Before calibration ..... ±3 LSB max

Monotonicity ..... 12 bits, guaranteed after calibration

Offset error

- After calibration ..... ±1.0 mV max
- Before calibration ..... ±200 mV max

Gain error (relative to internal reference)

- After calibration ..... ±0.01% of output max
- Before calibration ..... ±0.5% of output max

Gain error

(relative to external reference) ..... 0% to +0.5% of output max, not adjustable

Voltage Output

Ranges ..... ±10 V, 0 to 10 V, ±EXTREF, 0 to EXTREF (software selectable)

Output coupling ..... DC

Output impedance ..... 0.1 Ω max

Current drive ..... ±5 mA max

Protection ..... Short-circuit to ground

Power-on state ..... 0 V

External reference input

Range ..... ±11 V

Overvoltage protection ..... ±35 V powered on,
±25 V powered off

Input impedance ..... 10 kΩ

Bandwidth (–3 dB) ..... 300 kHz

Dynamic Characteristics

Settling time for full-scale step ..... 10 µs to ±0.5 LSB accuracy

Slew rate ..... 10 V/µs

Noise ..... 200 µVrms, DC to 1 MHz

Glitch energy (at midscale transition)

Magnitude ..... ±100 mV

Duration ..... 3 µs

Stability

Offset temperature coefficient ..... ±50 µV/° C

Gain temperature coefficient

Internal reference ..... ±25 ppm/° C

External reference ..... ±25 ppm/° C

Digital I/O

Number of channels

AT-MIO-16E-10 ..... 8 input/output

AT-MIO-16DE-10 ..... 32 input/output

Compatibility ..... TTL/CMOS

Digital logic levels

Level	Min	Max
Input low voltage	0 V	0.8 V
Input high voltage	2 V	5 V

Level	Min	Max
Input low current (V_{in} = 0 V)	—	–320 µA
Input high current (V_{in} = 5 V)	—	10 µA
Output low voltage (I_{OL} = 24 mA)	—	0.4 V
Output high voltage (I_{OH} = 13 mA)	4.35 V	—

PA<0..7>, PB<0..7>, PC<0..7> (AT-MIO-16DE-10 only)

Level	Min	Max
Input low voltage	0 V	0.8 V
Input high voltage	2 V	5 V
Input low current (V_{in} = 0 V)	—	–60 µA
Input high current (V_{in} = 5 V)	—	10 µA
Output low voltage (I_{OL} = 2.5 mA)	—	0.4 V
Output high voltage (I_{OH} = 2.5 mA)	3.9 V	—

Handshaking
(AT-MIO-16DE-10 only) 3-wire

Power-on state..... Input (High-Z)

Data transfers

AT-MIO-16E-10..... Programmed I/O

AT-MIO-16DE-10 ..... Interrupts, programmed I/O

Timing I/O

Number of channels ..... 2 up/down counter/timers,
1 frequency scaler

Resolution
- Counter/timers .....24 bits
- Frequency scalers.....4 bits

Compatibility.....TTL/CMOS

Base clocks available
- Counter/timers .....20 MHz, 100 kHz
- Frequency scaler .....10 MHz, 100 kHz

Base clock accuracy.....±0.01%

Max source frequency.....20 MHz

Min source pulse duration.....10 ns in edge-detect mode

Min gate pulse duration .....10 ns in edge-detect mode

Data transfers.....DMA, interrupts, programmed I/O

DMA modes .....Single transfer

Triggers

Digital Trigger

Compatibility.....TTL

Response.....Rising or falling edge

Pulse width .....10 ns min

RTSI

Trigger lines 7

Calibration

Recommended warm-up time.....15 min

Calibration interval .....1 year

External calibration reference .....>6 and <10V

Onboard calibration reference

Level ..... 5.000 V (±2.5 mV) (actual value stored in EEPROM)

Temperature coefficient..... ±5 ppm/° C max

Long-term stability ..... ±15 ppm/ $\sqrt{1,000h}$

Bus Interface

Type ..... Slave

Power Requirement

+5 VDC (±5%)..... 0.7 A

Power available at I/O connector..... +4.65 VDC to +5.25 VDC at 1 A

Physical

Dimensions
(not including connectors)..... 17.45 by 10.56 cm (6.87 by 4.16 in.)

I/O connector

AT-MIO-16E-10..... 68-pin male SCSI-II type

AT-MIO-16DE-10 ..... 100-pin female 0.050 D-type

Environment

Operating temperature..... 0° to 55° C

Storage temperature ..... –55° to 150° C

Relative humidity ..... 5% to 90% noncondensing

AT-MIO-16XE-10 and AT-AI-16XE-10

Analog Input

Input Characteristics

Number of channels .....16 single-ended or 8 differential (software-selectable)

Type of ADC .....Successive approximation

Resolution.....16 bits, 1 in 65,536

Maximum sampling rate .....100 kS/s guaranteed

Input signal ranges

Board Gain (Software Selectable)	Board Range (Software Selectable)	
	Bipolar	Unipolar
1	±10.0 V	0 to 10 V
2	±5.0 V	0 to 5 V
5	±2.0 V	0 to 2 V
10	±1.0 V	0 to 1 V
20	±0.5 V	0 to 0.5 V
50	±0.2 V	0 to 0.2 V
100	±0.1 V	0 to 0.1 V

Input coupling ..... DC

Maximum working voltage ..... Each input should remain within ±11 V of ground

Overvoltage protection ..... ±25 V powered on, ±15 V powered off

Inputs protected ..... ACH<0..15>, AISENSE

FIFO buffer size ..... 512 samples

Data transfers ..... DMA, interrupts, programmed I/O

DMA modes ..... Single transfer, demand transfer

Configuration memory size ..... 512 words

Transfer Characteristics

Relative accuracy ..... ±0.75 LSB typ, ±1 LSB max

DNL ..... ±0.5 LSB typ, ±1 LSB max

No missing codes ..... 16 bits, guaranteed

Offset error

Pregain error after calibration ..... ±3 µV max

Pregain error before calibration ... ±2.2 mV max

Postgain error after calibration .... ±76 µV max

Postgain error before calibration.. ±102 mV max

Gain error (relative to calibration reference)

After calibration (gain = 1) ..... ±30.5 ppm of reading max

Before calibration ..... ±2,150 ppm of reading max

With gain error adjusted to 0 at gain = 1

Gain ≠ 1 ..... ±200 ppm of reading

Amplifier Characteristics

Input impedance

Normal, powered on .....100 GΩ in parallel with 100 pF
Powered off.....820 Ω min
Overload .....820 Ω min

Input bias current .....±1 nA

Input offset current .....±2 nA

CMRR, DC to 60 Hz

Gain = 1 .....92 dB
Gain = 2 .....97 dB
Gain = 5 .....101 dB
Gain = 10 .....104 dB
Gain = 20 .....105 dB
Gain = 50 .....105 dB
Gain = 100 .....105 dB

Dynamic Characteristics

Bandwidth

All gains.....255 kHz

Settling time for full-scale step, all gains and ranges

To ±0.5 LSB .....40 µs typ
To ±1 LSB .....20 µs typ
To ±4 LSB .....10 µs typ

System noise (including quantization noise)

Gain = 1, 2, 5, 10 .....0.6 LSB rms bipolar,
0.8 LSB rms unipolar
Gain = 20 .....0.7 LSB rms bipolar,
1.1 LSB rms unipolar
Gain = 50 .....1.1 LSB rms bipolar,
2.0 LSB rms unipolar
Gain = 100 .....2.0 LSB rms bipolar,
3.8 LSB rms unipolar

Dynamic range ..... 91.7 dB, full-scale input with gain 1 to 10

Crosstalk ..... –70 dB max, DC to 100 kHz

Stability

Offset temperature coefficient

Pregain ..... ±5 µV/° C

Postgain ..... ±120 µV/° C

Gain temperature coefficient ..... ±7 ppm/° C

Analog Output (AT-MIO-16XE-10 only)

Output Characteristics

Number of channels ..... 2 voltage

Resolution ..... 16 bits, 1 in 65,536

Max update rate ..... 100 kS/s

Type of DAC ..... Double-buffered

FIFO buffer size ..... 2,048 samples

Data transfers ..... DMA, interrupts, programmed I/O

DMA modes ..... Single transfer, demand transfer

Transfer Characteristics

Relative accuracy (INL).....±0.5 LSB typ, ±1 LSB max

DNL.....±1 LSB max

Monotonicity .....16 bits, guaranteed

Offset error

After calibration.....305 µV max

Before calibration.....20 mV max

Gain error (relative to internal reference)

After calibration.....±30.5 ppm max

Before calibration.....±2,000 ppm max

Voltage Output

Range.....±10 V, 0 to 10 V (software selectable)

Output coupling .....DC

Output impedance .....0.1 Ω

Current drive.....±5 mA

Protection .....Short-circuit to ground

Power-on state .....0 V (± 20 mV)

Dynamic Characteristics

Settling time for full-scale step .....10 µs to ±1 LSB accuracy

Slew rate.....5 V/µs

Noise .....60 µVrms, DC to 1 MHz

Stability

Offset temperature coefficient ..... ±50 µV/° C

Gain temperature coefficient ..... ±7.5 ppm/° C

Digital I/O

Number of channels ..... 8 input/output

Compatibility ..... TTL/CMOS

Digital logic levels

Level	Min	Max
Input low voltage	0 V	0.8 V
Input high voltage	2 V	5 V
Input low current	—	–320 µA
Input high current	—	10 µA
Output low voltage (I_{OL} = 24 mA)	—	0.4 V
Output high voltage (I_{OH} = 13 mA)	4.35 V	—

Power-on state..... Input (High-Z)

Data transfers ..... Programmed I/O

Timing I/O

Number of channels ..... 2 up/down counter/timers,
1 frequency scaler

Resolution

Counter/timers..... 24 bits

Frequency scaler..... 4 bits

Compatibility ..... TTL/CMOS

Base clocks available
- Counter/timers .....20 MHz, 100 kHz
- Frequency scaler .....10 MHz, 100 kHz

Base clock accuracy.....±0.01%

Max source frequency.....20 MHz

Min source pulse duration .....10 ns, edge-detect mode

Min gate pulse duration .....10 ns, edge-detect mode

Data transfers.....DMA, interrupts, programmed I/O

DMA modes .....Single transfer

Triggers

Analog Trigger

Source.....ACH<0..15>, PFI0/TRIG1

Level.....± Full-scale, internal; ±10 V, external

Slope.....Positive or negative (software selectable)

Resolution.....12 bits, 1 in 4,096

Hysteresis .....Programmable

Bandwidth (–3 dB).....255 kHz internal, 4 MHz external

External input (PFI0/TRIG1)
- Impedance.....10 kΩ
- Coupling .....DC
- Protection.....–0.5 to Vcc +0.5 V when configured as a digital signal

  ±35 V when configured as an

analog trigger signal or disabled
±35 V powered off

Accuracy ..... ±1% of full-scale range

Digital Trigger

Compatibility ..... TTL

Response ..... Rising or falling edge

Pulse width..... 10 ns min

RTSI

Trigger Lines..... 7

Calibration

Recommended warm-up time ..... 15 min

Calibration interval ..... 1 year

External calibration reference ..... >6 and <9.999V

Onboard calibration reference

- Level ..... 5.000 V (±0.5 mV) (actual value stored in EEPROM)
- Temperature coefficient..... ±0.6 ppm/° C max
- Long-term stability ..... ±6 ppm/ $\sqrt{1,000h}$

Bus Interface

Type ..... Slave

Power Requirement

+5 VDC (±5%)..... 1.2 A

Power available at I/O connector..... +4.65 VDC to +5.25 VDC at 1 A

Physical

Dimensions
(not including connectors) .....33.8 by 9.9 cm (13.3 by 3.9 in)

I/O connector .....68-pin male SCSI-II type

Environment

Operating temperature .....0 to 55°C

Storage temperature .....–55 to 150° C

Relative humidity .....5% to 90% noncondensing

AT-MIO-16XE-50

Analog Input

Input Characteristics

Number of channels ..... 16 single-ended or 8 differential (software-selectable)

Type of ADC..... Successive approximation

Resolution ..... 16 bits, 1 in 65,536

Maximum sampling rate ..... 20 kS/s guaranteed

Input signal ranges

Board Gain (Software Selectable)	Board Range (Software Selectable)	
	Bipolar	Unipolar
1	±10 V	0 to 10 V
2	±5 V	0 to 5 V
10	±1 V	0 to 1 V
100	±0.1 V	0 to 0.1 V

Input coupling ..... DC

Maximum working voltage

(signal + common mode) ..... The average voltage of each differential pair should remain within ±8 V of ground

Overvoltage protection ..... ±25 V powered on, ±15 V powered off

Inputs protected ..... ACH<0..15>, AISENSE

FIFO buffer size ..... 512 samples

Data transfers.....DMA, interrupts, programmed I/O

DMA modes .....Single transfer, demand transfer

Configuration memory size.....512 words

Transfer Characteristics

Relative accuracy.....±0.5 LSB typ, ±1 LSB max

DNL.....±0.5 LSB typ, ±1 LSB max

No missing codes.....16 bits, guaranteed

Offset error

- Pregain error after calibration.....±3 µV max
- Pregain error before calibration....±1 mV max
- Postgain error after calibration.....±76 µV max
- Postgain error before calibration ..±4 mV max

Gain error (relative to calibration reference)

- After calibration (gain = 1).....±30.5 ppm of reading max
- Before calibration.....±2250 ppm of reading max

With gain error adjusted to 0 at gain = 1

- Gain = 2, 10 .....±100 ppm of reading
- Gain = 100 .....±250 ppm of reading

Amplifier Characteristics

Input impedance

- Normal, powered on.....7 GΩ in parallel with 100 pF
- Powered off.....820 Ω min
- Overload .....820 Ω min

Input bias current.....±10 nA

Input offset current .....±20 nA

CMRR, DC to 60 Hz

- Gain = 1 .....80 dB

Gain = 2 ..... 86 dB
Gain = 10..... 100 dB
Gain = 100..... 120 dB

Dynamic Characteristics

Bandwidth

Gain = 1, 2..... 63 kHz
Gain = 10..... 57 kHz
Gain = 100..... 33 kHz

Settling time for full-scale step ..... 50 µs max to ± 1 LSB, all gains and ranges

System noise (including quantization noise)

Gain = 1, 2, 10..... 0.5 LSB rms
Gain = 100..... 0.8 LSB rms bipolar, 1.4 LSB rms unipolar

Crosstalk ..... –85 dB max, DC to 20 kHz

Stability

Offset temperature coefficient

Pregain ..... ±1 µV/° C
Postgain..... ±12 µV/° C

Gain temperature coefficient ..... ±5 ppm/° C

Analog Output

Output Characteristics

Number of channels ..... 2 voltage

Resolution ..... 12 bits, 1 in 4,096

Max update rate..... 20 kS/s

Type of DAC ..... Double-buffered

FIFO buffer size..... None

Data transfers.....DMA, interrupts, programmed I/O

DMA modes .....Single transfer

Transfer Characteristics

Relative accuracy (INL).....±0.5 LSB max

DNL.....±1 LSB max

Monotonicity .....12 bits, guaranteed

Offset error

After calibration.....±0.5 mV max

Before calibration.....±85 mV max

Gain error (relative to calibration reference)

After calibration.....±0.01% of output max

Before calibration.....±1% of output max

Voltage Output

Range.....±10 V

Output coupling .....DC

Output impedance .....0.1 Ω max

Current drive.....±5 mA

Protection .....Short-circuit to ground

Power-on state .....0 V (± 85 mV)

Dynamic Characteristics

Settling time for full-scale step .....50 µs to ±0.5 LSB accuracy

Slew rate.....2 V/µs

Noise .....40 µVrms, DC to 1 MHz

Glitch energy (at midscale transition)

Magnitude .....±30 mV

Duration ..... 10 µs

Stability

Offset temperature coefficient ..... ±25 µV/° C

Gain temperature coefficient ..... ±15 ppm/° C

Digital I/O

Number of channels ..... 8 input/output

Compatibility ..... TTL/CMOS

Digital logic levels

Level	Min	Max
Input low voltage	0 V	0.8 V
Input high voltage	2 V	5 V
Input low current	—	–320 µA
Input high current	—	10 µA
Output low voltage (I_{OL} = 24 mA)	—	0.4 V
Output high voltage (I_{OH} = 13 mA)	4.35 V	—

Power-on state..... Input (High-Z)

Data transfers ..... Programmed I/O

Timing I/O

Number of channels ..... 2 up/down counter/timers,
1 frequency scaler

Resolution

Counter/timers..... 24 bits

Frequency scaler..... 4 bits

Compatibility.....TTL/CMOS

Base clocks available

Counter/timers .....20 MHz, 100 kHz

Frequency scaler .....10 MHz, 100 kHz

Base clock accuracy.....±0.01%

Max source frequency.....20 MHz

Min source pulse duration .....10 ns, edge-detect mode

Min gate pulse duration .....10 ns, edge-detect mode

Data transfers.....DMA, interrupts, programmed I/O

DMA modes .....Single transfer

Triggers

Digital Trigger

Compatibility.....TTL

Response.....Rising or falling edge

Pulse width .....10 ns min

RTSI

Trigger Lines 7

Calibration

Recommended warm-up time.....15 min

Calibration interval .....1 year

External calibration reference .....>6 and <9.999V

Onboard calibration reference

Level ..... 5.000 V (±2 mV) (actual value stored in EEPROM)

Temperature coefficient..... ±2 ppm/° C max

Long-term stability ..... ±15 ppm/ $\sqrt{1,000h}$

Bus Interface

Type ..... Slave

Power Requirement

+5 VDC (±5%)..... 0.75 A

Power available at I/O connector..... +4.65 VDC to +5.25 VDC at 1 A

Physical

Dimensions
(not including connectors)..... 33.8 by 9.9 cm (13.3 by 3.9 in)

I/O connector ..... 68-pin male SCSI-II type

Environment

Operating temperature..... 0 to 55° C

Storage temperature ..... –55 to 150° C

Relative humidity..... 5% to 90% noncondensing

Optional Cable Connector Descriptions

Appendix
B

This appendix describes the connectors on the optional cables for the AT E Series boards.

Figure B-1 shows the pin assignments for the 68-pin MIO connector. This connector is available when you use the SH6868 or R6868 cable assemblies with the AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-16E-10, AT-MIO-16XE-10, AT-AI-16XE-10, or AT-MIO-16XE-50. It is also one of the two 68-pin connectors available when you use the SH1006868 cable assembly with the AT-MIO-16DE-10 or AT-MIO-64E-3.

ACH8	34	68	ACH0
ACH1	33	67	AIGND
AIGND	32	66	ACH9
ACH10	31	65	ACH2
ACH3	30	64	AIGND
AIGND	29	63	ACH11
ACH4	28	62	AISENSE
AIGND	27	61	ACH12
ACH13	26	60	ACH5
ACH6	25	59	AIGND
AIGND	24	58	ACH14
ACH15	23	57	ACH7
DAC0OUT[1]	22	56	AIGND
DAC1OUT[1]	21	55	AOGND
EXTREF[2]	20	54	AOGND
DIO4	19	53	DGND
DGND	18	52	DIO0
DIO1	17	51	DIO5
DIO6	16	50	DGND
DGND	15	49	DIO2
+5 V	14	48	DIO7
DGND	13	47	DIO3
DGND	12	46	SCANCLK
PFI0/TRIG1	11	45	EXTSTROBE*
PFI1/TRIG2	10	44	DGND
DGND	9	43	PFI2/CONVERT*
+5 V	8	42	PFI3/GPCTR1_SOURCE
DGND	7	41	PFI4/GPCTR1_GATE
PFI5/UPDATE*	6	40	GPCTR1_OUT
PFI6/WFTRIG	5	39	DGND
DGND	4	38	PFI7/STARTSCAN
PFI9/GPCTR0_GATE	3	37	PFI8/GPCTR0_SOURCE
GPCTR0_OUT	2	36	DGND
FREQ_OUT	1	35	DGND

[1] Not available on AT-AI-16XE-10

[2] Not available on AT-MIO-16XE-10, AT-AI-16XE-10, or AT-MIO-16XE-50

Figure B-1. 68-Pin MIO Connector Pin Assignments

Figure B-2 shows the pin assignments for the 68-pin DIO connector. This is the other 68-pin connector available when you use the SH1006868 cable assembly with the AT-MIO-16DE-10.

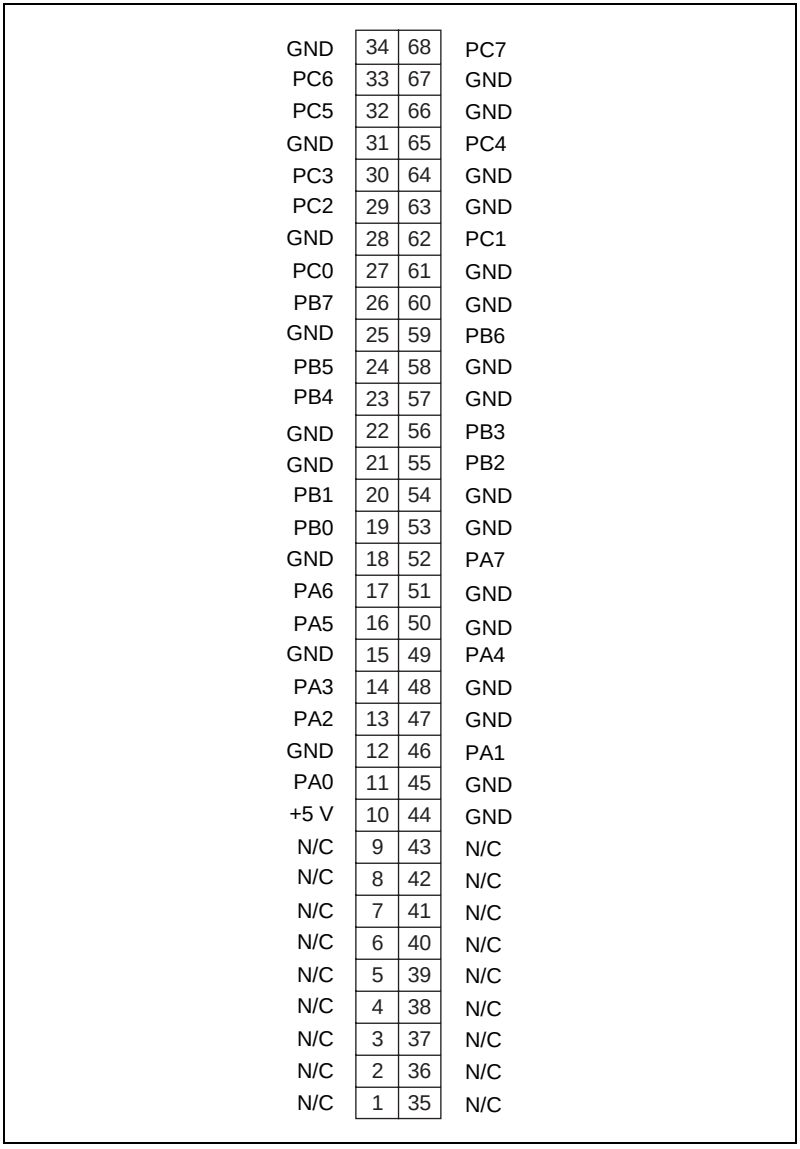


Figure B-2. 68-Pin DIO Connector Pin Assignments

Figure B-3 shows the pin assignments for the 68-pin extended analog input connector. This is the other 68-pin connector available when you use the SH1006868 cable assembly with the AT-MIO-64E-3.

ACH 24	34	68	ACH 16
ACH 17	33	67	ACH 25
ACH 18	32	66	ACH 26
ACH 27	31	65	ACH 19
ACH 20	30	64	ACH 28
ACH 21	29	63	ACH 29
ACH 30	28	62	ACH 22
ACH 23	27	61	ACH 31
ACH 32	26	60	ACH 40
ACH 41	25	59	ACH 33
ACH 34	24	58	ACH 42
ACH 35	23	57	ACH 43
AIGND	22	56	AISENSE2
ACH 44	21	55	ACH 36
ACH 37	20	54	ACH 45
ACH 38	19	53	ACH 46
ACH 47	18	52	ACH 39
ACH 48	17	51	ACH 56
ACH 49	16	50	ACH 57
ACH 58	15	49	ACH 50
ACH 51	14	48	ACH 59
ACH 52	13	47	ACH 60
ACH 61	12	46	ACH 53
ACH 54	11	45	ACH 62
ACH 55	10	44	ACH 63
N/C	9	43	N/C
N/C	8	42	N/C
N/C	7	41	N/C
N/C	6	40	N/C
N/C	5	39	N/C
N/C	4	38	N/C
N/C	3	37	N/C
N/C	2	36	N/C
N/C	1	35	N/C

Figure B-3. 68-Pin Extended Analog Input Connector Pin Assignments

Figure B-4 shows the pin assignments for the 50-pin MIO connector. This connector is available when you use the SH6850 or R6850 cable assemblies with the AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-16E-10, AT-MIO-16XE-10, AT-AI-16XE-10, or AT-MIO-16XE-50. It is also one of the two 50-pin connectors available when you use the R1005050 cable assembly with the AT-MIO-16DE-10 or AT-MIO-64E-3.

AIGND	1	2	AIGND
ACH0	3	4	ACH8
ACH1	5	6	ACH9
ACH2	7	8	ACH10
ACH3	9	10	ACH11
ACH4	11	12	ACH12
ACH5	13	14	ACH13
ACH6	15	16	ACH14
ACH7	17	18	ACH15
AISENSE	19	20	DAC0OUT
DAC1OUT	21	22	EXTREF
AOGND	23	24	DGND
DIO0	25	26	DIO4
DIO1	27	28	DIO5
DIO2	29	30	DIO6
DIO3	31	32	DIO7
DGND	33	34	+5 V
+5 V	35	36	SCANCLK
EXTSTROBE*	37	38	PFI0/TRIG1
PFI1/TRIG2	39	40	PFI2/CONVERT*
PFI3/GPCTR1_SOURCE	41	42	PFI4/GPCTR1_GATE
GPCTR1_OUT	43	44	PFI5/UPDATE*
PFI6/WFTRIG	45	46	PFI7/STARTSCAN
PFI8/GPCTR0_SOURCE	47	48	PFI9/GPCTR0_GATE
GPCTR0_OUT	49	50	FREQ_OUT

Figure B-4. 50-Pin MIO Connector Pin Assignments

Figure B-5 shows the pin assignments for the 50-pin DIO connector. This is the other 50-pin connector available when you use the R1005050 cable assembly with the AT-MIO-16DE-10.

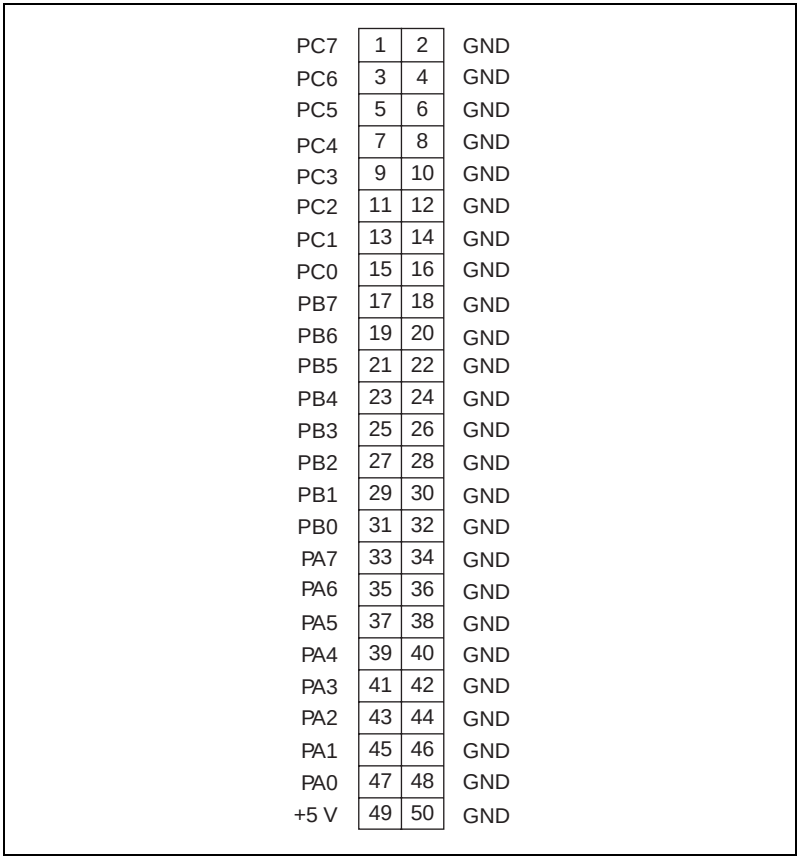


Figure B-5. 50-Pin DIO Connector Pin Assignments

Figure B-6 shows the pin assignments for the 50-pin extended analog input connector. This is the other 50-pin connector available when you use the R1005050 cable assembly with the AT-MIO-64E-3.

ACH16	1	2	ACH24
ACH17	3	4	ACH25
ACH18	5	6	ACH26
ACH19	7	8	ACH27
ACH20	9	10	ACH28
ACH21	11	12	ACH29
ACH22	13	14	ACH30
ACH23	15	16	ACH31
ACH32	17	18	ACH40
ACH33	19	20	ACH41
ACH34	21	22	ACH42
ACH35	23	24	ACH43
AISENSE2	25	26	AIGND
ACH36	27	28	ACH44
ACH37	29	30	ACH45
ACH38	31	32	ACH46
ACH39	33	34	ACH47
ACH48	35	36	ACH56
ACH49	37	38	ACH57
ACH50	39	40	ACH58
ACH51	41	42	ACH59
ACH52	43	44	ACH60
ACH53	45	46	ACH61
ACH54	47	48	ACH62
ACH55	49	50	ACH63

Figure B-6. 50-Pin Extended Analog Input Connector Pin Assignments

Common Questions

Appendix
C

This appendix contains a list of commonly asked questions and their answers relating to usage and special features of your AT E Series board.

General Information

1. What are the AT E Series boards?

The AT E Series boards are switchless and jumperless, enhanced MIO boards that use the DAQ-STC for timing.

2. What is the DAQ-STC?

The DAQ-STC is the new system timing control ASIC (application-specific integrated circuit) designed by National Instruments and is the backbone of the AT E Series boards. The DAQ-STC contains seven 24-bit counters and three 16-bit counters. The counters are divided into three groups:

- Analog input—two 24-bit, two 16-bit counters
- Analog output—three 24-bit, one 16-bit counters
- General-purpose counter/timer functions—two 24-bit counters

The groups can be configured independently with timing resolutions of 50 ns or 10 µs. With the DAQ-STC, you can interconnect a wide variety of internal timing signals to other internal blocks. The interconnection scheme is quite flexible and completely software configurable. New capabilities such as buffered pulse generation, equivalent time sampling, and seamlessly changing the sampling rate are possible.

3. How fast is each AT E Series board?

The last numeral in the name of an AT E Series board specifies the settling time in microseconds for that particular board. For example, the AT-MIO-16E-2 has a 2 µs settling time, which corresponds to a sampling rate of 500 kS/s. These sampling rates are aggregate: one channel at 500 kS/s or two channels at 250 kS/s per channel illustrates the relationship. Notice, however,

that some AT E Series boards have settling times that vary with gain and accuracy. See Appendix A for exact specifications.

4. **What type of 5 V protection do the AT E Series boards have?**

   The AT E Series boards have 5 V lines equipped with a self-resetting 1 A fuse.

Installation and Configuration

5. **How do I configure an AT E Series board on an EISA computer?**

   You must configure the board with `the NIDAQ Configuration Utility`; you cannot use an EISA configuration utility to configure the board.

6. **How do you set the base address for an AT E Series board?**

   For Windows NT or Windows 3.1*x*, use the NI-DAQ Configuration Utility to type in the desired base I/O address. For Windows 95, the base address can be changed in the Device Manager. Note that for Windows 95 or 3.1*x*, the operating system detects the board and preassigns a base address. 0x180, 200, 220, 240, 280, and 300 are typical base addresses.

7. **What jumpers should I be aware of when configuring my AT E Series board?**

   The AT E Series boards do not contain any jumpers; they are also switchless.

8. **Which National Instruments manual should I read first to get started using DAQ software?**

   If you are using LabVIEW, Chapter 1 of the *LabVIEW Data Acquisition VI Reference Manual* is the best place to get started. If you are programming with NI-DAQ function calls or using LabWindows/CVI, the *NI-DAQ User Manual for PC Compatibles* is the best starting place.

9. **What version of NI-DAQ must I have to program my AT E Series board?**

   You must have version 4.9.0 or higher for the AT-MIO-16XE-10 and AT-AI-16XE-10, version 4.8.0 or higher for the

AT-MIO-16E-1, and version 4.6.1 or higher for all other AT E Series boards.

For AT-MIO-16E-10 and AT-MIO-16DE-10 users, you must have version 5.04 for Windows 3.1*x* or 5.1 for Windows 95 and Windows NT to use boards after and including board N. Previous boards before N require NI-DAQ 4.6.1 or higher.

10. What special calls must be made in DOS or LabWindows to use AT E Series boards?

To link in the AT E Series function calls, you must call `USE_E_Series` or one of its subsets.

11. What is the best way to test my board without having to program the board?

If you are using Windows, the `NI-DAQ Configuration` Utility has a Test menu with some excellent tools for doing simple functional tests of the board, such as analog input and output, digital I/O, and counter/timer tests. Also, the Test Configuration option will verify that the base address, interrupt, and DMA settings for the board are functioning properly.

12. I have several DAQ boards that use more total interrupt and DMA channels than I have available in my PC. What should I do?

By using the proper configuration utility, `NI-DAQ Configuration Utility`, you can disable interrupt and DMA channels for the board you are using. You may be more limited in the functionality of the board (usually regarding high-speed acquisition), but you should at least be able to use basic functionality for all boards in the system.

13. How can I select an AT E Series board as my device type in `the NI-DAQ Configuration Utility`?

First, make sure your board is plugged into your computer. The `NI-DAQ Configuration` Utility can scan your system for any AT E Series devices. If no AT E Series boards are found, the AT E Series device types are not given as choices.

Analog Input and Output

14. I'm using my board in differential analog input mode and I have connected a differential input signal, but my readings are random and drift rapidly. What's wrong?

Check your ground reference connections. Your signal may be referenced to a level that is considered *floating* with reference to the board ground reference. Even if you are in differential mode, the signal *must* still be referenced to the same ground level as the board reference. There are various methods of achieving this while maintaining a high common-mode rejection ratio (CMRR). These methods are outlined in Chapter 4, *Signal Connections*.

15. Can I sample across a number of channels on an AT E Series board while each channel is being sampled at a different rate?

NI-DAQ for PC compatibles version 4.5.1 or later features a new function called `SCAN_Sequence_Setup`, which allows for multirate scanning of your analog input channels. Refer to the *NI-DAQ Function Reference Manual for PC Compatibles* for more details.

16. I'm using the DACs to generate a waveform, but I discovered with a digital oscilloscope that there are glitches on the output signal. Is this normal?

When it switches from one voltage to another, any DAC produces glitches due to released charges. The largest glitches occur when the most significant bit (MSB) of the D/A code switches. You can build a lowpass deglitching filter to remove some of these glitches, depending on the frequency and nature of your output signal. The AT-MIO-16E-1, AT-MIO-16E-2 and the AT-MIO-64E-3 boards have built-in reglitchers, which can be enabled through software, on their analog output channels. See the *Analog Output Reglitch Selection* section in Chapter 3, *Hardware Overview*, for more information about reglitching.

17. Can I synchronize a one-channel analog input data acquisition with a one-channel analog output waveform generation on my AT E Series board?

Yes. One way to accomplish this is to use the waveform generation timing pulses to control the analog input data acquisition. To do this, follow steps a through d below, in addition to the usual steps for data acquisition and waveform generation configuration.

a. Enable the PFI5 line for output, as follows:

   If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_PFI_5, ND_OUT_UPDATE, ND_HIGH_TO_LOW)`.

   If you are using LabVIEW, invoke Route Signal VI with signal name set to PFI5 and signal source set to AO Update.

b. Set up data acquisition timing so that the timing signal for A/D conversion comes from PFI5, as follows:

   If you are using NI-DAQ, call `Select_Signal(deviceNumber, ND_IN_CONVERT, ND_PFI_5, ND_HIGH_TO_LOW)`.

   If you are using LabVIEW, invoke AI Clock Config VI with clock source code set to PFI pin, high to low, and clock source string set to 5.

c. Initiate analog input data acquisition, which will start only when the analog output waveform generation starts.

   For example, if you are using NI-DAQ, you can call `DAQ_Start` with appropriate parameters.

   Similarily, if you are using LabVIEW, you can invoke AI Control VI with control code set to 0 (start).

d. Initiate analog output waveform generation.

   If you are using NI-DAQ, call `WFM_Group_Control` with operation set to 1 (start).

   If you are using LabVIEW, you can invoke AO Control VI with control code set to 0 (start).

Timing and Digital I/O

18. What types of triggering can be implemented in hardware on my AT E Series board?

Digital triggering is supported by hardware on every AT E Series MIO board. In addition, the AT-MIO-16E-1, AT-MIO-16E-2, AT-MIO-64E-3, AT-MIO-16XE-10, and AT-AI-16XE-10 support analog triggering in hardware.

19. What added functionality does the DAQ-STC make possible in contrast to the Am9513?

The DAQ-STC incorporates much more than just 10 Am9513-style counters within one chip. In fact, the DAQ-STC has the complexity

of more than 24 chips. The DAQ-STC makes possible PFI lines, analog triggering, selectable logic level, and frequency shift keying. The DAQ-STC also makes buffered operations possible, such as direct up/down control, single or pulse train generation, equivalent time sampling, buffered period, and buffered semiperiod measurement.

20. What is the difference in timebases between the Am9513 counter/timer and the DAQ-STC?

The DAQ-STC-based MIO boards have a 20 MHz timebase. The Am9513-based MIO boards have a 1 MHz or 5 MHz timebase.

21. The counter/timer examples supplied with NI-DAQ are not compatible with an AT E Series board. Where can I find examples to illustrate the use of the DAQ-STC as a general-purpose counter/timer?

If you are using the NI-DAQ language interface and a C compiler under DOS, a new subdirectory called `GPCTR`, which lies beneath the `examples` directory, contains 16 examples of the most common uses of the DAQ-STC.

22. Will the counter/timer applications that I wrote previously work with the DAQ-STC?

If you are using NI-DAQ with LabVIEW, some of your applications drawn using the CTR VIs will still run. However, there are many differences in the counters between the AT E Series and other boards; the counter numbers are different, timebase selections are different, the DAQ-STC counters are 24-bit counters (unlike the 16-bit counters on boards without the DAQ-STC).

If you are using NI-DAQ language interface, LabWindows, or LabWindows/CVI, the answer is, no, the counter/time applications that you wrote previously will not work with the DAQ-STC. You must use the GPCTR functions; ICTR and CTR functions will not work with the DAQ-STC. The GPCTR functions have the same capabilities as the ICTR and CTR functions, plus more, but you must rewrite the application with the GPCTR function calls.

23. I'm using one of the general-purpose counter/timers on my AT E Series board, but I do not see the counter/timer output on the I/O connector. What am I doing wrong?

If you are using NI-DAQ language interface or LabWindows/CVI, you must configure the output line to output the signal to the I/O connector. Use the `Select_Signal` call in NI-DAQ to configure the output line. By default, all timing I/O lines except EXTSTROBE* are tri-stated.

24. How does NI-DAQ treat bogus missed data transfer errors that can arise during DMA-driven GPCTR buffered-input operations?

When doing buffered transfers using GPCTR function calls with DMA, you can call `GPCTR_Watch` to indicate **dataTransfer** errors. NI-DAQ takes a snapshot of transfers and counts how many points have been transferred. If all the points have been transferred and the first instance of this error occurs, NI-DAQ returns a **gpctrDataTransferWarning** indicating that the error could be bogus. If all the points have not been transferred, NI-DAQ returns the genuine error. The error continues to be returned until the acquisition completes. The above error occurs because NI-DAQ disarms the counter from generating any more requests in the interrupt service routine. Due to interrupt latencies, it is possible that the counter may have generated some spurious requests which the DMA controller may not satisfy because it has already transferred the required number of points.

25. What are the PFIs and how do I configure these lines?

PFIs are Programmable Function Inputs. These lines serve as connections to virtually all internal timing signals.

If you are using NI-DAQ language interface, LabWindows, or LabWindows/CVI, use the `Select_Signal` function to route internal signals to the I/O connector, route external signals to internal timing sources, or tie internal timing signals together.

If you are using NI-DAQ with LabVIEW and you want to connect external signal sources to the PFI lines, you can use AI Clock Config, AI Trigger Config, AO Clock Config, AO Trigger and Gate Config, CTR Mode Config, and CTR Pulse Config advanced level VIs to indicate which function the connected signal will serve. Use the Route Signal VI to enable the PFI lines to output internal signals.

Caution: ***If you enable a PFI line for output, do not connect any external signal source to it; if you do, you can damage the board, the computer, and the connected equipment.***

26. What are the power-on states of the PFI and DIO lines on the I/O connector?

At system power-on and reset, both the PFI and DIO lines are set to high impedance by the hardware. This means that the board circuitry is not actively driving the output either high or low. However, these lines may have pull-up or pull-down resistors connected to them as shown in Tables 4-1 to 4-4, *I/O Signal Summary*. These resistors weakly pull the output to either a logic high or logic low state. For example, DIO(0) will be in the high impedance state after power on, and Table 4-1 shows that there is a 50 kΩ pull-up resistor. This pull-up resistor will set the DIO(0) pin to a logic high when the output is in a high impedance state.

Customer Communication

Appendix
D

For your convenience, this appendix contains forms to help you gather the information necessary to help us solve your technical problems and a form you can use to comment on the product documentation. When you contact us, we need the information on the Technical Support Form and the configuration form, if your manual contains one, about your system configuration to answer your questions as quickly as possible.

National Instruments has technical assistance through electronic, fax, and telephone systems to quickly provide the information you need. Our electronic services include a bulletin board service, an FTP site, a fax-on-demand system, and e-mail support. If you have a hardware or software problem, first try the electronic support systems. If the information available on these systems does not answer your questions, we offer fax and telephone support through our technical support centers, which are staffed by applications engineers.

Electronic Services

Bulletin Board Support

National Instruments has BBS and FTP sites dedicated for 24-hour support with a collection of files and documents to answer most common customer questions. From these sites, you can also download the latest instrument drivers, updates, and example programs. For recorded instructions on how to use the bulletin board and FTP services and for BBS automated information, call (512) 795-6990. You can access these services at:

United States: (512) 794-5422
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United Kingdom: 01635 551422
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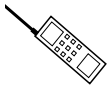
E-Mail Support (currently U.S. only)

You can submit technical support questions to the applications engineering team through e-mail at the Internet address listed below. Remember to include your name, address, and phone number so we can contact you with solutions and suggestions.

`support@natinst.com`

Telephone and Fax Support

National Instruments has branch offices all over the world. Use the list below to find the technical support number for your country. If there is no National Instruments office in your country, contact the source from which you purchased your software to obtain support.



	Telephone	Fax
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Austria	0662 45 79 90 0	0662 45 79 90 19
Belgium	02 757 00 20	02 757 03 11
Canada (Ontario)	905 785 0085	905 785 0086
Canada (Quebec)	514 694 8521	514 694 4399
Denmark	45 76 26 00	45 76 26 02
Finland	09 725 725 11	09 725 725 55
France	01 48 14 24 24	01 48 14 24 14
Germany	089 741 31 30	089 714 60 35
Hong Kong	2645 3186	2686 8505
Israel	03 5734815	03 5734816
Italy	02 413091	02 41309215
Japan	03 5472 2970	03 5472 2977
Korea	02 596 7456	02 596 7455
Mexico	5 520 2635	5 520 3282
Netherlands	0348 433466	0348 430673
Norway	32 84 84 00	32 84 86 00
Singapore	2265886	2265887
Spain	91 640 0085	91 640 0533
Sweden	08 730 49 70	08 730 43 70
Switzerland	056 200 51 51	056 200 51 55
Taiwan	02 377 1200	02 737 4644
United Kingdom	01635 523545	01635 523154
United States	512 795 8248	512 794 5678

Technical Support Form

Photocopy this form and update it each time you make changes to your software or hardware, and use the completed copy of this form as a reference for your current configuration. Completing this form accurately before contacting National Instruments for technical support helps our applications engineers answer your questions more efficiently.

If you are using any National Instruments hardware or software products related to this problem, include the configuration forms from their user manuals. Include additional pages if necessary.

Name _____

Company _____

Address _____

_____

Fax (___)_____ Phone (___) _____

Computer brand _____ Model _____ Processor_____

Operating system (include version number) _____

Clock speed _____MHz RAM _____MB Display adapter _____

Mouse ___yes ___no Other adapters installed _____

Hard disk capacity _____MB Brand _____

Instruments used _____

_____

National Instruments hardware product model _____ Revision _____

Configuration _____

National Instruments software product _____ Version _____

Configuration _____

The problem is: _____

_____

_____

_____

_____

List any error messages: _____

_____

_____

The following steps reproduce the problem:_____

_____

_____

_____

_____

_____

AT E Series Hardware and Software Configuration Form

Record the settings and revisions of your hardware and software on the line to the right of each item. Complete a new copy of this form each time you revise your software or hardware configuration, and use this form as a reference for your current configuration. Completing this form accurately before contacting National Instruments for technical support helps our applications engineers answer your questions more efficiently.

National Instruments Products

AT E Series Board _____

AT E Series Board Serial Number _____

Interrupt Level of AT E Series Board _____

DMA Channels of AT E Series Board _____

Base I/O Address of AT E Series Board _____

Programming Choice (NI-DAQ, LabVIEW, LabWindows/CVI, or other) _____

Software Version _____

Other Products

Computer Model _____

Microprocessor _____

Clock Frequency _____

Type of Video Board Installed _____

Operating System (DOS or Windows) _____

Operating System Version _____

Operating System Mode _____

Programming Language _____

Programming Language Version _____

Other Boards in System _____

Base I/O Address of Other Boards _____

DMA Channels of Other Boards _____

Interrupt Level of Other Boards _____

Documentation Comment Form

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Please comment on the completeness, clarity, and organization of the manual.

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If you find errors in the manual, please record the page numbers and describe the errors.

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Prefix	Meaning	Value
p-	pico-	10^{-12}
n-	nano-	10^{-9}
µ-	micro-	10^{-6}
m-	milli-	10^{-3}
k-	kilo-	10^{3}
M-	mega-	10^{6}
G-	giga-	10^{9}

Symbols

%	percent
±	plus or minus
°	degrees
/	per
+	positive of, or plus
–	negative of, or minus
Ω	ohms
$\sqrt{\ }$	square root of
+5V	+5 VDC source signal

A

A	amperes
AC	alternating current
ACH	analog input channel signal
A/D	analog-to-digital
ADC	A/D converter
AIGATE	analog input gate signal
AIGND	analog input ground signal
AISENSE	analog input sense signal
AISENSE2	analog input sense 2 signal
ANSI	American National Standards Institute
AOGND	analog output ground signal
ASIC	application-specific integrated circuit

B

BIOS	basic input/output system or built-in operating system

C

C	Celsius
CalDAC	calibration DAC
CMOS	complementary metal-oxide semiconductor
CMRR	common-mode rejection ratio
CONVERT*	convert signal

D

D/A	digital-to-analog
DAC	D/A converter
DAC0OUT	analog channel 0 output signal
DAC1OUT	analog channel 1 output signal
DAQ	data acquisition
DC	direct current
DGND	digital ground signal
DIFF	differential mode
DIO	digital input/output
DMA	direct memory access
DNL	differential nonlinearity

E

EEPROM	electrically erasable programmable read-only memory
EISA	Extended Industry Standard Architecture
EXTREF	external reference signal
EXTSTROBE	external strobe signal

F

FIFO	first-in-first-out
FREQ_OUT	frequency output signal
ft	feet

G

GPCTR0_GATE	general purpose counter 0 gate signal
GPCTR1_GATE	general purpose counter 1 gate signal
GPCTR0_OUT	general purpose counter 0 output signal
GPCTR1_OUT	general purpose counter 1 output signal
GPCTR0_SOURCE	general purpose counter 0 clock source signal
GPCTR1_SOURCE	general purpose counter 1 clock source signal

H

h	hour
hex	hexadecimal
Hz	hertz

I

I/O	input/output
I_{OH}	current, output high
I_{OL}	current, output low
ISA	Industry Standard Architecture

L

LASTCHAN	last channel (bit)
LSB	least significant bit

M

MB	megabytes of memory
min	minimum
min.	minutes
MIO	multifunction I/O
MSB	most significant bit

N

NRSE	nonreferenced single-ended mode

O

OUT	output

P

PC	personal computer
PFI	Programmable Function Input
PGIA	Programmable Gain Instrumentation Amplifier
ppm	parts per million

R

rms	root mean square
RSE	referenced single-ended mode
RTD	resistive temperature device
RTSI	Real-Time System Integration

S

s	seconds
S	samples
SCANCLK	scan clock signal
SCXI	Signal Conditioning eXtensions for Instrumentation
SE	single-ended inputs
SISOURCE	SI counter clock signal
STARTSCAN	start scan signal

T

TC	terminal count
THD	total harmonic distortion
TRIG	trigger signal
TTL	transistor-transistor logic

U

UI	update interval
UISOURCE	update interval counter clock signal
UPDATE	update signal

V

V	volts
VDC	volts direct current
V_{IH}	volts, input high

V_{IL}	volts, input low
V_{in}	volts in
V_{OH}	volts, output high
V_{OL}	volts, output low
V_{ref}	reference voltage

W

WFTRIG	waveform generation trigger signal

Index

Symbols

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