USER MANUAL

PXIe-6674T

PXI Express Timing and Synchronization Module

The PXIe-6674T enables you to pass PXI timing and trigger signals between PXI Express chassis. The PXIe-6674T can generate and route clock signals between devices in multiple chassis, providing a method to synchronize multiple devices in a multichassis PXI Express system.

This manual describes the electrical and mechanical aspects of the PXIe-6674T and contains information concerning its operation and programming.

National Instruments Documentation

The PXIe-6674T User Manual is one piece of the documentation set for your measurement system. You could have any of several other documents describing your hardware and software. Use the documentation you have as follows:

- Measurement hardware documentation—This documentation contains detailed information about the measurement hardware that plugs into or is connected to the computer. Use this documentation for hardware installation and configuration instructions, specifications about the measurement hardware, and application hints.

- Software documentation—Refer to the NI-Sync Help, available at `ni.com/manuals`.

You can download NI documentation from `ni.com/manuals`.

Related Documentation

The following documents contain information that you might find helpful as you read this manual:

- *PICMG 2.0 R3.0, CompactPCI Core Specification*, available from PICMG at `www.picmg.org`.
- *PXI Specification, Revision 2.1*, available from `www.pxisa.org`.
- *NI-VISA User Manual*, available from `ni.com/manuals`.
- *NI-VISA Help*, included with the NI-VISA software.
- *NI-Sync User Manual*, available from `ni.com/manuals`.
- *PXIe-6674T Calibration Procedure*, available from `ni.com/manuals`.

NATIONAL INSTRUMENTS™

Contents

Introduction

The PXIe-6674T timing and synchronization module enables you to share clocks and triggers between modules in a PXI Express chassis and other PXI chassis or non-PXI systems. The PXIe-6674T module generates and routes clock signals between devices in multiple chassis, providing a method for synchronizing multiple devices in a PXI Express system. It also features a precision OCXO for improving the stability and accuracy of the PXI Express backplane reference clocks.

Unpacking

The PXIe-6674T is shipped in an antistatic package to prevent electrostatic damage to the module. Electrostatic discharge (ESD) can damage the module.

⚠ **Caution** Never touch the exposed pins of connectors.

To avoid such damage in handling the module, take the following precautions:

- Ground yourself using a grounding strap or by touching a grounded object.
- Touch the antistatic package to the metal part of the computer chassis before removing the module from the package.

Remove the module from the package and inspect the module for loose components or any sign of damage. Notify NI if the module appears damaged in any way. Do not install a damaged module into the computer.

Store the PXIe-6674T in the antistatic envelope when not in use.

Software Programming Choices

When programming the PXIe-6674T, you can use NI application development environment (ADE) software such as LabVIEW or LabWindows/CVI, or you can use other ADEs, such as Visual C/C++.

LabVIEW features interactive graphics, a state-of-the-art interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of virtual instruments for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW.

LabWindows/CVI is a complete ANSI C ADE that features an interactive video interface, code generation tools, and the LabWindows/CVI Data Acquisition and Easy I/O libraries.

Safety Information

The following section contains important safety information that you must follow when installing and using the product.

Do not operate the product in a manner not specified in this document. Misuse of the product can result in a hazard. You can compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to National Instruments for repair.

Do not substitute parts or modify the product except as described in this document. Use the product only with the chassis, modules, accessories, and cables specified in the installation instructions. You must have all covers and filler panels installed during operation of the product.

Do not operate the product in an explosive atmosphere or where there may be flammable gases or fumes. If you must operate the product in such an environment, it must be in a suitable rated enclosure.

If you need to clean the product, use a soft, nonmetallic brush. The product must be completely dry and free from contaminants before you return it to service.

Operate the product only at or below Pollution Degree 2. Pollution is foreign matter in a solid, liquid , or gaseous state that can reduce dielectric strength or surface resistivity. The following is a description of pollution degrees:

- Pollution Degree 1 means no pollution or only dry, nonconductive pollution occurs. The pollution has no influence.
- Pollution Degree 2 means that only nonconductive pollution occurs in most cases. Occasionally, however, a temporary conductivity caused by condensation must be expected.
- Pollution Degree 3 means that conductive pollution occurs, or dry, nonconductive pollution occurs that becomes conductive due to condensation.

You must insulate signal connections for the maximum voltage for which the product is rated. Do not exceed the maximum ratings for the product. Do not install wiring while the product is live with electrical signals. Do not remove or add connector blocks when power is connected to the system. Avoid contact between your body and the connector block signal when hot swapping modules. Remove power from signal lines before connecting them to or disconnecting them from the product.

Operate the product at or below the measurement category[1] marked on the hardware label. Measurement circuits are subjected to working voltages[2] and transient stresses (overvoltage) from the circuit to which they are connected during measurement or test. Measurement categories establish standard impulse to withstand voltage levels that commonly occur in electrical distribution systems. The following is a description of measurement categories:

- Measurement Category I is for measurements performed on circuits not directly connected to the electrical distribution system referred to as MAINS[3] voltage. This category is for measurements of voltages from specially protected secondary circuits. Such voltage measurements include signal levels, special hardware, limited-energy parts of hardware, circuits powered by regulated low-voltage sources, and electronics.
- Measurement Category II is for measurements performed on circuits directly connected to the electrical distribution system (MAINS[3]). This category refers to local-level electrical distribution, such as that provided by a standard wall outlet (for example, 115 AC voltage for U.S. or 230 AC voltage for Europe). Examples of Measurement Category II are measurements performed on household appliances, portable tools, and similar hardware.
- Measurement Category III is for measurements performed in the building installation at the distribution level. This category refers to measurements on hard-wired hardware such as hardware in fixed installations, distribution boards, and circuit breakers. Other

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[1] Measurement categories, also referred to as overvoltage or installation categories, are defined in electrical safety standard IEC 61010-1 and IEC 60664-1.

[2] Working voltage is the highest rms value of an AC or DC voltage that can occur across any particular insulation.

[3] MAINS is defined as a hazardous live electrical supply system that powers hardware. Suitably rated measuring circuits may be connected to the MAINS for measuring purposes.

examples are wiring, including cables, bus bars, junction boxes, switches, socket outlets in the fixed installation, and stationary motors with permanent connections to fixed installations.

- Measurement Category IV is for measurements performed at the primary electrical supply installation typically outside buildings. Examples include electricity meters and measurements on primary overcurrent protection devices and on ripple control units.

What You Need to Get Started

To set up and use the PXIe-6674T, you need the following items:

- PXIe-6674T Timing and Synchronization Module
- PXIe-6674T User Manual
- NI-Sync driver
- One of the following software packages and documentation:
  - LabVIEW
  - LabWindows™/CVI™
  - Microsoft Visual C++ (MSVC)
- PXI EMC filler panels, National Instruments part number 778700-01
- PXI Express chassis
- PXI Express embedded controller or a desktop computer connected to the PXI Express chassis using MXI-Express hardware.

The *NI-Sync User Manual* offers more detailed information on the software used to program the PXIe-6674T. You can find this manual at `ni.com/manuals`.

Installing and Configuring

This chapter describes how to install the PXIe-6674T hardware and software and how to configure the device.

Installing the Software

Refer to the `readme.htm` file tha accompanies the NI-Sync driver for software installation directions.

📝 **Note** Be sure to install the driver software before installing the PXIe-6674T hardware.

Installing the Hardware

The following are general installation instructions. Consult the chassis user manual or technical reference manual for specific instructions and warnings about installing new modules.

1. Power off and unplug the chassis.
2. Locate the system timing slot for your PXI Express chassis. It is identified by the glyph shown in *Figure 1.* on page 6:

Figure 1. System Timing Slot Indicator Glyph
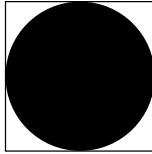
3. Remove the filler panel for the system timing slot, if applicable.
4. Ground yourself using a grounding strap or by touching a grounded object. Follow the ESD protection precautions described in the *Unpacking* section of the *Introduction*.
5. Carefully insert the PXIe-6674T into the system timing slot, making sure to not scrape the module on any adjacent modules. Use the injector/ejector handle to fully insert the module into the chassis.
6. Screw the front panel of the device to the front panel mounting rail of the chassis.
7. If adjacent slots are not populated, use EMC filler panels to cover the opening.

⚠️ **Caution**
- To ensure the specified EMC performance, you must install PXI EMC filler panels, National Instruments part number 778700-01, in all open chassis slots.
- To ensure the specified EMC performance, operate this product only with double-shielded cables and accessories (for example, RG-223 cables).

8. Visually verify the installation. Ensure that the module is fully inserted into the slot.
9. Plug in and power on the chassis.

The PXIe-6674T is now installed.

Configuring the Module

The PXIe-6674T is completely software configurable. The system software automatically allocates all module resources.

The two LEDs on the front panel provide information about module status. The front panel description sections of the Hardware Overview describe the LEDs in greater detail.
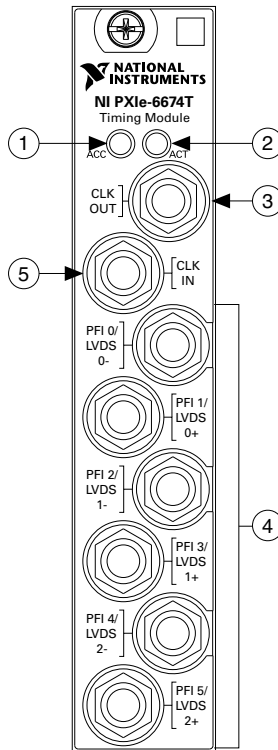
Hardware Overview

This chapter presents an overview of the hardware functions of the PXIe-6674T. Refer to *Figure 2.* on page 8 for a functional overview of the PXIe-6674T hardware.

Figure 2. PXIe-6674T Functional Overview
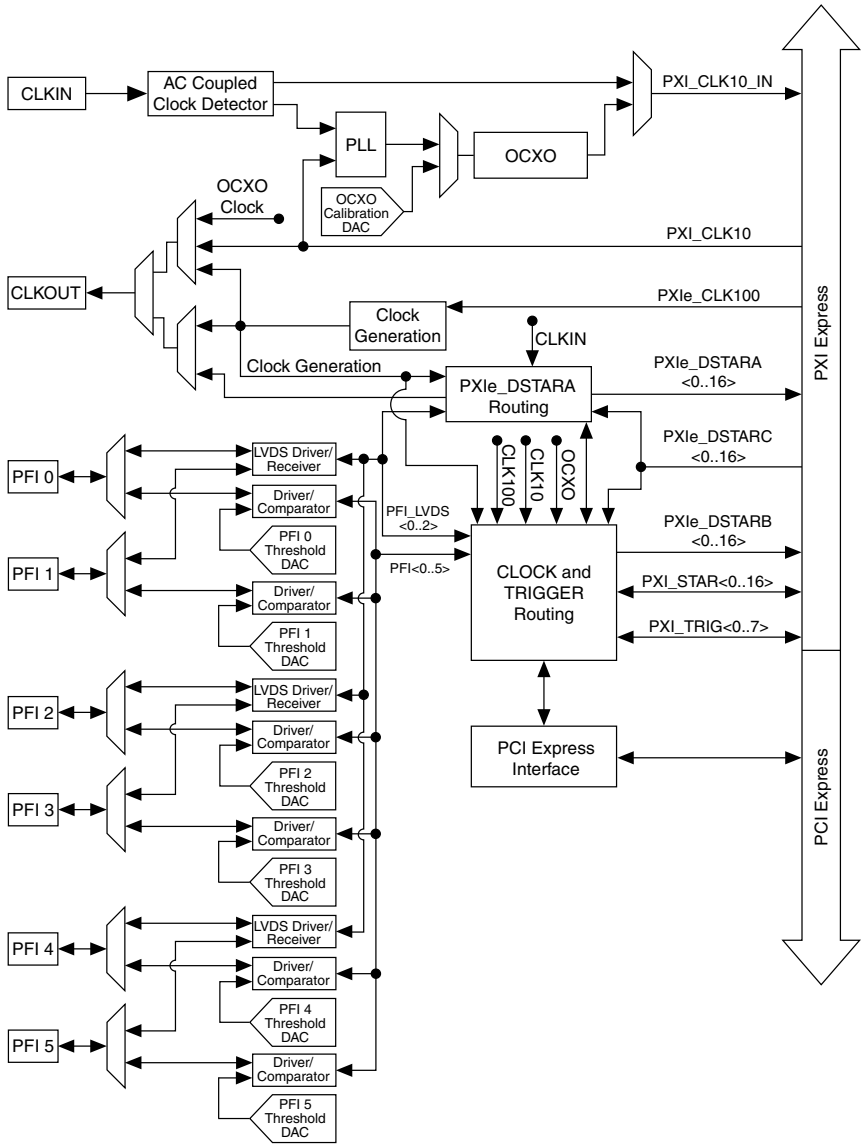
PXIe-6674T Front Panel

Figure 3. PXIe-6674T Front Panel Connectors

1. Access LED
2. Active LED
3. CLKOUT Connector
4. PFI<0..5> Connectors
5. CLKIN Connector

Access LED

The Access LED indicates the communication status of the PXIe-6674T. Refer to *Figure 3.* on page 9 for the location of the Access LED.

Table 1. on page 10 summarizes what the Access LED colors represent:

Table 1. Access LED Color Indications

Color	Status
Off	Module is not yet functional.
Green	Driver has initialized the module.
Amber	Module is being accessed. The Access LED flashes amber for 50 ms when the module is accessed.
Blinking Red	Module has detected an over-temperature condition.
Solid Red	A hardware error has been detected.

⚠ **Caution** If the Access LED is observed to be blinking red, the module has detected an over-temperature condition. Continued use of the PXIe-6674T in this condition is not recommended as product reliability has been compromised. Since several common problems can cause an over-temperature condition, please investigate the following:

- Check that all chassis covers, filler panels, and/or slot blockers are installed.
- Make sure that the chassis fan speed is set to the highest setting.
- If applicable, check that the chassis fan air intake is not blocked and that the fan filters are clean.
- Make sure that the ambient temperature around the chassis isn't above the rated temperature specifications. If so, move the chassis to a cooler ambient temperature location.

⚠ **Caution** If the Access LED is observed to be solid red, a hardware failure has been detected that may impact the performance of the PXIe-6674T. Contact National Instruments for support.

Active LED

The active LED indicates an error or phase-locked loop (PLL) activity. You can change the Active LED to amber, unless an error overrides the selection. Refer to *Figure 3.* on page 9 for the location of the active LED.

💡 **Tip** Changing the Active LED color to amber is helpful when you want to identify devices in a multichassis situation or when you want an indication that your application has reached a predetermined section of the code.

Table 2. on page 11 summarizes what the Active LED colors represent.

Table 2. PXIe-6674T Active LED Status Colors

Active LED Color	Status
Off	The 10 MHz PLL is not in use and no errors are present.
Green	The 10 MHz PLL is active and locked.
Solid Amber	The user can set the Active LED to amber through software.
Solid Red	10 MHz PLL is attempting to lock to the reference supplied on CLKIN.

Connectors

This section describes the connectors on the front panel of the PXIe-6674T.

- CLKIN—AC coupled, 50 Ω clock input. CLK IN can be routed directly to PXI_CLK10_IN, to the 10 MHz PLL, to PXIe_DSTARA, or to the FPGA for use as a synchronization clock.
- CLKOUT—AC couple clock output. CLKOUT can be sourced from the OCXO, PXI-CLK10, Clock Generation, or from the PXIe-DSTARA network.
- PFI<0...5>/PFI)LVDS<0...2>—Programmable Function Interface which can be individually configured for either single ended operation or LVDS operation. In LVDS mode, the connectors are paired and can be programmatically set as either inputs or outputs, but not both simultaneously.

Refer to *Figure 3.* on page 9 for a diagram showing the locations of these connections on the PXIe-6674T front panel.

⚠ **Caution** Connections that exceed any of the maximum ratings of input or output signals on the PXIe-6674T can damage the module and the computer. NI is not liable for any damage resulting from such signal connections.

Hardware Features

The PXIe-6674T performs two broad functions:

- Generating clock and trigger signals.
- Routing internally or externally generated signals from one location to another.

Table 3. on page 12 outlines the function and direction of the signals discussed in detail in the remainder of this chapter:

Table 3. PXIe-6674T Signals

Signal Name	Direction	Description
PXI_CLK10_IN	Out (to chassis)	This is a signal that can be used to provide the backplane with a reference 10 MHZ signal from the system timing slot. When a 10 MHz signal is connected to PXI_CLK10_IN, the PXI Express chassis is required to derive PXI_CLK10 and PXIe_CLK100 from this reference. Refer to the user manual for your PXI Express chassis for more information on how it uses PXI_CLK10_IN.
PXI_CLK10	In (from chassis)	This signal is the PXI 10 MHz backplane clock. This signal is the output of the native 100 MHz oscillator in the chassis divided by ten.
PXIe-CLK100	In (from chassis)	This signal is the PXI Express 100 MHz backplane clock. PXIe_CLK100 offers tighter slot to slot timing than PXI_CLK10.
OCXO Clock	Out (internal)	This is the output of the 10 MHz OCXO. THe OCXO is an extremely stable and accurate frequency source.
CLKIN	In (from front panel)	CLKIN is the signal connected to the SMA input connector of the same name. CLKIN can be routed directly to PXI_CLK10_IN, to the 10 MHz PLL, to PXIe_DSTARA, or to the FPGA.
CLKOUT	Out (to front panel)	CLKOUT is the signal on the SMA output connector of the same name. CLKOUT can be sourced from the OCXO, PXI_CLK10, Clock Generation, or from the PXIe_DSTARA network.
Clock Generation	Out (internal)	Clock Generation refers to the clock signal coming from the onboard clock generation circuitry of the PXIe-6674T. The clock generation circuitry can generate a clock from sub-1 Hz to 1 GHz with fine granularity and is automatically locked in phase to PXIe_CLK100.
PFI<0..5>	In/Out (to/from front panel)	The single ended Programmable Function Interface pins on the PXIe-6674T route timing and triggering signals between multiple PXI Express chassis. A wide variety of input and output signals can be routed to or from the PFI lines.

Table 3. PXIe-6674T Signals (Continued)

Signal Name	Direction	Description
PFI_LVDS<0..2>	In/Out (to/ from front panel)	The LVDS Programmable Function Interface can be used to route timing and triggering signals between multiple PXI Express chassis. The use of LVDS logic allows much faster speeds than can be achieved with the single ended PFIs. When used as outputs, the LVDS PFIs can be sourced from the PXIe_DSTARA network, the FPGA, or the clock generation circuitry. As inputs, the LVDS PFIs can be routed to the PXIe_DSTARA network and to the FPGA.
PXI_TRIG<0..7>	In/Out (to/ from chassis)	The PXI trigger bus consists of eight digital lines shared among all slots in the PXI Express chassis. The PXIe-6674T can route a wide variety of signals to and from these lines. **Note** PXI_TRIG<0..5> are also known as RTSI<0..5> in some hardware devices and APIs. However, PXI_TRIG<6..7> are not identical to RTSI<6..7>.
PXI_STAR<0..16>	In/Out (to/ from chassis)	The PXI star trigger bus connects the system timing slot to other peripheral slots in a star configuration. The electrical paths of each star line are closely matched to minimize intermodule skew. A PXIe-6674T in the system timing slot can route signals to all available PXI_STAR lines in the PXI Express chassis.
PXIe_DSTARA	Out (to chassis)	The PXIe_DSTARA lines connect the system timing module to each peripheral slot in a PXI Express chassis, allowing the system timing module to distribute a clock signal to every slot. PXIe_DSTARA uses differential LVPECL signaling and is capable of high speed clock distribution. Refer to *PXIe_DSTARA Network* on page 17 for more information.

Table 3. PXIe-6674T Signals (Continued)

Signal Name	Direction	Description
PXIe_DSTARB	Out (to chassis)	The PXIe_DSTARB lines connect the system timing module to each peripheral slot in a PXI Express chassis, allowing the system timing module to send out high speed triggers to every slot. PXIe_DSTARB uses differential LVDS signaling and is capable of sending out higher speed trigger signals.
PXIe_DSTARC	In (from chassis)	The PXIe_DSTARC lines connect each peripheral slot in a PXI Express chassis to the system timing module, allowing the system timing module to receive high speed clock and trigger signals from every slot. PXIe_DSTARC uses differential LVDS signaling.

Generating and Routing Clocks

The PXIe-6674T can generate two types of clock signals. The first clock is generated using the onboard clock generation circuitry, and the second is generated with a precise 10 MHz oscillator. The following sections describe the two types of clock generation and explain the considerations for choosing either type.

Clock Generation

The PXIe-6674T includes built-in advanced clock generation circuitry for generating clock signals from below 1 Hz to 1 GHz with very fine frequency resolution. The clock generation circuitry is based on a direct digital synthesis (DDS with an 800 MHz reference phase locked to PXI_CLK100. This allows the DDS to generate a 150 MHz to 300 MHz signal with microhertz resolution. The output from the DDS can then be divided down to lower frequencies, used directly, or multiplied up using a phase locked voltage controlled oscillator.

The individual components which make up the clock generation circuitry are controlled by NI-Sync software, which allows the user to simply specify the frequency they wish the clock generation circuitry to produce. NI-Sync will then configure the clock generation circuitry to give the closest possible frequency match to the requested frequency and do so with the configuration that gives the lower possible phase noise. The user may request a clock frequency of 1 GHz (frequencies beyond 1 GHz are possible, but performance is not specified). The precision of the frequency generated is that of the DDS scaled up or down for any division or multiplacation done to generate the requested frequency, as shown in *Table 4*.

Table 4. Clock Generation Frequency and Resolution

Clock Generation Frequency	Resolution
18.75 MHz to 37.5 MHz	0.355 ΩHz
37.5 MHz to 75 MHz	0.711 ΩHz
75 MHz to 150 MHz	1.42 ΩHz
150 MHz to 300 MHz	2.84 ΩHz
300 MHz to 600 MHz	5.68 ΩHz
600 MHz to 1GHz	11.4 ΩHz

Because the 800 MHz reference of the clock generation circuitry is phase locked to PXIe_CLK100, its frequency accuracy is inherited from PXIe_CLK100. To give the best frequency accuracy, the OCXO of the PXIe-6674T can be routed to PXI_CLK10_IN, which the chassis can then use to lock PXIe_CLK100 and PXI_CLK10. In addition, using the OCXO will also lower the phase noise of the generated clock frequency.

PXI_CLK10 and PXIe_CLK100

The PXI Express architecture allows a module in the system timing slot to provide a 10 MHz reference clock to the backplane for use in creating PXI_CLK10 and PXIe_CLK100. This is done by using the PXI_CLK10_IN pin on the backplane connector.

Most PXI Express backplane architectures employ a PLL to lock a 100 MHz reference oscillator to the signal coming from the PXI_CLK10_IN pin. This 100 MHz reference is then used to directly create PXIe_CLK100 and is divided down by ten to create PXI_CLK10. This architecture has the advantage the PXI_CLK10 and PXIe_CLK100 are always sourced from the same reference oscillator, and therefore it is impossible to lose PXI_CLK10 or PXIe_CLK100 by disconnecting the reference provided on PXI_CLK10_IN. For the same reason, it is also impossible for a runt pulse or glitch to occur on these lines as references are switched in and out, protecting the integrity of digital circuitry operating on these clocks. Another feature of this architecture is that the phase noise performance of PXI_CLK10 and PXIe_CLK100 is fixed beyond the bandwidth of the PLL loop of the backplane, regardless of the quality of the reference used. This is advantageous if a reference with poor phase noise performance is used, but it also means that supplying a high end low phase noise reference will not greatly improve PXI_CLK10 or PXIe_CLK100.

Using PXI_CLK10_IN

The PXIe-6674T provides three options for driving a clock to the backplane using PXI_CLK10_IN: OCXO, CLKIN, and 10 MHz PLL.

OCXO

The PXIe-6674T features a precision 10 MHz Oven Controlled Crystal Oscillator (OCXO). The main source of frequency error in reference oscillators is temperature variation. An OCXO minimizes this error by housing the crystal oscillator circuit inside a sealed oven, which is maintained at a constant temperature higher than the ambient temperature external to

the OCXO. This results in a reference oscillator that is several orders of magnitude more stable and accurate than regular crystal oscillators.

Because the OCXO must warm up to a higher temperature than the ambient temperature around it, there is a warm up time required to achieve the specified frequency accuracy. For this reason, to achieve the most stable operation of the OCXO it is desirable to avoid powering off the OCXO.

The OCXO used by the PXIe-6674T features electronic frequency control. This allows the OCXO to be fine-tuned by varying the control voltage to the OCXO. The PXIe-6674T uses a 16-bit digital analog converter to give precise control of the tuning voltage. While the tuning voltage can be varied by the user, it is normally controlled automatically by software, which sets it to the calibration tuning voltage. The PXIe-6674T is calibrated during the manufacturing process and should be recalibrated annually to remove frequency error that accumulates over time (such as crystal aging). Refer to the PXIe-6674T Calibration Procedure at `ni.com/calibration` for more details.

The OCXO can also be routed to the CLKOUT SMA and be used as a trigger synchronization clock inside the FPGA.

CLKIN

The PXIe-6674T allows the user to connect their own 10 MHz reference directly to PXI_CLK10_IN by using the CLKIN SMA on the front panel. CLKIN is an AC coupled, 50 Ω terminated input to the PXIe-6674T. In order to increase the amplitude of signals the CLKIN receiver can use, the CLKIN circuitry features software enabled attenuation, which will attenuate the input signal by a factor of five when enabled. NI-Sync software will by default configure the attenuation to be enabled. If the input signal supplied to CLKIN is less than 1.2 V_{pp}, the attenuation should be turned off in order to extend down the range of amplitudes CLKIN can receive.

When using CLKIN for driving PXI_CLK10_IN, please refer to the user manual for your PXI Express chassis for information on the frequency range your chassis is capable of receiving on PXI_CLK10_IN.

CLKIN can also be routed to the DSTARA network and be used as a trigger synchronization clock inside the FPGA.

10 MHz PLL

The PXIe-6674T features a phase locked loop (PLL) circuit for aligning the frequency of the OCXO with a reference clock supplied by the user from CLKIN. In this configuration, the OCXO is routed to the backplane on PXI_CLK10_IN. The PXI Express backplane will in turn phase lock the PXI_CLK10 and PXIe_CLK10 signal to the PXI_CLK10_IN signal. The PXIe-6674T uses the PXI_CLK10 signal it receives from the backplane as feedback to the 10 MHz PLL circuitry. The PLL circuitry controls the frequency of the OCXO by varying the tuning voltage used for electronic frequency control. By increasing or decreasing the

frequency of the OCXO as needed, the 10 MHz PLL of the PXIe-6674T is able to match the OCXO frequency to the reference clock supplied by the user from CLKIN.

Use of the 10 MHz PLL of the PXIe-6674T has advantages over using just CLKIN to drive PXI_CLK10_IN:

- Reference frequencies other than 10 MHz can be used. The 10 MHz PLL includes internal dividers to divide both the reference from CLKIN and PXI_CLK10 down as needed in order to make both a common frequency. This frequency is called the phase detector frequency, as it is the frequency at which the PLL compares edge alignment to determine if it should speed up or slow down the OCXO. NI-Sync allows any reference frequency that is an integer multiple of 1 MHz to be used.

- The 10 MHz PLL acts as a zero-delay buffer between the CLKIN SMA and PXI_CLK10/PXIe_CLK100 at the backplane connector. Because the 10 MHz PLL uses PXI_CLK10 for feedback, it is able to create a known fixed phase relation between PXI_CLK10 and the reference supplied on CLKIN. During manufacturing, the phase relation the 10 MHz PLL maintains is adjusted so that a rising edge at the CLKIN SMA will align in time with a rising edge of PXI_CLK10 at the peripheral slot connector of the backplane. This phase relation will remain in place regardless of the PXI Express chassis used, allowing for simpler multi-chassis system synchronization.

PXIe_DSTARA, PXIe_DSTARB, and PXIe_DSTARC

The PXI Express architecture includes a set of three high speed differential signal paths to connect the system timing slot to each PXI Express peripheral slot (up to 17 peripheral slots). These signals are PXIe_DSTARA, PXIe_DSTARB, and PXIe_DSTARC.

- PXIe_DSTARA—PXIe_DSTARA is used to send clock signals from the system timing slot to each PXI Express peripheral slot in a star configuration. PXIe_DSTARA uses LVPECL signaling and closely matched trace lengths to achieve low skew, high speed clock routing capabilities. Refer to *PXIe_DSTARA Network* on page 17 for details on how the PXIe-6674T implements PXIe_DSTARA.

- PXIe_DSTARB—PXIe_DSTARB is used to send trigger signals from the system timing slot to each PXI Express peripheral slot in a star configuration. PXIe_DSTARB uses LVDS signaling and closely matched trace lengths to achieve faster, more precise triggering than is achievable with PXI_STAR or PXI_TRIG.

- PXIe_DSTARC—PXIe_DSTARC is used to send trigger signals from each PXI Express peripheral slot to the system timing slot in a star configuration. PXIe_DSTARC uses LVDS signaling and closely matched trace lengths and can be used to send a trigger signal or clock signal to the system timing slot module. The PXIe-6674T receives each PXIe_DSTARC signal and sends a copy to the PXIe_DSTARA network for clock sharing and to the FPGA for trigger routing.

PXIe_DSTARA Network

To achieve the high speed, low skew routing performance required for PXIe_DSTARA, the PXIe-6674T uses circuitry specifically designed for routing clock signals to PXIe_DSTARA<0..16>. NI-Sync software automatically handles the routing through the PXIe_DSTARA network. However because the PXIe_DSTARA Network limits the number of

connections that can be made, it is important to understand the underlying hardware architecture. *Figure 4.* on page 18 provides an overview of the PXIe_DSTARA network:

Figure 4. PXIe_DSTARA Network
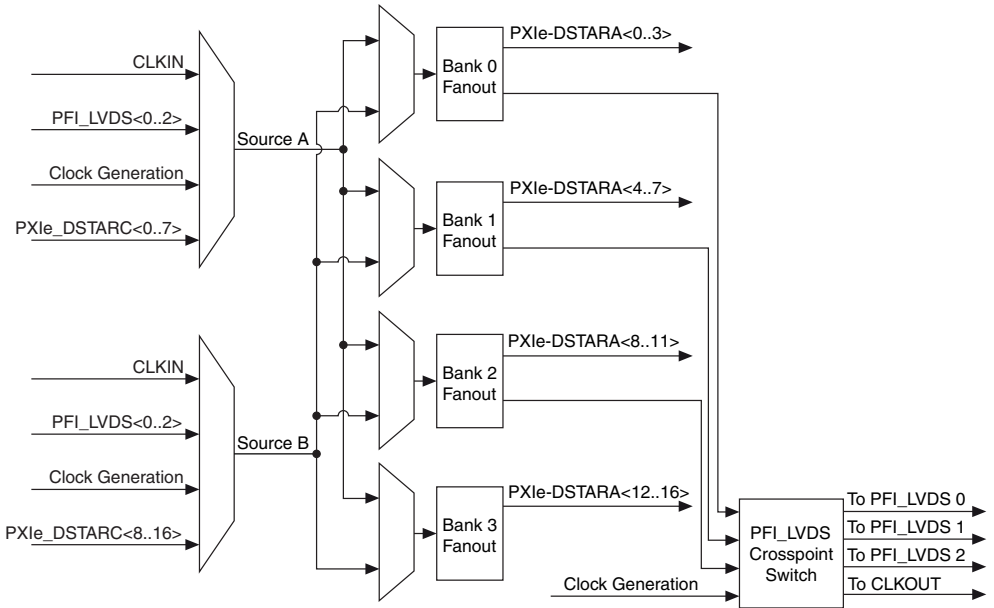
To drive signals out on the PXIe_DSTARA lines, the PXIe_DSTARA network divides the 17 PXIe_DSTARA lines into four banks, as shown in *Table 5.* on page 18:

Table 5. PXIe_DSTARA Divisions

Bank 0	Bank 1	Bank 2	Bank 3
PXIe_DSTARA<0..3>	PXIe_DSTARA<4..7>	PXIe_DSTARA<8.11>	PXIe_DSTARA<12..16>
PFI_LVDS cross point	PFI_LVDS cross point	PFI_LVDS cross point	—

Each one of the Banks can select from either Source A or Source B and all the PXIe_DSTARA lines that a Bank drives out must share the same source. Banks 0, 1, and 2 send a copy of their output to the PFI_LVDS cross point switch for routing out the front panel using PFI lines in LVDS mode. Refer to the *PFI_LVDS<0..2>* section for more information.

📝 **Note** Only clock signals should be routed through the PXIe_DSTARA lines. PXIe_DSTARA lines may exhibit unexpected behavior when routing conventional triggers.

> **Note** Because a single integrated circuit is used to make the five outputs in each bank, tighter skew is achieved within a single Bank than from Bank to Bank.

PFI_LVDS<0..2>

To allow for sending and receiving signals between system timing modules that are too fast for single ended PFI signaling, two PFI SMA connectors can be combined to send or receive LVDS signals. *Table 6.* on page 19 shows the relation between the front panel SMA connectors used for PFI and PFI_LVDS.

Table 6. Combinations of PFI Lines for PFI_LVDS

PFI Line	PFI_LVDS Line
PFI 0	PFI_LVDS 0 Negative
PFI 1	PFI_LVDS 0 Positive
PFI 2	PFI_LVDS 1 Negative
PFI 3	PFI_LVDS 1 Positive
PFI 4	PFI_LVDS 2 Negative
PFI 5	PFI_LVDS 2 Positive

Each of the three PFI_LVDS can be enabled for LVDS operation or used for two single ended PFIs. When enabled for LVDS operation, the PFI_LVDS pair can be configured as either an input or an output. PFI_LVDS lines can not be used as an input and output at the same time.

Because of the increased speed capabilities, the PFI_LVDS includes additional routing capabilities not offered with the single ended PFI. When used as an input, the PFI_LVDS signal goes to both the FPGA for trigger routing and to the PXIe_DSTARA Network for use in routing high speed clocks. When used as an output, the PFI_LVDS can be sourced from the FPGA for trigger usage, or from a 4x4 cross point switch which allows for any of the four inputs to be connected to any of the four outputs. *Table 7.* on page 19 shows the inputs and outputs of the cross point switch.

Table 7. PFI_LVDS Inputs and Outputs

Inputs	Outputs
PXIe_DSTARA Network Bank 0	PFI_LVDS 0
PXIe_DSTARA Network Bank 1	PFI_LVDS 1
PXIe_DSTARA Network Bank 2	PFI_LVDS 2
Clock Generation	High Speed CLKOUT

If the PFI_LVDS output is used for trigger routing, it is sourced from the FPGA and has all the same trigger routing characteristics as other trigger destinations. Refer to the *Using Front Panel PFIs for LVDS Triggers* section for details on using PFI_LVDS for sending and receiving trigger signals.

CLKOUT

The CLKOUT SMA connector on the front panel provides a means to export a clock signal from the PXIe-6674T to an external device or another system timing module. The CLKOUT driver uses two separate circuits for driving CLKOUT, one for low speed frequencies (50 MHz and below) and one for high speed (above 50 MHz). The low speed driver uses 5 V CMOS logic with source impedance of 50 Ω and is AC coupled. The high speed driver produces an 800 mV$_{pp}$ swing into a 50 Ω load and is also AC coupled.

The sources available to be routed to CLKOUT differ depending on whether the low speed or high speed driver is used. The sources available to the low speed driver are PXI_CLK10, OCXO, and Clock Generation for generated frequencies 100 MHz and below. Sources available to the high speed CLKOUT are Clock Generation and outputs from the PXIe_DSTARA network through the PFI_LVDS cross point switch.

NI-Sync software will select the low speed or high speed driver automatically based on the source connected to CLKOUT.

Routing Signals

The PXIe-6674T has versatile trigger routing capabilities. It can route signals to and from the front panel, the PXI star triggers, PXIe_DSTARB, and PXIe_DSTARC.

Figure 5. on page 21 and *Figure 6.* on page 22 summarize the routing features of the PXIe-6674T. The remainder of this chapter details the capabilities and constraints of the routing architecture.

**Figure 5.** High-Level Schematic of PXIe-6674T Signal Routing Architecture

*PXI_STAR<0..16>, PXI_TRIG<0..7>, PFI<0..5>, PFI_LVDS<0..2>, PXIe_DSTARC<0..16>, Steady Logic, and Software Trigger are routed to SOURCE of each Selection Circuitry block.
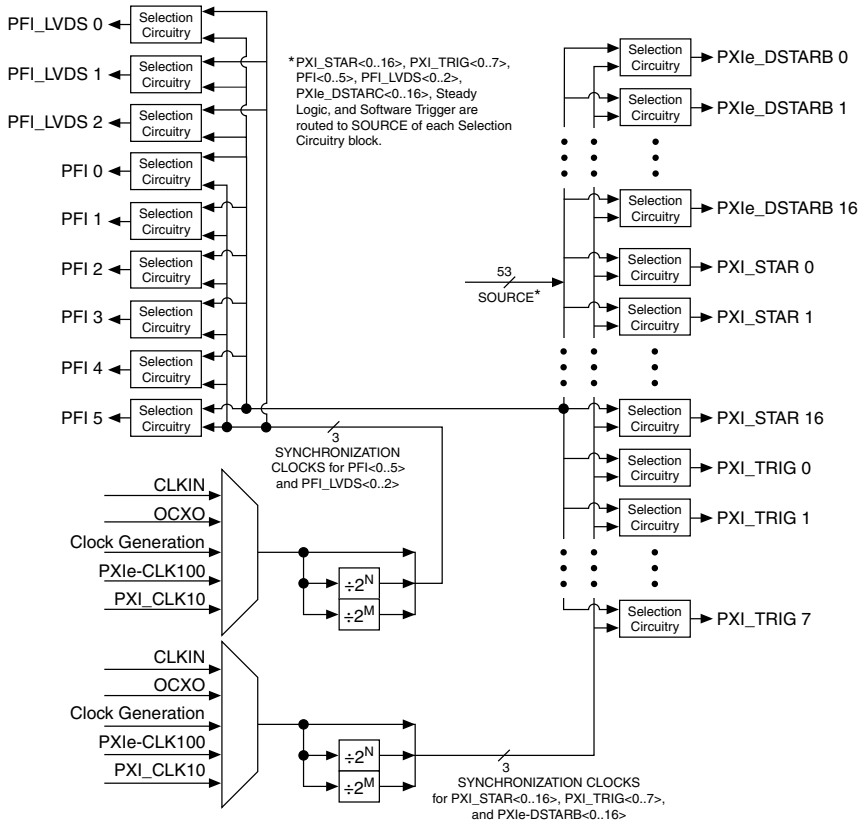
Figure 6. on page 22 provides a more detailed view of the Selection Circuitry referenced in _Figure 5_.

Figure 6. PXIe-6674T Signal Selection Circuitry Diagram
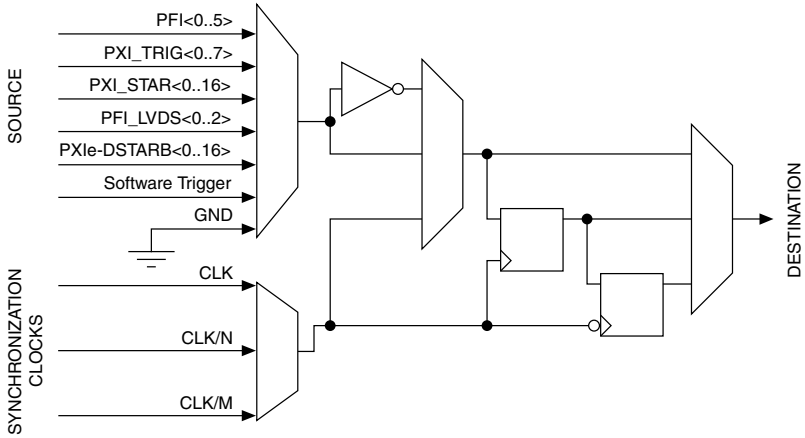
Determining Sources and Destinations

All signal routing operations can be characterized by a *source* (input) and a *destination*. In addition, synchronous routing operations must also define a third signal known as the *synchronization clock*. Refer to the *Choosing the Type of Routing* section for more information on synchronous versus asynchronous routing.

Figure 7. on page 23 summarizes the sources and destinations of the PXIe-6674T. The destinations are listed in the horizontal heading row, and the sources are listed in the column at the far left. A check in a cell indicates that the source and destination combination defined by that cell is a valid routing combination.

			Destinations								
			Front Panel			Backplane					Onboard
			CLK OUT	PFI <0..5>	PFI LVDS <0..2>	PXI CLK 10 IN	PXI Star Trigger <0..16>	PXI TRIG <0..7>	DSTARA <0..16>	DSTARB <0..16>	OCXO Ref PLL
Sources	Front Panel	CLK IN	✓	✓†	✓†	✓	✓†	✓†	✓	✓†	✓
		PFI<0..5>		✓	✓		✓	✓		✓	
		PFI LVDS <0..2>		✓	✓		✓	✓	✓	✓	
	Backplane	PXI CLK 10	✓	✓†	✓†		✓†	✓†		✓†	
		PXI CLK 100	✓	✓†	✓†		✓†	✓†		✓†	
		PXI STAR <0..16>		✓	✓		✓	✓		✓	
		PXI TRIG <0..7>		✓	✓		✓	✓		✓	
		DSTARC <0..16>		✓	✓		✓	✓	✓	✓	
	Onboard	OCXO	✓	✓†	✓†	✓	✓†	✓†		✓†	
		Clock Gen	✓	✓†	✓		✓†	✓†	✓	✓†	
		Global Software Trigger		✓	✓		✓	✓		✓	

† Routing PXI_CLK10, PXIe_CLK100, OCXO or ClkGen is accomplished by setting the synchronization clock (using the NI-Sync Property Node) to the desired clock source and then routing the synchronization clock as the source.

(dark)	Route through the FPGA.
(light)	Route to PFI LVDS can be made through the FPGA when used as a trigger, or through the PXIe-DSTARA network when used as a clock.

Using Front Panel PFIs as Single Ended Inputs

The front-panel PFIs can receive external signals from 0 to +5 V. They can be terminated programmatically with 50 Ω resistances to match the cable impedance and minimize reflections.

Note Terminating the signals with a 50 Ω resistance is recommended when the source is another PXIe-6674T or any other source with a 50 Ω output.

The voltage thresholds for the front-panel PFI inputs are programmable. The input signal is generated by comparing the input voltage on the PFI connectors to the voltage output of software-programmable DACs. The thresholds for the PFI lines are individually programmable, which is useful if you are importing signals from multiple sources with different voltage swings.

Using Front Panel PFIs as Single Ended Outputs

The front panel PFI outputs are +3.3 V drivers with 50 Ω output impedance. The outputs can drive 50 Ω loads, such as a 50 Ω coaxial cable with a 50 Ω receiver. This cable configuration is the recommended setup to minimize reflections. With this configuration, the receiver sees a

single +1.6 V step—a +3.3 V step split across the 50 Ω resistors at the source and the destination.

You also can drive a 50 Ω cable with a high-impedance load. The destination sees a single step to +3.3 V, but the source sees a reflection. This cable configuration is acceptable for low-frequency signals or short cables.

You can independently select the output signal source for each PFI line from one of the following sources.

- Another PFI<0..5>
- Another PFI pair in LVDS mode.
- PXI triggers <0..7> (PXI_TRIG<0..7>
- PXI_STAR<0..16>
- Global software trigger
- PFI synchronization clock
- PXIe_DSTARC
- Steady logic high or low.

The PXI synchronization clock may be any of the following signals:

- Clock Generation
- PXI_CLK10
- PXIe_CLK100
- OCXO
- CLKIN
- Any of the previously listed signals divided by the first frequency divider (2^n, up to 512)
- Any of the previously listed signals divided by the second frequency divider(2^m, up to 512)

Refer to *Choosing the Type of Routing* section for more information on the sychronization clock.

> **Note** The PFI synchronization clock is the same for all routing operations in which PFI<0..5> or PFI_LVDS<0..2> is defined as the output, although the divide-down ratio for this clock (full rate, first divider, second divider) may be chosen on a per-route basis.

Using Front Panel PFIs for LVDS Triggers

To allow for sending and receiving signals between system timing modules that are too fast for single ended PFI signaling, two PFI SMA connectors can be combined to send or receive LVDS signals. *Table 6.* on page 19 shows the relation between the front panel SMA connectors used for PFI and PFI_LVDS.

When used for trigger routing, the PFI_LVDS signals are routed to and from the FPGA. You can independently select the output signal source for each PFI_LVDS line from one of the following sources:

- Another PFI<0..5>
- Another PFI pair in LVDS mode.
- PXI triggers <0..7> (PXI_TRIG<0..7>)

- PXI_STAR<0..16>
- Global software trigger
- PFI synchronization clock
- PXIe_DSTARC
- Steady logic high or low.

The PFI synchronization clock is also used for the PFI_LVDS and as such may be one of the following signals:
- Clock Generation
- PXI_CLK10
- PXIe_CLK100
- OCXO
- CLKIN
- Any of the previously listed signals divided by the first frequency divider (2^n, up to 512)
- Any of the previously listed signals divided by the second frequency divider (2^m, up to 512)

Refer to the *Choosing the Type of Routing* section for more information on the synchronization clock.

> **Note** The PFI synchronization clock is the same for all routing operations in which PFI<0..5> or PFI_LVDS<0..2> is defined as the output, although the divide-down ratio for this clock (full rate, first divider, second divider) may be chosen on a per route basis.

Using the PXI Triggers

The PXI triggers go to all the slots in the chassis. All modules receive the same PXI triggers, so PXI trigger 0 is the same for the system timing slot as it is for Slot 3, and so on. This feature makes the PXI triggers convenient in situations where you want, for instance, to start an acquisition on several devices at the same time because all modules will receive the same trigger.

The frequency on the PXI triggers should not exceed 5 MHz to preserve signal integrity. The signals do not reach each slot at precisely the same time. A difference of several nanoseconds between slots can occur in an eight-slot chassis. However, this delay is not a problem for many applications.

You can independently select the output signal source for each PXI trigger line from one of the following sources.
- PFI<0..5>
- PFI_LVDS<0..2>
- Another PXI trigger <0..7> (PXI_TRIG<0..7>)
- PXI_STAR<0..16>
- Global software trigger
- Backplane synchronization clock
- PXIe_DSTARC
- Steady logic high or low

The backplane synchronization clock may be any of the following signals.

- Clock Generation
- PXI_CLK10
- PXIe_CLK100
- OCXO
- CLKIN
- Any of the previously listed signals divided by the first frequency divider (2^n, up to 512).
- Any of the previously listed signals divided by the second frequency divider (2^m, up to 512).

Refer to the *Choosing the Type of Routing* section for more information about the synchronization clock.

> **Note** The backplane synchronization clock is the same for all routing operations in which PXI_TRIG<0..7>, PXIe_DSTARB<0..16>, or PXI_STAR<0..16> is defined as the output, although the divide-down ratio for this clock (full rate, first divider, second divider) may be chosen on a per route basis.

Using the PXI Star Triggers

There are up to 17 PXI star triggers per chassis. Each trigger line is a dedicated connection between the system timing slot and one other slot. The *PXI Specification, Revision 2.1*, requires that the propagation delay along each star trigger line be matched to within 1 ns. A typical upper limit for the skew in most NI PXI Express chassis is 500 ps. The low skew of the PXI star trigger bus is useful for applications that require triggers to arrive at several modules nearly simultaneously.

The star trigger lines are bidirectional, so signals can be sent to the system timing slot from a module in another slot or from the system timing slot to the other module.

You can independently select the output signal source for each PXI star trigger line from one of the following sources:

- PFI<0..5>
- PFI_LVDS<0..2>
- PXI triggers <0..7> (PXI_TRIG<0..7>)
- Another PXI star trigger line (PXI_STAR<0..16>)
- Global software trigger
- Backplane synchronization clock
- PXIe_DSTARC
- Steady logic high or low

Refer to the *Using the PXI Triggers* section for more information on the backplane synchronization clock.

Using the PXIe_DSTARB and PXIe_DSTARC Triggers

To improve beyond the performance the PXI Star triggers offer in low skew trigger routing, PXI Express implements PXIe_DSTARB and PXIe_DSTARC triggers. Each PXI Express peripheral slot in a PXI Express chassis has independent PXIe_DSTARB and PXIe_DSTARC

connections with the system timing slot module. This allows peripheral modules to send triggers to the system timing module using PXIe_DSTARC and for the system timing module to send triggers to peripheral modules using PXIe_DSTARB. Both PXIe_DSTARB and PXIe_DSTARC are one directional. The PXI Express Specification requires PXI Express chassis to limit the skew between any two PXIe_DSTAR routes to 150 ps.

The PXIe-6674T receives PXIe_DSTARC and can route it to both the PXIe_DSTARA network for use as a clock source and to the FPGA for use as a trigger source. The PXIe-6674T can independently select from the following sources to be routed to PXIe_DSTARB:

- PFI<0..5>
- PFI_LVDS<0..2>
- PXI Triggers<0..7> (PXI_TRIG<0..7>)
- PXI Star Triggers (PXI_STAR<0..16>)
- PXIe_DSTARC<0..16>
- Global Software Trigger
- Steady logic high or low
- Backplane synchronization clock

Refer to the *Using the PXI Triggers* section for more information on the backplane synchronization clock.

Choosing the Type of Routing

The PXIe-6674T routes signals in one of two ways: asynchronously or synchronously. The following sections describe the two routing types and the considerations for choosing each type.

Asynchronous Routing

Asynchronous routing is the most straightforward method of routing signals. Any asynchronous route can be defined in terms of two signals: a *source* and a *destination*. A digital pulse or train comes in on the source and is propagated to the destination. When the source signal goes from low to high, this rising edge is transferred to the destination after a propagation delay through the module. *Figure 8.* on page 27 illustrates an asynchronous routing operation.

Figure 8. Asynchronous Routing Operation
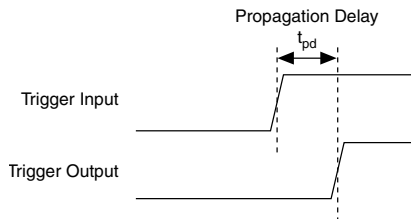
Some delay is always associated with an asynchronous route, and this delay varies among PXIe-6674T modules, depending on variations in temperature and chassis voltage. Typical delay times in the PXIe-6674T for asynchronous routes between various sources and destinations are given in the device's Specifications.

Asynchronous routing works well if the total system delays are not too long for the application. Propagation delay could be caused by the following reasons:

• Output delay on the source.
• Propagation delay of the signal across the backplane(s) and cable(s).
• Propagation delay of the signal through the PXIe-6674T.
• Time for the receiver to recognize the signal.

Both the source and the destination of an asynchronous routing operation on the PXIe-6674T can be any of the following lines:

• Any front panel PFI pin (PFI<0..5>) as single ended.
• Any front panel PFI pin as LVDS (PFI_LVDS<0..2>)
• Any PXI star trigger line (PXI_STAR<0..16>)
• Any PXI trigger line (PXI_TRIG<0..7>)
• Any PXIe_DSTARB<0..16>

Synchronous Routing

A synchronous routing operation is defined in terms of three signals: a *source*, a *destination*, and a *synchronization clock*. Unlike asynchronous routing, the output of a synchronous routing operation does not directly follow the input after a propagation delay. Instead, the logic state of the input is sampled on each active edge of the synchronization clock, and the output is set to that logic state after a small delay, as shown in the following figure. Thus, the output is said to be *synchronous* with this clock.

Figure 9. on page 29 shows a timing diagram that illustrates synchronous routing.

Figure 9. Synchronous Routing Operation
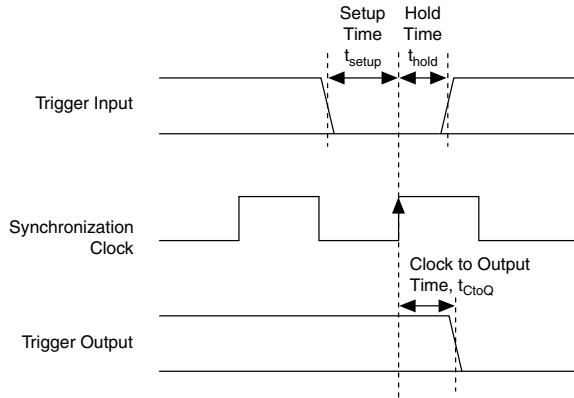
The PXIe-6674T board supports synchronous routing to either the rising or falling edge of the synchronization clock. In addition, the polarity of the destination signal can be inverted, which is useful when handling active-low digital signals. Synchronous routing can be useful for eliminating skew when sending triggers to several destinations. For example, when sending triggers using the PXI Trigger lines, the trigger arrives at each slot at a slightly different time. However, if the trigger is sent and received synchronously using a low-skew synchronization clock (for example, PXI_CLK10), all receiving devices can act on the trigger at the same time, as shown in :

Figure 10. Synchronous Routing to Multiple Destinations
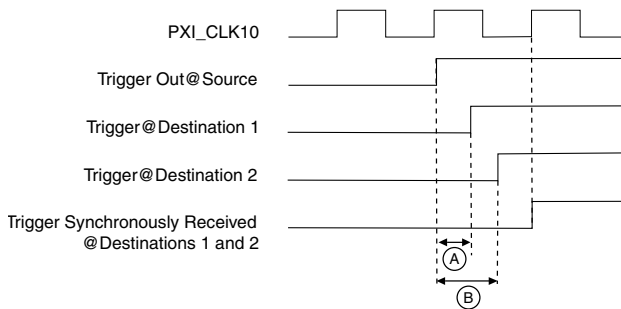
A: Propagation delay from source to destination 1.

B: Propagation delay from source to destination 2.

Synchronous routing requires the input to be stable at a logic low or logic high state within a window of time around the clock edge. This window of time around the clock edge is defined by the setup time (t_{setup}) and hold time (t_{hold}). If the input signal changes within this window of time, it is undetermined whether the output of the synchronous route will go to the old or new logic state. This is important, for example, if a source is being routed synchronously to several

destinations. If the source signal changes within the setup-and-hold window around the synchronization clock edge, one of the destinations might go to the new logic level while the other destination might remain at the old logic level and change when the next synchronization clock edge occurs, as shown in

Figure 11. Synchronous Routing Uncertainty with Setup-and-Hold Variation
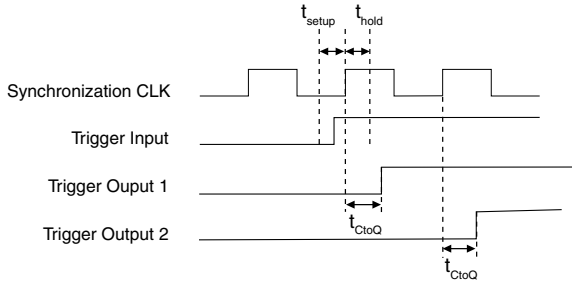
Therefore, if your application requires that the trigger arrive at the multiple destinations simultaneously, you must ensure that the input is stable within the setup and hold window around the synchronization clock edge. For more information and possible methods to ensure this requirement is met, go to `ni.com/info` and enter the Info Code `SyncTriggerRouting`.

Possible sources for synchronous routing with the PXIe-6674T include the following sources:

- Any front panel PFI pin as single ended.
- Any front panel PFI pin as LVDS.
- Any PXI star trigger line (PXI_STAR<0..16>)
- Any PXI trigger line (PXI_TRIG<0..7>)
- Any PXIe_DSTARC<0..16>
- Global software trigger
- The synchronization clock itself.

The synchronization clock for a synchronous route can be any of the following signals:

- 10 MHz PXI_CLK10
- 100 MHz PXIe_CLK100
- Clock Generation
- OCXO
- CLKIN
- One of two "divided copies" of any of the previously listed five signals. The PXIe-6674T includes two clock-divider circuits that can divide the synchronization clock signals by any power of 2 up to 512.

Refer to for an illustration of how the PXIe-6674T performs synchronous routing operations.

Calibration

This chapter discusses the calibration of the PXIe-6674T.

Calibration consists of verifying the measurement accuracy of a device and correcting for any measurement error. The PXIe-6674T is factory calibrated before shipment at approximately 25 °C to the levels indicated in the PXIe-6674T Specifications. The associated calibration constants—the corrections that were needed to meet specifications—are stored in the onboard nonvolatile memory (EEPROM). The driver software uses these stored values.

Factory Calibration

The factory calibration of the PXIe-6674T involves calculating and storing four calibration constants. These values control the accuracy of two features of the device, which are discussed in the following sections.

OCXO Frequency

The OCXO frequency can be varied over a small range. The output frequency of the OCXO is adjusted using this constant to meet the specification listed in the PXIe-6674T Specifications.

PXI_CLK10 Phase

When using the PLL to lock PXI_CLK10 to an external reference clock, the phase between the clocks can be adjusted. The time between rising edges of PXI_CLK10 and the input clock is minimized using this constant.

> **Note** The PXI_CLK10 phase is set during manufacturing and does not need to be recalibrated.

Additional Information

Refer to `ni.com/calibration` for additional information on NI calibration services.

Compliance

Electromagnetic Compatibility Information

This hardware has been tested and found to comply with the applicable regulatory requirements and limits for electromagnetic compatibility (EMC) as indicated in the hardware's Declaration of Conformity (DoC)[4]. These requirements and limits are designed to provide reasonable protection against harmful interference when the hardware is operated in the intended electromagnetic environment. In special cases, for example when either highly

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[4] The Declaration of Conformity (DoC) contains important EMC compliance information an dinstructions for the user or installer. To obtain the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

sensitive or noisy hardware is being used in close proximity, additional mitigation measures may have to be employed to minimize the potential for electromagnetic interference.

⚠ **Caution** To ensure the specified EMC performance, operate this product only with double-shielded cables and accessories (for example, RG-223 cables).

While this hardware is compliant with the applicable regulatory EMC requirements, there is no guarantee that interference will not occur in a particular installation. To minimize the potential for the hardware to cause interference to radio and television reception or to experience unacceptable performance degradation, install and use this hardware in strict accordance with the instructions in the hardware documentation and the DoC[4].

If this hardware does cause interference with licensed radio communications services or other nearby electronics, which can be determined by turning the hardware off and on, you are encouraged to try to correct the interference by one or more of the following measures:

- Reorient the antenna of the receiver (the device suffering interference).
- Relocate the transmitter (the device generating interference) with respect to the receiver.
- Plug the transmitter into a different outlet so that the transmitter and the receiver are on different branch circuits.

Some hardware may require the use of a metal, shielded enclosure (windowless version) to meet the EMC requirements for special EMC environments, such as for marine use or in heavy industrial areas. Refer to the hardware's user documentation and the DoC[4] for product installation requirements.

When the hardware is connected to a test object or to test leads, the system may become more sensitive to disturbances or may cause interference in the local electromagnetic environment.

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