SC Express

PXIe-4309 User Manual

32 Ch (8 ADC), 2 MS/s, 18 - 28 bit, Flexible Resolution PXI Analog Input Module

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1 Getting Started

The PXIe-4309 is a flexible resolution voltage input module that supports up to 32 channels. The module multiplexes its analog input channels across eight simultaneously sampling ADCs.

The PXIe-4309 can sample eight input channels up to 2 MS/s/ch (single channel per ADC), and 32 input channels up to 400 kS/s aggregate (up to 4 channels per ADC).

Installation

Refer to the *PXIe-4309 and TB-4309 (ST)/TB-4309 (MT) Getting Started Guide and Terminal Block Specifications* document for step-by-step installation instructions, accessory details, and a complete listing of supported accessories.

Note For a complete list of terminal blocks supported by a specific release of NI-DAQmx, refer to the *NI-DAQmx Readme*, available on the version-specific download page or installation media.

Module Specifications

Refer to the *PXIe-4309 Specifications* document for module specifications.

2

Using the PXIe-4309

This chapter describes how to connect voltage signals to the PXIe-4309. It also provides the I/O connector pin assignments of the module.

Driver support for the PXIe-4309 was first available in NI-DAQmx 17.1. For the list of devices supported by a specific release, refer to the *NI-DAQmx Readme*, available on the version-specific download page or installation media.

Connecting Signals

This section provides information regarding the connection of voltage signals.

Caution To ensure the specified EMC performance, operate this product only with shielded, twisted pair cables, and shielded accessories.

Caution To ensure the specified EMC performance, the length of all I/O cables must be no longer than 3 m (10 ft.).

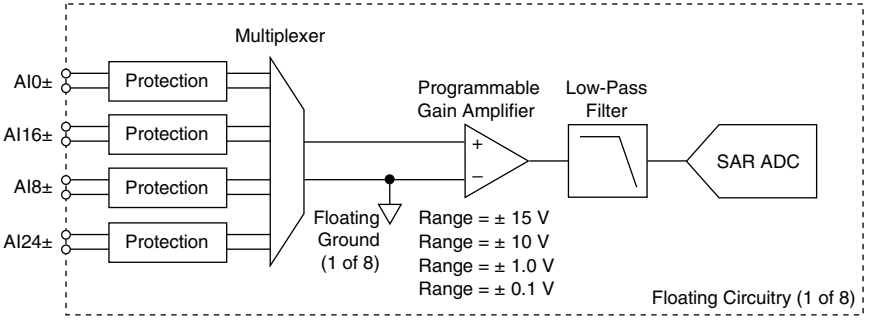
Caution This icon denotes a caution, which advises you of precautions to take to avoid injury, loss of data, or a system crash.

Connecting Voltage Signals

Note The TB-4309 (ST) or TB-4309 (MT) terminal block is available for measuring voltage signals.

Analog Input Circuitry

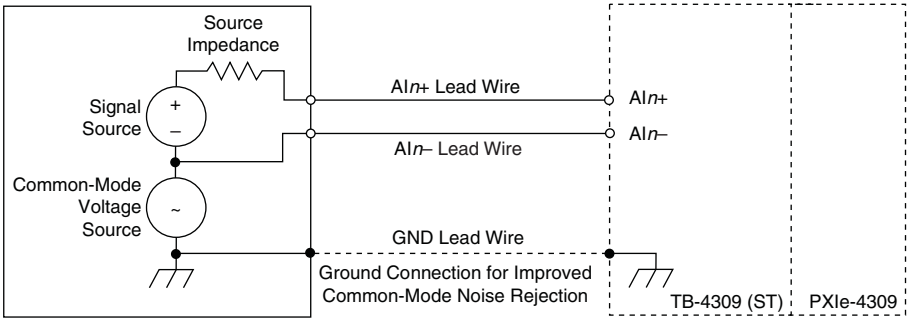
Figure 2-1. Analog Input Circuitry



Input signals on each channel are conditioned, buffered, and then sampled by a SAR ADC.

The PXIe-4309 has eight independent signal conditioning paths and ADCs, enabling simultaneous sampling of up to eight input channels. Each ADC can scan through four independent input channels for a total of 32 input channels.

Figure 2-2. Signal Source with Common-Mode Connected to an Analog Input Channel



Source Impedance

Best measurement performance is achieved with source impedance of 50 Ω or lower; refer to the *Source Impedance Error* section of the *PXIe-4309 Specifications* for information on the error introduced by source impedances greater than 50 Ω.

Common-Mode Rejection Ratio (CMRR)

The analog input circuitry is floating to provide best in class CMRR of DC common-mode voltages.

Floating analog input circuits have an inherent input impedance mismatch. To minimize the effect of this mismatch on CMRR of AC common-mode voltages, keep the DC resistance and AC impedance of the AI*n*- lead wire to a minimum.

Common-Mode Noise

Floating power supplies inject common-mode current onto its floating ground. To minimize the effect of this current on measurement noise, keep the DC resistance and AC impedance of the AI*n*- lead wire to a minimum.

Shielding

For best noise immunity use double-shielded twisted pair cabling.

Figure 2-3. Recommended Wiring for a Floating Source

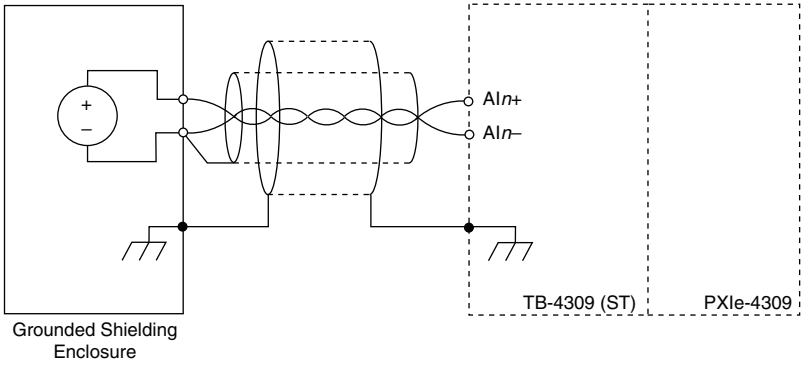


Figure 2-4. Recommended Wiring for a Grounded Source with Common-Mode

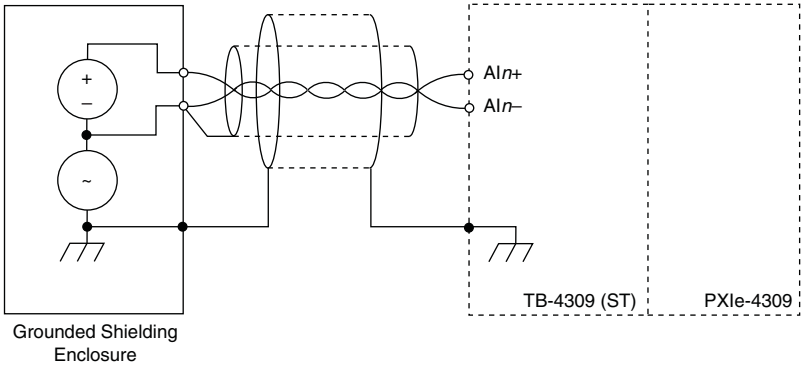
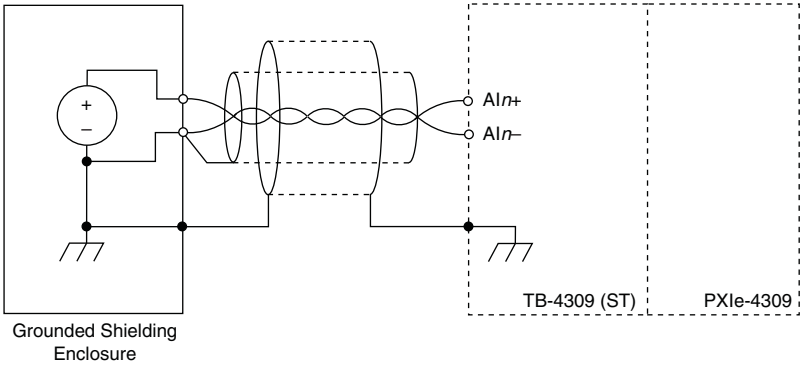


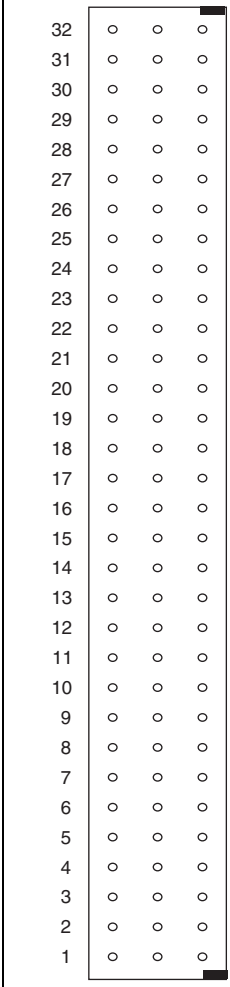
Figure 2-5. Recommended Wiring for a Grounded Source



Module Pinout

Table 2-1 shows the pinout of the front connector of the PXIe-4309. Refer to the *I/O Connector Signal Descriptions* section for definitions of each signal. Refer to the *PXIe-4309 and TB-4309 (ST)/TB-4309 (MT) Getting Started Guide and Terminal Block Specifications* for signal locations on the terminal blocks.

Table 2-1. PXIe-4309 Front Connector Signal Pin Assignments

Front Connector Diagram	Row Number	Column A	Column B	Column C
	32	GND	AI16+	AI0+
	31	AI8+	AI16-	AI0-
	30	AI8-	AI24-	AI24+
	29	GND	AI20+	AI4+
	28	AI12+	AI20-	AI4-
	27	AI12-	AI28-	AI28+
	26	GND	AI21+	AI5+
	25	AI13+	AI21-	AI5-
	24	AI13-	AI29-	AI29+
	23	GND	AI17+	AI1+
	22	AI9+	AI17-	AI1-
	21	AI9-	AI25-	AI25+
	20	GND	NC	NC
	19	REF+	NC	NC
	18	REF-	NC	NC
	17	GND	AI18+	AI2+
	16	AI10+	AI18-	AI2-
	15	AI10-	AI26-	AI26+
	14	GND	AI22+	AI6+
	13	AI14+	AI22-	AI6-
	12	AI14-	AI30-	AI30+
	11	GND	AI23+	AI7+
	10	AI15+	AI23-	AI7-
	9	AI15-	AI31-	AI31+
	8	GND	AI19+	AI3+
	7	AI11+	AI19-	AI3-
	6	AI11-	AI27-	AI27+
	5	PFI GND	PFI0	PFI1
	4	NC	GND	GND
	3	NC	NC	NC
RSVD is reserved NC is no connection	2	RSVD	RSVD	RSVD
	1	RSVD	RSVD	RSVD

I/O Connector Signal Descriptions

Table 2-2 describes the signals found on the I/O connector.

Table 2-2. I/O Connector Signal Descriptions

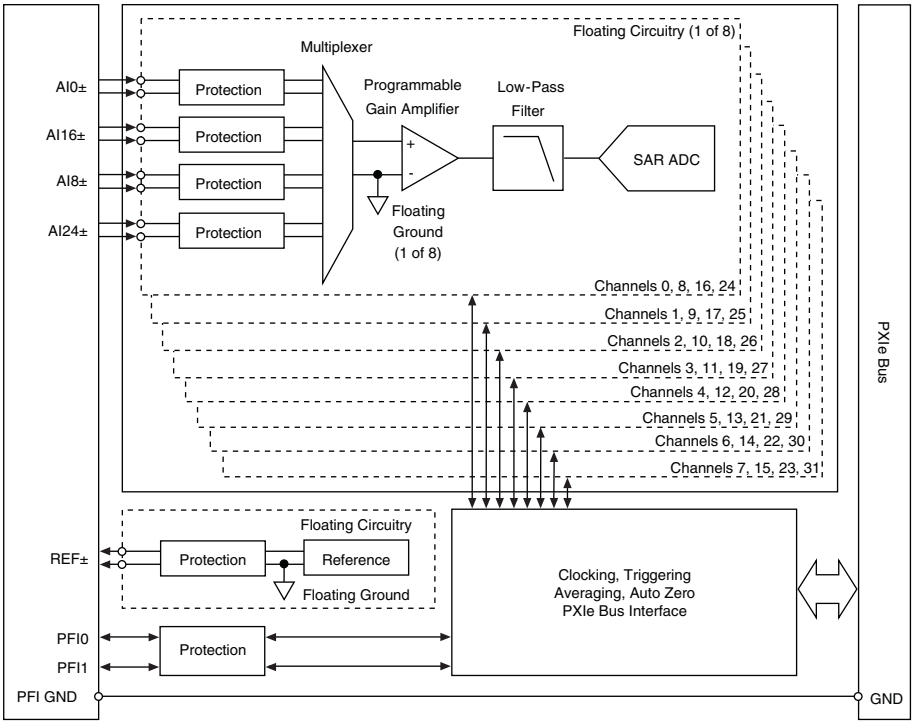
Signal Names	Direction	Description
GND	—	Ground
AI<0..31>+	Input	Positive inputs of the differential analog input channels 0 to 31.
AI<0..31>-	Input	Negative inputs of the differential analog input channels 0 to 31.
RSVD	—	Reserved for communication with the accessory.
PFI<0..1>	Input/Output	Configurable 5.0 V tolerant digital input or 3.3 V digital output for sending or receiving trigger and synchronization signals. PFI lines are referenced to PFI GND.
PFI GND	—	Digital ground reference for PFI lines.
REF+	Output	Positive output of the internal reference used for self-calibration. Refer to the *PXIe-4309 Specifications* and *PXIe-4309 Calibration Procedure*.
REF-	Output	Negative output of the internal reference used for self-calibration. Refer to the *PXIe-4309 Specifications* and *PXIe-4309 Calibration Procedure*.

PXIe-4309 Block Diagram

Input signals on each channel are conditioned, buffered, and then sampled by a SAR ADC. The PXIe-4309 supports averaging and auto zero in hardware.

The PXIe-4309 has 8 independent signal conditioning paths and ADCs, enabling simultaneous sampling of up to eight input channels. Each ADC can scan through four independent input channels for a total of 32 input channels. Figure 2-6 shows the block diagram of the PXIe-4309.

Figure 2-6. PXIe-4309 Block Diagram



Signal Acquisition Considerations

This section contains information about signal acquisition concepts, including operation modes, SAR converters, timing, triggering, and synchronization.

ADC

The PXIe-4309 has eight simultaneously sampled 18-bit 2 MS/s successive approximation (SAR) ADCs. SAR involves a binary search through all possible quantization levels before finally converging upon a digital output for each conversion.

Single Channel per ADC

The PXIe-4309 can sample eight simultaneous input channels up to 2 MS/s when only one channel per ADC is selected.

Multiple Channels per ADC

The PXIe-4309 can sample 32 input channels when multiple channel per ADC are selected. In this mode of operation, each ADC can scan through four independent input channels up to an aggregate sample rate of 400 kS/s. The mapping of input channels to ADCs is shown in Table 2-3.

Table 2-3. AI Channel to ADC Mapping

ADC	AI Channels
0	ai0, ai8, ai16, ai24
1	ai1, ai9, ai17, ai25
2	ai2, ai10, ai18, ai26
3	ai3, ai11, ai19, ai27
4	ai4, ai12, ai20, ai28
5	ai5, ai13, ai21, ai29
6	ai6, ai14, ai22, ai30
7	ai7, ai15, ai23, ai31

The signal conditioning circuitry of each ADC has a non-zero settling time when it changes the input multiplexer to scan through multiple channels.

The settling time increases as the aggregate sample rate decreases to allow for more settling time. This reduces settling and ghosting errors.

Sample Modes

The PXIe-4309 has two sampling modes: averaging and single sample. The sampling mode is selected based on the timing mode. Refer to *Sample Timing Modes* section for more information.

Terminology for *Averaging Acquisition* and *Single Convert Acquisition* sections:

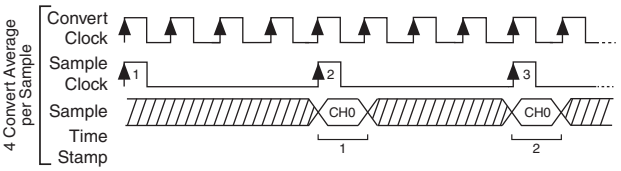
- *Convert* is a single ADC quantized digitization of the input signal.
- *Sample* is the data returned from hardware.

Averaging Acquisition

The PXIe-4309 supports averaging in hardware. Based on the sample rate, the PXIe-4309 will average as many converts per sample as possible to deliver the best resolution for a given sample rate. Refer to the *PXIe-4309 Specifications* for *Noise versus Sample Rate* information.

Figure 2-7 depicts an averaging acquisition of two samples of a single channel.

Figure 2-7. Single Channel Averaging



Note Samples are timestamped to the time when the sample clock takes place, but are acquired throughout the sample period. This introduces a phase shift of half a sample period when channel expanding to other types of data acquisition devices.

Figure 2-8 depicts an averaging acquisition of two converts per sample of two channels on the same ADC. The settling time increases as the aggregate sample rate decreases to allow for more settling time to reduce settling and ghosting errors.

Figure 2-8. Multiple Channel Averaging

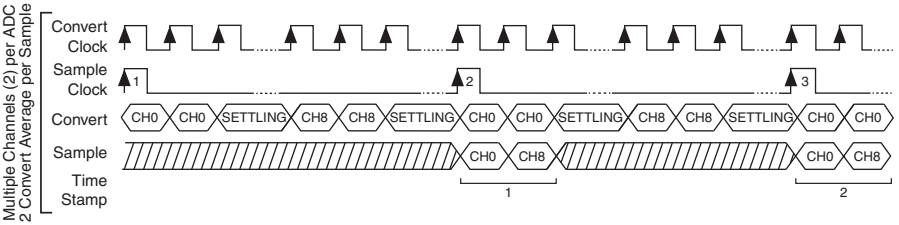


Table 2-4 shows the max sampling rate based on the maximum number of channels per ADC.

Table 2-4. Maximum Sample Rate

Maximum Channels per ADC	Maximum Sample Rate	Aggregate Rate
1	2 MHz	2 MHz
2	200 kHz	400 kHz
3	133 kHz	
4	100 kHz	

Single Convert Acquisition

The PXIe-4309 takes a single convert per channel and returns that as a sample. Figure 2-9 depicts a single convert acquisition of a single channel.

Figure 2-9. Single Convert Acquisition of a Single Channel

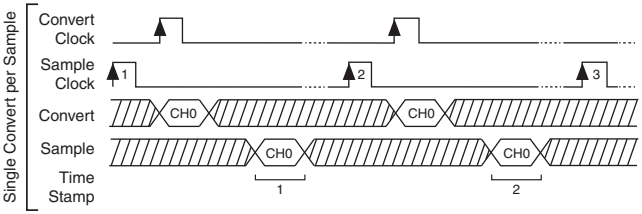


Figure 2-10 depicts a single convert acquisition of two channels on the same ADC. The settling time increases as the aggregate sample rate decreases to allow for more settling time to reduce settling and ghosting errors.

Figure 2-10. Single Convert Acquisition of Two Channels on the Same ADC

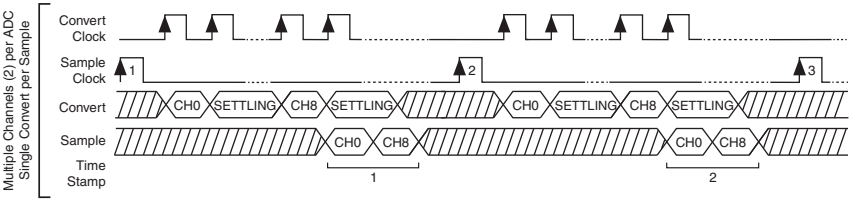


Table 2-5 shows the max sampling rate based on the maximum number of channels per ADC.

Table 2-5. Maximum Sample Rate (Hardware-Timed Single Point, On-Demand, and External Sample Clock)

Maximum Channels per ADC	Maximum Sample Rate	Aggregate Rate
1	900 kHz	900 kHz
2	180 kHz	360 kHz
3	120 kHz	
4	90 kHz	

Sample Timing Modes

The PXIe-4309 supports four timing modes that fall into two categories: software-timed and hardware-timed.

Note Software-timed, hardware timed single point (HWTSP), and external sample clock use single sample acquisition to minimize latency. Refer to the *Single Convert Acquisition* section for more information.

Software-Timed Acquisitions

Software controls the rate of the acquisition. Software sends a separate command to the hardware to acquire each sample. In NI-DAQmx, software-timed acquisitions are referred to as having on-demand timing. Software-timed acquisitions are also referred to as immediate or static acquisitions and are typically used for reading a single sample of data.

Hardware-Timed Acquisitions

A digital hardware signal (AI Sample Clock) controls the rate of the acquisition. This signal can be generated internally by the PXIe-4309 or provided externally.

Hardware-timed acquisitions have several advantages over software-timed acquisitions:

- The time between samples can be much shorter.
- The timing between samples is deterministic.
- Hardware-timed acquisitions can use hardware triggering.

Hardware-timed operations can be buffered or HWTSP. A buffer is a temporary storage in computer memory for to-be-transferred samples.

- **Buffered**—In a buffered acquisition, data is moved from the onboard FIFO memory of the DAQ device to a PC buffer using DMA before it is transferred to application memory. Buffered acquisitions typically allow for much faster transfer rates than HWTSP acquisitions because data is moved in large blocks, rather than one point at a time.

  One property of buffered I/O operations is the sample mode. The sample mode can be either finite or continuous:

  – Finite sample mode acquisition refers to the acquisition of a specific, predetermined number of data samples. Once the specified number of samples has been read, the acquisition stops. If you use a reference trigger, you must use finite sample mode.

  – Continuous acquisition refers to the acquisition of an unspecified number of samples. Instead of acquiring a set number of data samples and stopping, a continuous acquisition continues until you stop the operation. Continuous acquisition is also referred to as double-buffered or circular-buffered acquisition.

    If data cannot be transferred across the bus fast enough, the FIFO becomes full. For more information refer to *NI-DAQmx Help*.

- **HWTSP**—Typically used to read single samples at known time intervals. While buffered operations are optimized for high throughput, HWTSP operations are optimized for low latency and low jitter. In addition, HWTSP can notify software if it falls behind hardware. These features make HWTSP ideal for real time control applications. HWTSP operations, in conjunction with the wait for next sample clock function, provide tight synchronization between the software layer and the hardware layer. Refer to the *NI-DAQmx Hardware-Timed Single Point Lateness Checking* document, for more information. To access this document, go to `ni.com/info` and enter the Info Code `daqhwtsp`.

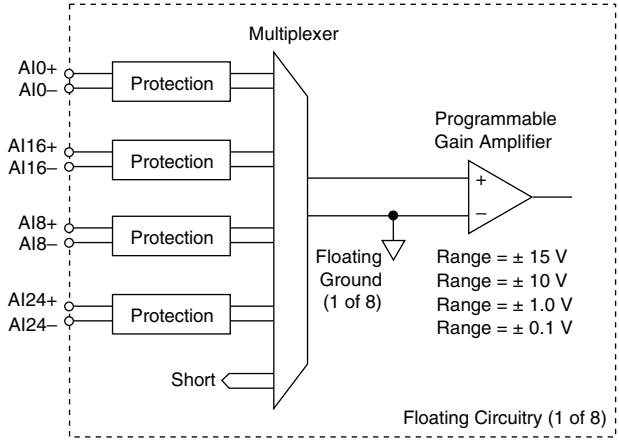
Offset Error Cancellation Techniques

The PXIe-4309 supports two types of offset error cancellation techniques: auto zero and chopping.

Auto Zero

Each signal conditioning path of the PXIe-4309 has an internal channel to measure its offset error as shown in Figure 2-11. When Auto Zero is set to once or every sample, the offset error is measured and subtracted from the input measurement, effectively canceling the offset error.

Figure 2-11. Analog Input Auto Zero



Use the **DAQmx Channel Property Node (Analog Input»General Properties»Advanced» High Accuracy Settings»Auto Zero Mode)** to configure Auto Zero behavior as none, once, or every sample.

Note To read the offset error add `_aignd_vs_aignd<0..7>` to the acquisition task, where each channel index represents the ADC index. The offset error can only be read with Auto Zero set to none.

Note For a single PXIe-4309 module, the Auto Zero setting must be consistent across all channels for a given task; for channel expansion across multiple PXIe-4309, each module can have a different Auto Zero setting.

Note When Auto Zero is set to Once or Every Sample, the Input Voltage Range setting must be consistent across all channels per ADC for a given task.

Auto Zero Once

With Auto Zero set to once, the offset error is measured when the acquisition task starts. The offset error measurement introduces a delay from start to the first sample clock. The start delay may be queried with the DAQmx Trigger Property Node **(Start»More»Delay)**.

Note The start delay is in units of 100 MHz timebase ticks by default.

With auto zero set to once, the offset error temperature coefficient is the same as with auto zero none, making Auto Zero once an effective offset cancellation technique so long as the ambient temperature is stable throughout an acquisition.

Note Auto Zero Once has no impact on low frequency noise performance.

Refer to the *PXIe-4309 Specifications* for performance specifications of Auto Zero Once.

Auto Zero Every Sample

With Auto Zero set to every sample, the offset error is measured at the beginning of every sample period. Refer to the *PXIe-4309 Specifications* for performance specifications of Auto Zero Every Sample.

With Auto Zero Every Sample the offset error temperature coefficient is reduced, making auto zero every sample an effective offset cancellation technique in the presence of ambient temperature fluctuations.

Note Auto Zero Every Sample improves low frequency noise performance.

Refer to the *PXIe-4309 Specifications* for performance specifications of Auto Zero Every Sample.

Table 2-6 shows the maximum sample rate with Auto Zero set to every sample based on the maximum number of channels per ADC.

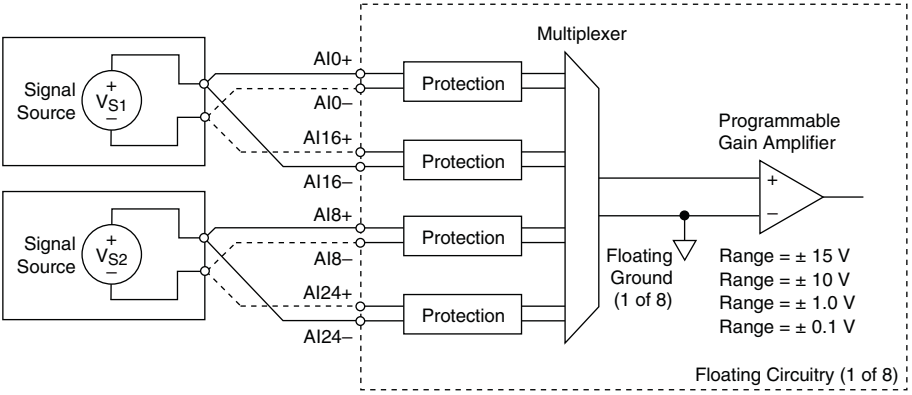
Table 2-6. Maximum Sample Rate (Auto Zero Every Sample)

Maximum Channels per ADC	Maximum Sample Rate	Aggregate Rate
1	10 kHz	10 kHz
2	5 kHz	
3	3.3 kHz	
4	2.5 kHz	

Chopping

Figure 2-12 shows the connections required to use two input channels of the same ADC to enable chopping for the measurement of two voltage sources.

Figure 2-12. Analog Input Chopping



The first channel measures the source voltage, while the second channel measures the negative source voltage; in both measurements the offset error of the signal conditioning path adds to the measured voltage as follows:

$$V_{AI0} = V_{S1} + V_O$$

$$V_{AI16} = -V_{S1} + V_O$$

Using these measurements it is possible to cancel out the offset error of the signal conditioning path.

$$0.5 \times (V_{AI0} - V_{AI16}) = 0.5 \times ([V_{S1} + V_O] - [-V_{S1} + V_O]) = 0.5 \times 2\, V_{S1} = V_{S1}$$

The PXIe-4309 performs these mathematical operations in hardware when chopping is enabled. Refer to the *PXIe-4309 Specifications* for performance specifications of Chopping.

Table 2-7 shows the AI channel connections that are paired to create a chopping channel.

Table 2-7. AI Channel Connection Pairing for Chopping Channels

Chopping Channel	AI Channel
ai0	ai0, ai16
ai1	ai1, ai17
ai2	ai2, ai18
ai3	ai3, ai19
ai4	ai4, ai20
ai5	ai5, ai21
ai6	ai6, ai22
ai7	ai7, ai23
ai8	ai8, ai24
ai9	ai9, ai25
ai10	ai10, ai26
ai11	ai11, ai27
ai12	ai12, ai28
ai13	ai13, ai29
ai14	ai14, ai30
ai15	ai15, ai31

Table 2-8 shows the maximum sample rate when chopping is enabled based on the maximum number of chopping channels per ADC.

Table 2-8. Maximum Sample Rate (Chopping Enabled)

Maximum Chopping Channels per ADC	Maximum Sample Rate	Aggregate Rate
1	10 kHz	10 kHz
2	5 kHz	

Use the DAQmx Channel Property Node **(Analog Input»General Properties»Advanced» High Accuracy Settings»Chop»Enable)** to enable or disable chopping. For a LabVIEW example to enable chopping, refer to ni.com/info and enter the Info Code chopexp.

Note Chopping, Auto Zero Once, and Auto Zero Every Sample are mutually exclusive configurations.

Timing and Triggering

This section contains information about timing and triggering for the PXIe-4309.

Sample Clock Timebase

The PXIe-4309 sample clock is derived from the onboard 100 MHz clock, which can be locked to the PXIe backplane 100 MHz clock to synchronize multiple modules.

External Clock

The PXIe-4309 sample clock can be driven from external sources by either PXI_TRIG<0..7>, PFI<0..1>, PXI_STAR, or PXIe_DSTAR<A,B>.

Note When using the external sample clock, the PXIe-4309 does not support averaging, auto zero, or chopping.

Digital Triggering

The PXIe-4309 supports acquisition start in response to a digital trigger signal from one of the PXI Express backplane trigger lines or the PFI from the front connector. The trigger circuit can respond either to a rising or a falling edge.

PFI

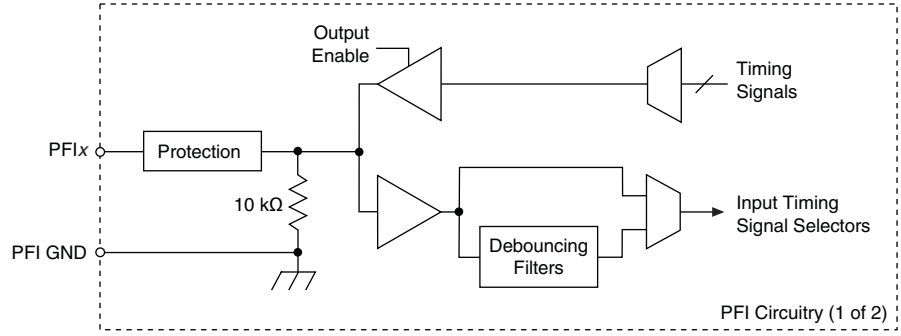
Each PFI can be individually configured as the following:

- A timing input signal for AI.
- A timing output signal from AI.

Each PFI input has a programmable debouncing filter.

Figure 2-13 shows the PFI circuitry.

Figure 2-13. PFI Circuitry



On the I/O connector, each terminal is labeled PFI*x*.

Refer to the *PXIe-4309 Specifications* for the PFI input and output specifications.

Using PFI Terminals as Timing Input Signals

Use PFI terminals to route external timing signals to different functions of the PXIe 4309. Each PFI input can be routed to any of the following signals:

- AI Sample Clock (ai/SampleClock)
- AI Start Trigger (ai/StartTrigger)
- AI Reference Trigger (ai/ReferenceTrigger)
- AI Pause Trigger (ai/PauseTrigger)
- AI Sample Clock Timebase (ai/SampleClockTimebase)

Note The polarity of PFI inputs is configurable for most functions.

Note Pause triggers are only sensitive to the level of the source, not the edge.

Exporting Timing Output Signals Using PFI Terminals

You can route any of the following timing signals to any PFI terminal configured as an output:

- AI Reference Trigger (ai/ReferenceTrigger)
- AI Sample Clock (ai/SampleClock)
- AI Start Trigger (ai/StartTrigger)
- AI Pause Trigger (ai/PauseTrigger)
- PXI_STAR
- PXI_Trig <0..7>

Connecting PFI Input Signals

All PFI I/O lines are referenced to PFI GND.

PFI Filters

The PXIe-4309 has programmable debouncing filters on each PFI, PXI_Trig, PXI_STAR, or PXI_DSTAR. When filters are enabled, the PXIe-4309 uses the onboard oscillator as the filter clock to sample the filter input on each rising edge and to generate the filtered digital signal.

Note Enabling filters introduces jitter on the input signal. The maximum jitter is one period of the filter clock.

Figure 2-14 shows an example of a low-to-high transition for a custom filter with N set to 5.

Figure 2-14. Low-to-High Transition for a Custom Filter with N Set to 5

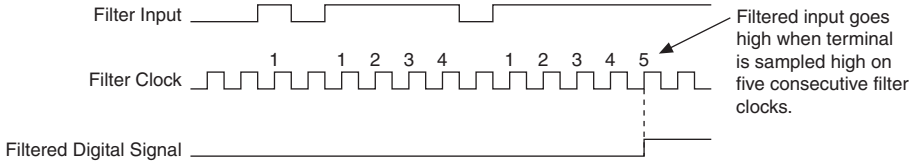


Table 2-9 shows the debouncing filters supported by the PXIe-4309.

Table 2-9. Debouncing Filters

Filter Setting	Filter Clock	N (Filter Clocks Needed to Pass Signal)	Pulse Width Guaranteed to Pass Filter	Pulse Width Guaranteed to Not Pass Filter
None	—	—	—	—
90 ns (short)	100 MHz	9	90 ns	80 ns
5.12 µs (medium)	100 MHz	512	5.12 µs	5.11 µs
Custom	100 MHz	*N*	$\frac{N}{100\ \text{MHz}}$	$\frac{(N - 1)}{100\ \text{MHz}}$

The filter setting for each input can be configured independently. Filters are disabled on power up.

I/O Protection

Each PFI signal is protected against overvoltage, undervoltage, and overcurrent conditions as well as ESD events; however, avoid these fault conditions by following these guidelines:

- When using PFI lines as an output, do *not* connect them to any external signal source, ground, or power supply; understand the current requirements of the load connected to these lines; do not exceed the specified current drive of the device. NI has several signal conditioning solutions for digital applications requiring high current drive.
- When using PFI lines as an input, do *not* drive the line with voltages outside of its normal operating range. The PFI lines have a smaller operating range than the analog input channels.
- Treat the device as you would treat any static sensitive device. *Always* properly ground yourself and the equipment when handling the device or connecting to it.

Synchronization

Some applications require tight synchronization between input and output operations on multiple modules. Synchronization is important to minimize skew between channels and to eliminate clock drift between modules in long-duration operations. You can synchronize the analog input operations on two or more PXIe-4309 modules to extend the channel count for your measurements. In addition, the PXIe-4309 can synchronize with 62XX (M Series) and 63XX (X Series) devices/modules, such as the PXI-6289 and PXIe-6363, respectively. Refer to the *Reference Clock Synchronization* section for more information.

Reference Clock Synchronization

With reference clock synchronization, master and slave modules generate their ADC sample clock from the shared 100 MHz reference clock from the PXIe backplane (PXIe_CLK100). The backplane supplies an identical copy of this clock to each peripheral slot. In addition, multiple chassis can be synchronized by using a timing and synchronization board to lock the 100 MHz clock across chassis.

When acquiring data from multiple modules within the same NI-DAQmx task, NI-DAQmx will automatically handle all of the Reference Clock Synchronization details required to synchronize the modules within the task. This is known as a multi-device task.

To perform reference clock synchronization when using multiple NI-DAQmx tasks that are acquiring at the same rate, complete the following steps to synchronize the hardware.

1. Specify PXIe_CLK100 as the reference clock source for all modules to force all the modules to lock to the reference clock on the PXIe chassis.
2. Choose one module to be the start trigger master.
3. Configure the rest of the modules in your system to receive their start trigger from the start trigger master module. This ensures that all modules will begin returning data on the same sample.

4. Set the synchronization type of the Start Trigger slaves at **DAQmx Trigger»Advanced» Synchronization»Synchronization Type** to Slave and that of the Master to Master.
5. Start all of the start trigger slave module tasks. This sets them up to expect the start trigger from the master.
6. Start the start trigger master module task. You can now acquire data.

Tip Consider using a multi-device task when synchronizing multiple devices at the same rate.

Tip You can find example VIs in the NI Example Finder. Select **Help»Find Examples** to launch the NI Example Finder.

Accessory Auto-Detection

SC Express modules automatically detect compatible accessories or terminal blocks. The RSVD pins on the I/O connector provide power to the accessories as well as digital communication lines. This allows software to detect when accessories are inserted or removed. In addition, software can automatically identify the specific terminal block as well as access any calibration or scaling information associated with the terminal block.

MAX allows you to see which accessories are currently connected to your module. In MAX, expand **Devices and Interfaces** and locate your module. If a terminal block is connected to your module, it will be displayed beneath the module. Unsupported terminal blocks appear in MAX with an X next to them.

NI-DAQmx property nodes can be used to programmatically access information about connected accessories in your application. Refer to the *NI-DAQmx Help* for documentation about programmatically accessing accessory status.

3

SC Express Considerations

This chapter details the clock and trigger functionality available through the PXI Express chassis.

SC Express Clock and Trigger Signals

PXIe_CLK100

PXIe_CLK100 is a common, low-skew 100 MHz reference clock used for synchronization of multiple modules in a PXI Express measurement or control system. The PXIe backplane is responsible for generating PXIe_CLK100 independently to each peripheral slot in a PXI Express chassis. For more information, refer to the *PXI Express Specification* at `www.pxisa.org`.

PXI_CLK10

PXI_CLK10 is a common, low-skew 10 MHz reference clock for synchronization of multiple modules in a PXI measurement or control system. The PXI backplane is responsible for generating PXI_CLK10 independently to each peripheral slot in a PXI chassis. In PXIe chassis, the PXI_CLK10 signal is in phase with PXIe_CLK100.

Note PXI_CLK10 cannot be used as a reference clock for SC Express modules.

PXI Triggers

A PXI/PXIe chassis provides eight bused trigger lines to each module in a system. Triggers may be passed from one module to another, allowing precisely timed responses to asynchronous external events that are being monitored or controlled. Triggers can be used to synchronize the operation of several different PXI peripheral modules.

In a PXI chassis with more than eight slots, the PXI trigger lines may be divided into multiple independent buses. Refer to the documentation for your chassis for details.

PXI_STAR Trigger

In a PXI Express system, the Star Trigger bus implements a dedicated trigger line between the system timing slot and the other peripheral slots. The Star Trigger can be used to synchronize multiple modules or to share a common trigger signal among modules.

A system timing controller can be installed in the system timing slot to provide trigger signals to other peripheral modules. Systems that do not require this functionality can install any standard peripheral module in this system timing slot.

An SC Express module receives the Star Trigger signal (PXI_STAR) from a System timing controller. PXI_STAR can be used as a trigger signal for input operations.

An SC Express module is not a System timing controller. An SC Express module can be used in the system timing slot of a PXI system, but the system will not be able to use the Star Trigger feature.

PXIe_DSTAR<A..C>

PXI Express devices can provide high-quality and high-frequency point-to-point connections between each slot and a system timing slot. These connections come in the form of three low-voltage differential star triggers that route between a PXI Express system timing controller and a peripheral device. Using multiple connections simplifies the creation of applications because of the increased routing capabilities.

Table 3-1 describes the three differential star (DSTAR) lines and how they are used.

Table 3-1. PXIe_DSTAR Line Descriptions

Trigger Line	Purpose
PXIe_DSTARA	Distributes high-speed, high-quality clock signals from the system timing slot to the peripherals (input).
PXIe_DSTARB	Distributes high-speed, high-quality trigger signals from the system timing slot to the peripherals (input).
PXIe_DSTARC	Sends high-speed, high-quality trigger or clock signals from the peripherals to the system timing slot (output).

The DSTAR lines are only available for PXI Express devices when used with a PXI Express system timing module. For more information, refer to the *PXI Express Specification* at `www.pxisa.org`.

A

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